NMOS 4-BIT MICROCONTROLLER

TMP4720P, TMP4740P
TMP4720N, TMP4740N

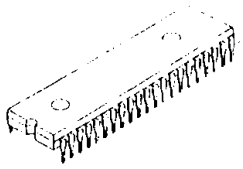
The 4720/40 are high speed and high performance 4-bit single chip microcomputers, integrating ROM, RAM, input/output ports, timer/counters, and a serial interface on a chip.
The 4720/40 are the standard type devices in the TCLS-47 NMOS series.

PART No.	ROM	RAM	PACKAGE	PIGGYBACK
TMP4720P	2048 x 8-bit	128 x 4-bit	DIP42	TMP4799C
TMP4720N			SDIP42	TMP4799E
TMP4740P	4096 x 8-bit	256 x 4-bit	DIP42	TMP4799C
TMP4740N			SDIP42	TMP4799E

FEATURES

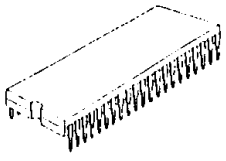
- ◆4-bit single chip microcomputer
- ◆Instruction execution time: 1.9μs (at 4.2MHz)
- ◆90 basic instructions
- ◆Table look-up instrucitons
- ◆5-bit to 8-bit data conversion instruction
- ◆Subroutine nesting : 15 levels max.
- ◆6 interrupt sources (External :2, Internal : 4)
  All sources have independent latches each, and multiple interrupt control is available.
- ◆I/O port (35 pins)
  - Input 1 port 4 pins
  - Output 2 ports 8 pins
  - I/O 6 ports 23 pins
- ◆Interval Timer
- ◆Two 12-bit Timer/Counters
  Timer, event counter, and pulse width measurement mode
- ◆Serial Interface with 4-bit buffer
  External/internal colck, and leading/trailing edge mode
- ◆High current outputs
  LED direct drive capability (typ.20mA x 8bits)
- ◆Memory holding function
  Battery back-up
- ◆Real Time Emulator: BM4721A

DIP42



TMP4720P
TMP4740P

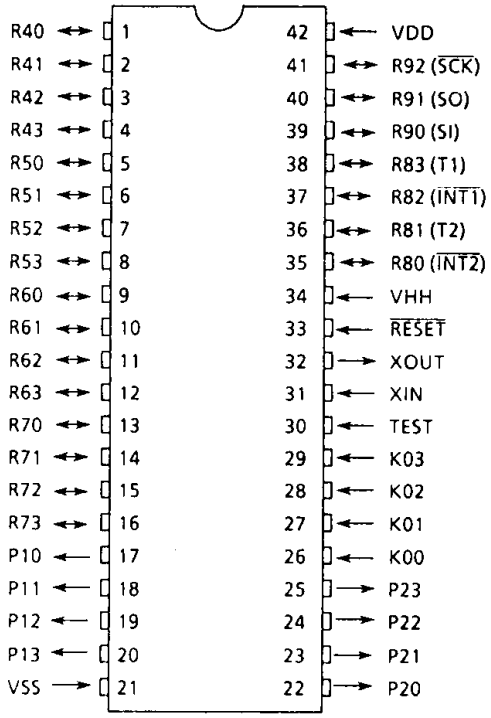
SDIP42



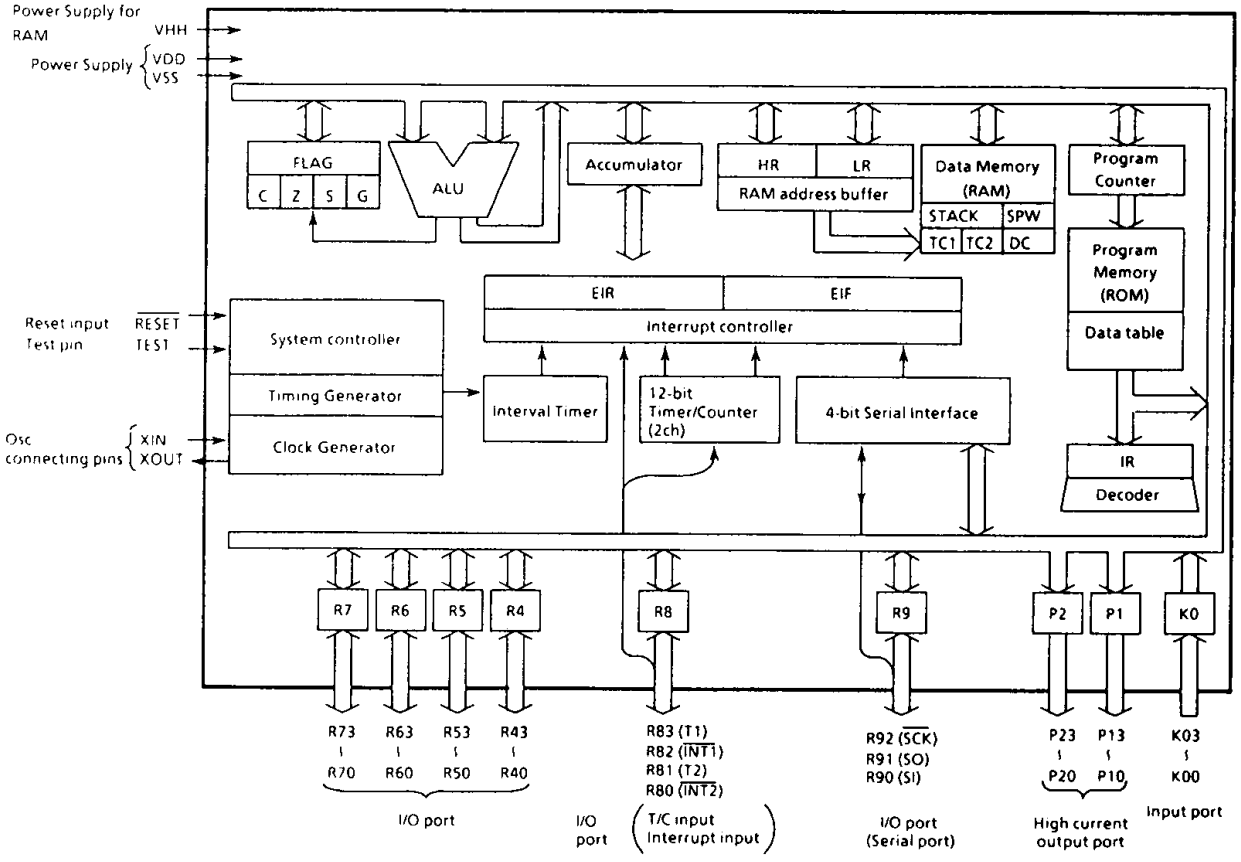
TMP4720N
TMP4740N

PIN ASSIGNMENT (TOP VIEW)

DIP42, SDIP42



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS	
K03 - K00	Input	4-bit input port	
P13 - P10	Output	4-bit output port with latch. 8-bit data are output by the 5-bit to 8-bit data conversion instruction [OUTB @HL].	
P23 - P20			
R43 - R40	I/O	4-bit I/O port with latch. When used as input port, the latch must be set to "1". Every bit data is possible to be set, clear and tested by the manupilation of the L-register indirect addressing.	
R53 - R50			
R63 - R60			
R73 - R70			
R83 (T1)	I/O (Input)	4-bit I/O port with latch. When used as input port, external interrupt input pin, or timer/counter input pin, the latch must be set to "1".	Timer/Counter 1 external input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer/Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 input
R92 ($\overline{SCK}$)	I/O (I/O)	3-bit I/O port with latch. When used as input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O (Output)		Serial data output
R90 (SI)	I/O (Input)		Serial data input
XIN	Input	Resonator connecting pins. For inputting external clock, XIN is used and XOUT is opened.	
XOUT	Output		
$\overline{RESET}$	Input	Reset signal input	
TEST	Input	Test pin for out-going test. Be opened or fixed to low level.	
VDD	Power supply	+ 5V	
VHH		+ 5V (Power supply for RAM)	
VSS		0V (GND)	

OPERATIONAL DESCRIPTION

The 4720/40 are the standard devices for the TLCS-47 NMOS series, and functions similarly to the 47C200A/400A (TLCS-47 CMOS series standard devices) except the memory holding function. Refer to the technical data sheets for the 47C200A/400A (The 4720/40, however, do not have a hold function).

MEMORY HOLDING FUNCTION

By connecting a back-up power supply to the VHH pin, the RAM data can be protected with low power consumption even if VDD is cut off. The following procedure is used for memory holding operation.

(1) $\overline{\text{RESET}}$ pin is set to low level before VDD drops below the minimum operating voltage.
(2) Even if VDD is cut off, $\overline{\text{RESET}}$ pin is set to low level and VHH is kept at a voltage higher than the minimum holding voltage.
(3) When the system returns to the normal operation mode from the memory holding operation, after VHH and then VDD are confirmed to be at the minimum operating voltage or higher, $\overline{\text{RESET}}$ pin is set to high level (Reset is released).

This function makes it possible to conserve power during stand-by. With the NMOS series, the power for the data memory (RAM) and reset circuit is supplied through VHH. Thus, it is necessary that operating voltage is applied to both pins VDD and VHH.

Port address (**)	Port		Input/Output instructions						
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A, %p OUT@HL, %p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p, b	SET @L CLR @L TEST @L
00_H	K0 Input port	——	○	–	–	–	–	○	–
01	P1 output latch	P1 output port	○	○	○	○ (Note2)	○	○	–
02	P2 output latch	P2 output port	○	○	○	○	○	○	–
03	——	——	–	–	–	–	–	–	–
04	R4 input port	R4 output port	○	○	○	–	○	○	○
05	R5 input port	R5 output port	○	○	○	–	○	○	○
06	R6 input port	R6 output port	○	○	○	–	○	○	○
07	R7 input port	R7 output port	○	○	○	–	○	○	○
08	R8 input port	R8 output port	○	○	○	–	○	○	–
09	R9 input port	R9 output port	○	○	○	–	○	○	–
0A	——	——	–	–	–	–	–	–	–
0B	——	——	–	–	–	–	–	–	–
0C	——	——	–	–	–	–	–	–	–
0D	——	——	–	–	–	–	–	–	–
0E	SIO status	——	○	–	–	–	–	○	–
0F	Serial receive buffer	Serial transmit buffer	○	○	○	–	–	–	–
10_H	Undefined	——	–	–	–	–	–	–	–
11	Undefined	——	–	–	–	–	–	–	–
12	Undefined	——	–	–	–	–	–	–	–
13	Undefined	——	–	–	–	–	–	–	–
14	Undefined	——	–	–	–	–	–	–	–
15	Undefined	——	–	–	–	–	–	–	–
16	Undefined	——	–	–	–	–	–	–	–
17	Undefined	——	–	–	–	–	–	–	–
18	Undefined	——	–	–	–	–	–	–	–
19	Undefined	Interval Timer interrupt control	–	○	–	–	–	–	–
1A	Undefined	——	–	–	–	–	–	–	–
1B	Undefined	——	–	–	–	–	–	–	–
1C	Undefined	Timer/Counter 1 control	–	○	–	–	–	–	–
1D	Undefined	Timer/Counter 2 control	–	○	–	–	–	–	–
1E	Undefined	——	–	–	–	–	–	–	–
1F	Undefined	Serial interface control	–	○	–	–	–	–	–

Note1: "——" means the reserved state. Unavailable for the user programs.

Note2: The 5-bit to 8-bit data conversi.. instruction [OUTB @HL], automatic access to ports P1 and P2.

Table 1-1. Port Address Assignments and Available I/O Instructions.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		− 0.5 to 7	V
	V_{HH}			
Input Voltage	V_{IN}		− 0.5 to 7	V
Output Voltage	V_{OUT1}	Except sink open drain pin	− 0.5 to 7	V
	V_{OUT2}	Sink open drain pin	− 0.5 to 10	
Output Current (Per 1 pin)	I_{OUT}	Ports P1, P2	30	mA
Power Dissipation [T_{opr} = 70°C]	PD		850	mW
Soldering Temperature (time)	T_{sld}		260 (10sec)	°C
Storage Temperature	T_{stg}		− 55 to 125	°C
Operating Temperature	T_{opr}		− 30 to 70	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = − 30 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		In the Normal mode	4.5	5.5	V
	V_{HH}					
			In the Memory Holding mode	3.5		
Input High Voltage	V_{IH1}	Ports R4 to R7		2.2	V_{DD}	V
	V_{IH2}	Except ports R4 to R7		3.0		
Input Low Voltage	V_{IL1}	Except port K0		0	0.8	V
	V_{IL2}	Port K0			1.2	
Clock Frequency	fc			0.4	4.2	MHz

D.C. CHARACTERISTICS

(V_{SS} = 0V, T_{opr} = − 30 to 70℃)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		−	0.5	−	V
Input Current	I_{IN1}	Port K0, $\overline{RESET}$, TEST	$V_{DD} = V_{HH} = 5.5V$, $V_{IN} = 5.5V$	−	−	20	μA
	I_{IN2}	Open drain R port	$V_{DD} = 5.5V$, $V_{IN} = 0.5V$	−	−	20	
Input Low Current	I_{IL}	Port R with pull-up resistor	$V_{DD} = 5.5V$, $V_{IN} = 0.4V$	−	−	− 2	mA
Output Leakage Current	I_{LO}	All open drain ports	$V_{DD} = 5.5V$,	−	−	20	μA
Output High Voltage	V_{OH}	All ports with pull-up resistor	$V_{DD} = 4.5V$, I_{OH} = − 200μA	2.4	−	−	V
Output Low Voltage	V_{OL}	Except XOUT and ports P1, P2	$V_{DD} = 4.5V$, $I_{OL} = 1.6mA$	−	−	0.4	
Output Low Current	I_{OL}	Ports P1, P2	$V_{DD} = 4.5V$, $V_{OL} = 1.0V$	−	20	−	mA
Supply Current (in the Normal mode)	I_{DD} + I_{HH}		$V_{DD} = V_{HH} = 5.5V$	−	70	120	mA
Supply Current (in the Memory holding mode)	I_{HH}		$V_{DD} = V_{SS}$, $V_{HH} = 3.5V$	−	5	10	

Note1. Typ. values show those at T_{opr} = 25℃, $V_{DD} = V_{HH} = 5V$.

Note2. Input Current I_{IN1} : The current through resistor is not included, when the pull-up/pull-down resistor is contained.

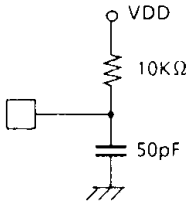
A.C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = V_{HH} = 4.5 to 5.5V, T_{opr} = − 30 to 70℃)

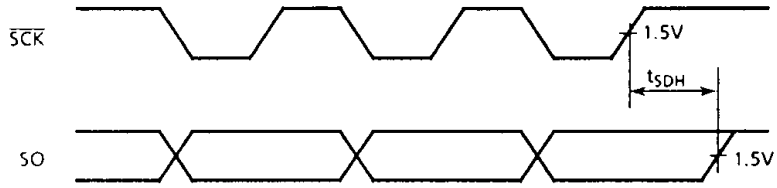
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}		1.9	−	20	μs
High level Clock pulse Width	t_{WCH}	External clock mode	80	−	−	ns
Low level Clock pulse Width	t_{WCL}					
Shift Data Hold Time	t_{SDH}		0.5tcy − 300	−	−	ns

Note. Shift data Hold Time :

External circuit for $\overline{SCK}$ pin and SO pin



Serial port (completion of transmission)



RECOMMENDED OSCILLATING CONDITIONS

(V_{SS} = 0V, V_{DD} = V_{HH} = 4.5 to 5.5V, T_{opr} = − 30 to 70℃)

(1) 4MHz

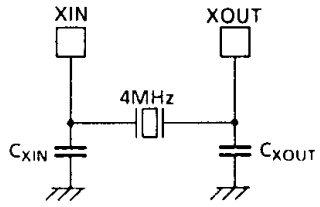
Ceramic Resonator

CSA4.00MG (MURATA) C_{XIN} = C_{XOUT} = 47pF

KBR-4.00MS (KYOCERA) C_{XIN} = C_{XOUT} = 47pF

Crystal Oscillator

204B-6F4.0000 (TOYOCOM) C_{XIN} = C_{XOUT} = 20pF

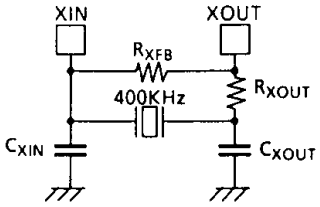


(2) 400KHz

Ceramic Resonator

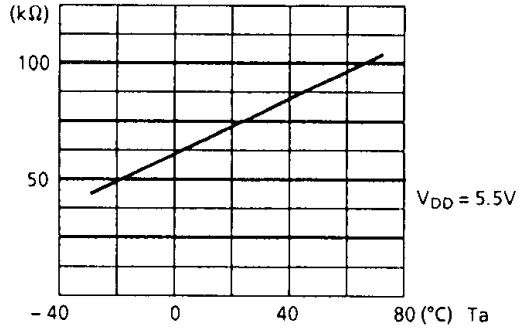
CSA400B (MURATA) C_{XIN} = C_{XOUT} = 390pF, R_{XOUT} = 2.2KΩ, R_{XFB} = 1MΩ

KBR-400B (KYOCERA) C_{XIN} = C_{XOUT} = 390pF, R_{XOUT} = 2.2KΩ, R_{XFB} = 1MΩ

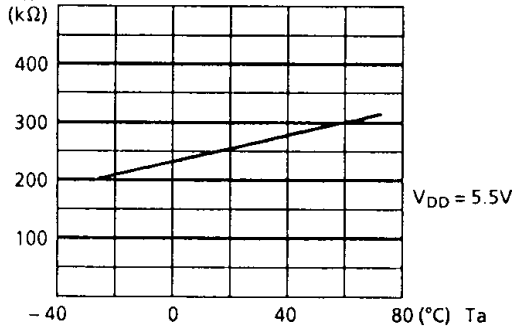


TYPICAL CHARACTERISTICS

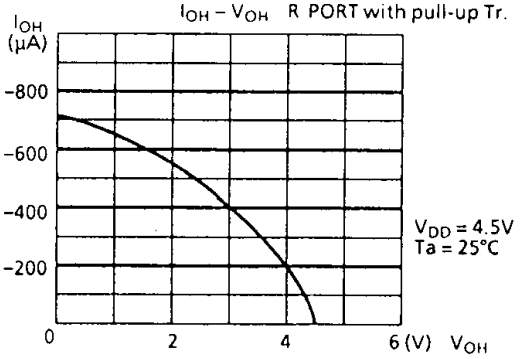
R – Ta K0 PORT



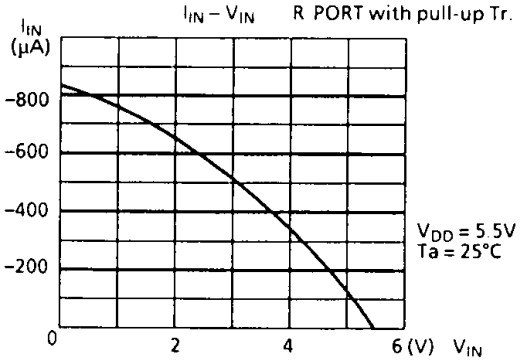
R – Ta $\overline{\text{RESET}}$ PIN



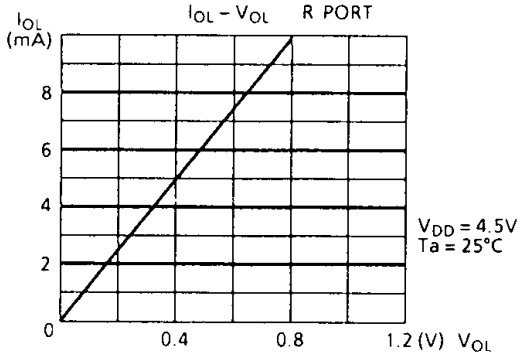
I_{OH} – V_{OH} R PORT with pull-up Tr.



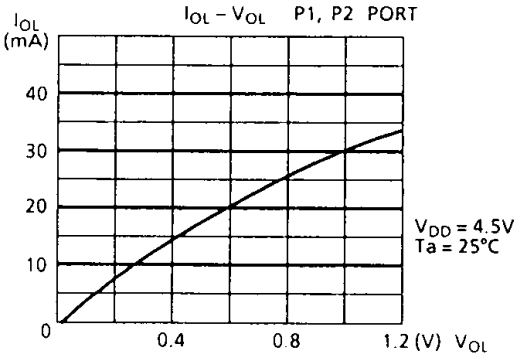
I_{IN} – V_{IN} R PORT with pull-up Tr.



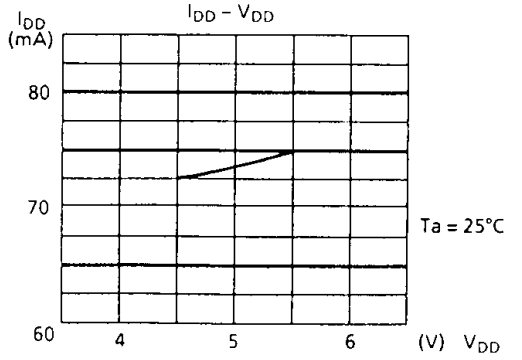
I_{OL} – V_{OL} R PORT



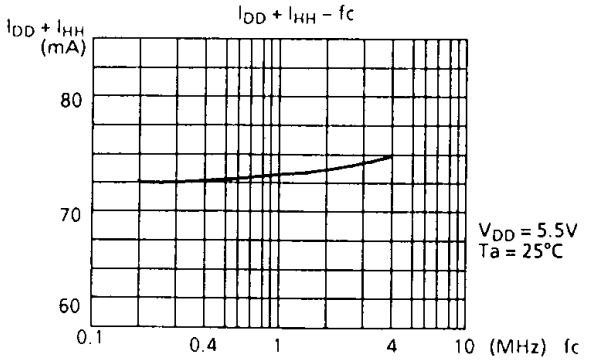
I_{OL} – V_{OL} P1, P2 PORT



I_{DD} – V_{DD}



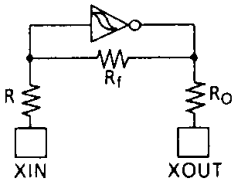
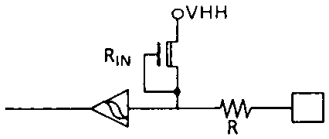
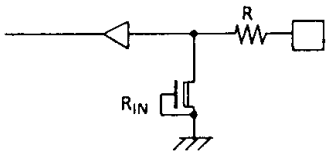
I_{DD} + I_{HH} – fc



INPUT/OUTPUT CIRCUITRY

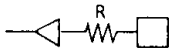
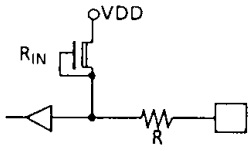
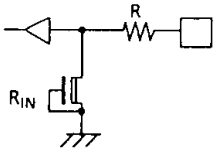
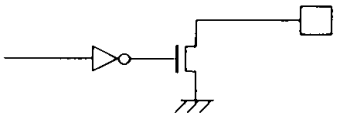
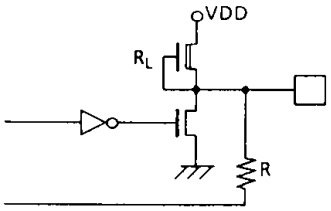
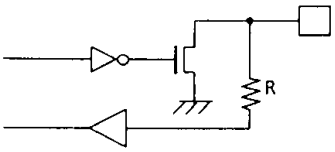
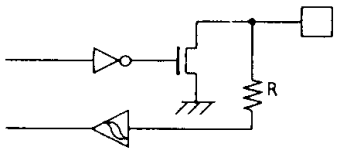
(1) Control pins

Input/Output circuitries of the 4720/40 control pins are shown below.

CONTROL PIN	I/O	CIRCUITRY	REMARK
XIN XOUT	Input Output		Resonator connectiong pins Hysteresis input R = 1KΩ (typ.) R_f = 300KΩ (typ.) R_O = 500KΩ (typ.)
$\overline{RESET}$	Input		Hysteresis input Pull-up resistor R_{IN} = 300KΩ (typ.) R = 1KΩ (typ.)
TEST	Input		Pull-down resistor R_{IN} = 70KΩ (typ.) R = 1KΩ (typ.)

(2) I/O Ports

The input/output circuitries of the 4720/40 I/O ports are shown below, any one of the circuitries can be chosen by a code as a mask option.

PORT	I/O	INPUT/OUTPUT CIRCUITRY and CODE	REMARKS
K0	Input	AA:  AE, AH:  AF, AI: 	Pull-up/pull-down resistor R_{IN} = 100KΩ (typ.) R = 1KΩ (typ.)
P1 P2	Output		Sink open drain output Initial "Hi-Z" High current I_{OL} = 20mA (typ.)
R4 R5 R6	I/O	AA, AE, AF (Initial "High"), AH, AI (Initial "Low"): 	Sink open drain output Pull-up resistor R_L = 5KΩ (typ.) R = 1KΩ (typ.)
R7	I/O		Sink open drain output Initial "Hi-Z" R = 1KΩ (typ.)
R8 R9	I/O		Sink open drain output Initial "Hi-Z" Hysteresis input R = 1KΩ (typ.)