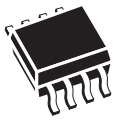
STTS75

Digital temperature sensor and thermal watchdog

Features

- Measures temperatures from –55°C to +125°C (–67°F to +257°F)
  - ±2°C Accuracy from –25°C to +100°C (max)
- Low operating current: 75µA (typ)
- No external components required
- 2-wire I^2C/SMBus-compatible serial interface
  - Selectable serial bus address allows connection of up to eight devices on the same bus
- Thermometer resolution is user-configurable from 9 (Default) to 12 bits (0.5°C to 0.0625°C)
- 9-bit conversion time is 45ms (typ)
- Programmable temperature threshold and hysteresis set points
- Wide power supply range-operating voltage range: 2.7V to 5.5V
- Power saving one-shot temperature measurement
- Power up defaults permit stand-alone operation as thermostat
- Shutdown mode to minimize power consumption
- Separate open drain output pin operates as an interrupt or comparator/thermostat output (dual purpose event pin)
- Packages:
  - SO8
  - MSOP8 (TSSOP8)[a]



SO8 (M)

MSOP8 (TSSOP8)
(DS)

a. Contact local ST sales office for availability

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1 Summary description

The STTS75 is a high-precision CMOS (Digital) temperature sensor IC with a Delta-Sigma analog-to-digital (ADC) converter and an I^2C-compatible serial digital interface (see *Figure 1 on page 7*). It is targeted for general applications such as personal computers, system thermal management, electronics equipment, and industrial controllers, and is packaged in the industry standard 8-lead TSSOP and SO8 packages (see *Figure 2 on page 8*).

The device contains a band gap temperature sensor and programmable 9-to 12-bit ADC which monitor and digitize the temperature to a resolution up to 0.0625°C. The STTS75 is typically accurate to (±3°C - max) over the full temperature measurement range of –55°C to 125°C with ±2°C accuracy in the –25°C to +100°C range. At power-up, the STTS75 defaults to 9-bit resolution for software compatibility with the STLM75.

STTS75 is specified for operating at supply voltages from 2.7V to 5.5V. Operating at 3.3V, the supply current is typically (75µA).

The on-board delta sigma analog-to-digital converter (ADC) converts the measured temperature to a digital value that is calibrated in °C; for Fahrenheit applications a lookup table or conversion routine is required.

The STTS75 is factory-calibrated and requires no external components to measure temperature.

1.1 Serial communications

The STTS75 has a simple 2-wire I^2C-compatible digital serial interface which allows the user to access the data in the temperature register at any time. It communicates via the serial interface with a master controller which operates at speeds up to 400kHz. Three pins (A0, A1, and A2) are available for address selection, and enable the user to connect up to 8 devices on the same bus without address conflict.

In addition, the serial interface gives the user easy access to all STTS75 registers to customize operation of the device.

1.2 Temperature sensor output

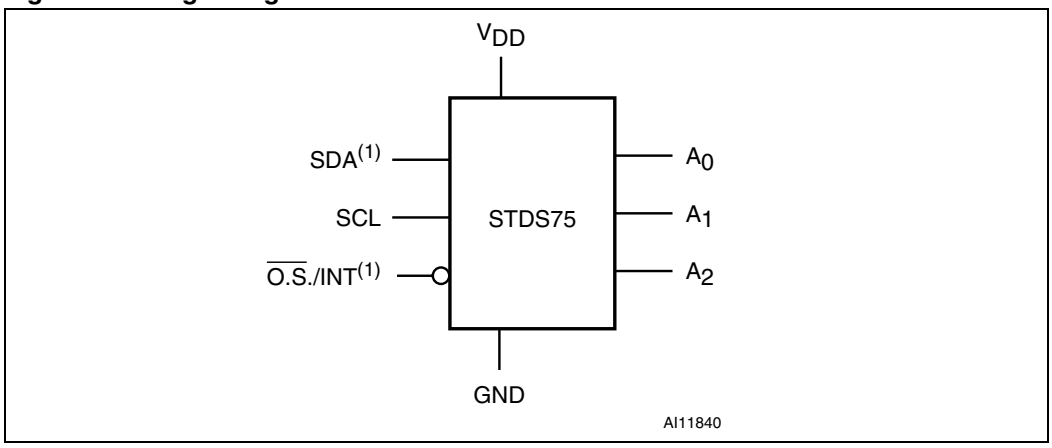
The STTS75 Temperature Sensor has a dedicated open drain Over-Limit Signal/Alert ($\overline{OS}$/INT/Alert) output which features a thermal Alarm function. This function provides a user-programmable trip and turn-off temperature. It can operate in either of two selectable modes:

- *Section 2.3: Comparator mode*, and
- *Section 2.4: Interrupt mode*.

At power-up the STTS75 comes up in 9-bit mode and immediately begins measuring the temperature and converting the temperature to a digital value. The resolution of the digital output data is user-configurable to 9, 10, 11, or 12 bits which correspond to temperature increments of 0.5°C, 0.25°C, 0.125°C, and 0.0625°C, respectively.

The measured temperature value is compared with a temperature limit (which is stored in the 16-bit (T_{OS}) READ/WRITE register), and the hysteresis temperature (which is stored in the 16-bit (T_{HYS}) READ/WRITE register). If the measured value exceeds these limits, the $\overline{OS}$/INT pin is activated (see *Figure 3 on page 8*).

Figure 1. Logic diagram



1. SDA and $\overline{OS}$/INT are open drain.

Note: See Pin descriptions on page 9 for details.

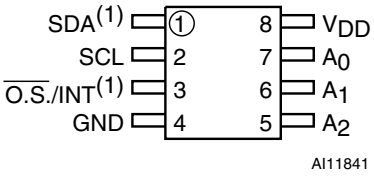
Table 1. Signal names

Pin	Symbol/Name	Type/Direction	Description
1	SDA(1)	Input/ Output	Serial data input/output
2	SCL	Input	Serial clock input
3	$\overline{OS}$/INT(1)	Output	Over-limit signal/interrupt alert output
4	GND	Supply ground	Ground
5	A_2	Input	Address2 input
6	A_1	Input	Address1 input
7	A_0	Input	Address0 input
8	V_{DD}	Supply power	Supply voltage (2.7V to 5.5V)

1. SDA and $\overline{OS}$/INT are open drain.

Note: See Pin descriptions on page 9 for details.

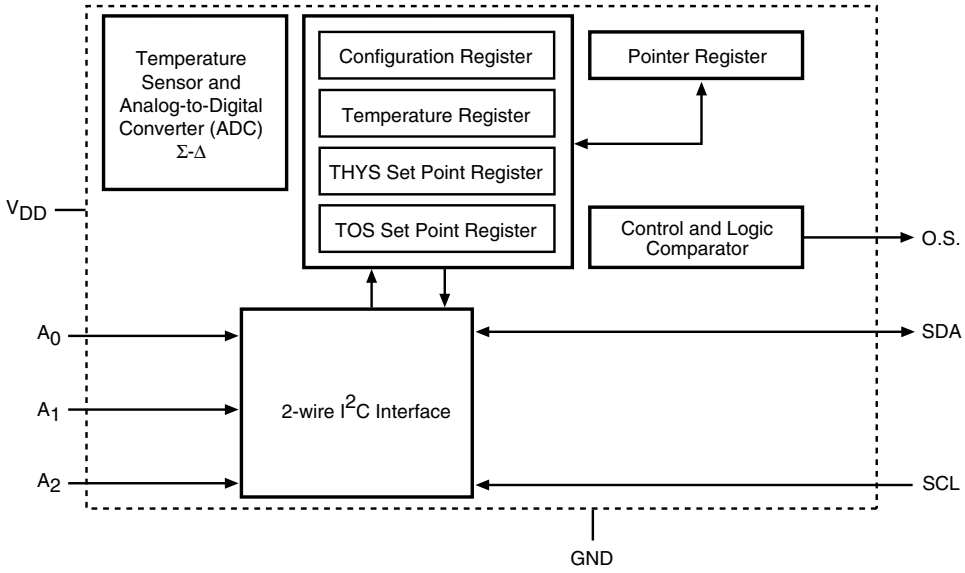
Figure 2. Connections (SO8, TSSOP8)



1. SDA and $\overline{OS}$/INT are open drain.

Note: See Pin descriptions on page 9 for details.

Figure 3. Functional block diagram



1.3 Pin descriptions

See *Figure 1 on page 7* and *Table 1 on page 7* for a brief overview of the signals connected to this device.

1.3.1 SDA (open drain)

This is the Serial Data Input/Output pin for the 2-wire serial communication port.

1.3.2 SCL

This is the Serial Clock Input pin for the 2-wire serial communication port.

1.3.3 $\overline{OS}$/INT (open drain)

This is the Over-Limit Signal/Interrupt Alert Output pin. It is open drain, so it needs a pull-up resistor.

Note: The open drain thermostat output that indicates if the temperature has exceeded user-programmable limits (Over/Under Temperature indicator).

1.3.4 GND

Ground; it is the reference for the power supply. It must be connected to system ground.

1.3.5 A2, A1, A0

A2, A1, and A0 are selectable address pins for the 3LSBs of the I^2C interface address. They can be set to V_{DD} or GND to provide 8 unique address selections.

1.3.6 V_{DD}

This is the supply voltage pin, and ranges from +2.7V to +5.5V.

2 Operation

After each temperature measurement and analog-to-digital conversion, the STTS75 stores the temperature as a 16-bit two's complement number in the 2-byte temperature register. The most significant Bit (S, Bit 15) indicates if the temperature is positive or negative:

- for positive numbers S = 0, and
- for negative numbers S = 1.

The most recently converted digital measurement can be read from the temperature register at any time. Since temperature conversions are performed in the background, reading the temperature register does not affect the operation in progress.

Bits 3 through 0 of the temperature register are hardwired to logic '0.' When the STTS75 is configured for 12-bit resolution, the 12MSBs (Bits 15 through 4) of the temperature register will contain temperature data. For 11-bit resolution, the 11MSBs (Bits 15 through 5) of the temperature register will contain data, and Bit 4 will read out as logic '0.' For 10-bit resolution, the 10MSbs (Bits 15 through 6) will contain data, and for 9-bit resolution the 9MSbs (Bits 15 through 7) will contain data and all unused LSBs will contain '0s.'

Table 4 on page 15 gives examples of 12-bit resolution digital output data and the corresponding temperatures. The data is compared to the values in the T_{OS} and T_{HYS} registers, and then the $\overline{OS}$/INT is updated based on the result of the comparison and the operating mode. The number of T_{OS} and T_{HYS} bits used during the thermostat comparison is equal to the conversion resolution set by the FT1 and FT0 Bits in the Configuration register. For example, if the resolution is 9 bits, only the 9MSbs of T_{OS} and T_{HYS} will be used by the thermostat comparator. The alarm fault tolerance is controlled by the FTI and FTO Bits in the Configuration register. They are used to set up a fault queue. This prevents false tripping of the $\overline{OS}$/INT pin when the STTS75 is used in a noisy environment (see *Table 2 on page 14*).

The STTS75 also supports a special one-shot mode feature that performs a single temperature measurement and returns to shutdown mode. This is especially useful for low-power applications. This features is accessed by first putting the device in shutdown mode, then enabling the one-shot mode (OSM) bit in the configuration register.

The active state of the $\overline{OS}$/INT output can be changed via the Polarity (POL) Bit in the Configuration register. The power-up default is active-low.

If the user does not wish to use the thermostat capabilities of the STTS75, the $\overline{OS}$/INT output should be left floating.

Note: If the thermostat is not used, the T_{OS} and T_{HYS} registers can be used for general storage of system data.

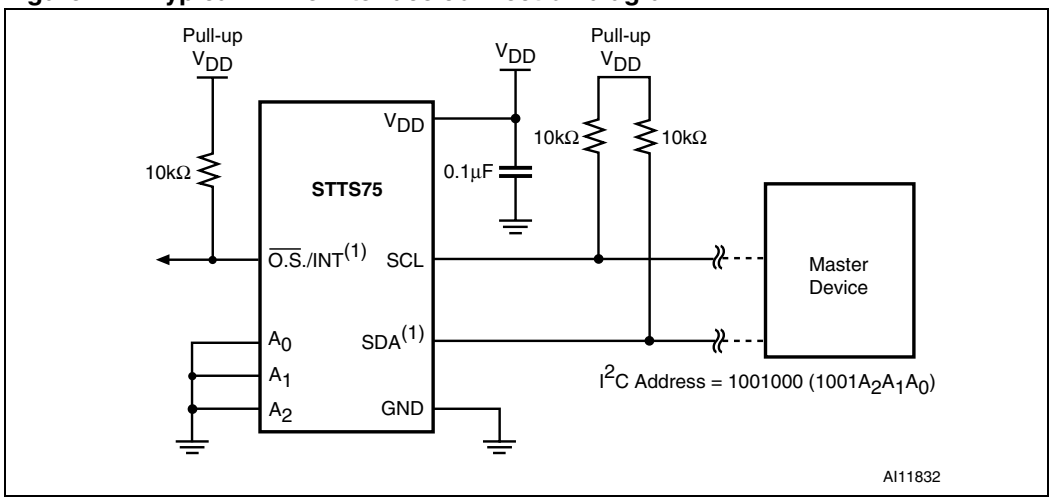
2.1 Applications information

STTS75 digital Temperature Sensors are optimal for thermal management and thermal protection applications. They require no external components for operations except for pull-up resistors on SCL, SDA, and $\overline{OS}$/INT outputs. A 0.1µF bypass capacitor is recommended. The sensing device of STTS75 is the chip itself. The typical interface connection for this type of digital sensor is shown in *Figure 4 on page 11*.

Intended Applications include:

- System Thermal Management
- Computers/Disk Drivers
- Electronics/Test Equipment
- Power Supply Modules
- Consumer Products
- Battery Management
- FAX/Printers Management
- Automotive

Figure 4. Typical 2-wire interface connection diagram



1. SDA and $\overline{OS}$/INT are open drain.

2.2 Thermal alarm function

The STTS75 thermal alarm function provides user-programmable thermostat capability and allows the STTS75 to function as a standalone thermostat without using the serial interface. The $\overline{OS}$/INT output is the alarm output. This signal is an open drain output, and at power-up, this pin is configured with active-low polarity by default.

2.3 Comparator mode

In Comparator mode, each time a temperature-to-digital (T-to-D) temperature conversion occurs, the new digital temperature is compared to the value stored in the T_{OS} and T_{HYS} registers. If a fault tolerance number of consecutive temperature measurements are greater than the value stored in the T_{OS} register, the $\overline{OS}$/INT output will be activated.

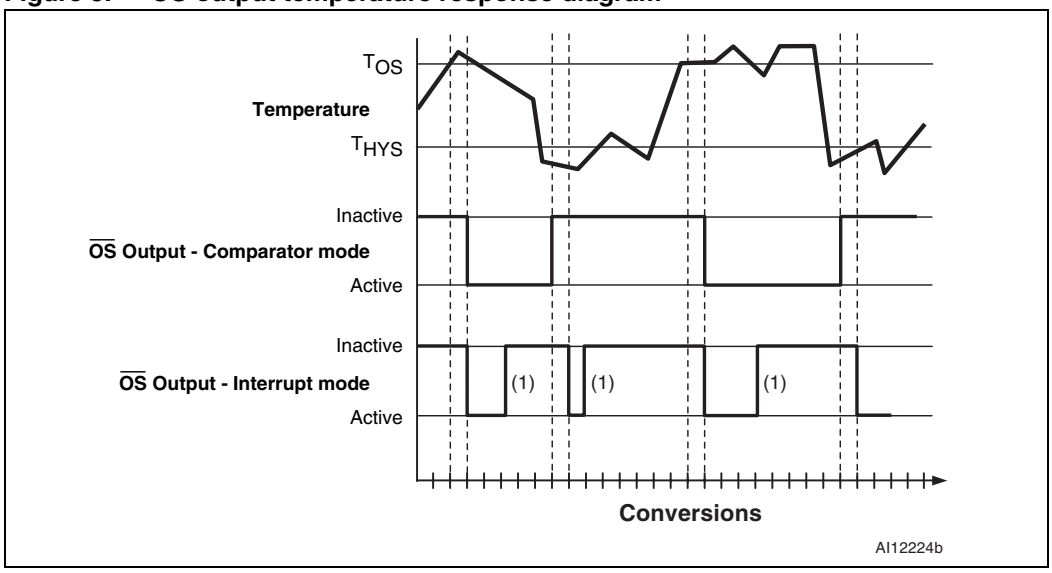
For example, if the FT1 and FT0 Bits are equal to “10” (fault tolerance = 4), four consecutive temperature measurements must exceed T_{OS} to activate the $\overline{OS}$/INT output. Once the $\overline{OS}$/INT output is active, it will remain active until the first time the measured temperature drops below the temperature stored in the T_{HYS} register.

When the thermostat is in comparator mode, the $\overline{OS}$/INT can be programmed to operate with any amount of hysteresis. The $\overline{OS}$/INT output becomes active when the measured temperature exceeds the T_{OS} value a consecutive number of times as defined by the FT1 and FT0 fault tolerance (FT) Bits in the configuration register. The $\overline{OS}$/INT then stays active when the temperature falls below the value stored in T_{HYS} register for a consecutive number of times as defined by the fault tolerance bits (FT1 and FT0). Putting the device into shutdown mode does not clear $\overline{OS}$/INT in comparator mode.

2.4 Interrupt mode

In Interrupt mode, the $\overline{OS}$/INT output first becomes active when the measured temperature exceeds the T_{OS} value a consecutive number of times equal to the FT value in the Configuration register. Once activated, the $\overline{OS}$/INT can only be cleared by either putting the STTS75 into shutdown mode or by reading from any register (temperature, configuration, T_{OS}, or T_{HYS}) on the device. Once the $\overline{OS}$/INT has been deactivated, it will only be reactivated when the measured temperature falls below the T_{HYS} value a consecutive number of times equal to the FT value. *Figure 5* illustrates typical $\overline{OS}$ output temperature response for STTS75 configured to have a fault tolerance of 2. The interrupt/clear process is cyclical between T_{OS} and T_{HYS}.

Figure 5. $\overline{OS}$ output temperature response diagram



1. This assumes that a READ has occurred.

Note: The STTS75 is configured to have a fault tolerance of 2 in this example.

2.5 Fault tolerance

For both Comparator and Interrupt modes, the alarm “fault tolerance” setting plays a role in determining when the $\overline{OS}$/INT output will be activated. Fault tolerance refers to the number of consecutive times an error condition must be detected before the user is notified. Higher fault tolerance settings can help eliminate false alarms caused by noise in the system. The alarm fault tolerance is controlled by the bits (Bits 4 and 3) in the Configuration Register. These bits can be used to set the fault tolerance to 1, 2, 4, or 6 as shown in *Table 2*. At power-up, these bits both default to logic '0.'

Table 2. Fault tolerance setting

FT1	FT0	STTS75 (Consecutive Faults)	Comments
0	0	1	Power-up default
0	1	2	
1	0	4	
1	1	6	

2.6 Shutdown mode

For power-sensitive applications, the STTS75 offers a low-power shutdown mode. The SD Bit in the Configuration register controls shutdown mode. When SD is changed to login '1,' the conversion in progress will be completed and the result stored in the temperature register, after which the STTS75 will go into a low-power standby state. The $\overline{OS}$/INT output will be cleared if the thermostat is operating in Interrupt mode and the $\overline{OS}$/INT will remain unchanged in Comparator mode. The 2-wire interface remains operational in shutdown mode, and writing a '0' to the SD Bit returns the STTS75 to normal operation.

Table 3. Shutdown mode and one-shot mode description

Operational mode	One-shot mode (OSM) (bit 7)	Shutdown (SD) (bit 0)
Continuous conversion	0	0
Shutdown (1)	0	1
Continuous conversion	1	0
One-shot	1	1

1. The shutdown command needs to be programmed before sending a one-shot command.

2.7 Temperature data format

Table 4 shows the relationship between the output digital data and the external temperature for 12-bit resolution.

Temperature data for Temperature, T_{OS} and T_{HYS} Registers is represented by 9-bit, 10-bit, 11-bit, and 12-bit depending upon the resolution bits RC1, RC0 (Bits 6 and 5) in the Configuration Register (see *Table 7 on page 17*). The default resolution is 9-bits.

The left-most bit in the output data stream controls temperature polarity information for each conversion. If the Sign Bit is '0', the temperature is positive and of the Sign Bit is '1', the temperature is negative.

Table 4. Relationship between temperature and digital output

Temperature	Sign	Number of Bits used by Conversion Resolution		9	10	11	12	Always Zero	Digital output (HEX)
	12-Bit Resolution							0000	
	11- Bit Resolution						0	0000	
	10-Bit Resolution					0	0	0000	
	9-Bit Resolution				0	0	0	0000	
+125°C	0	111	1101	0	0	0	0	0000	7D00
+25.0625°C	0	001	1001	0	0	0	1	0000	1910
+10.125°C	0	000	1010	0	0	1	0	0000	0A20
+0.5°C	0	000	0000	1	0	0	0	0000	0080
0°C	0	000	0000	0	0	0	0	0000	0000
–0.5°C	1	111	1111	1	0	0	0	0000	FF80
–10.25°C	1	111	0101	1	1	1	0	0000	F5E0
–25.0625°C	1	110	0110	1	1	1	1	0000	E6F0
–55°C	1	100	1001	0	0	0	0	0000	C900

2.8 Bus timeout feature

The STTS75 supports an SMSBus compatible timeout function which will reset the serial I^2C/SMBus interface if SDA is held low for a period greater than the timeout duration between a START and STOP condition. If this occurs, the device will release the bus and wait for another START condition.

3 Functional description

The STTS75 registers have unique pointer designations which are defined in *Table 6 on page 16*. Whenever any READ/WRITE operation to the STTS75 register is desired, the user must “point” to the device register to be accessed.

All of these user-accessible registers can be accessed via the digital serial interface at anytime (see *Serial interface on page 20*), and they include:

- Command Register/Address Pointer Register
- Configuration Register
- Temperature Register
- Over-Limit Signal Temperature Register (T_{OS})
- Hysteresis Temperature Register (T_{HYS})

3.1 Registers and register set formats

3.1.1 Command/pointer register

The Most Significant Bits (MSBs) of the Command Register must always be zero. Writing a '1' into any of these bits will cause the current operation to be terminated (see *Table 5*).

The Command Register retains pointer information between operations. Therefore, this register only needs to be updated once for consecutive READ operations from the same register. All bits in the Command Register default to '0' at power-up.

Table 5. Command/pointer register format

MSB							LSB
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
0	0	0	0	0	0	P1	P0
						Pointer	

Table 6. Register pointers selection summary

Pointer Value (H)	P1	P0	Name	Description	Width (Bits)	Type (R/W)	Power-on default	Comments
00	0	0	TEMP	Temperature Register	16	Read only	N/A	To store Measured Temperature Data
01	0	1	CONF	Configuration Register	8	R/W	00	
02	1	0	T_{HYS}	Hysteresis Register	16	R/W	4800	Default = 75°C
03	1	1	T_{OS}	Over-temperature Shutdown	16	R/W	5000	Set point for Over-temperature Shutdown (T_{OS}) limit default = 80°C

3.1.2 Configuration register

The Configuration register is used to store the device settings such as Device Operation mode, $\overline{OS}$/INT Operation mode, $\overline{OS}$/INT Polarity, and $\overline{OS}$/INT Fault Queue.

The Configuration register allows the user to program various options such as conversion resolution (see *Table 8*), thermostat fault tolerance, thermostat polarity, thermostat operating mode, and shutdown mode. The user has READ/WRITE access to all of the bits in the Configuration register. The entire register is volatile and thus powers-up in its default state only.

Table 7. Configuration register format

Byte	MSB							LSB
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
STTS75	OSM	RC1	RC0	FT1	FT0	POL	M	SD
Default	0	0	0	0	0	0	0	0

Keys: SD =Shutdown Control Bit
M =Thermostat Mode(1)
POL =Output Polarity(2)
FT0 =Fault Tolerance0 Bit
FT1 =Fault Tolerance1 Bit
RC0 =Resolution Conversion0 Bit
RC1 =Resolution Conversion1 Bit
OSM =One-shot mode bit

1. Indicates Operation mode; 0 = Comparator mode, and 1 = Interrupt mode (see *Comparator mode* and *Interrupt mode on page 13*).
2. The $\overline{OS}$/INT is active-low ('0').

Table 8. Programmable resolution configurations

RC1	RC0	Resolution		Conversion Time (max)	Remarks
0	0	9-bit	0.5°C	85ms	Default Resolution
0	1	10-bit	0.25°C	170ms	
1	0	11-bit	0.125°C	340ms	
1	1	12-bit	0.0625°C	680ms	

3.1.3 Temperature register

The Temperature Register is a two-byte (16-bit) “Read only” register (see *Table 9 on page 18*). Digital temperatures from the ADC are stored in the Temperature Register in two’s complement format, and the contents of this register are updated each time the A/D conversion is finished.

The user can read data from the Temperature Register at any time. When a A/D conversion is completed, the new data is loaded into a comparator buffer to evaluate fault conditions, and will update the Temperature Register if a read cycle is not ongoing. The STTS75 is continuously evaluating fault conditions regardless of READ or WRITE activity on the bus. If a READ is ongoing, the previous temperature will be read. The readable temperature will be updated upon the completion of the next A/D conversion that is not masked by a read cycle.

Depending on the A/D conversion resolution, the 9-, 10-, 11- or 12-bit MSBs of the register will contain temperature data. All unused bits following the digital temperature will be zero. The MSB (Bit 15) of the Temperature Register denotes whether the temperature data is positive or negative. A '0' in Bit 15 is positive and a '1' is negative.

Table 9. Temperature register format

Bytes	MS Byte								LS Byte							
Bits	MSB	THSB							TLSB							LSB
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STTS75	SB	TMSB	TD	TD	TD	TD	TD	TD	9-bit LSB	10-bit LSB	11-bit LSB	12-bit LSB	0	0	0	0

Keys: SB =Two’s complement Sign Bit
TMSB =Temperature MSB
TLSB =Temperature LSB
TD =Temperature Data

3.1.4 Over-limit temperature register (T_{OS})

The T_{OS} Register is a two-byte (16-bit) READ/WRITE register that stores the user-programmable upper trip-point temperature for the thermal alarm in two’s complement format (see *Table 10 on page 19*). This register defaults to 80°C at power-up (i.e., 0101 0000 0000 0000).

The format of the T_{OS} Register is identical to that of the Temperature Register. The 4 LSBs of the T_{OS} Register are hardwired to zero, so data written to these register bits will be ignored. The MSB position contains the sign bit for the digital temperature and Bit14 contains the temperature MSB.

The resolution setting for the A/D conversion determines how many bits of the T_{OS} Register are used by the thermal alarm. For example, for 9-bit conversions, the trip-point temperature is defined by the 9 MSBs of the T_{OS} register, and all remaining bits are “Don’t cares.”

3.1.5 Hysteresis temperature register (T_{HYS})

T_{HYS} Register is a two-byte (16-bit) READ/WRITE register that stores the user-programmable lower trip-point temperature for the thermal alarm in two's complement format (see *Table 10*). This register defaults to 75°C at power-up (i.e., 0100 1011 0000 0000).

The format of this register is the same as that of the Temperature Register. The 4 LSBs of the T_{HYS} Register are hardwired to zero, so data written to these bits is ignored. The MSB position contains the sign bit for the digital temperature and Bit14 contains the temperature MSB.

The resolution setting for the A/D conversion determines how many bits of the T_{HYS} Register are used by the thermal alarm. For example, for 9-bit conversions, the hysteresis temperature is defined by the 9 MSBs of the T_{HYS} Register, and all remaining bits are "Don't cares."

Table 10. T_{OS} and T_{HYS} register format

Bytes	MS Byte								LS Byte							
Bits	MSB	THSB							TLSB							LSB
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STTS75	SB	TMSB	TD	TD	TD	TD	TD	TD	9-bit LSB	10-bit LSB	11-bit LSB	12-bit LSB	0	0	0	0

Keys: SB =Two's complement Sign Bit
TMSB =Temperature MSB
TLSB =Temperature LSB
TD =Temperature Data

3.2 Power-up default conditions

The STTS75 always powers up in the following default states:

- Thermostat mode = Comparator Mode
- Polarity = Active-low
- Fault tolerance = 1 fault (i.e., relevant bits set to '0' in the Configuration register)
- T_{OS} = 80°C
- T_{HYS} = 75°C
- OSM = 0 (disabled)
- Register pointer = 00 (Temperature register)
- Conversion resolution = 9-bit (i.e., RC0 = 0 and RC1 = 0 in the Configuration register; see *Table 7 on page 17*)

Note: After power-up these conditions can be reprogrammed via the serial interface.

3.3 Serial interface

Writing to and reading from the STTS75 registers is accomplished via the two-wire serial interface protocol which requires that one device on the bus initiates and controls all READ and WRITE operations. This device is called the “master” device. The master device also generates the SCL signal which provides the clock signal for all other devices on the bus. These other devices on the bus are called “slave” devices. The STTS75 is a slave device (see *Table 11*). Both the master and slave devices can send and receive data on the bus.

During operations, one data bit is transmitted per clock cycle. All operations follow a repeating, nine-clock-cycle pattern that consists of eight bits (one byte) of transmitted data followed by an acknowledge (ACK) or not acknowledge (NACK) from the receiving device.

Note: There are no unused clock cycles during any operation, so there must not be any breaks in the data stream and ACKs/NACKs during data transfers. Conversely, having too few clock cycles can lead to incorrect operation if an inadvertent 8-bit READ from a 16-bit register occurs.

Table 11. STTS75 serial bus slave addresses

MSB							LSB
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
1	0	0	1	A2	A1	A0	R/W

3.4 2-wire bus characteristics

The bus is intended for communication between different ICs. It consists of two lines: a bi-directional data signal (SDA) and a clock signal (SCL). Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

- The following protocol has been defined:
- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is High.
- Changes in the data line, while the clock line is High, will be interpreted as control signals.

Accordingly, the following bus conditions have been defined (see *Figure 6 on page 21*):

3.4.1 Bus not busy

Both data and clock lines remain High.

3.4.2 Start data transfer

A change in the state of the data line, from high to Low, while the clock is High, defines the START condition.

3.4.3 Stop data transfer

A change in the state of the data line, from Low to High, while the clock is High, defines the STOP condition.

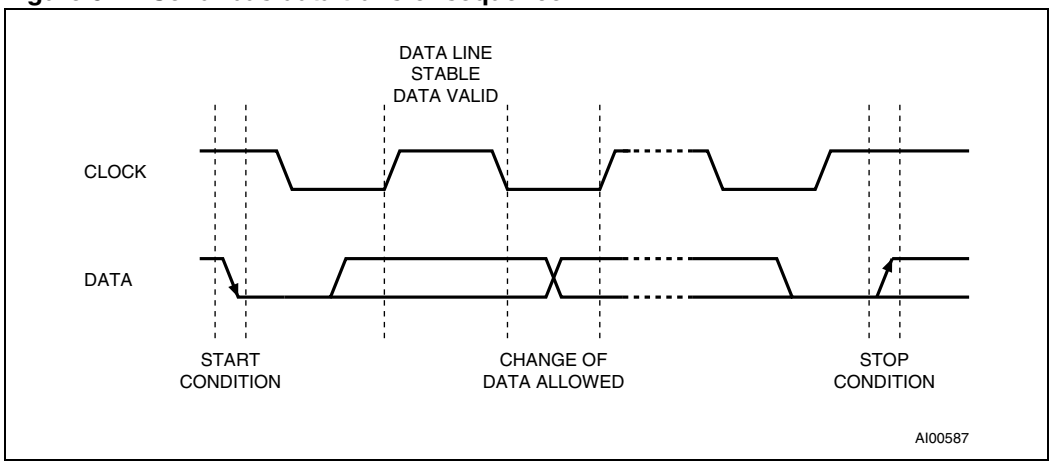
3.4.4 Data valid

The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

By definition a device that gives out a message is called “transmitter,” the receiving device that gets the message is called “receiver.” The device that controls the message is called “master.” The devices that are controlled by the master are called “slaves.”

Figure 6. Serial bus data transfer sequence

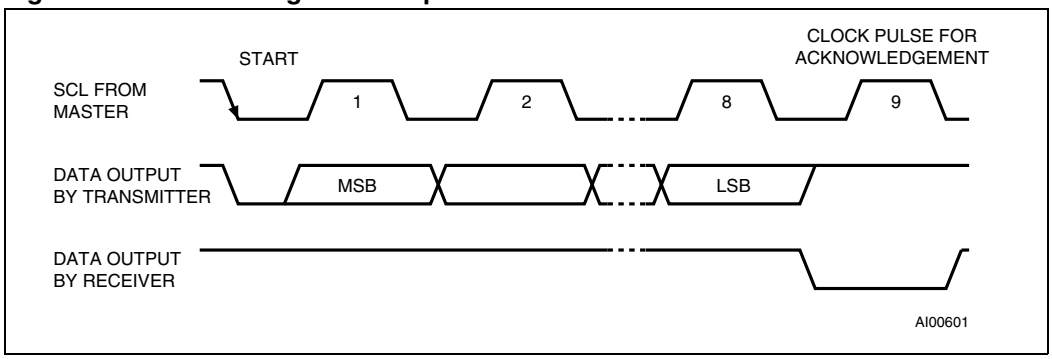


3.4.5 Acknowledge

Each byte of eight bits is followed by one Acknowledge Bit. This Acknowledge Bit is a low level put on the bus by the receiver whereas the master generates an extra acknowledge related clock pulse (see *Figure 7 on page 22*). A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable Low during the High period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line High to enable the master to generate the STOP condition.

Figure 7. Acknowledgement sequence



3.5 READ mode

In this mode the master reads the STTS75 slave after setting the slave address (see *Figure 8*). Following the WRITE mode Control Bit (R/$\overline{W}$=0) and the Acknowledge Bit, the word address 'An' is written to the on-chip address pointer.

There are two READ modes:

- Preset pointer locations (e.g. Temperature, T_{OS} and T_{HYS} registers), and
- Pointer setting (the pointer has to be set for the register that is to be read).

Note: The Temperature register pointer is usually the default pointer.

These modes are shown in the READ mode typical timing diagrams (see *Figure 9*, *Figure 10*, and *Figure 11 on page 24*).

Figure 8. Slave address location

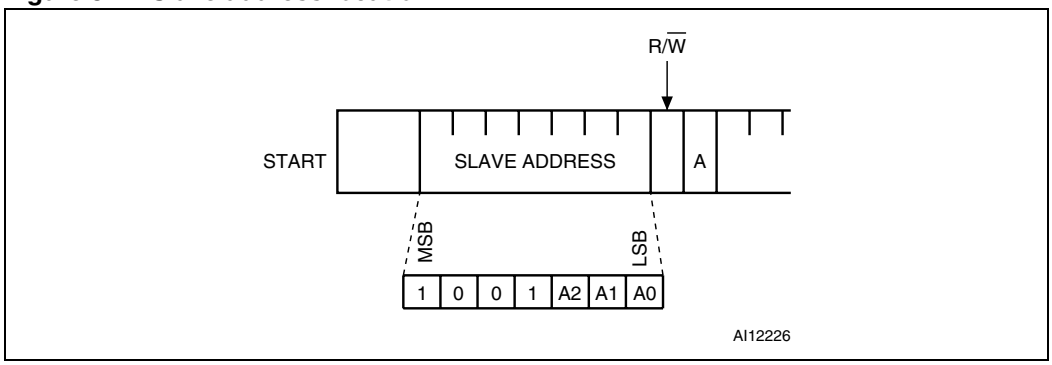


Figure 9. Typical 2-byte READ from preset pointer location (e.g. temp - T_{OS}, T_{HYS})

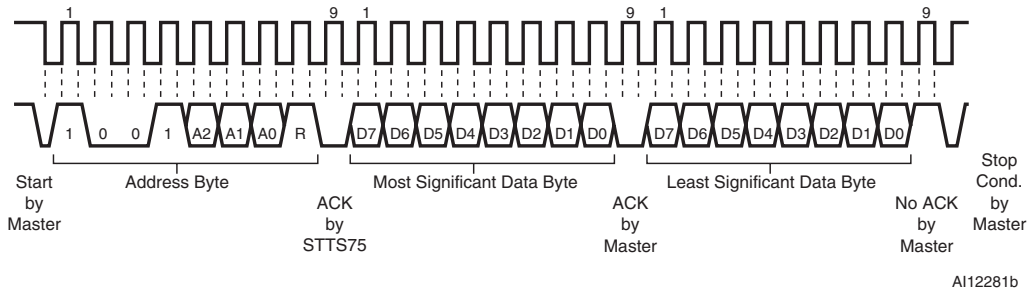


Figure 10. Typical pointer set followed by an immediate READ for 2-byte register (e.g. temp)

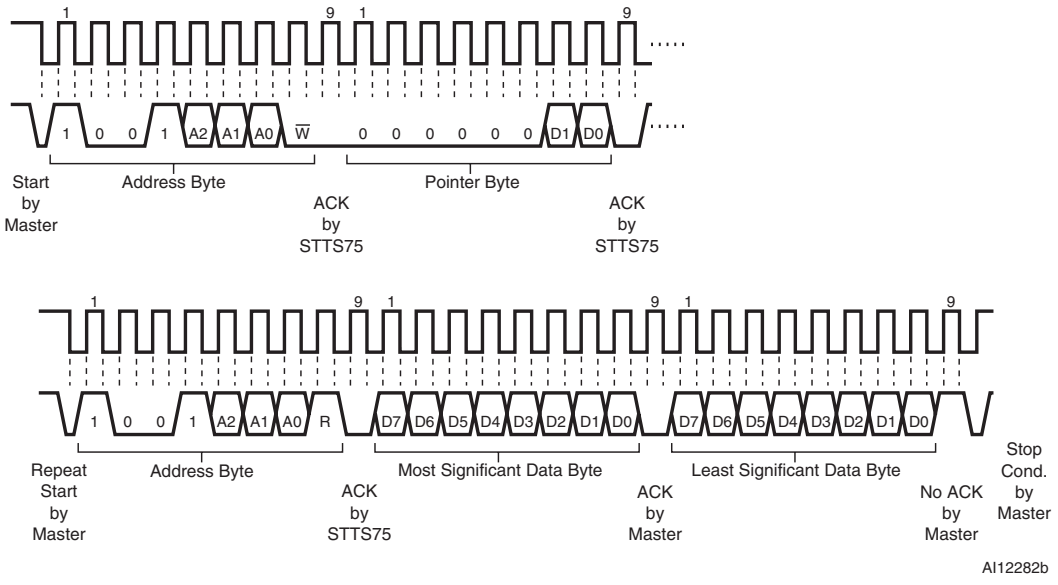
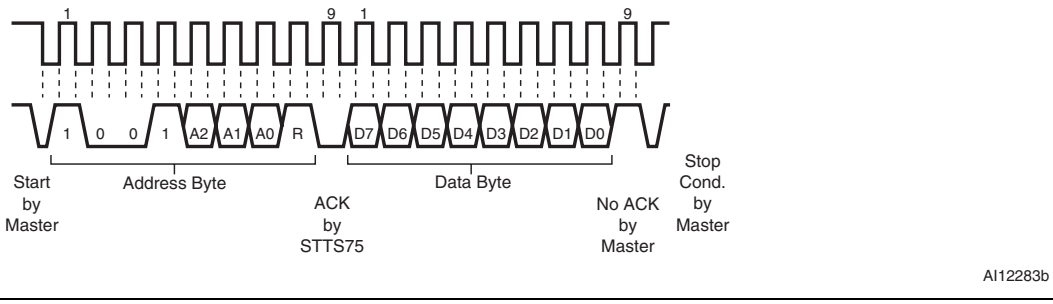


Figure 11. Typical 1-byte READ from the configuration register with preset pointer



3.6 WRITE mode

In this mode the master transmitter transmits to the STTS75 slave receiver. Bus protocol is shown in *Figure 12*. Following the START condition and slave address, a logic '0' (R/$\overline{W}$ = 0) is placed on the bus and indicates to the addressed device that word address will follow and is to be written to the on-chip address pointer.

These modes are shown in the WRITE mode typical timing diagrams (see *Figure 12*, and *Figure 13*, and *Figure 14 on page 26*).

Figure 12. Typical pointer set followed by an Immediate READ from the configuration register

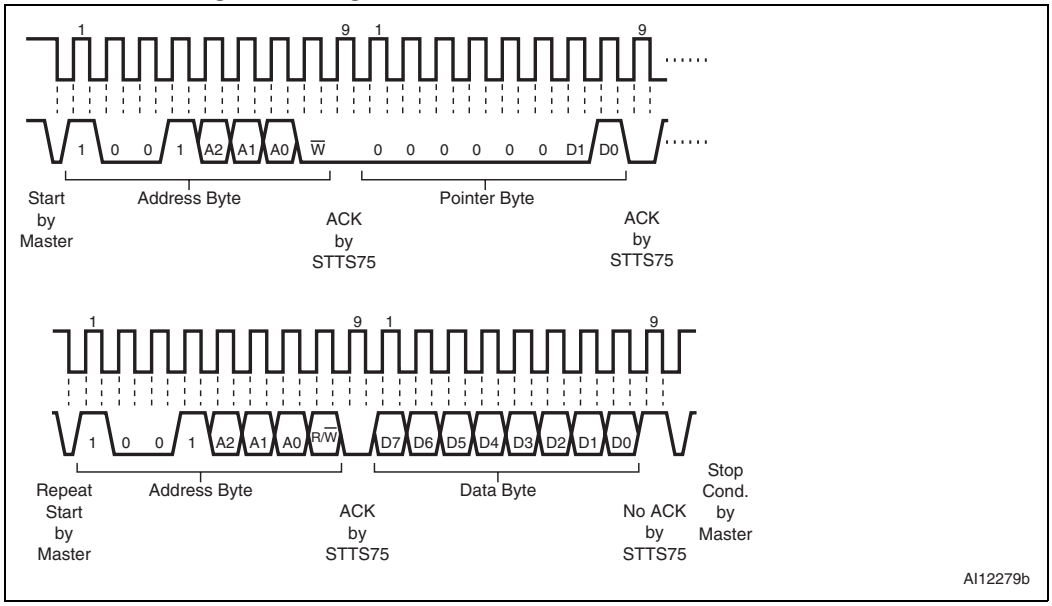


Figure 13. Configuration register WRITE

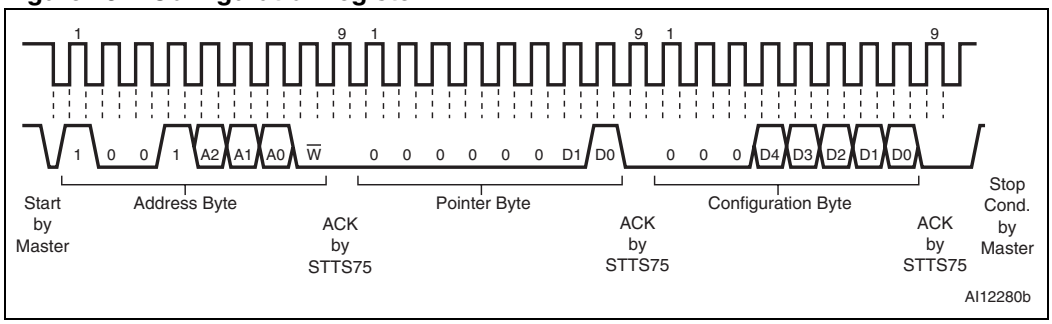
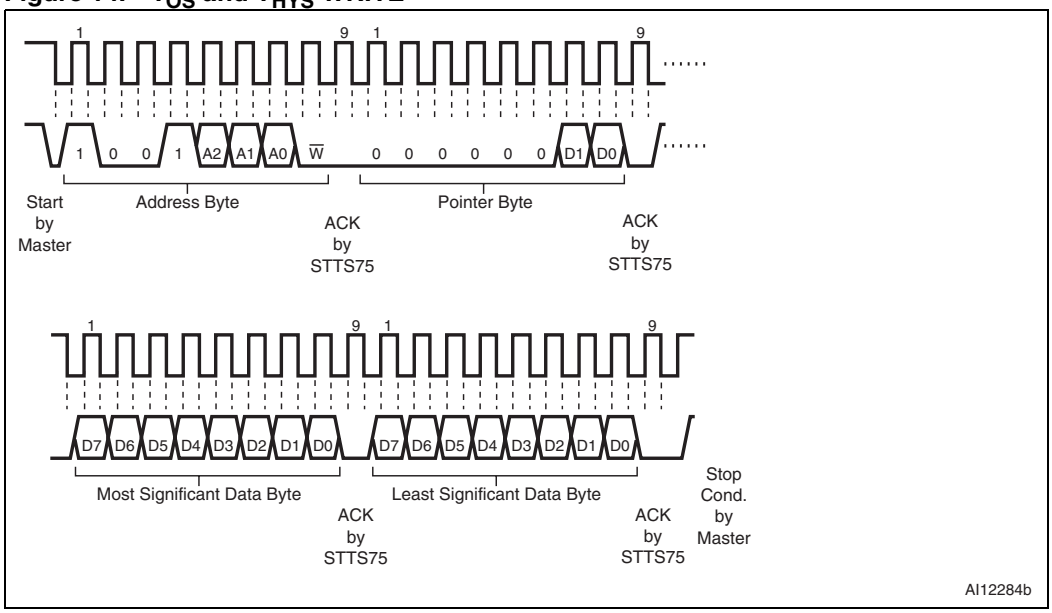
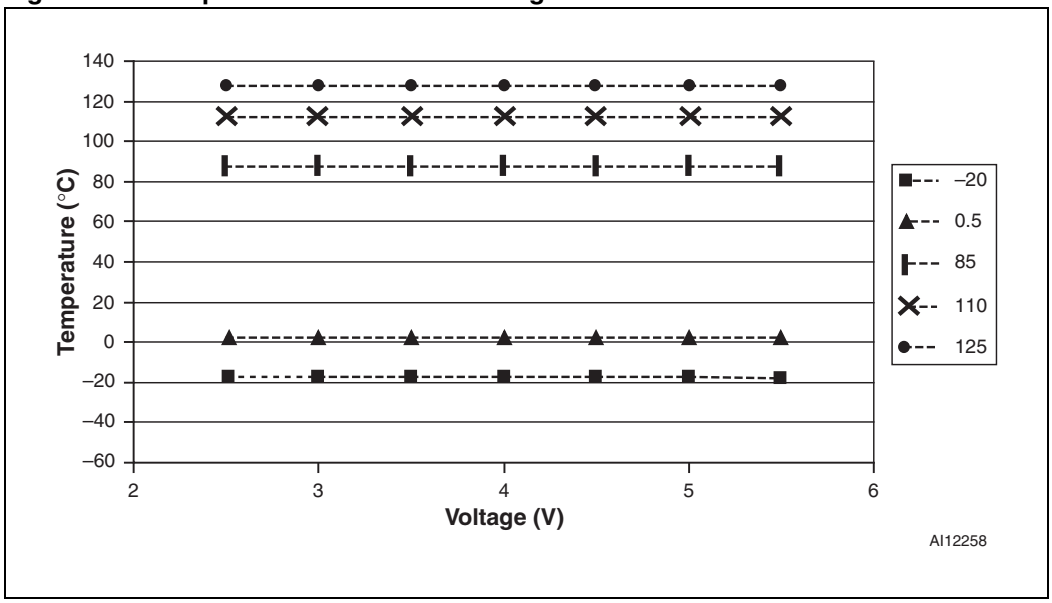


Figure 14. T_{OS} and T_{HYS} WRITE



4 Typical operating characteristics

Figure 15. Temperature variation vs. voltage



5 Maximum rating

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 12. Absolute maximum ratings

Symbol	Parameter	Value	Unit
T_{STG}	Storage temperature	–60 to 150	°C
T_{SLD}(1)	Lead solder temperature for 10 seconds	260	°C
V_{IO}	Input or output voltage	V_{DD} +0.5	V
V_{DD}	Supply voltage	7.0	V
V_{OUT}	Output voltage	V_{DD} + 0.5	V
I_O	Output current	10	mA
P_D	Power dissipation	320	mW

1. Reflow at peak temperature of 255°C to 260°C for < 30 seconds (total thermal budget not to exceed 180°C for between 90 to 150 seconds).

6 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in *Table 13*. Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 13. Operating and AC measurement conditions

Parameter	STTS75	Unit
Supply voltage	2.7 to 5.5	V
Ambient operating temperature (T_A)	–55 to 125	°C
Input rise and fall times	≤ 5	ns
Input pulse voltages	0.2 to 0.8V_{DD}	V
Input and output timing reference voltages	0.3 to 0.7V_{DD}	V

Table 14. DC and AC characteristics

Sym	Description	Test Condition(1)	Min	Typ(2)	Max	Unit
V_{DD}	Supply voltage	T_A = –55 to +125°C	2.7		5.5	V
I_{DD}	V_{DD} supply current, active temperature conversions	V_{DD} = 3.3V		75	100	µA
	V_{DD} supply current, communication only	T_A = 25°C			100	µA
I_{DD1}	Standby supply current, serial port inactive	T_A = 25°C			1.0	µA
	Accuracy for corresponding range 2.7V ≤ V_{DD} ≤ 5.5V	–25°C < T_A < 100			±2.0	°C
		–55°C < T_A < 125			±3.0	°C
	Resolution	9 to 12-bit Temperature Data	0.5		0.0625	°C
			9		12	bits
t_{CONV}	Conversion time	9		45	85	ms
		10		90	170	ms
		11		180	340	ms
		12		360	680	ms
T_{OS}	Over-temperature shutdown	Default Value		80		°C
T_{HYS}	Hysteresis	Default Value		75		°C
V_{OL1}	$\overline{OS}$/INT saturation voltage (V_{DD} = 5V)	4mA sink current			0.5	V
V_{IH}	Input logic high	Digital pins (SCL, SDA, A2-A0)	0.5 x V_{DD}		V_{DD} + 0.5	V
V_{IL}	Input logic low	Digital pins	-0.45		0.3 x V_{DD}	V
V_{OL2}	Output logic low (SDA)	I_{OL2}= 3mA			0.4	V
CIN	Capacitance			5		pF

1. Valid for ambient operating temperature: T_A = –55 to 125°C; V_{DD} = 2.7V to 5.5V (except where noted).
2. Typical number taken at V_{DD} = 3.3V, T_A=25°C

Figure 16. Bus timing requirements sequence

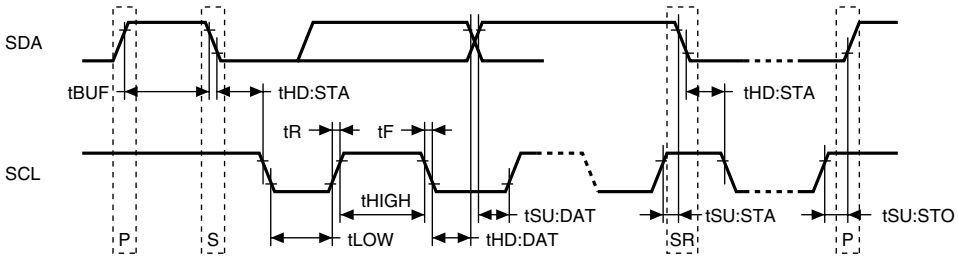


Table 15. AC characteristics

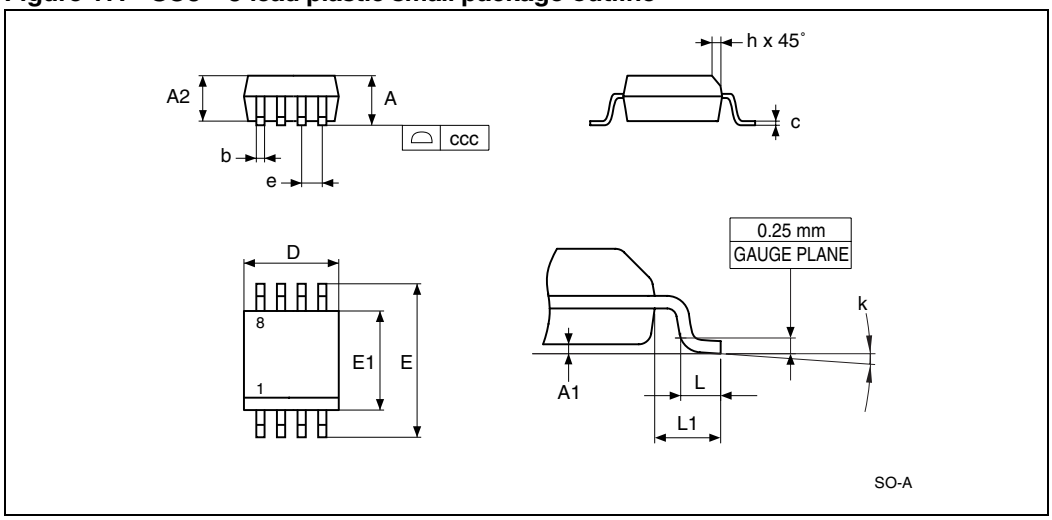
Sym	Parameter[1]	Min	Max	Unit
f_{SCL}	SCL clock frequency	0	400	kHz
t_{BUF}	Time the bus must be free before a new transmission can start	1.3		µs
t_F	SDA and SCL fall time		300	ns
$t_{HD:DAT}$[2]	Data hold time		0.9	µs
$t_{HD:STA}$	START condition hold time (after this period the first clock pulse is generated)	600		ns
t_{HIGH}	Clock high period	600		ns
t_{LOW}	Clock low period	1.3		µs
t_R	SDA and SCL rise time		300	ns
$t_{SU:DAT}$	Data setup time	100		ns
$t_{SU:STA}$	START condition setup time (only relevant for a repeated start condition)	600		ns
$t_{SU:STO}$	STOP condition setup time	600		ns
$t_{TIME-OUT}$	SDA low time for reset of serial interface [3]	75	325	ns

1. Valid for ambient operating temperature: T_A = –55 to 125°C; V_{DD} = 2.7V to 5.5V (except where noted).
2. Transmitter must internally provide a hold time to bridge the undefined region (300ns max) of the falling edge of SCL.
3. For SMBus compatibility STTS75 supports bus timeout. Holding the SDA line low for a period greater than timeout duration will cause STTS75 to reset the SDA line to the state of serial bus communication (SDA high).

7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 17. SO8 – 8-lead plastic small package outline

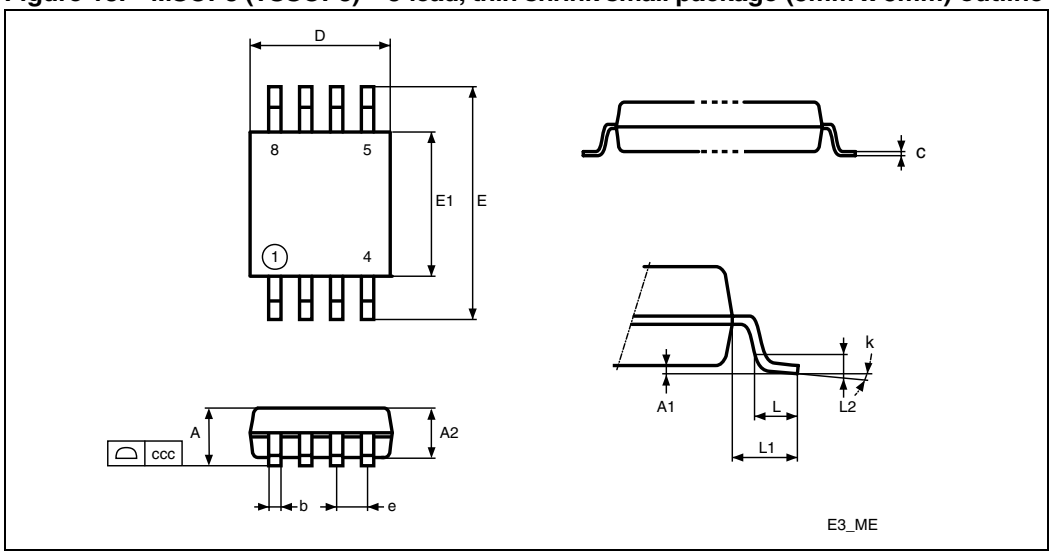


Note: Drawing is not to scale.

Table 16. SO8 – 8-lead plastic small outline package mechanical data

Sym	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.75			0.069
A1		0.10	0.25		0.004	0.010
A2		1.25			0.049	
b		0.28	0.48		0.011	0.019
c		0.17	0.23		0.007	0.009
ccc			0.10			0.004
D	4.90	4.80	5.00	0.193	0.189	0.197
E	6.00	5.80	6.20	0.236	0.228	0.244
E1	3.90	3.80	4.00	0.154	0.150	0.157
e	1.27	–	–	0.050	–	–
h		0.25	0.50		0.010	0.020
k		0°	8°		0°	8°
L		0.40	1.27		0.016	0.050
L1	1.04			0.041		

Figure 18. MSOP8 (TSSOP8) – 8-lead, thin shrink small package (3mm x 3mm) outline



Note: Drawing is not to scale.

Table 17. MSOP8 (TSSOP8) – 8-lead, thin shrink small package (3mm x 3mm) outline mechanical data

Sym	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.10			0.043
A1		0.00	0.15		0.000	0.006
A2	0.85	0.75	0.95	0.034	0.030	0.037
b		0.22	0.40		0.009	0.016
c		0.08	0.23		0.003	0.009
D	3.00	2.80	3.20	0.118	0.110	0.126
E	4.90	4.65	5.15	0.193	0.183	0.203
E1	3.00	2.80	3.10	0.118	0.110	0.122
e	0.65			0.026		
L	0.60	0.40	0.80	0.024	0.016	0.032
L1	0.95			0.037		
L2	0.25			0.010		
k		0°	8°		0°	8°
ccc			0.10			0.004

8 Part numbering

Table 18. Ordering information scheme

Example: STTS75 M 2 F

Device type

STTS75

Package

M = SO8

DS = MSOP8 (TSSOP8)(1)

Temperature range

2 = –55 to 125°C

Shipping method

F = ECOPACK package, Tape & Reel

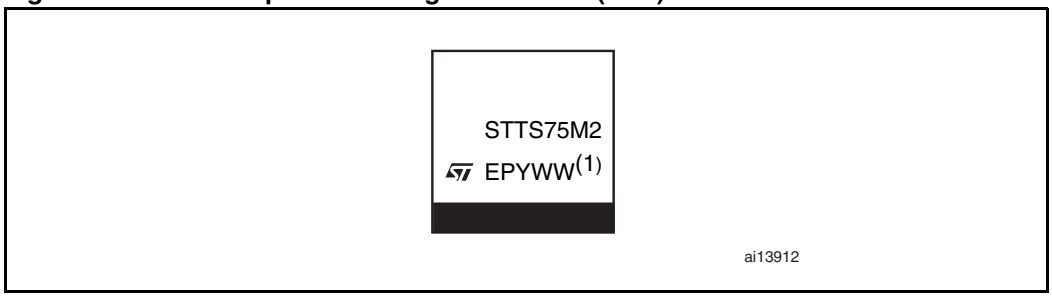
E = ECOPACK package, Tube

1. Contact local ST sales office for availability

For other options, or for more information on any aspect of this device, please contact the ST Sales Office nearest you.

9 Package marking information

Figure 19. Device topside marking information (SO8)



1. Traceability codes

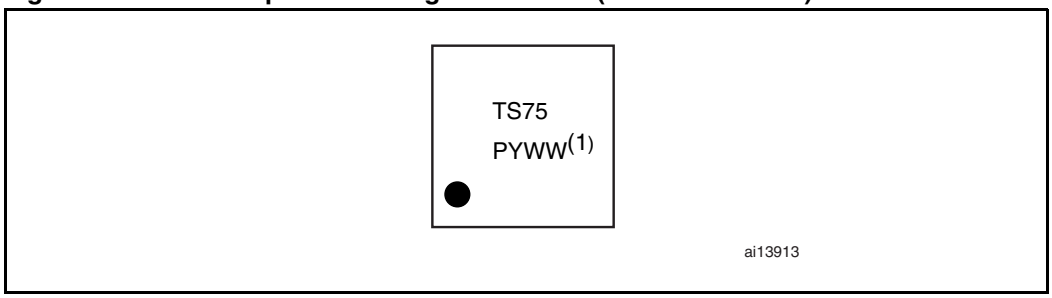
E = Additional information

P = Plant code

Y = Year

WW = Work Week

Figure 20. Device topside marking information (MSOP8/TSSOP8)



1. Traceability codes

P = Plant code

Y = Year

WW = Work Week

10 Revision history

Table 19. Revision history

Date	Revision	Changes
14-Jun-2006	1	Initial release.
22-Jan-2007	2	Update features (cover page), DC and AC characteristics (*Table 14*), package mecanical information (*Figure 17*, *Table 16*, *Figure 18*, *Table 17*) and part numbering (*Table 18*).
01-Mar-2007	3	Update cover page (package information); *Section 2: Operation*; *Section 2.3: Comparator mode*; *Section 2.8: Bus timeout feature*; *Table 14*; package mechanical data (*Figure 18* and *Table 17*); and part numbering (*Table 18*).
18-Apr-2007	4	Package information (DFN8) added to cover page, *Figure 2*, *Figure 19*, *Table 18*. Added*Section 9: Package marking information*. Updated *Table 12*, *13*, *15*, and *18*.
09-May-2007	5	Updated cover page, *Figure 19*, *22*, *Table 14*, and *18*.
16-May-2007	6	Updated cover page, *Figure 4*, *Section 3.1.3*, *Section 3.1.5*, *Table 8*, *14*, and *15*.
06-Jun-2007	7	Updated cover page, document status upgraded to full datasheet, updated *Figure 2*, *Section 7*, *8*, *9*.

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