



STTS424E02

Memory module temperature sensor with a 2 Kb SPD EEPROM

Features

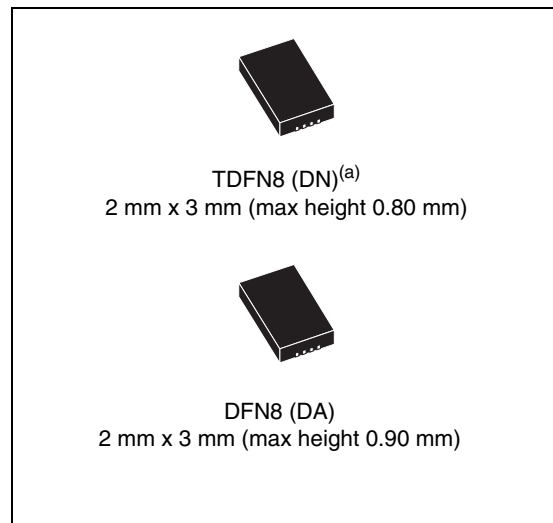
- STTS424E02 includes a JEDEC JC 42.4 compatible temperature sensor, integrated with industry standard 2 Kbit Serial Presence Detect (SPD) EEPROM

Temperature sensor

- Temperature sensor resolution: 0.25°C (typ)/LSB
- Temperature sensor accuracy:
 - ± 1°C from +75°C to +95°C
 - ± 2°C from +40°C to +125°C
 - ± 3°C from -40°C to +125°C
- ADC conversion time: 125 ms (max)
- Supply voltage: 2.7 V to 3.6 V
- Maximum operating supply current: 210 µA (EEPROM inactive)
- Hysteresis selectable set points from: 0, 1.5, 3, 6.0°C
- Ambient temperature sensing range: -40°C to +125°C

2Kb SPD EEPROM

- Functionality identical to ST's M34E02 SPD EEPROM
- Permanent and reversible software data protection for the lower 128 bytes
- Single supply voltage: 2.7 V to 3.6 V
- Byte and page write (up to 16 bytes)
- Self-time WRITE cycle (5 ms, max)
- Automatic address incrementing
- More than 1 million erase/WRITE cycles
- Operating temperature range:
 - -40°C to +85°C (DA package only)
 - -40°C to +125°C (DN package only)



Two-wire bus

- 2-wire SMBus/I²C - compatible serial interface
- Temperature sensor supports SMBus timeout
- Supports up to 400 kHz transfer rate

Packages

- DN: 2 mm x 3 mm TDFN8, height: 0.80 mm (max)^(a)
- DA: 2 mm x 3 mm DFN8, height: 0.90 mm (max)
- RoHS compliant, halogen-free

a. Compliant to JEDEC MO-229, WCED-3

Contents

| | | |
|----------|---|-----------|
| 1 | Description | 6 |
| 2 | Serial communications | 7 |
| 2.1 | Device type identifier (DTI) code | 7 |
| 2.2 | Pin descriptions | 10 |
| 2.2.1 | A0, A1, A2 | 10 |
| 2.2.2 | V _{SS} (ground) | 10 |
| 2.2.3 | SDA (open drain) | 10 |
| 2.2.4 | SCL | 10 |
| 2.2.5 | $\overline{\text{EVENT}}$ (open drain) | 10 |
| 2.2.6 | V _{DD} (power) | 10 |
| 3 | Temperature sensor operation | 11 |
| 3.1 | SMBus/I ² C communications | 11 |
| 3.2 | SMBus/I ² C slave sub-address decoding | 13 |
| 3.3 | SMBus/I ² C AC timing consideration | 14 |
| 4 | Temperature sensor registers | 16 |
| 4.1 | Capability register (read-only) | 17 |
| 4.1.1 | Alarm window trip | 17 |
| 4.1.2 | Critical trip | 17 |
| 4.2 | Configuration register (read/write) | 19 |
| 4.2.1 | Event thresholds | 19 |
| 4.2.2 | Interrupt mode | 19 |
| 4.2.3 | Comparator mode | 19 |
| 4.2.4 | Shutdown mode | 19 |
| 4.2.5 | Event output pin functionality | 22 |
| 4.3 | Temperature register (read-only) | 24 |
| 4.3.1 | Temperature format | 24 |
| 4.4 | Temperature trip point registers (r/w) | 25 |
| 4.5 | Manufacturer ID register (read-only) | 27 |
| 4.6 | Device ID and device revision ID register (read-only) | 27 |

| | | |
|-----------|--|-----------|
| 5 | SPD EEPROM operation | 28 |
| 5.1 | 2 Kb SPD EEPROM operation | 28 |
| 5.2 | Internal device reset - SPD EEPROM | 28 |
| 5.3 | Memory addressing | 29 |
| 5.4 | Setting the write protection | 30 |
| 5.4.1 | SWP and CWP | 31 |
| 5.4.2 | PSWP | 31 |
| 5.5 | Write operations | 31 |
| 5.5.1 | Byte write | 32 |
| 5.5.2 | Page write | 32 |
| 5.5.3 | Minimizing system delays by polling on ACK | 33 |
| 5.6 | Read operations - SPD | 34 |
| 5.6.1 | Random address read - SPD | 34 |
| 5.6.2 | Current address read - SPD | 34 |
| 5.6.3 | Sequential read - SPD | 34 |
| 5.6.4 | Acknowledge in read mode | 34 |
| 6 | Initial delivery state - SPD | 36 |
| 7 | Use in a memory module | 36 |
| 7.1 | Programming the SPD | 36 |
| 7.1.1 | DIMM isolated | 36 |
| 7.1.2 | DIMM inserted in the application motherboard | 37 |
| 8 | Maximum ratings | 39 |
| 9 | DC and AC parameters | 40 |
| 10 | Package mechanical data | 42 |
| 11 | Part numbering | 46 |
| 12 | Package marking information | 47 |
| 13 | Landing pattern | 48 |
| 14 | Revision history | 50 |

List of tables

| | | |
|-----------|--|----|
| Table 1. | Signal names | 8 |
| Table 2. | AC SMBus and I ² C compatibility timings | 15 |
| Table 3. | Temperature sensor registers summary | 16 |
| Table 4. | Pointer register format | 16 |
| Table 5. | Pointer register select bits (type, width, and default values) | 17 |
| Table 6. | Capability register format | 18 |
| Table 7. | Capability register bit definitions | 18 |
| Table 8. | Configuration register format | 19 |
| Table 9. | Configuration register bit definitions | 20 |
| Table 10. | Hysteresis as applied to temperature movement | 21 |
| Table 11. | Legend for Figure 9: Event output boundary timings | 23 |
| Table 12. | Temperature register format | 24 |
| Table 13. | Temperature register bit definitions | 25 |
| Table 14. | Temperature trip point register format | 25 |
| Table 15. | Alarm temperature upper boundary register format | 25 |
| Table 16. | Alarm temperature lower boundary register format | 26 |
| Table 17. | Critical temperature register format | 26 |
| Table 18. | Manufacturer ID register format | 27 |
| Table 19. | Device ID and device revision ID register format | 27 |
| Table 20. | Device select code | 29 |
| Table 21. | Operating modes | 30 |
| Table 22. | DRAM DIMM connections | 36 |
| Table 23. | Acknowledge when writing data or defining the write-protection (instructions with R/W bit=0) | 37 |
| Table 24. | Acknowledge when reading the write protection (instructions with R/W bit=1) | 38 |
| Table 25. | Absolute maximum ratings | 39 |
| Table 26. | Operating and AC measurement conditions | 40 |
| Table 27. | DC/AC characteristics - temperature sensor component with EEPROM | 40 |
| Table 28. | DFN8 – 8-lead dual flat, no-lead (2 mm x 3 mm) mechanical data (DA) | 43 |
| Table 29. | TDFN8 – 8-lead thin dual flat, no-lead (2 mm x 3 mm) mechanical data (DN) | 45 |
| Table 30. | Ordering information scheme | 46 |
| Table 31. | Parameters for landing pattern - TDFN package (DN) | 49 |
| Table 32. | Document revision history | 50 |

List of figures

| | | |
|------------|---|----|
| Figure 1. | Logic diagram | 8 |
| Figure 2. | DFN8 and TDFN8 connections (top view) | 8 |
| Figure 3. | Block diagram | 9 |
| Figure 4. | SMBus/I ² C write to pointer register | 12 |
| Figure 5. | SMBus/I ² C write to pointer register, followed by a read data word. | 12 |
| Figure 6. | SMBus/I ² C write to pointer register, followed by a write data word | 13 |
| Figure 7. | SMBus/I ² C timing diagram | 14 |
| Figure 8. | Hysteresis | 21 |
| Figure 9. | Event output boundary timings | 23 |
| Figure 10. | Result of setting the write protection. | 30 |
| Figure 11. | Setting the write protection ($\overline{WC} = 0$) | 31 |
| Figure 12. | Write mode sequences in a non write-protected area of SPD | 32 |
| Figure 13. | Write cycle polling flowchart using ACK | 33 |
| Figure 14. | Read mode sequences - SPD | 35 |
| Figure 15. | DFN8 – 8-lead dual flat, no-lead (2 mm x 3 mm) package outline (DA) | 42 |
| Figure 16. | TDFN8 – 8-lead thin dual flat, no-lead (2 mm x 3 mm) package outline (DN) | 44 |
| Figure 17. | DA package topside marking information (DFN-8L) | 47 |
| Figure 18. | DN package topside marking information (TDFN-8L) | 47 |
| Figure 19. | Landing pattern - TDFN package (DN) | 48 |

1 Description

The STTS424E02 is targeted for DIMM Modules in Mobile Personal Computing Platforms (Laptops), Server Memory Modules and other industrial applications. The Thermal Sensor (TS) in the STTS424E02 is compliant with the JEDEC specification, which defines Memory Module Thermal Sensors requirements for Mobile platforms. The 2 Kbit Serial Presence Detect (SPD) I²C-compatible Electrically Erasable Programmable Memory (EEPROM) in the STTS424E02 is organized as 256 x 8 bits and is functionally identical to the industry standard M34E02.

The TS-SPD EEPROM combination provides space as well as cost savings for Mobile and Server Platform Dual Inline Memory Modules (DIMM) manufacturers, as it is packaged in the compact 2 mm x 3 mm 8-lead DFN package which is available in two variations. The DA package has a maximum height of 0.90 mm. The DN package has an identical footprint as the DA package with a thinner maximum height of 0.80 mm. The DN package is compliant to JEDEC MO-229, variation WCED-3.

The temperature sensor includes a band gap-based temperature sensor and 10-bit Analog-to-Digital Converter (ADC) which monitor and digitize the temperature to a resolution of up to 0.25°C. The typical accuracies over these temperature ranges are:

- ±3°C (max) over the full temperature measurement range of -40°C to 125°C,
- ±2°C in the +40°C to +125°C temperature range, and
- ±1°C in the +75°C to +95°C temperature range.

The temperature sensor in the STTS424E02 is specified for operating at supply voltages from 2.7 V to 3.6 V. Operating at 3.3 V, the supply current is 100 µA (typ).

The on-board sigma delta ADC converts the measured temperature to a digital value that is calibrated in °C. For Fahrenheit applications, a lookup table or conversion routine is required. The STTS424E02 is factory-calibrated and requires no external components to measure temperature.

The digital temperature sensor component has user-programmable registers that provide the capabilities for DIMM temperature-sensing applications. The open drain Event output pin is active when the monitoring temperature exceeds a programmable limit, or it falls above or below an alarm window. The user has the option to set the Event output as a critical temperature output. This pin can be configured to operate in either a comparator mode for thermostat operation or in interrupt mode.

The 2 Kbit serial EEPROM memory in the STTS424E02 has the ability to permanently lock the data in its first half (upper) 128 bytes (locations 00h to 7Fh). This facility has been designed specifically for use in DRAM DIMMs with SPD. All of the information concerning the DRAM module configuration (e.g. access speed, size, and organization) can be kept write protected in the first half of the memory. The second half (lower) 128 bytes of the memory can be write protected using two different software write protection mechanisms.

By sending the device a specific sequence, the first 128 bytes of the memory become write protected: permanently or resettable. In the STTS424E02 the EEPROM Write Control (WC) is always held low. Thus, the write protection of the memory array is dependent on whether the software protection has been set.

2 Serial communications

The STTS424E02 has a simple 2-wire SMBus™/I²C-compatible digital serial interface which allows the user to access both the 2 Kbit serial EEPROM and the data in the temperature register at any time. It communicates via the serial interface with a master controller which operates at speeds of up to 400 kHz. It also gives the user easy access to all of the STTS424E02 registers in order to customize device operation.

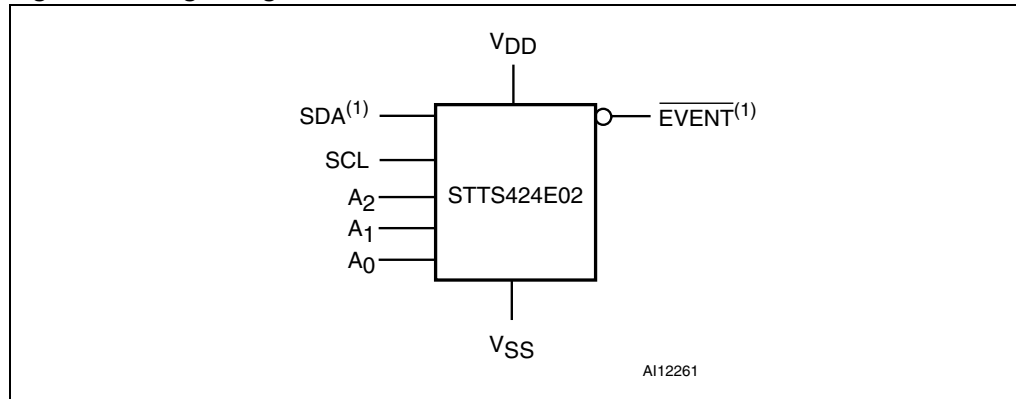
2.1 Device type identifier (DTI) code

The JEDEC temperature sensor and EEPROM each have their own unique I²C address, which ensures that there are no compatibility or data translation issues. This is due to the fact that each of the devices have their own 4-bit DTI code, while the remaining three bits are configurable. This enables the EEPROM and thermal sensors to provide their own individual data via their unique addresses and still not interfere with each others' operation in any way. The DTI codes are:

- '0011' for the TS, and
- '1010' for addressing the EEPROM memory array, and
- '0110' to access the software write protection settings of the EEPROM.

Note: The EEPROM in the STTS424E02 package has its \overline{WC} pin internally tied to the V_{SS} (Ground) pad inside the package while the A0, A1, and A2 pins in the logic diagram (see [Figure 1 on page 8](#)) correspond to the chip enable pins E0, E1 and E2 of EEPROM.

Figure 1. Logic diagram



1. SDA and $\overline{\text{EVENT}}$ are open drain.

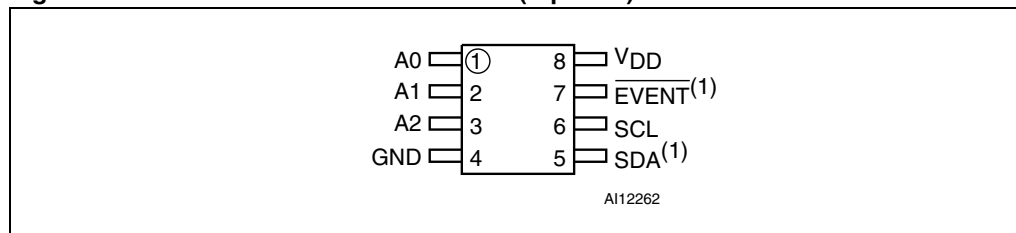
Table 1. Signal names

| Pin | Symbol | Description | Direction |
|-----|---------------------------------|---|--------------|
| 1 | A0 | Serial bus address selection pin. Can be tied to V_{SS} or V_{DD} . | Input |
| 2 | A1 | Serial bus address selection pin. Can be tied to V_{SS} or V_{DD} . | Input |
| 3 | A2 | Serial bus address selection pin. Can be tied to V_{SS} or V_{DD} . | Input |
| 4 | V_{SS} | Supply ground. | |
| 5 | $\text{SDA}^{(1)}$ | Serial data. | Input/output |
| 6 | SCL | Serial clock. | Input |
| 7 | $\overline{\text{EVENT}}^{(1)}$ | Event output pin. Open drain and active-low. | Output |
| 8 | V_{DD} | Supply power (2.7 V to 3.6 V). | |

1. SDA and $\overline{\text{EVENT}}$ are open drain.

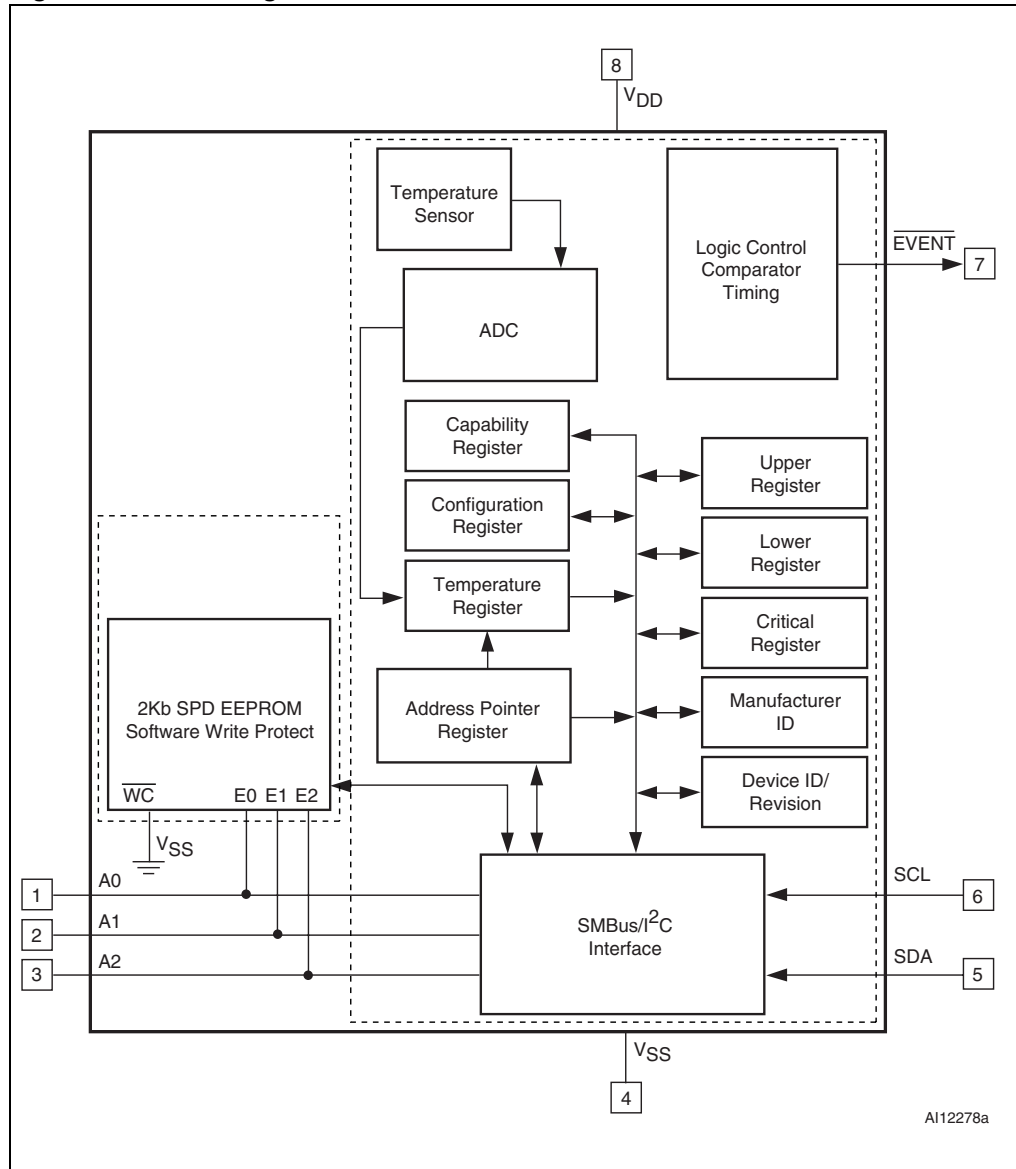
Note: See [Section 2.2: Pin descriptions on page 10](#) for details.

Figure 2. DFN8 and TDFN8 connections (top view)



1. SDA and $\overline{\text{EVENT}}$ are open drain.

Figure 3. Block diagram



2.2 Pin descriptions

2.2.1 A0, A1, A2

A2, A1, and A0 are selectable address pins for the 3 LSBs of the I²C interface address. They can be set to V_{DD} or GND to provide 8 unique address selections. These pins are internally connected to the E2, E1, E0 (chip selects) of EEPROM.

2.2.2 V_{SS} (ground)

This is the reference for the power supply. It must be connected to system ground.

2.2.3 SDA (open drain)

This is the Serial Data input/output pin.

2.2.4 SCL

This is the Serial Clock input pin.

2.2.5 $\overline{\text{EVENT}}$ (open drain)

This output pin is open drain and active-low, and functions as an Alert interrupt.

2.2.6 V_{DD} (power)

This is the supply voltage pin, and ranges from +2.7 V to +3.6 V.

3 Temperature sensor operation

The temperature sensor continuously monitors the ambient temperature and updates the temperature data register at least eight times per second. Temperature data is latched internally by the device and may be read by software from the bus host at any time.

The SMBus/I²C slave address selection pins allow up to 8 such devices to co-exist on the same bus. This means that up to 8 memory modules can be supported, given that each module has one such slave device address slot.

After initial power-on, the configuration registers are set to the default values. The software can write to the configuration register to set bits per the bit definitions in [Section 3.1: SMBus/I²C communications](#).

For details of operation and usage of 2 Kb SPD EEPROM, refer to [Section 5: SPD EEPROM operation](#).

3.1 SMBus/I²C communications

The registers in this device are selected by the Pointer register. At power-up, the Pointer register is set to "00", which is the Capability register location. The Pointer register latches the last location it was set to. Each data register falls into one of three types of user accessibility:

1. Read-only
2. Write-only, and
3. WRITE/READ same address

A WRITE to this device will always include the address byte and the pointer byte. A WRITE to any register other than the pointer register, requires two data bytes.

Reading this device is achieved in one of two ways:

- If the location latched in the Pointer register is correct (most of the time it is expected that the Pointer register will point to one of the Read Temperature registers because that will be the data most frequently read), then the READ can simply consist of an address byte, followed by retrieval of the two data bytes.
- If the Pointer register needs to be set, then an address byte, pointer byte, repeat start, and another address byte will accomplish a READ.

The data byte transfers the MSB first. At the end of a READ, this device can accept either an Acknowledge (ACK) or No Acknowledge (No ACK) status from the Master. The No ACK status is typically used as a signal for the slave that the Master has read its last byte. This device subsequently takes up to 125 ms to measure the temperature.

Figure 4. SMBus/I²C write to pointer register

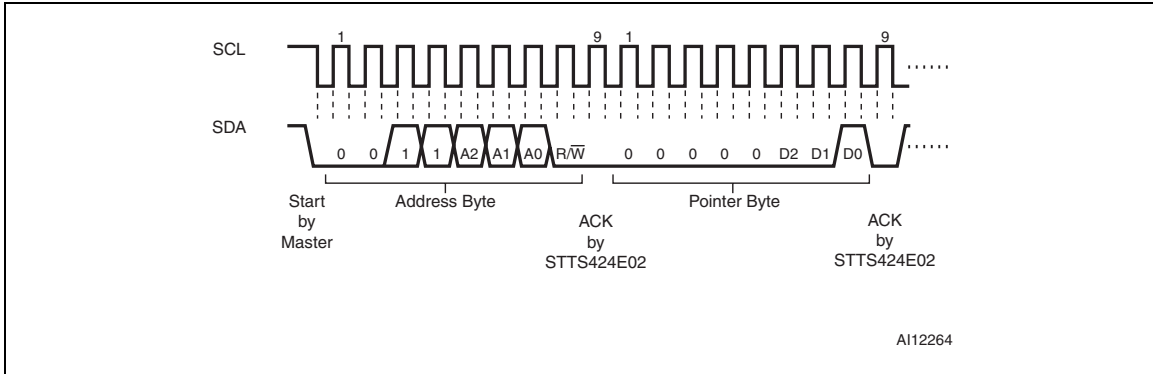


Figure 5. SMBus/I²C write to pointer register, followed by a read data word

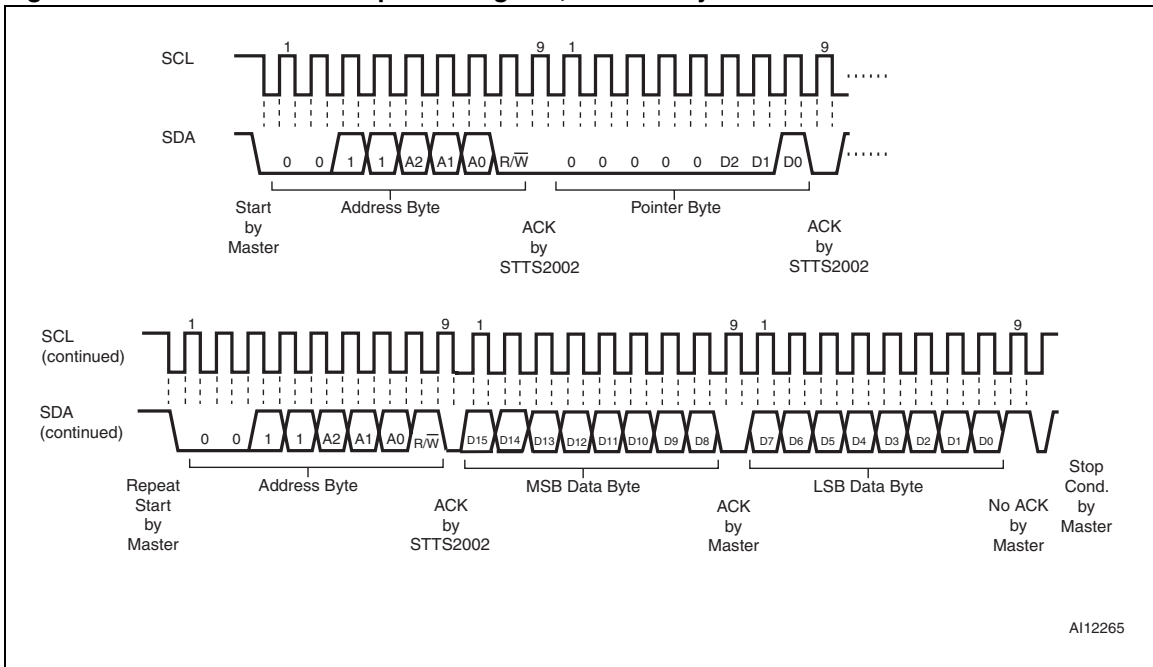
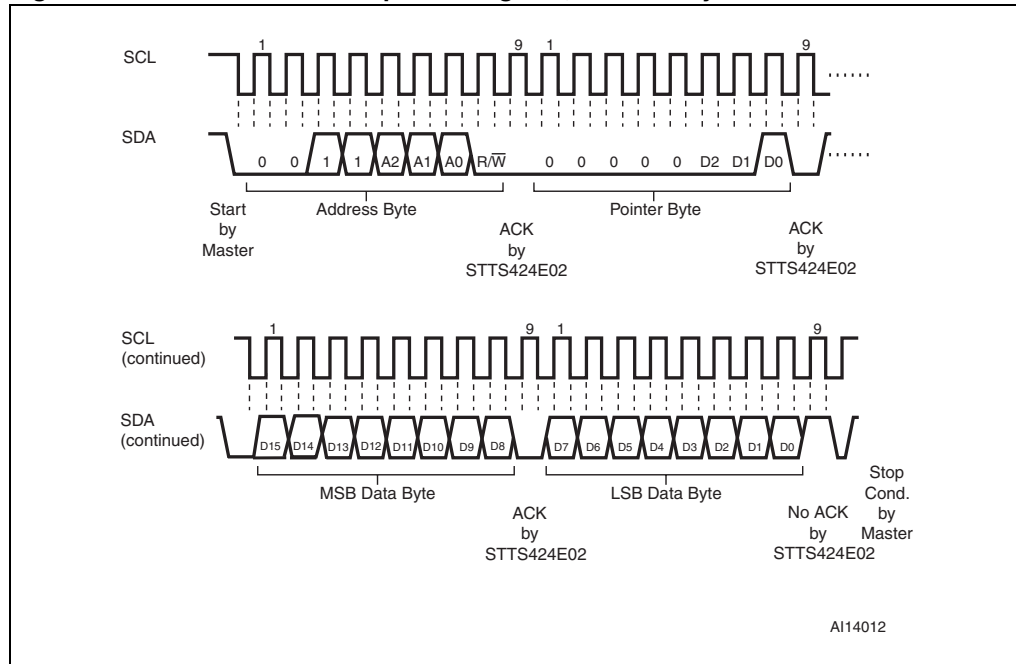


Figure 6. SMBus/I²C write to pointer register, followed by a write data word



3.2 SMBus/I²C slave sub-address decoding

The physical address for the TS is different than that used by the EEPROM. The TS physical address is binary 0 0 1 1 A2 A1 A0 RW, where A2, A1, and A0 are the three slave sub-address pins, and the LSB "RW" is the READ/WRITE flag.

The EEPROM physical address is binary 1 0 1 0 A2 A1 A0 RW for the memory array and is 0 1 1 0 A2 A1 A0 RW for permanently set write protection mode.

3.3 SMBus/I²C AC timing consideration

In order for this device to be both SMBus- and I²C-compatible, it complies to a subset of each specification. The requirements which enable this device to co-exist with devices on either an SMBus or an I²C bus include:

- The SMBus minimum clock frequency is required.
- The 300 ns SMBus data hold time (THD:DAT) is required (see [Figure 7](#) and [Table 2](#) on [page 15](#)).
- The SMBus time-out is maximum 40 ms (temperature sensor only).

Note: Since the voltage levels are specified only within $3.3\text{ V} \pm 10\%$, there are no compatibility concerns with the SMBus/I²C DC specifications.

Figure 7. SMBus/I²C timing diagram

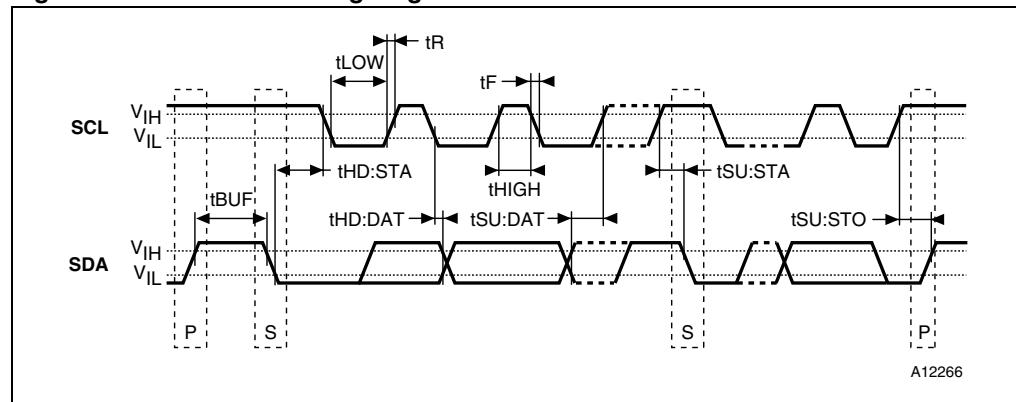


Table 2. AC SMBus and I²C compatibility timings

| Symbol | Parameter | DA package | | DN package | | Units |
|------------------------------------|--|------------|------|------------|-----|-------|
| | | Min | Max | Min | Max | |
| t _{BUF} | Bus free time between stop (P) and start (S) conditions | 4.7 | – | 1.3 | – | µs |
| t _{HD:STA} | Hold time after (repeated) start condition. After this period, the first clock cycle is generated. | 4.0 | – | 0.6 | – | µs |
| t _{SU:STA} ⁽¹⁾ | Repeated start condition setup time | 4.7 | – | 1.3 | – | µs |
| t _{HIGH} | Clock high period | 4.0 | – | 0.6 | – | µs |
| t _{LOW} | Clock low period | 4.7 | – | 1.3 | – | µs |
| t _F | Clock/data fall time | – | 300 | – | 300 | ns |
| t _R | Clock/data rise time | – | 1000 | – | 300 | ns |
| t _{SU:DAT} | Data setup time | 250 | – | 100 | – | ns |
| t _{HD:DAT} | Data hold time | 300 | – | 300 | – | ns |
| t _{SU:STO} | Stop condition setup time | 4.0 | – | 0.6 | – | µs |
| t _W ⁽²⁾ | WRITE time for EEPROM | – | 10 | – | 10 | ms |
| f _{SCL} | SMBUS/I ² C clock frequency | 10 | 100 | 10 | 400 | KHz |
| t _{timeout} | Bus timeout (temperature sensor only) | 25 | 50 | 25 | 50 | ms |

1. For a restart condition, or following a WRITE cycle.

2. This parameter reflects maximum WRITE time for EEPROM.

4 Temperature sensor registers

The temperature sensor component is comprised of various user-programmable registers. These registers are required to write their corresponding addresses to the Pointer register. They can be accessed by writing to their respective addresses (see [Table 3](#)). Pointer register Bits 7-3 must always be written to '0' (see [Table 4](#)). This must be maintained, as not setting these bits to '0' may keep the device from performing to specifications.

The main registers include:

- [Capability register \(read-only\)](#)
- [Configuration register \(read/write\)](#)
- [Temperature register \(read-only\)](#)
- [Temperature trip point registers \(r/w\)](#), including
 - Alarm Temperature Upper Boundary,
 - Alarm Temperature Lower Boundary, and
 - Critical Temperature.
- [Manufacturer ID register format](#)
- [Device ID and device revision ID register format](#)

See [Table 5 on page 17](#) for Pointer register selection bit details.

Table 3. Temperature sensor registers summary

| Address (Hex) | Register name | | Power-on default |
|----------------|---------------------------------------|------------|------------------|
| Not applicable | Address pointer | | Undefined |
| 00 | Capability | C-grade | 0x002D |
| | | B-grade | 0x002F |
| 01 | Configuration | | 0x0000 |
| 02 | Alarm temperature upper boundary trip | | 0x0000 |
| 03 | Alarm temperature lower boundary trip | | 0x0000 |
| 04 | Critical temperature trip | | 0x0000 |
| 05 | Temperature | | Undefined |
| 06 | Manufacturer's ID | | 0x104A |
| 07 | Device ID/revision | DA package | 0x0000 |
| | | DN package | 0x0001 |

Table 4. Pointer register format

| MSB | | | | | | | LSB | |
|------|------|------|------|------|------|------------------------------|------|--|
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
| 0 | 0 | 0 | 0 | 0 | P2 | P1 | P0 | |
| | | | | | | Pointer/register select bits | | |

Table 5. Pointer register select bits (type, width, and default values)

| P2 | P1 | P0 | Name | Register description | Width (bits) | Type (R/W) | Default state (POR) | |
|----|----|----|----------|----------------------------------|--------------|------------|---------------------|--------|
| 0 | 0 | 0 | CAPA | Thermal sensor capabilities | C-grade | 16 | R | 0x002D |
| | | | | | B-grade | | | 0x002F |
| 0 | 0 | 1 | CONF | Configuration | 16 | R/W | 0x0000 | |
| 0 | 1 | 0 | UPPER | Alarm temperature upper boundary | 16 | R/W | 0x0000 | |
| 0 | 1 | 1 | LOWER | Alarm temperature lower boundary | 16 | R/W | 0x0000 | |
| 1 | 0 | 0 | CRITICAL | Critical temperature | 16 | R/W | 0x0000 | |
| 1 | 0 | 1 | TEMP | Temperature | 16 | R | 0x0000 | |
| 1 | 1 | 0 | MANU | Manufacturer ID | 16 | R | 0x104A | |
| 1 | 1 | 1 | ID | Device ID/revision | DA package | 16 | R | 0x0000 |
| | | | | | DN package | | | 0x0001 |

4.1 Capability register (read-only)

This 16-bit register is Read-only, and provides the TS capabilities which comply with the minimum JEDEC 424.4 specifications (see [Table 6](#) and [Table 7 on page 18](#)). The STTS424E02 provides temperatures at 0.25 resolution (10-bit).

4.1.1 Alarm window trip

The device provides a comparison window with an upper temperature trip point in the Alarm Upper Boundary register, and a lower trip point in the Alarm Lower Boundary register. When enabled, the Event output will be triggered whenever entering or exiting (crossing above or below) the Alarm window.

4.1.2 Critical trip

The device can be programmed in such a way that the Event output is only triggered when the temperature exceeds the critical trip point. The Critical Temperature setting is programmed in the Critical Temperature register. When the temperature sensor reaches the critical temperature value in this register, the device is automatically placed in Comparator mode, which means that the Critical Event output cannot be cleared by using software to set the Clear Event bit.

Table 6. Capability register format

| Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit9 | Bit8 |
|-------|-------|-----------------|-------|-------|-------------|------------------|--------------------------|
| RFU | RFU | RFU | RFU | RFU | RFU | RFU | RFU |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| RFU | RFU | V _{HV} | TRES1 | TRES0 | Wider range | Higher precision | Alarm and critical trips |

Table 7. Capability register bit definitions

| Bit | Definition |
|------|---|
| 0 | Basic capability – 0 = Alarm and critical trips turned OFF. – 1 = Alarm and critical trips turned ON. |
| 1 | Accuracy – 0 = Accuracy $\pm 2^{\circ}\text{C}$ over the active range and $\pm 3^{\circ}\text{C}$ over the monitoring range (C-Grade). – 1 = High accuracy $\pm 1^{\circ}\text{C}$ over the active range and $\pm 2^{\circ}\text{C}$ over the monitoring range (B-Grade). |
| 2 | Range width – 0 = Values lower than 0°C will be clamped and represented as binary value '0'. – 1 = Temperatures below 0°C can be read and the Sign bit will be set accordingly. |
| 4:3 | Temperature resolution – 01 = This 10-bit value is fixed for STTS424E02, providing temperatures at 0.25°C resolution (LSB). |
| 5 | (V _{HV}) High voltage support for A0 (pin 1) – 1 = STTS424E02 supports a voltage up to 10 volts on the A0 pin - (default) |
| 15:6 | Reserved These values must be set to '0'. |

4.2 Configuration register (read/write)

The 16-bit Configuration register stores various configuration modes that are used to set up the sensor registers and configure according to application and JEDEC requirements (see [Table 8 on page 19](#) and [Table 9 on page 20](#)).

4.2.1 Event thresholds

All Event thresholds use hysteresis as programmed in register address 0x01 (Bits 10 through 9) to be set when they de-assert.

4.2.2 Interrupt mode

The Interrupt mode allows an event to occur where software may write a '1' to the Clear Event bit (Bit 5) to de-assert the Event Interrupt output until the next trigger condition occurs.

4.2.3 Comparator mode

Comparator mode enables the device to be used as a thermostat. READs and WRITEs on the device registers will not affect the Event output in Comparator mode. The Event signal will remain asserted until temperature drops outside the range or is re-programmed to make the current temperature “out of range”.

4.2.4 Shutdown mode

The STTS424E02 features a Shutdown mode which disables all power-consuming activities (e.g. temperature sampling operations), and leaves the serial interface active. This is selected by setting Shutdown bit (Bit 8) to '1'. In this mode, the devices consume the minimum current (I_{SHDN}), as shown in [Table 27 on page 40](#).

Note: Bit 8 cannot be set to '1' while Bits 6 and 7 (the lock bits) are set to '1'.

The device may be enabled for continuous operation by clearing Bit 8 to '0'. In Shutdown mode, all registers may be read or written to. Power recycling will also clear this bit and return the device to continuous mode as well.

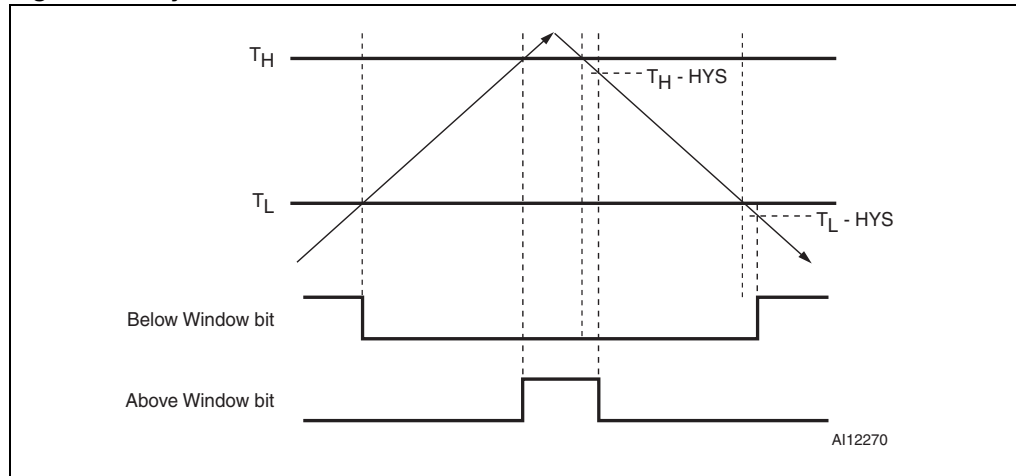
Table 8. Configuration register format

| Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit9 | Bit8 |
|-------------------|----------------|-------------|---------------------|----------------------|---------------------|----------------|---------------|
| RFU | RFU | RFU | RFU | RFU | Hysteresis | Hysteresis | Shutdown mode |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| Critical lock bit | Alarm lock bit | Clear event | Event output status | Event output control | Critical event only | Event polarity | Event mode |

Table 9. Configuration register bit definitions

| Bit | Definition |
|------|---|
| 0 | Event mode – 0 = Comparator output mode (this is the default). – 1 = Interrupt mode; when either of the lock bits is set, this bit cannot be altered until it is unlocked. |
| 1 | Event polarity – 0 = Active-low (this is the default). – 1 = Active-high; when either of the lock bits is set, this bit cannot be altered until it is unlocked. |
| 2 | Critical Event only – 0 = Event output on alarm or critical temperature event (this is the default). – 1 = Event only if the temperature is above the value in the critical temperature register; when the alarm window lock bit is set, this bit cannot be altered until it is unlocked. |
| 3 | Event output control – 0 = Event output disabled (this is the default). – 1 = Event output enabled; when either of the lock bits is set, this bit cannot be altered until it is unlocked. |
| 4 | Event status (read-only) ⁽¹⁾ – 0 = Event output condition is not being asserted by this device. – 1 = Event output condition is being asserted by this device via the alarm window or critical trip event. |
| 5 | Clear Event (write-only) ⁽²⁾ – 0 = No effect. – 1 = Clears the active event in interrupt mode. |
| 6 | Alarm window lock bit – 0 = Alarm trips are not locked and can be altered (this is the default). – 1 = Alarm trip register settings cannot be altered. This bit is initially cleared. When set, this bit returns a logic '1' and remains locked until cleared by an internal power-on reset. These bits can be written to with a single WRITE, and do not require double WRITES. |
| 7 | Critical trip lock bit – 0 = Critical trip is not locked and can be altered (this is the default). – 1 = Critical trip register settings cannot be altered. This bit is initially cleared. When set, this bit returns a logic '1' and remains locked until cleared by an internal power-on reset. These bits can be written to with a single WRITE, and do not require double WRITES. |
| 8 | Shutdown mode – 0 = TS is enabled (this is the default). – 1 = Shutdown TS when the shutdown, device, and A/D converter are disabled in order to save power. No event conditions will be asserted; when either of the lock bits is set, this bit cannot be altered until it is unlocked. However, it can be cleared at any time. |
| 10:9 | Hysteresis enable (see Figure 8 and Table 10) – 00 = Hysteresis is disabled. – 01 = Hysteresis is enabled at 1.5°C. – 10 = Hysteresis is enabled at 3°C. – 11 = Hysteresis is enabled at 6°C. |

1. The actual incident causing the event can be determined from the read temperature register. Interrupt events can be cleared by writing to the clear event bit (writing to this bit will have no effect on overall device functioning).
2. Writing to this register has no effect on overall device functioning in comparator mode. When read, this bit will always return a logic '0' result.

Figure 8. Hysteresis

1. T_U = Value stored in the alarm temperature upper boundary trip register.
2. T_L = Value stored in the alarm temperature lower boundary trip register.
3. HYS = Absolute value of selected hysteresis

Table 10. Hysteresis as applied to temperature movement

| | Below alarm window bit | | Above alarm window bit | |
|--------|------------------------|-----------------------|------------------------|-----------------------|
| | Temperature slope | Temperature threshold | Temperature slope | Temperature threshold |
| Sets | Falling | $T_L - HYS$ | Rising | T_H |
| Clears | Rising | T_L | Falling | $T_H - HYS$ |

4.2.5 Event output pin functionality

The Event outputs can be programmed to be configured as either a comparator output or as an interrupt. This is done by enabling the Output Control bit (Bit 3) and setting the Event mode bit (Bit 0). The output pin polarity can also be specified as active-high or active-low by setting the Event polarity bit (Bit 1).

When the Hysteresis bits (Bits 10 and 9) are enabled, hysteresis may be used to sense temperature movement around trigger points. For example, when using the “Above Alarm window” bit (Temperature register Bit 14, see [Table 12 on page 24](#)) and hysteresis is set to 3°C, as the temperature rises, Bit 14 is set (Bit 14 = 1). The temperature is above the alarm window and the Temperature register contains a value that is greater than the value set in the Alarm Temperature Upper Boundary register (see [Table 15 on page 25](#)).

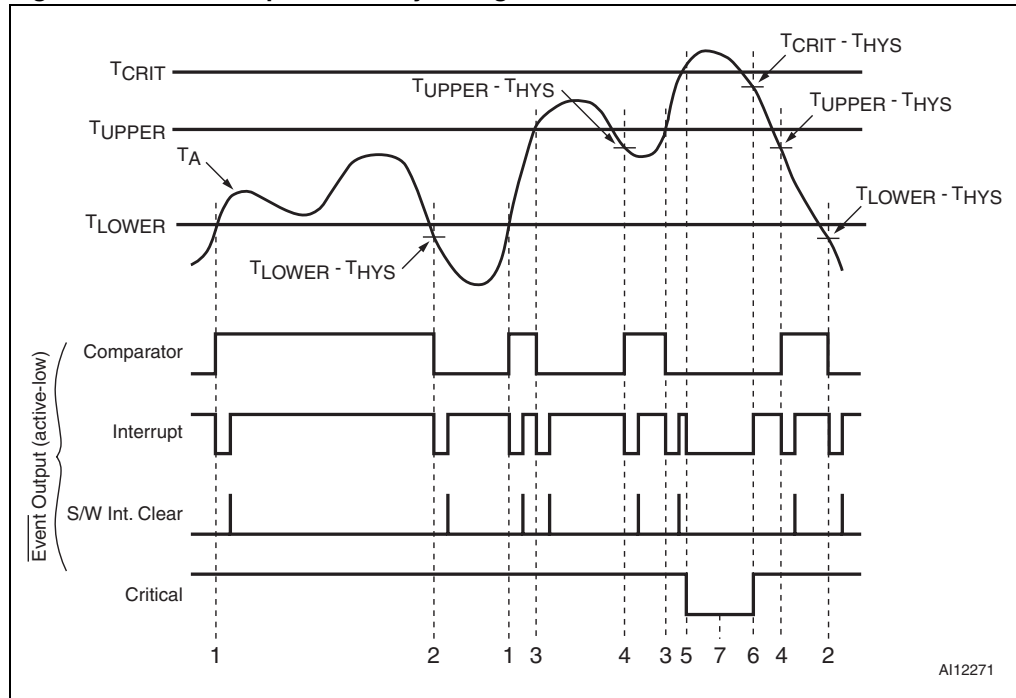
If the temperature decreases, Bit 14 will remain set until the measured temperature is less than or equal to the value in the Alarm Temperature Upper Boundary register minus 3°C (see [Figure 8 on page 21](#) and [Table 10 on page 21](#) for details).

Similarly, when using the “Below Alarm window” bit (Temperature register Bit 13, see [Table 12 on page 24](#)) will be set to '0'. The temperature is equal to or greater than the value set in the Alarm Temperature Lower Boundary register (see [Table 16 on page 26](#)). As the temperature decreases, Bit 13 will be set to '1' when the value in the Temperature register is less than the value in the Alarm Temperature Lower Boundary register minus 3°C (see [Figure 8 on page 21](#) and [Table 10 on page 21](#) for details).

The device will retain the previous state when entering the Shutdown mode. If the device enters the Shutdown mode while the $\overline{\text{EVENT}}$ pin is low, the Shutdown current will increase due to the additional event output pull-down current.

Note: Hysteresis is also applied to the $\overline{\text{EVENT}}$ pin functionality. When either of the Lock bits (Bits 6 and 7) are set, these bits cannot be altered.

Figure 9. Event output boundary timings



AI12271

Table 11. Legend for Figure 9: Event output boundary timings.

| Note | Event output boundary conditions | Event output | | | T _A bits | | |
|------|---|--------------|-----------|----------|---------------------|----|----|
| | | Comparator | Interrupt | Critical | 15 | 14 | 13 |
| 1 | $T_A \geq T_{LOWER}$ | H | L | H | 0 | 0 | 0 |
| 2 | $T_A < T_{LOWER} - T_{HYS}$ | L | L | H | 0 | 0 | 1 |
| 3 | $T_A > T_{UPPER}$ | L | L | H | 0 | 1 | 0 |
| 4 | $T_A < T_{UPPER} - T_{HYS}$ | H | L | H | 0 | 0 | 0 |
| 5 | $T_A \geq T_{CRIT}$ | L | L | L | 1 | 1 | 0 |
| 6 | $T_A < T_{CRIT} - T_{HYS}$ | L | H | H | 0 | 1 | 0 |
| 7 | When $T_A \geq T_{CRIT}$ and $T_A < T_{CRIT} - T_{HYS}$, the event output is in comparator mode and bit 0 of the configuration register (interrupt mode) is ignored. | | | | | | |

4.3 Temperature register (read-only)

This 16-bit, Read-only register stores the temperature measured by the internal band gap TS as shown in [Table 12](#). The STTS424E02 meets the JEDEC mandatory 0.25°C resolution requirement. When reading this register, the MSBs (Bit 15 to Bit 8) are read first, and then the LSBs (Bit 7 to Bit 0) are read. The result is the current-sensed temperature. The data format is 2s complement with one LSB = 0.25°C. The MSB has a 128°C resolution.

The Trip status bits represent the internal temperature trip detection, and are not affected by the status of the Event or Configuration bits (e.g. Event output control or Clear Event). If neither of the Above or Below values are set (i.e. both are 0), then the Temperature is exactly within the user-defined alarm window boundaries.

4.3.1 Temperature format

The 16-bit value used in the Trip Point Set and Temperature Read-back registers is 2s complement, with the LSB equal to 0.0625°C (see [Table 13](#)). For example:

1. a value of 019Ch represents 25.75°C,
2. a value of 07C0h represents 124°C, and
3. a value of 1E74h represents -24.75°C

All unused resolution bits are set to zero. The MSB will have a resolution of 128°C. The STTS424E02 supports the 0.25°C/LSB only.

The upper 3 bits indicate Trip status based on the current temperature, and are not affected by the Event output status.

Table 12. Temperature register format

| | | | Sign MSB | | | | | | | | | | | LSB | | |
|---|---|---|-------------|-----------|-----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|--|
| Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
| Above critical input ⁽¹⁾ | Above alarm window ⁽¹⁾ | Below alarm window ⁽¹⁾ | Temperature | | | | | | | | | | 0 | 0 | | |

1. See [Table 13](#) for explanation.

Table 13. Temperature register bit definitions

| Bit | Definition with Hysteresis = 0 |
|-----|--|
| 13 | Below (temperature) alarm window – 0 = Temperature is equal to or above the alarm window lower boundary temperature. – 1 = Temperature is below the alarm window. |
| 14 | Above (temperature) alarm window. – 0 = Temperature is equal to or below the alarm window upper boundary temperature. – 1 = Temperature is below the alarm window. |
| 15 | Above critical trip – 0 = Temperature is below the critical temperature setting. – 1 = Temperature is equal to or above the critical temperature setting. |

4.4 Temperature trip point registers (r/w)

The STTS424E02 Alarm mode registers provide for 11-bit data in 2s complement format. The data provides for one LSB = 0.25°C. All unused bits in these registers are read as '0'.

The STTS424E02 has three temperature trip point registers (see [Table 14](#)):

- Alarm temperature upper boundary threshold ([Table 15](#)),
- Alarm temperature lower boundary threshold ([Table 16](#)), and
- Critical temperature trip point value ([Table 17](#)).

Note: If the upper or lower boundary threshold values are being altered in-system, all interrupts should be turned off until a known state can be obtained to avoid superfluous interrupt activity.

Table 14. Temperature trip point register format

| P2 | P1 | P0 | Name | Register description | Width (bits) | Type (R/W) | Default state (POR) |
|----|----|----|----------|----------------------------------|--------------|------------|---------------------|
| 0 | 1 | 0 | UPPER | Alarm temperature upper boundary | 16 | R/W | 00 00 |
| 0 | 1 | 1 | LOWER | Alarm temperature lower boundary | 16 | R/W | 00 00 |
| 1 | 0 | 0 | CRITICAL | Critical temperature | 16 | R/W | 00 00 |

Table 15. Alarm temperature upper boundary register format

| | | | Sign MSB | | | | | | | | | | LSB | | |
|--------|--------|--------|---|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | 0 | 0 | Alarm window upper boundary temperature | | | | | | | | | 0 | 0 | | |

Table 16. Alarm temperature lower boundary register format

| | | | Sign MSB | | | | | | | | | | | LSB | | |
|-----------|-----------|-----------|---|-----------|-----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|--|
| Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
| 0 | 0 | 0 | Alarm window lower boundary temperature | | | | | | | | | | 0 | 0 | | |

Table 17. Critical temperature register format

| | | | Sign MSB | | | | | | | | | | | LSB | | |
|-----------|-----------|-----------|---------------------------------|-----------|-----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|--|
| Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
| 0 | 0 | 0 | Critical temperature trip point | | | | | | | | | | 0 | 0 | | |

4.5 Manufacturer ID register (read-only)

The Manufacturer's ID (Programmed Value 104Ah) in this register is the STMicroelectronics Identification provided by the Peripheral Component Interconnect Special Interest Group (PCiSIG).

Table 18. Manufacturer ID register format

| Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit9 | Bit8 |
|--------------------|-------|-------|-------|-------|-------|------|------|
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| Device ID | | | | | | | |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| Device revision ID | | | | | | | |

4.6 Device ID and device revision ID register (read-only)

The Device IDs and Device revision IDs are maintained in this register. The register format is shown in [Table 19](#). The Device IDs and Device revision IDs are currently '0' and will be incremented whenever an update of the device is made.

Table 19. Device ID and device revision ID register format

| Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit9 | Bit8 |
|--------------------|-------|-------|-------|-------|-------|------|---------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Device ID | | | | | | | |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 ⁽¹⁾ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 or 1 |
| Device revision ID | | | | | | | |

1. DA package, bit0 is 0 (see [Table 27 on page 40](#)).
 DN package, bit0 is 1 (see [Table 27 on page 40](#)).

5 SPD EEPROM operation

5.1 2 Kb SPD EEPROM operation

The 2 Kbit serial EEPROM is able to lock permanently the data in its first half (from location 00h to 7Fh). This facility has been designed specifically for use in DRAM DIMMs (Dual in line Memory Modules) with Serial Presence Detect. All the information concerning the DRAM module configuration (such as its access speed, its size, its organization) can be kept write protected in the first half of the memory.

The first half of the memory area can be write-protected using two different software write protection mechanisms. By sending the device a specific sequence, the first 128 bytes of the memory become write protected: permanently or resettable.

These I²C-compatible electrically erasable programmable memory (EEPROM) devices are organized as 256x8 bits.

I²C uses a two wire serial interface, comprising a bi-directional data line and a clock line. The device carries a built-in 4-bit Device Type Identifier code (1010) in accordance with the I²C bus definition to access the memory area and a second Device Type Identifier Code (0110) to define the protection. These codes are used together with the voltage level applied on the three chip enable inputs (A2, A1, A0). These input signals are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit Device Select Code. In the end application, A0, A1 and A2 must be directly (not through a pull-up or pull-down resistor) connected to V_{DD} or V_{SS} to establish the Device Select Code. When these inputs are not connected, an internal pull-down circuitry makes (A0,A1,A2) = (0,0,0).

The A0 input is used to detect the V_{HV} voltage, when decoding an SWP or CWP instruction (refer to [Table 20: Device select code](#)).

The device behaves as a slave device in the I²C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a START condition, generated by the bus master. The START condition is followed by a Device Select Code and RW bit (as described in [Table 20: Device select code](#)), terminated by an acknowledge bit.

When writing data to the memory, the memory inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a STOP condition after an Ack for WRITE, and after a NoAck for READ.

5.2 Internal device reset - SPD EEPROM

In order to prevent inadvertent Write operations during Power-up, a Power On Reset (POR) circuit is included.

At Power-up (phase during which V_{DD} is lower than V_{DDmin} but increases continuously), the device will not respond to any instruction until V_{DD} has reached the Power On Reset threshold voltage (this threshold is lower than the minimum V_{DD} operating voltage defined in [Table 2: AC SMBus and I²C compatibility timings](#)). Once V_{DD} has passed the POR threshold, the device is reset.

Prior to selecting the memory and issuing instructions, a valid and stable V_{DD} voltage must be applied. This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W).

At Power-down (phase during which V_{DD} decreases continuously), as soon as V_{DD} drops from the normal operating voltage below the Power On Reset threshold voltage, the device stops responding to any instruction sent to it.

Table 20. Device select code

| | Chip enable signals | | | Device type identifier | | | | Chip enable bits | | | \overline{RW} |
|--|---------------------|----------|----------|------------------------|----|----|----|------------------|----|----|-----------------|
| | | | | b7 ⁽¹⁾ | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Memory area select code (two arrays) ⁽²⁾ | A2 | A1 | A0 | 1 | 0 | 1 | 0 | A2 | A1 | A0 | \overline{RW} |
| Set write protection (SWP) | V_{SS} | V_{SS} | V_{HV} | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| Clear write protection (CWP) | V_{SS} | V_{DD} | V_{HV} | | | | | 0 | 1 | 1 | 0 |
| Permanently set write protection (PSWP) ⁽²⁾ | A2 | A1 | A0 | | | | | A2 | A1 | A0 | 0 |
| Read SWP | V_{SS} | V_{SS} | V_{HV} | | | | | 0 | 0 | 1 | 1 |
| Read CWP | V_{SS} | V_{DD} | V_{HV} | | | | | 0 | 1 | 1 | 1 |
| Read PSWP ⁽²⁾ | A2 | A1 | A0 | | | | | A2 | A1 | A0 | 1 |

1. The most significant bit, b7, is sent first.

2. A0, A1 and A2 are compared against the respective external pins on the memory device.

5.3 Memory addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the Device Select Code, shown in [Table 20: Device select code](#) (on Serial Data (SDA), most significant bit first).

The Device Select Code consists of a 4-bit Device Type Identifier, and a 3-bit Chip Enable "Address" (A2, A1, A0). To address the memory array, the 4-bit Device Type Identifier is 1010b; to access the write-protection settings, it is 0110b.

Up to eight memory devices can be connected on a single I²C bus. Each one is given a unique 3-bit code on the Chip Enable (A0, A1, A2) inputs. When the Device Select Code is received, the device only responds if the Chip Enable Address is the same as the value on the Chip Enable (A0, A1, A2) inputs.

The 8th bit is the Read/Write bit (\overline{RW}). This bit is set to 1 for Read and 0 for Write operations.

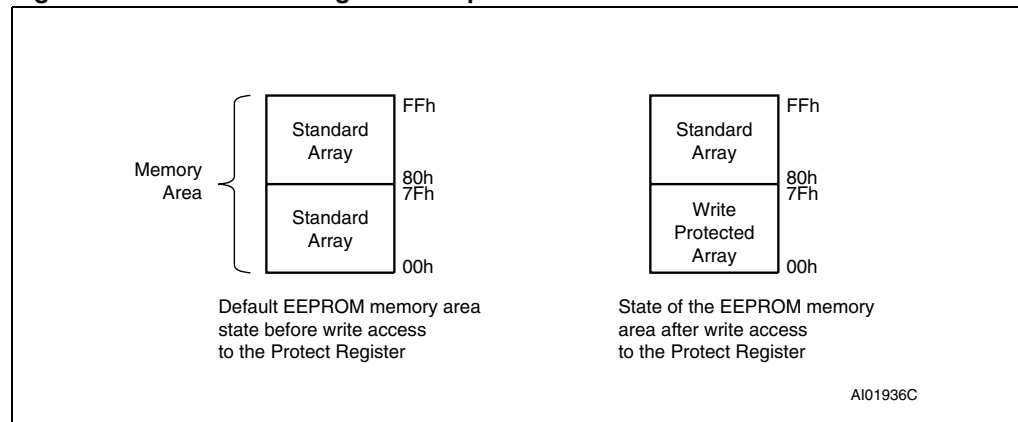
If a match occurs on the Device Select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time. If the device does not match the Device Select code, it deselects itself from the bus, and goes into Standby mode.

Table 21. Operating modes

| Mode | R \overline{W} bit | $\overline{W}C^{(1)}$ | Bytes | Initial sequence |
|----------------------|----------------------|-----------------------|-----------|---|
| Current address read | 1 | X | 1 | START, device select, $R\overline{W} = 1$ |
| Random address read | 0 | X | 1 | START, device select, $R\overline{W} = 0$, address |
| | 1 | X | | reSTART, device select, $R\overline{W} = 1$ |
| Sequential read | 1 | X | ≥ 1 | Similar to current or random address read |
| Byte write | 0 | V_{IL} | 1 | START, device select, $R\overline{W} = 0$ |
| Page write | 0 | V_{IL} | ≤ 16 | START, device select, $R\overline{W} = 0$ |

1. X = V_{IH} or V_{IL} .

Figure 10. Result of setting the write protection



5.4 Setting the write protection

The Write Control ($\overline{W}C$) is tied Low, hence the write protection of the memory array is dependent on whether software write-protection has been set.

Software write-protection allows the bottom half of the memory area (addresses 00h to 7Fh) to be write protected irrespective of subsequent states of the Write Control ($\overline{W}C$) signal.

Software write-protection is handled by three instructions:

- SWP: Set write protection
- CWP: Clear write protection
- PSWP: Permanently set write protection

The level of write-protection (set or cleared) that has been defined using these instructions, remains defined even after a power cycle.

5.4.1 SWP and CWP

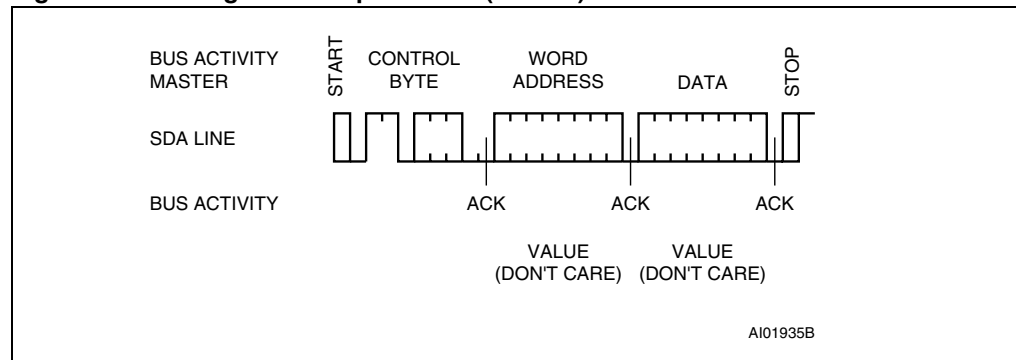
If the software write-protection has been set with the SWP instruction, it can be cleared again with a CWP instruction.

The two instructions (SWP and CWP) have the same format as a Byte Write instruction, but with a different Device Type Identifier (as shown in [Table 20](#)). Like the Byte Write instruction, it is followed by an address byte and a data byte, but in this case the contents are all “Don’t Care” ([Figure 11](#)). Another difference is that the voltage, V_{HV} , must be applied on the A0 pin, and specific logical levels must be applied on the other two address pins A1 and A2 (as shown in [Table 20](#)).

5.4.2 PSWP

If the software write-protection has been set with the PSWP instruction, the first 128 bytes of the memory are permanently write-protected. This write-protection cannot be cleared by any instruction, or by power-cycling the device, and regardless the state of Write Control (\overline{WC}). Also, once the PSWP instruction has been successfully executed, the SPD EEPROM no longer acknowledges any instruction (with a Device Type Identifier of 0110) to access the write-protection settings.

Figure 11. Setting the write protection ($\overline{WC} = 0$)



5.5 Write operations

Following a Start condition the bus master sends a Device Select Code with the \overline{RW} bit reset to 0. The device acknowledges this, as shown in [Figure 12](#), and waits for an address byte. The device responds to the address byte with an acknowledge bit, and then waits for the data byte.

When the bus master generates a Stop condition immediately after the Ack bit (in the “10th bit” time slot), either at the end of a Byte Write or a Page Write, the internal memory Write cycle is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

During the internal Write cycle, Serial Data (SDA) and Serial Clock (SCL) are ignored, and the device does not respond to any requests.

5.5.1 Byte write

After the Device Select Code and the address byte, the bus master sends one data byte. If the addressed location is hardware write-protected, the device replies to the data byte with NoAck, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in [Figure 12](#).

5.5.2 Page write

The Page Write mode allows up to 16 bytes to be written in a single Write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits are the same. If more bytes are sent than will fit up to the end of the page, a condition known as 'roll-over' occurs. This should be avoided, as data starts to become overwritten in an implementation dependent way.

The bus master sends from 1 to 16 bytes of data, each of which is acknowledged by the device if Write Control (\overline{WC}) is Low. After each byte is transferred, the internal byte address counter (the 4 least significant address bits only) is incremented. The transfer is terminated by the bus master generating a Stop condition.

Figure 12. Write mode sequences in a non write-protected area of SPD

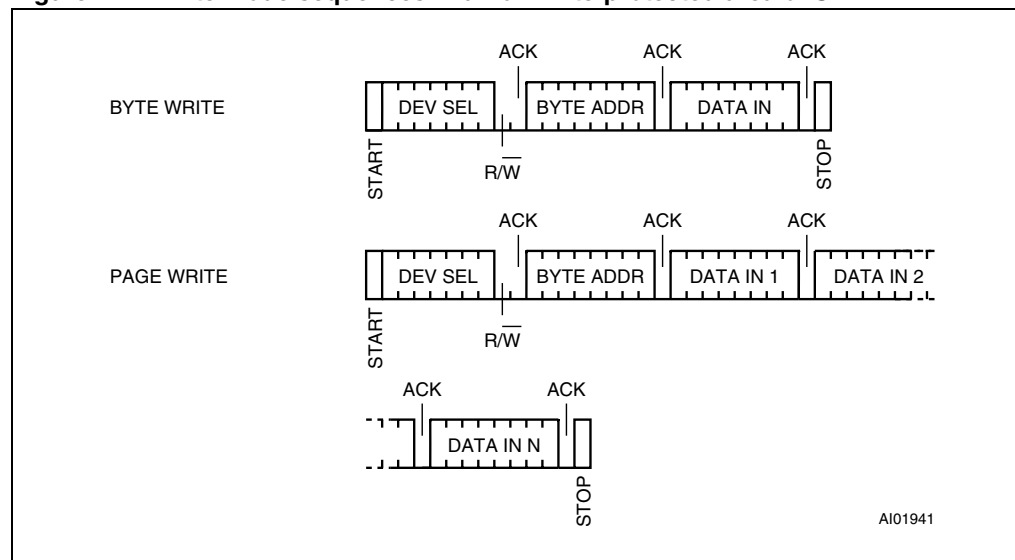
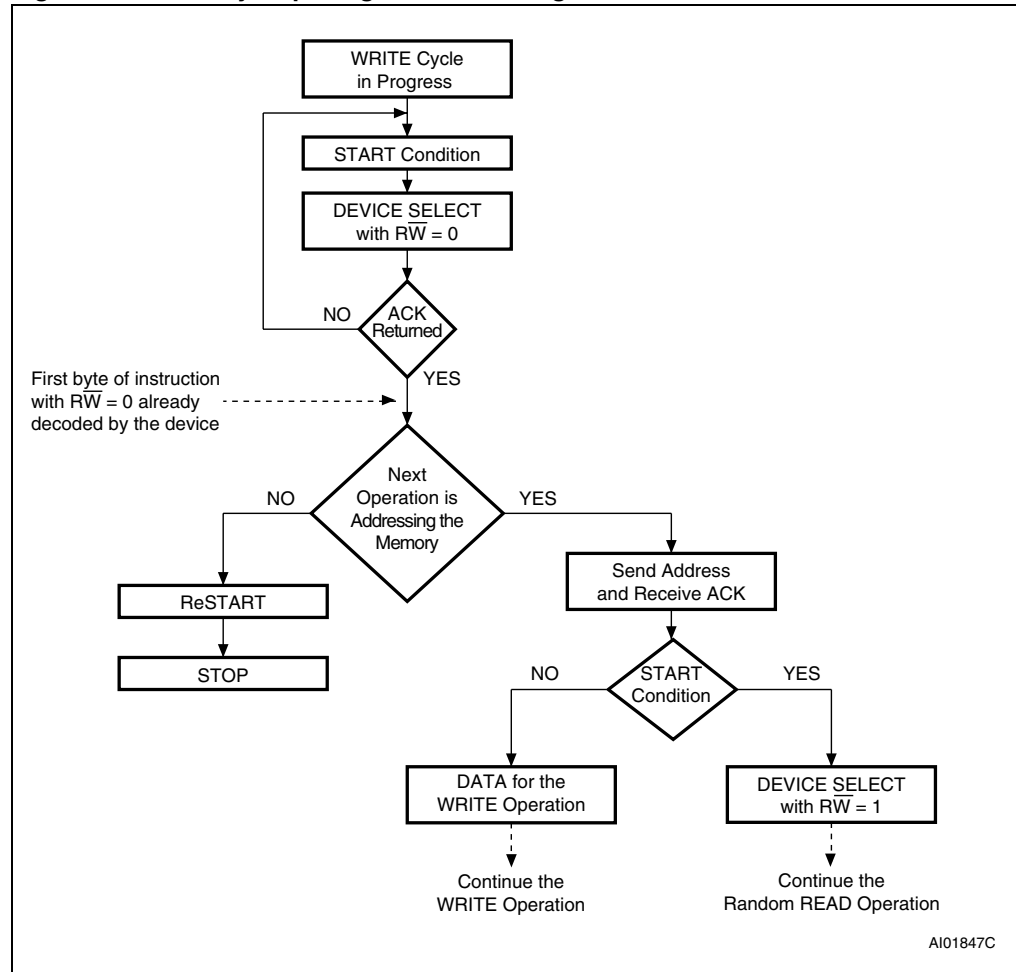


Figure 13. Write cycle polling flowchart using ACK



5.5.3 Minimizing system delays by polling on ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time (t_w) is shown in [Table 2: AC SMBus and I²C compatibility timings](#), but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in [Figure 13](#), is:

- Initial condition: a Write cycle is in progress.
- Step 1: the bus master issues a Start condition followed by a Device Select Code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

5.6 Read operations - SPD

Read operations are performed independently of whether hardware or software protection has been set.

The device has an internal address counter which is incremented each time a byte is read.

5.6.1 Random address read - SPD

A dummy Write is first performed to load the address into this address counter (as shown in [Figure 14](#)) but *without* sending a Stop condition. Then, the bus master sends another Start condition, and repeats the Device Select Code, with the \overline{RW} bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must *not* acknowledge the byte, and terminates the transfer with a Stop condition.

5.6.2 Current address read - SPD

For the Current Address Read operation, following a Start condition, the bus master only sends a Device Select Code with the \overline{RW} bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in [Figure 14](#), *without* acknowledging the byte.

5.6.3 Sequential read - SPD

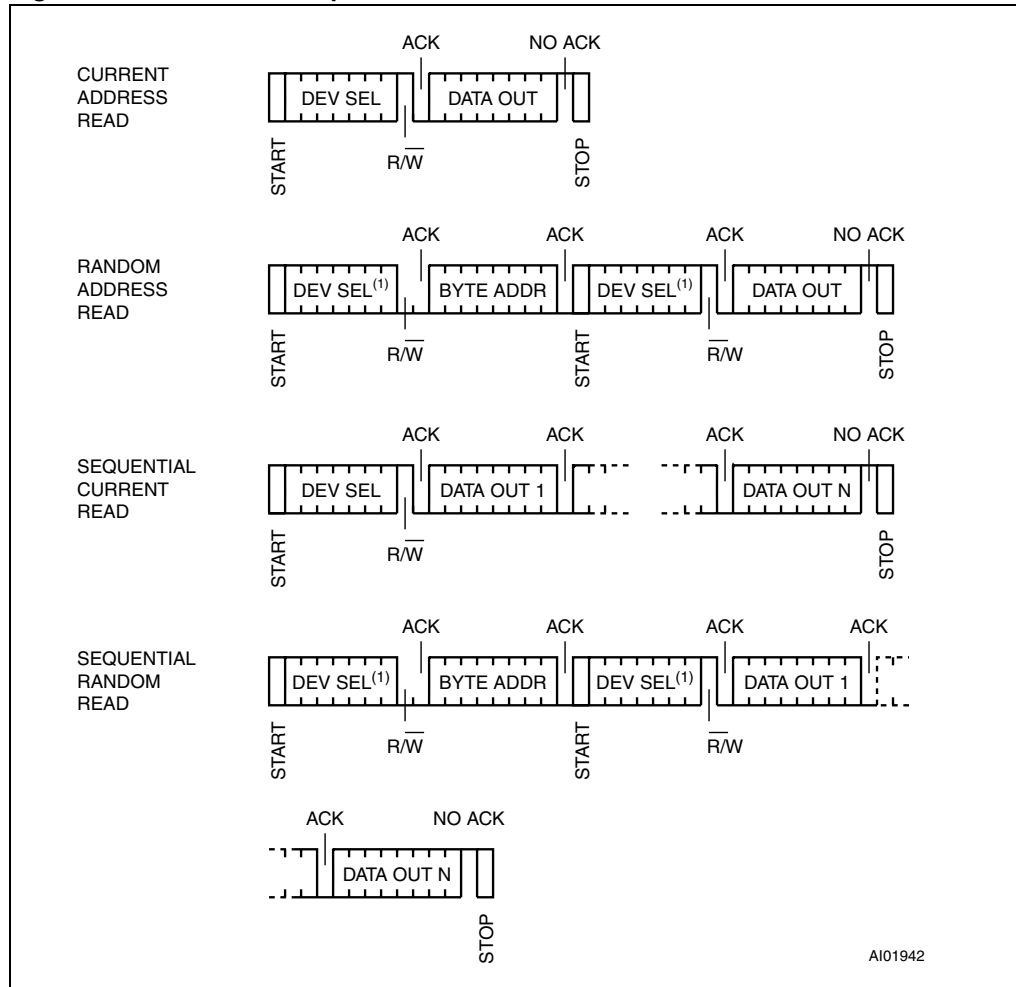
This operation can be used after a Current Address Read or a Random Address Read. The bus master *does* acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in [Figure 14](#).

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over', and the device continues to output data from memory address 00h.

5.6.4 Acknowledge in read mode

For all Read commands, the device waits, after each byte read, for an acknowledgment during the 9th bit time. If the bus master does not drive Serial Data (SDA) Low during this time, the device terminates the data transfer and switches to its Standby mode.

Figure 14. Read mode sequences - SPD



1. The seven most significant bits of the device select code of a random read (in the 1st and 3rd bytes) must be identical.

6 Initial delivery state - SPD

The device is delivered with all bits in the memory array set to '1' (each byte contains FFh).

7 Use in a memory module

In the Dual In line Memory Module (DIMM) application, the SPD is soldered directly on to the printed circuit module. The three Chip Enable inputs (A0, A1, A2) must be connected to V_{SS} or V_{DD} directly (that is without using a pull-up or pull-down resistor) through the DIMM socket (see [Table 22](#)).

The Write Control (\overline{WC}) of the device is tied to ground to maintain full read and write access.

Table 22. DRAM DIMM connections

| DIMM position | A2 | A1 | A0 |
|---------------|--------------|--------------|--------------|
| 0 | V_{SS} (0) | V_{SS} (0) | V_{SS} (0) |
| 1 | V_{SS} (0) | V_{SS} (0) | V_{DD} (1) |
| 2 | V_{SS} (0) | V_{DD} (1) | V_{SS} (0) |
| 3 | V_{SS} (0) | V_{DD} (1) | V_{DD} (1) |
| 4 | V_{DD} (1) | V_{SS} (0) | V_{SS} (0) |
| 5 | V_{DD} (1) | V_{SS} (0) | V_{DD} (1) |
| 6 | V_{DD} (1) | V_{DD} (1) | V_{SS} (0) |
| 7 | V_{DD} (1) | V_{DD} (1) | V_{DD} (1) |

7.1 Programming the SPD

The situations in which the SPD EEPROM is programmed can be considered under two headings:

- when the DIMM is isolated (not inserted on the PCB motherboard)
- when the DIMM is inserted on the PCB motherboard

7.1.1 DIMM isolated

With specific programming equipment, it is possible to define the SPD EEPROM content, using Byte and Page Write instructions, and its write-protection using the SWP and CWP instructions. To issue the SWP and CWP instructions, the DIMM must be inserted in the application-specific slot where the A0 signal can be driven to V_{HV} during the whole instruction. This programming step is mainly intended for use by DIMM makers, whose end application manufacturers will want to clear this write-protection with the CWP on their own specific programming equipment, to modify the lower 128 bytes, and finally to set permanently the write-protection with the PSWP instruction.

7.1.2 DIMM inserted in the application motherboard

As the final application cannot drive the A0 pin to V_{HV} , the only possible action is to freeze the write-protection with the PSWP instruction.

[Table 23](#) and [Table 24](#) show how the Ack bits can be used to identify the write-protection status.

Table 23. Acknowledge when writing data or defining the write-protection (instructions with R/W bit=0)

| Status | \overline{WC} Input Level | Instruction | Ack | Address | Ack | Data byte | Ack | Write cycle(t_W) |
|-----------------------|--------------------------------|---------------------------------------|-------|-----------------|-------|-----------------|-------|----------------------|
| Permanently protected | X | PSWP, SWP or CWP | NoAck | Not significant | NoAck | Not significant | NoAck | No |
| | | Page or byte write in lower 128 bytes | Ack | Address | Ack | Data | NoAck | No |
| Protected with SWP | 0 | SWP | NoAck | Not significant | NoAck | Not significant | NoAck | No |
| | | CWP | Ack | Not significant | Ack | Not significant | Ack | Yes |
| | | PSWP | Ack | Not significant | Ack | Not significant | Ack | Yes |
| | | Page or byte write in lower 128 bytes | Ack | Address | Ack | Data | NoAck | No |
| Not Protected | 0 | PSWP, SWP or CWP | Ack | Not significant | Ack | Not significant | Ack | Yes |
| | | Page or byte write | Ack | Address | Ack | Data | Ack | Yes |

Table 24. Acknowledge when reading the write protection (instructions with R/W bit=1)

| Status | Instruction | Ack | Address | Ack | Data byte | Ack |
|-----------------------|------------------|-------|-----------------|-------|-----------------|-------|
| Permanently protected | PSWP, SWP or CWP | NoAck | Not significant | NoAck | Not significant | NoAck |
| Protected with SWP | SWP | NoAck | Not significant | NoAck | Not significant | NoAck |
| | CWP | Ack | Not significant | NoAck | Not significant | NoAck |
| | PSWP | Ack | Not significant | NoAck | Not significant | NoAck |
| Not protected | PSWP, SWP or CWP | Ack | Not significant | NoAck | Not significant | NoAck |

8 Maximum ratings

Stressing the device above the ratings listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 25. Absolute maximum ratings

| Symbol | Parameter | Value | Unit | |
|-----------------|--|----------------------------------|------|------|
| T_{STG} | Storage temperature | -60 to 150 | °C | |
| $T_{SLD}^{(1)}$ | Lead solder temperature for 10 seconds | 260 | °C | |
| V_{IO} | Input or output voltage - all pins | $V_{SS} - 0.3$ to $V_{DD} + 0.5$ | V | |
| V_{DD} | Supply voltage | $V_{SS} - 0.3$ to 6.5 | V | |
| I_O | Output current | 10 | mA | |
| P_D | Power dissipation | 320 | mW | |
| θ_{JA} | Thermal resistance | DA package | 128 | °C/W |
| | | DN package | 130 | °C/W |

1. Reflow at peak temperature of 255°C to 260°C for < 30 seconds (total thermal budget not to exceed 180°C for between 90 to 150 seconds).

9 DC and AC parameters

This section summarizes the operating measurement conditions, and the dc and ac characteristics of the device. The parameters in the dc and ac characteristics tables that follow, are derived from tests performed under the measurement conditions summarized in [Table 26](#), Operating and AC measurement conditions. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 26. Operating and AC measurement conditions

| Parameter | Conditions | Unit |
|---|---------------------------|------|
| V _{DD} supply voltage - temperature sensor | 2.7 to 3.6 | V |
| Operating temperature | -40 to 85 | °C |
| Input rise and fall times | ≤ 5 | ns |
| Input pulse voltages | 0.2 to 0.8V _{DD} | V |
| Input and output timing reference voltages | 0.3 to 0.7V _{DD} | V |

Table 27. DC/AC characteristics - temperature sensor component with EEPROM

| Sym | Description | Test condition ⁽¹⁾ | Min | Typ ⁽²⁾ | Max | Unit |
|---|---|--|---------------------|--------------------|------|------|
| V _{DD} | Supply voltage | | 2.7 | 3.3 | 3.6 | V |
| I _{DD} | V _{DD} supply current, active temperature conversions (no communication) | EEPROM (inactive) SCL/SDA = V _{DD} | | 100 | 210 | μA |
| | V _{DD} supply current, communication only (no conversions) | EEPROM (not selected) | 100 kHz | 40 | | μA |
| | | | 400 kHz | 115 | | μA |
| I _{DD1} | Shutdown mode supply current | EEPROM, TS shutdown | | | 2.0 | mA |
| | | EEPROM inactive, TS shutdown | DA package at 85°C | 1.0 | 3 | μA |
| | | | DN package at 125°C | 1.0 | 5 | μA |
| I _{SINK} | SMBUS output low sink current | SDA forced to 0.6 V | 6 | | | mA |
| I _{IH} , I _{IL} , I _{OH} , I _{OL} | Input/output leakage current | | | | ±4 | μA |
| V _{POR} ⁽³⁾ | Power on Reset (POR) threshold | V _{DD} falling edge: DA package | | 0.6 | | V |
| | | V _{DD} falling edge: DN package | | 2.0 | | V |
| C-grade | Accuracy for corresponding range 2.7 V ≤ V _{DD} ≤ 3.6 V | +75°C < T _A < +95 | | ±1.0 | ±2.0 | °C |
| | | +40°C < T _A < +125 | | ±2.0 | ±3.0 | °C |
| | | -40°C < T _A < +125 | | ±3.0 | ±4.0 | °C |

Table 27. DC/AC characteristics - temperature sensor component with EEPROM (continued)

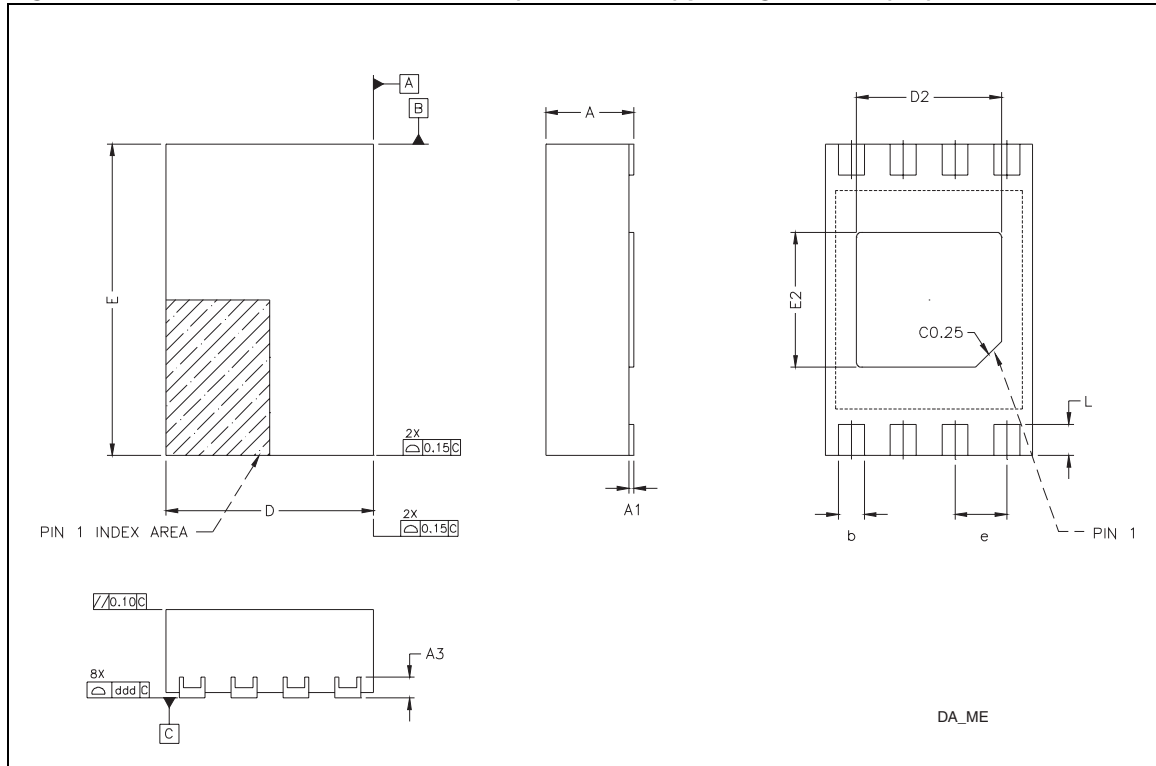
| Sym | Description | Test condition ⁽¹⁾ | Min | Typ ⁽²⁾ | Max | Unit |
|---------------------------------------|--|--|-----|--------------------|-----------|--------------------------------|
| B-grade | Accuracy for corresponding range $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ | $+75^{\circ}\text{C} < T_A < +95$ | | ± 0.5 | ± 1.0 | $^{\circ}\text{C}$ |
| | | $+40^{\circ}\text{C} < T_A < +125$ | | ± 1.0 | ± 2.0 | $^{\circ}\text{C}$ |
| | | $-40^{\circ}\text{C} < T_A < +125$ | | ± 2.0 | ± 3.0 | $^{\circ}\text{C}$ |
| | Resolution | 10-bit temperature data | | | 0.25 | $^{\circ}\text{C}/\text{L SB}$ |
| | | | | | 10 | bits |
| t_{CONV} | Conversion time | 10-bit | | | 125 | ms |
| T_{HYS} | Hysteresis | Default value | | 500 | | mV |
| V_{OL1} | Low level voltage | $\overline{\text{EVENT}}$; $I_{\text{OL}} = 2.1\text{ mA}$ | | | 0.4 | V |
| SMBus/I²C interface | | | | | | |
| V_{IH} | Input logic high | SCL, SDA, A0-A2 | 2.1 | | | V |
| V_{IL} | Input logic low | SCL, SDA, A0-A2 | | | 0.8 | V |
| C_{IN} | SMBus/I ² C input capacitance | | | 5 | | pF |
| f_{SCL} | SMBus/I ² C clock frequency | DA package | 10 | | 100 | kHz |
| | | DN package | 10 | | 400 | kHz |
| t_{timeout} | SMBus timeout | | 25 | | 50 | ms |
| V_{HV} | Allowable voltage on pin A0 | | | | 10 | V |
| L_{AO} | Leakage on pin A0 | In overvoltage state | | 500 | | μA |
| V_{OL2} | Low level voltage SDA | $I_{\text{OL}} = 6\text{ mA}$ | | | 0.6 | V |
| Z_{AIL} | (A0, A1, A2) input impedance | $V_{\text{IN}} < 0.3 V_{\text{CC}}$ | 30 | | | k Ω |
| Z_{AIH} | (A0, A1, A2) input Impedance | $V_{\text{IN}} > 0.7 V_{\text{CC}}$ | 800 | | | k Ω |
| T_A | Ambient operating temperature: | DA package | -40 | | 85 | $^{\circ}\text{C}$ |
| | | DN package | -40 | | 125 | $^{\circ}\text{C}$ |

1. Guaranteed operating temperature for DA package: $T_A = -40^{\circ}\text{C}$ to 85°C and for DN package: $T_A = -40^{\circ}\text{C}$ to 125°C ; $V_{DD} = 2.7\text{ V}$ to 3.6 V (except where noted).
2. Typical numbers taken at $V_{DD} = 3.3\text{ V}$, $T_A = 25^{\circ}\text{C}$.
3. DN is TDFN package max 0.80 mm height.
DA is DFN package max 0.90 mm height.

10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK[®] packages. These packages have a halogen-free and lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at www.st.com.

Figure 15. DFN8 – 8-lead dual flat, no-lead (2 mm x 3 mm) package outline (DA)

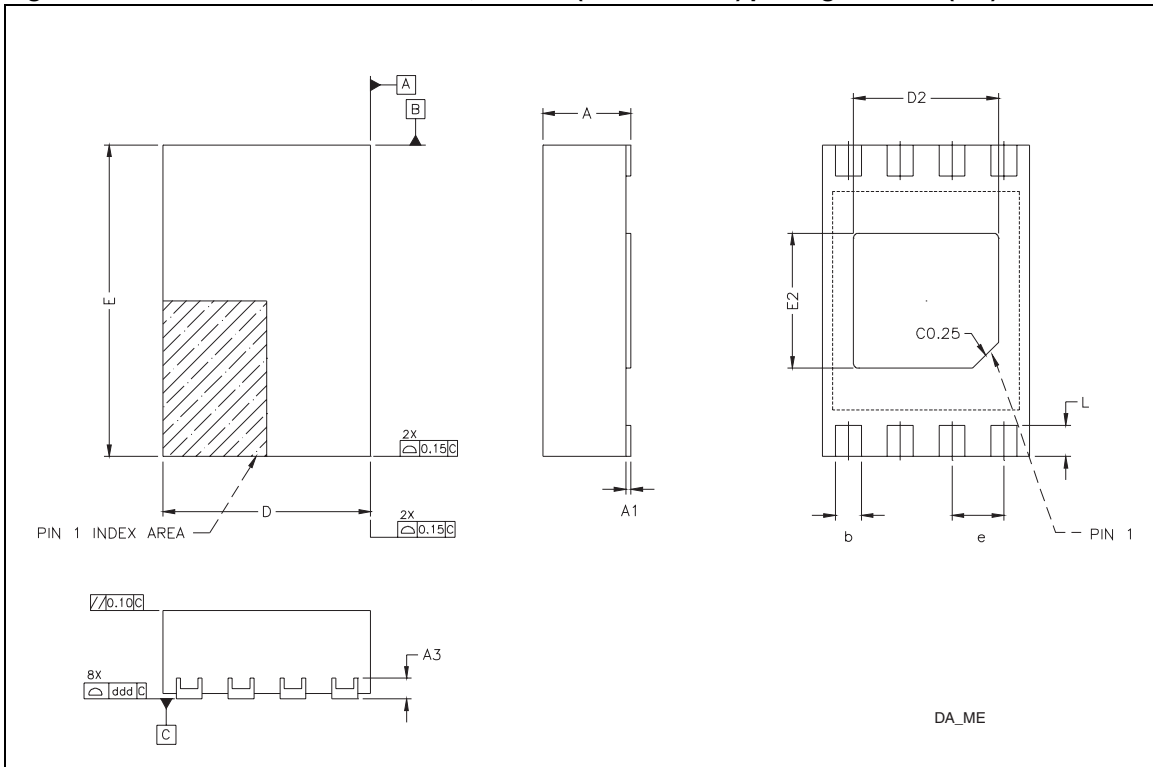


1. Drawing is not to scale.

Table 28. DFN8 – 8-lead dual flat, no-lead (2 mm x 3 mm) mechanical data (DA)

| Sym | mm | | | inches | | |
|-----|------|------|------|--------|-------|-------|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.80 | 0.85 | 0.90 | 0.031 | 0.033 | 0.035 |
| A1 | 0.00 | 0.00 | 0.05 | 0.000 | 0.000 | 0.002 |
| A3 | | 0.20 | | | 0.005 | |
| b | 0.20 | 0.25 | 0.30 | 0.008 | 0.010 | 0.012 |
| D | 1.95 | 2.00 | 2.05 | 0.075 | 0.078 | 0.079 |
| D2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| E | 2.95 | 3.00 | 3.05 | 0.116 | 0.118 | 0.120 |
| E2 | 1.25 | 1.30 | 1.35 | 0.049 | 0.051 | 0.053 |
| e | | 0.50 | | | 0.020 | |
| L | 0.20 | 0.30 | 0.40 | 0.008 | 0.012 | 0.016 |
| ddd | | | 0.08 | | | 0.003 |

Figure 16. TDFN8 – 8-lead thin dual flat, no-lead (2 mm x 3 mm) package outline (DN)^(a)



a. JEDEC MO-229, variation WCED-3 proposal

Table 29. TDFN8 – 8-lead thin dual flat, no-lead (2 mm x 3 mm) mechanical data (DN)⁽¹⁾

| Sym | mm | | | inches | | |
|-----|------|------|------|--------|-------|-------|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.70 | 0.75 | 0.80 | 0.028 | 0.030 | 0.031 |
| A1 | 0.00 | 0.00 | 0.05 | 0.000 | 0.000 | 0.002 |
| A3 | | 0.20 | | | 0.005 | |
| b | 0.20 | 0.25 | 0.30 | 0.008 | 0.010 | 0.012 |
| D | 1.95 | 2.00 | 2.05 | 0.075 | 0.078 | 0.079 |
| D2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| E | 2.95 | 3.00 | 3.05 | 0.116 | 0.118 | 0.120 |
| E2 | 1.25 | 1.30 | 1.35 | 0.049 | 0.051 | 0.053 |
| e | | 0.50 | | | 0.020 | |
| L | 0.30 | 0.35 | 0.40 | 0.012 | 0.014 | 0.016 |
| ddd | | | 0.08 | | | 0.003 |

1. JEDEC MO-229, variation WCED-3 proposal

11 Part numbering

Table 30. Ordering information scheme

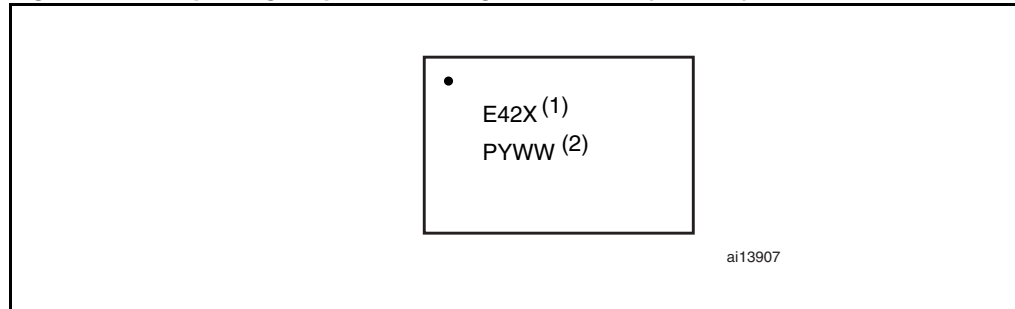
| Example: | STTS424E02 | B | DN | 3 | F |
|--|------------|---|----|---|---|
| Device type | | | | | |
| STTS424E02 | | | | | |
| Grade | | | | | |
| B: Maximum accuracy 75°C to 95°C = ± 1°C | | | | | |
| C: Maximum accuracy 75°C to 95°C = ± 2°C | | | | | |
| Package | | | | | |
| DN = TDFN8 (0.80 mm max height) ⁽¹⁾ | | | | | |
| DA = DFN8 (0.90 mm max height) ⁽²⁾ | | | | | |
| Temperature | | | | | |
| 3 = -40°C to 125°C (DN package only) | | | | | |
| 6 = -40°C to 85°C (DA package only) | | | | | |
| Shipping method | | | | | |
| F = ECOPACK® package, tape & reel packing | | | | | |
| E = ECOPACK® package, tube packing | | | | | |

1. DN package is only available in B accuracy grade and in temperature grade 3.
2. DA package available only in temperature grade 6.

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

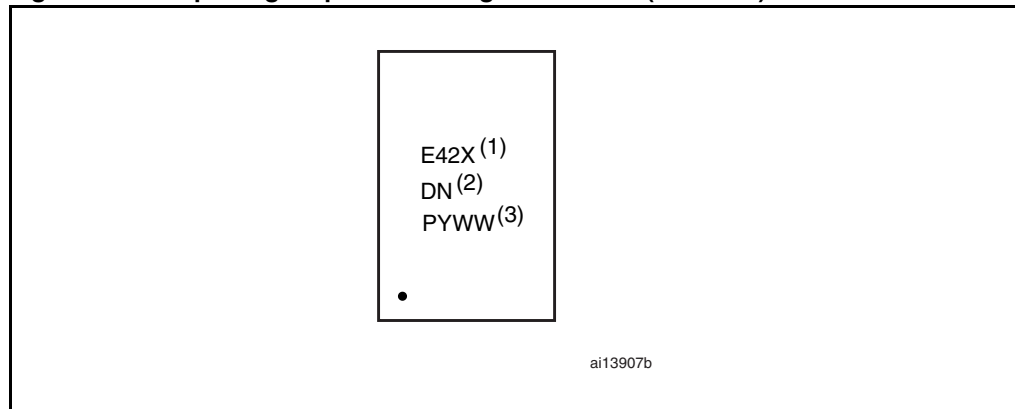
12 Package marking information

Figure 17. DA package topside marking information (DFN-8L)



1. Option codes:
X = B or C accuracy grade. For example, E42C is C-grade.
2. Traceability codes
P = Plant code
Y = Year
WW = Work Week

Figure 18. DN package topside marking information (TDFN-8L)



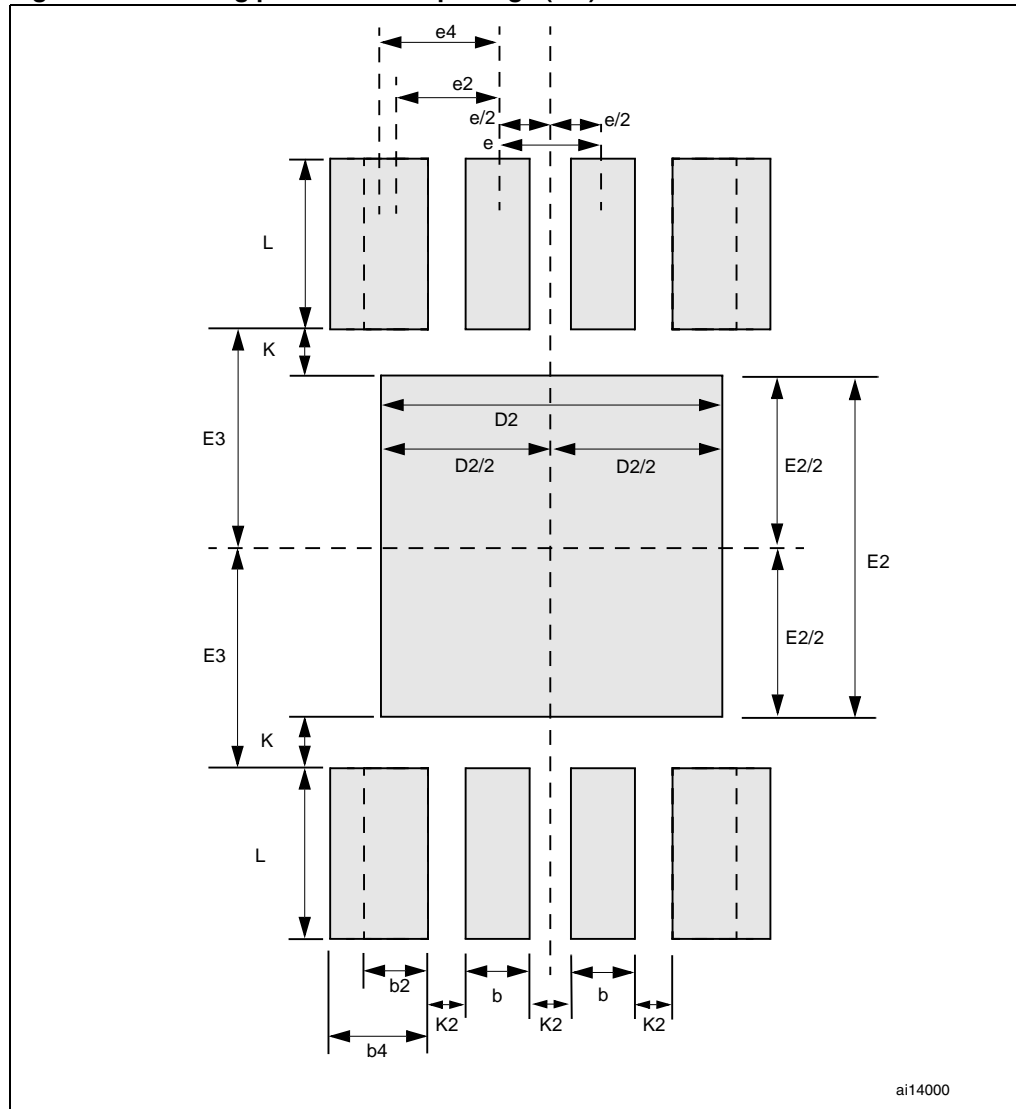
1. Option codes:
X = B or C accuracy grade. For example, E42C is C-grade.
2. TDFN package identifier
DN = 0.80 mm (package height)
3. Traceability codes
P = Plant code
Y = Year
WW = Work Week

13 Landing pattern

The landing pattern recommendations per the JEDEC proposal for the TDFN package (DN) are shown in *Figure 19*.

The preferred implementation with wide corner pads enhances device centering during assembly, but a narrower option is defined for modules with tight routing requirements.

Figure 19. Landing pattern - TDFN package (DN)



ai14000

[Table 31](#) lists variations of landing pattern implementations, ranked as “Preferred” and Minimum Acceptable” based on the JEDEC proposal.

Table 31. Parameters for landing pattern - TDFN package (DN)

| Parameter | Description | Dimension | | |
|-----------|--|-----------|------|------|
| | | Min | Nom | Max |
| D2 | Heat paddle width | 1.40 | - | 1.60 |
| E2 | Heat paddle height | 1.40 | - | 1.60 |
| E3 | Heat paddle centerline to contact inner locus | 1.00 | - | - |
| L | Contact length | 0.70 | - | 0.80 |
| K | Heat paddle to contact keepout | 0.20 | - | - |
| K2 | Contact to contact keepout | 0.20 | - | - |
| e | Contact centerline to contact centerline pitch for inner contacts | - | 0.50 | - |
| b | Contact width for inner contacts | 0.25 | - | 0.30 |
| e2 | Landing pattern centerline to outer contact centerline, “minimum acceptable” option ⁽¹⁾ | - | 0.50 | - |
| b2 | Corner contact width, “minimum acceptable option” ⁽¹⁾ | 0.25 | - | 0.30 |
| e4 | Landing pattern centerline to outer contact centerline, “preferred” option ⁽²⁾ | - | 0.60 | - |
| b4 | Corner contact width, “preferred” option ⁽²⁾ | 0.45 | - | 0.50 |

1. Minimum acceptable option to be used when routing prevents preferred width contact.

2. Preferred option to be used when possible.

14 Revision history

Table 32. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 13-Apr-2007 | 1 | Initial release. |
| 09-May-2007 | 2 | Updated Table 3 , 5 , 6 , 7 , 27 , 28 and 30 . |
| 04-Jun-2007 | 3 | Updated Table 27 . |
| 02-Jul-2007 | 4 | Added POR threshold values to Table 27 , updated Table 28 . |
| 18-Mar-2008 | 5 | Added TDFN package (cover page, Figure 16 , Table 29) and landing pattern recommendations (Figure 19 , Table 31); updated Section 1 , 2 , Table 2 , 3 , 5 , 6 , 7 , 11 , 19 , 25 , 27 , 28 , 29 , 30 , Figure 2 , 15 , 17 , 18). |
| 12-Jun-2008 | 6 | Updated cover page, Figure 4 , 5 , 8 , 14 ; Section 4.3.1 , Section 5.4.1 ; Table 5 , 11 , 25 , 27 , 30 ; added Figure 6 ; removed TSSOP8 package throughout datasheet. |

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2008 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

