SE97

DDR memory module temp sensor with integrated SPD, 3.3 V

Rev. 05 — 6 August 2009 **Product data sheet**

1. General description

The NXP Semiconductors SE97 measures temperature from –40 °C to +125 °C with JEDEC Grade B ±1 °C accuracy between +75 °C and +95 °C and also provide 256 bytes of EEPROM memory communicating via the I²C-bus/SMBus. It is typically mounted on a Dual In-line Memory Module (DIMM) measuring the DRAM temperature in accordance with the new JEDEC (JC-42.4) *Mobile Platform Memory Module Temperature Sensor Component* specification and also replacing the Serial Presence Detect (SPD) which is used to store memory module and vendor information.

The SE97 thermal sensor operates over the V_{DD} range of 3.0 V to 3.6 V and the EEPROM over the range of 3.0 V to 3.6 V write and 1.7 V to 3.6 V read.

Placing the Temp Sensor (TS) on a DIMM allows accurate monitoring of the DIMM module temperature to better estimate the DRAM case temperature (T_{case}) to prevent it from exceeding the maximum operating temperature of 85 °C. The chip set throttles the memory traffic based on the actual temperatures instead of the calculated worst-case temperature or the ambient temperature using a temp sensor mounted on the motherboard. There is up to 30 % improvement in thin and light notebooks that are using one or two 1 GB SO-DIMM modules. The TS is required on DDR3 RDIMM and RDIMM ECC. Future uses of the TS will include more dynamic control over thermal throttling, the ability to use the Alarm Window to create multiple temperature zones for dynamic throttling and to save processor time by scaling the memory refresh rate.

The TS consists of a ΔΣ Analog-to-Digital Converter (ADC) that monitors and updates its own temperature readings 10 times per second, converts the reading to a digital data, and latches them into the data temperature register. User-programmable registers, the specification of upper/lower alarm and critical temperature trip points, $\overline{\text{EVENT}}$ output control, and temperature shutdown, provide flexibility for DIMM temperature-sensing applications.

When the temperature changes beyond the specified boundary limits, the SE97 outputs an $\overline{\text{EVENT}}$ signal using an open-drain output that can be pulled up between 0.9 V and 3.6 V. The user has the option of setting the $\overline{\text{EVENT}}$ output signal polarity as either an active LOW or active HIGH comparator output for thermostat operation, or as a temperature event interrupt output for microprocessor-based systems. The $\overline{\text{EVENT}}$ output can even be configured as a critical temperature output.

The EEPROM is designed specifically for DRAM DIMMs SPD. The lower 128 bytes (address 00h to 7Fh) can be Permanent Write Protected (PWP) or Reversible Write Protected (RWP) by software. This allows DRAM vendor and product information to be stored and write protected. The upper 128 bytes (address 80h to FFh) are not write protected and can be used for general purpose data storage.

The SE97 has a single die for both the temp sensor and EEPROM for higher reliability and supports the industry-standard 2-wire I^2C-bus/SMBus serial interface. The SMBus TIMEOUT function is supported to prevent system lock-ups. Manufacturer and Device ID registers provide the ability to confirm the identity of the device. Three address pins allow up to eight devices to be controlled on a single bus.

2. Features

2.1 General features

- JEDEC (JC-42.4) TSE 2002B3 DIMM ± 0.5 °C (typ.) between 75 °C and 95 °C temperature sensor plus 256-byte serial EEPROM for Serial Presence Detect (SPD)
- Optimized for voltage range: 3.0 V to 3.6 V, but SPD can be read down to 1.7 V
- Shutdown current: 0.1 µA (typ.) and 5.0 µA (max.)
- 2-wire interface: I^2C-bus/SMBus compatible, 0 Hz to 400 kHz
- SMBus Alert Response Address and TIMEOUT (programmable)
- ESD protection exceeds 2500 V HBM per JESD22-A114, 250 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Available packages: TSSOP8, HVSON8, HXSON8, HWSON8 (JEDEC PSON8 VCED-3)

2.2 Temperature sensor features

- 11-bit ADC Temperature-to-Digital converter with 0.125 °C resolution
- Operating current: 250 µA (typ.) and 400 µA (max.)
- Programmable hysteresis threshold: off, 0 °C, 1.5 °C, 3 °C, 6 °C
- Over/under/critical temperature $\overline{\text{EVENT}}$ output
- B grade accuracy:
  - ±0.5 °C/±1 °C (typ./max.) → +75 °C to +95 °C
  - ±1.0 °C/±2 °C (typ./max.) → +40 °C to +125 °C
  - ±2.0 °C/±3 °C (typ./max.) → –40 °C to +125 °C

2.3 Serial EEPROM features

- Operating current:
  - Write → 0.6 mA (typ.) for 3.5 ms (typ.)
  - Read → 100 µA (typ.)
- Organized as 1 block of 256 bytes [(256 × 8) bits]
- 100,000 write/erase cycles and 10 years of data retention
- Permanent and Reversible Software Write Protect
- Software Write Protection for the lower 128 bytes

3. Applications

- DDR2 and DDR3 memory modules
- Laptops, personal computers and servers
- Enterprise networking
- Hard disk drives and other PC peripherals

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
SE97PW	SE97	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 4.4 mm	SOT530-1
SE97TK	SE97	HVSON8	plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 × 3 × 0.85 mm	SOT908-1
SE97TL[1]	97L	HXSON8	plastic thermal enhanced extremely thin small outline package; no leads; 8 terminals; body 2 × 3 × 0.5 mm	SOT1052-1
SE97TP[1][2]	S97	HWSON8	plastic thermal enhanced very very thin small outline package; no leads; 8 terminals; body 2 × 3 × 0.8 mm	SOT1069-1

[1] SE97TL and SE97TP offer improved V_{POR}/$\overline{EVENT}$ I_{OL}.

[2] Industry standard 2 mm × 3 mm × 0.8 mm package to JEDEC VCED-3 PSON8 in 8 mm × 4 mm pitch tape 4 k quantity reels.

5. Block diagram

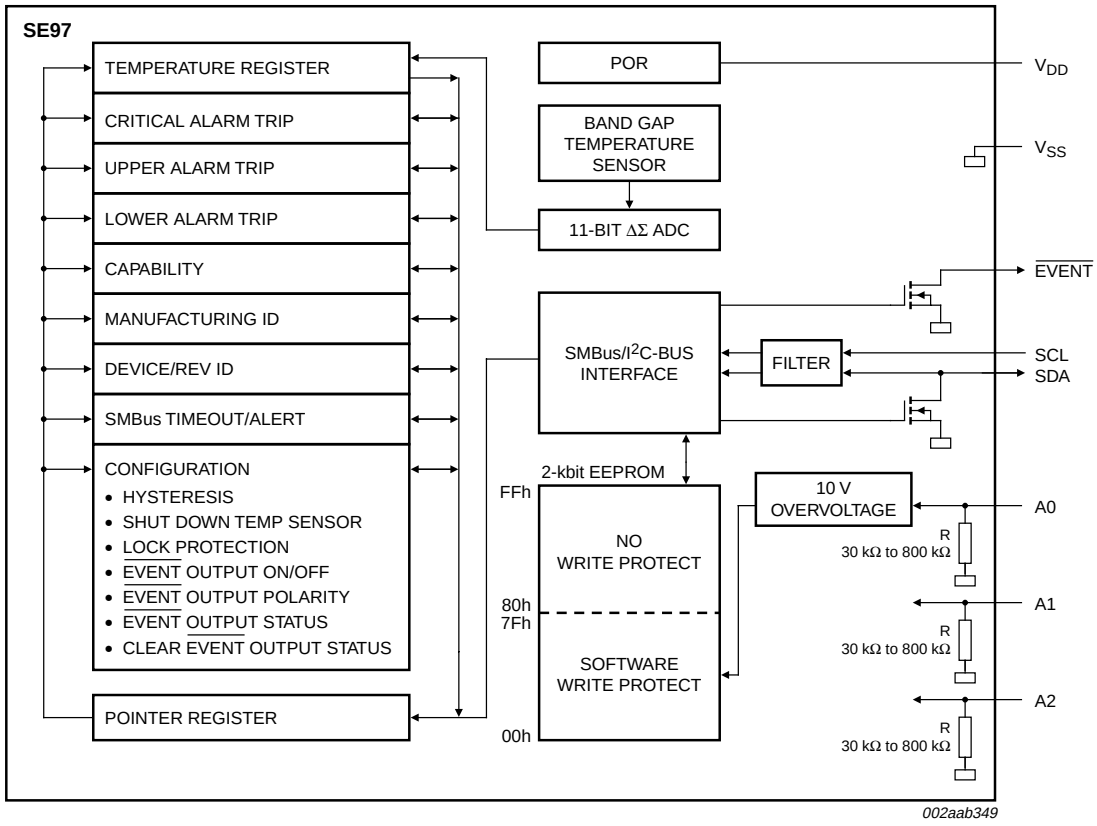


Fig 1. Block diagram of SE97

6. Pinning information

6.1 Pinning

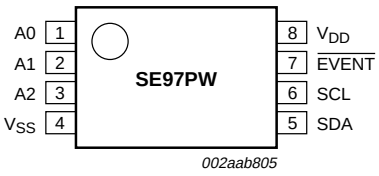


Fig 2. Pin configuration for TSSOP8

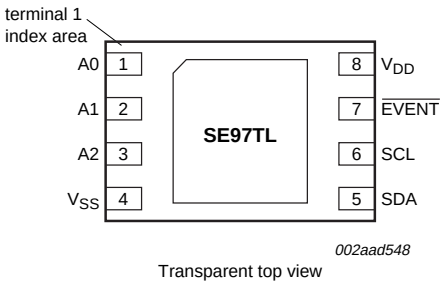


Fig 3. Pin configuration for HXSON8

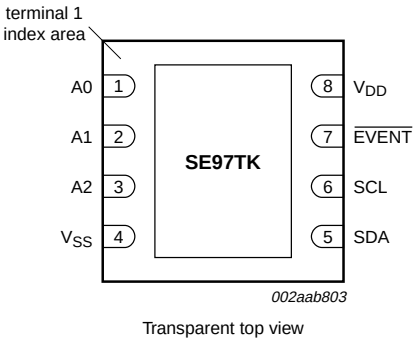


Fig 4. Pin configuration for HVSON8

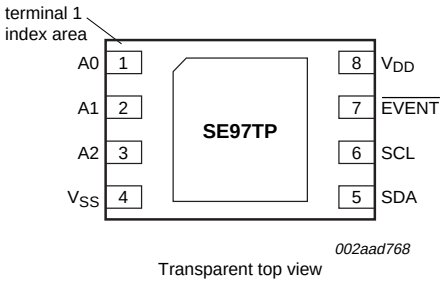


Fig 5. Pin configuration for HWSON8

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
A0	1	I	I^2C-bus/SMBus slave address bit 0 with internal pull-down. This input is overvoltage tolerant to support software write protection.
A1	2	I	I^2C-bus/SMBus slave address bit 1 with internal pull-down
A2	3	I	I^2C-bus/SMBus slave address bit 2 with internal pull-down
V_{SS}	4	ground	device ground
SDA	5	I/O	SMBus/I^2C-bus serial data input/output (open-drain). Must have external pull-up resistor.
SCL	6	I	SMBus/I^2C-bus serial clock input/output (open-drain). Must have external pull-up resistor.
$\overline{EVENT}$	7	O	Thermal alarm output for high/low and critical temperature limit (open-drain). Must have external pull-up resistor.
V_{DD}	8	power	device power supply (3.0 V to 3.6 V); supports 1.7 V for EEPROM read only.

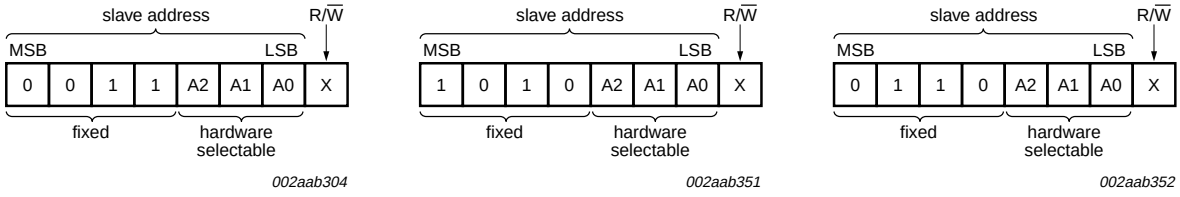
7. Functional description

7.1 Serial bus interface

The SE97 communicates with a host controller by means of the 2-wire serial bus (I^2C-bus/SMBus) that consists of a serial clock (SCL) and serial data (SDA) signals. The device supports SMBus, I^2C-bus Standard-mode and Fast-mode. The I^2C-bus standard speed is defined to have bus speeds from 0 Hz to 100 kHz, I^2C-bus fast speed from 0 Hz to 400 kHz, and the SMBus is from 10 kHz to 100 kHz. The host or bus master generates the SCL signal, and the SE97 uses the SCL signal to receive or send data on the SDA line. Data transfer is serial, bidirectional, and is one byte at a time with the Most Significant Bit (MSB) is transferred first. Since SCL and SDA are open-drain, pull-up resistors must be installed on these pins.

7.2 Slave address

The SE97 uses a 4-bit fixed and 3-bit programmable (A0, A1 and A2) 7-bit slave address that allows a total of eight devices to co-exist on the same bus. The A0, A1 and A2 pins are pulled LOW internally. The A0 pin is also overvoltage tolerant supporting 10 V software write protect. When it is driven higher than 7.8 V, writing a special command would put the EEPROM in reversible write protect mode (see Section 7.10.2 “Memory protection”). Each pin is sampled at the start of each I^2C-bus/SMBus access. The temperature sensor’s fixed address is ‘0011b’. The EEPROM’s fixed address for the normal EEPROM read/write is ‘1010b’, and for EEPROM software protection command is ‘0110b’. Refer to Figure 6.



a. Temperature sensor

b. EEPROM (normal read/write)

c. EEPROM (software protection command)

Fig 6. Slave address

7.3 $\overline{\text{EVENT}}$ output condition

The $\overline{\text{EVENT}}$ output indicates conditions such as the temperature crossing a predefined boundary. The $\overline{\text{EVENT}}$ modes are very configurable and selected using the configuration register (CONFIG). The interrupt mode or comparator mode is selected using CONFIG[0], using either TCRIT/UPPER/LOWER or TCRIT only temperature bands (CONFIG[2]) as modified by hysteresis (CONFIG[10:9]). The UPPER/LOWER (CONFIG[6]) and TCRIT (CONFIG[7]) bands can be locked. Figure 7 shows an example of the measured temperature versus time, with the corresponding behavior of the $\overline{\text{EVENT}}$ output in each of these modes.

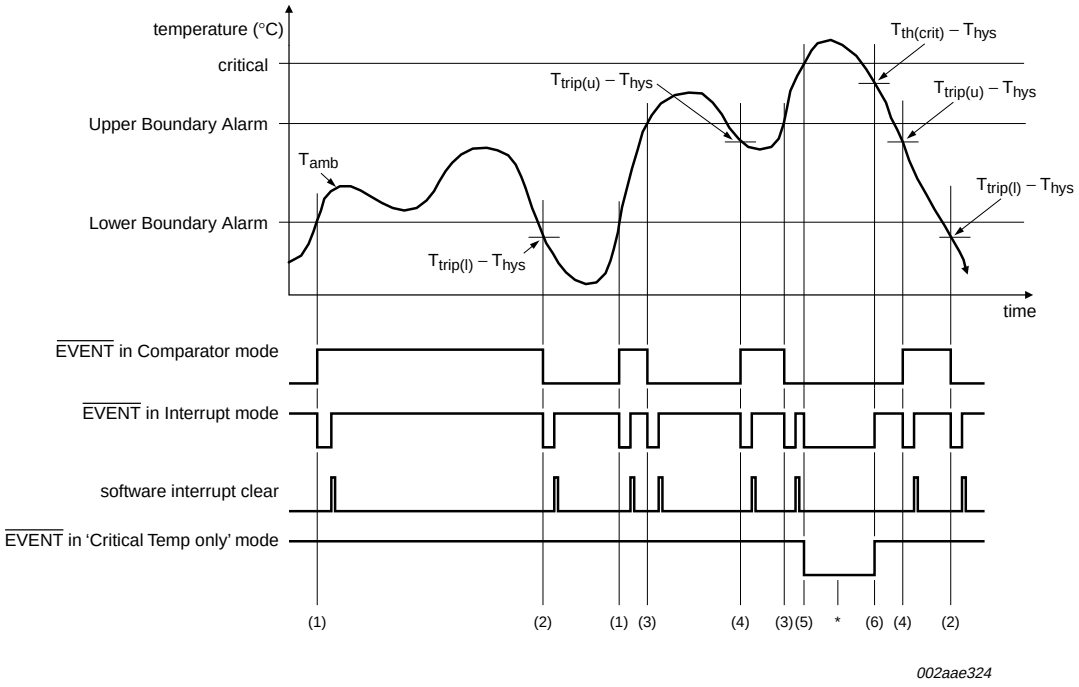
Upon device power-up, the default condition for the $\overline{\text{EVENT}}$ output is high-impedance to prevent spurious or unwanted alarms, but can be later enabled (CONFIG[3]). $\overline{\text{EVENT}}$ output polarity can be set to active HIGH or active LOW (CONFIG[1]). $\overline{\text{EVENT}}$ status can be read (CONFIG[4]) and cleared (CONFIG[5]).

- **Advisory note:**
  - NXP device: After power-up, bit 3 (1) and bit 2 or bit 0 (leave as 0 or 1) can be set at the same time (e.g., in same byte) but once bit 3 is set (1) then changing bit 2 or bit 0 has no effect on the device operation.
  - Competitor device: Does not require that bit 3 be cleared (e.g., set back to (0)) before changing bit 2 or bit 0.
  - Work-around: In order to change bit 2 or bit 0 once bit 3 (1) is set, bit 3 (0) must be cleared in one byte and then change bit 2 or bit 0 and reset bit 3 (1) in the next byte.
  - SE97B will allow bit 2 or bit 0 to be changed even if bit 3 is set.

If the device enters Shutdown mode (CONFIG[8]) with asserted $\overline{\text{EVENT}}$ output, the output remains asserted during shutdown.

7.3.1 $\overline{\text{EVENT}}$ pin output voltage levels and resistor sizing

The $\overline{\text{EVENT}}$ open-drain output is typically pulled up to a voltage level from 0.9 V to 3.6 V with an external pull-up resistor, but there is no real lower limit on the pull-up voltage for the $\overline{\text{EVENT}}$ pin since it is simply an open-drain output. It could be pulled up to 0.1 V and would not affect the output. From the system perspective, there will be a practical limit. That limit will be the voltage necessary for the device monitoring the interrupt pin to detect a HIGH on its input. A possible practical limit for a CMOS input would be 0.4 V. Another thing to consider is the value of the pull-up resistor. When a low supply voltage is applied to the drain (through the pull-up resistor) it is important to use a higher value pull-up resistor, to allow a larger maximum signal swing on the $\overline{\text{EVENT}}$ pin.



Refer to Table 3 for figure note information.

Fig 7. $\overline{\text{EVENT}}$ output condition

Table 3. $\overline{\text{EVENT}}$ output condition

Figure note	$\overline{\text{EVENT}}$ output boundary conditions	$\overline{\text{EVENT}}$ output			Temperature Register Status bits		
		Comparator mode	Interrupt mode	Critical Temp only mode	Bit 15 Above Critical Trip	Bit 14 Above Alarm Window	Bit 13 Below Alarm Window
(1)	$T_{amb} \geq T_{trip(l)}$	H	L	H	0	0	0
(2)	$T_{amb} < T_{trip(l)} - T_{hys}$	L	L	H	0	0	1
(3)	$T_{amb} > T_{trip(u)}$	L	L	H	0	1	0
(4)	$T_{amb} \leq T_{trip(u)} - T_{hys}$	H	L	H	0	0	0
(5)	$T_{amb} \geq T_{th(crit)}$	L	L	L	1	1	0
(6)	$T_{amb} < T_{th(crit)} - T_{hys}$	L	H	H	0	1	0

When $T_{amb} \geq T_{th(crit)}$ and $T_{amb} < T_{th(crit)} - T_{hys}$ the $\overline{\text{EVENT}}$ output is in Comparator mode and bit 0 of CONFIG ($\overline{\text{EVENT}}$ output mode) is ignored.

7.3.2 $\overline{\text{EVENT}}$ thresholds

7.3.2.1 Alarm window

The device provides a comparison window with an UPPER trip point and a LOWER trip point, programmed through the Upper Boundary Alarm Trip register (02h), and Lower Boundary Alarm Trip register (03h). The Upper Boundary Alarm Trip register holds the upper temperature trip point, while the Lower Boundary Alarm Trip register holds the lower temperature trip point as modified by hysteresis as programmed in the Configuration register. When enabled, the $\overline{\text{EVENT}}$ output triggers whenever entering or exiting (crossing above or below) the alarm window.

- **Advisory note:**
  - NXP Device: The $\overline{\text{EVENT}}$ output can be cleared through the Clear $\overline{\text{EVENT}}$ bit (CEVNT) or SMBus Alert.
  - Competitor Device: The $\overline{\text{EVENT}}$ output can be cleared only through the Clear $\overline{\text{EVENT}}$ bit (CEVNT).
  - Work-around: Only clear $\overline{\text{EVENT}}$ output using the Clear $\overline{\text{EVENT}}$ bit (CEVNT).
  - There will be no change to NXP devices.

The Upper Boundary Alarm Trip should always be set above the Lower Boundary Alarm Trip.

- **Advisory note:**
  - NXP device: Requires one conversion cycle (125 ms) after setting the alarm window before comparing the alarm limit with temperature register to ensure that there is correct data in the temperature register before comparing with the Alarm Window and operating $\overline{\text{EVENT}}$ output.
  - Competitor devices: Compares the alarm limit with temperature register at any time, so they get the $\overline{\text{EVENT}}$ output immediately when new UPPER or LOWER Alarm Windows and the $\overline{\text{EVENT}}$ output are set at the same time.
  - Work-around: Wait at least 125 ms before enabling $\overline{\text{EVENT}}$ output (EOCTL = 1).
  - SE97B will compare alarm window and temperature register immediately.

7.3.2.2 Critical trip

The $T_{th(crit)}$ temperature setting is programmed in the Critical Alarm Trip register (04h) as modified by hysteresis as programmed in the Configuration register. When the temperature reaches the critical temperature value in this register (and $\overline{\text{EVENT}}$ is enabled), the $\overline{\text{EVENT}}$ output asserts and cannot be de-asserted until the temperature drops below the critical temperature threshold. The Event cannot be cleared through the Clear $\overline{\text{EVENT}}$ bit (CEVNT) or SMBus Alert.

The Critical Alarm Trip should always be set above the Upper Boundary Alarm Trip.

- **Advisory note:**
  - NXP device: Requires one conversion cycle (125 ms) after setting the Alarm Window before comparing the alarm limit with temperature register to ensure that there is correct data in the temperature register before comparing with the Alarm Window and operating $\overline{\text{EVENT}}$ output.

- Competitor devices: Compares the Alarm Window with temperature register at any time, so they get the $\overline{EVENT}$ output immediately when new $T_{th(crit)}$ and $\overline{EVENT}$ output are set at the same time.
- Work-around: Wait at least 125 ms before enabling $\overline{EVENT}$ output (EOCTL = 1). Intel will change Nehalem BIOS so that $T_{th(crit)}$ is set for more than 125 ms before $\overline{EVENT}$ output is enabled and Event value is checked.
  1. Set $T_{th(crit)}$.
  2. Doing something else (make sure that exceeds 125 ms).
  3. Enable the $\overline{EVENT}$ output (EOCTL = 1).
  4. Wait 20 µs.
  5. Read Event value.
- SE97B will compare alarm window and temperature register immediately.

7.3.3 Event operation modes

7.3.3.1 Comparator mode

In comparator mode, the $\overline{EVENT}$ output behaves like a window-comparator output that asserts when the temperature is outside the window (e.g., above the value programmed in the Upper Boundary Alarm Trip register or below the value programmed in the Lower Boundary Alarm Trip register or above the Critical Alarm Trip resister if $T_{th(crit)}$ only is selected). Reads/writes on the registers do not affect the $\overline{EVENT}$ output in comparator mode. The $\overline{EVENT}$ signal remains asserted until the temperature goes inside the alarm window or the window thresholds are reprogrammed so that the current temperature is within the alarm window.

The comparator mode is useful for thermostat-type applications, such as turning on a cooling fan or triggering a system shutdown when the temperature exceeds a safe operating range.

7.3.3.2 Interrupt mode

In interrupt mode, $\overline{EVENT}$ asserts whenever the temperature crosses an alarm window threshold. After such an event occurs, writing a 1 to the Clear $\overline{EVENT}$ bit (CEVNT) in the configuration register de-asserts the $\overline{EVENT}$ output until the next trigger condition occurs.

In interrupt mode, $\overline{EVENT}$ asserts when the temperature crosses the alarm upper boundary. If the $\overline{EVENT}$ output is cleared and the temperature continues to increase until it crosses the critical temperature threshold, $\overline{EVENT}$ asserts again. Because the temperature is greater than the critical temperature threshold, a Clear $\overline{EVENT}$ command does not clear the $\overline{EVENT}$ output. Once the temperature drops below the critical temperature, $\overline{EVENT}$ de-asserts immediately.

- **Advisory note:**
  - NXP device: If the $\overline{EVENT}$ output is not cleared before the temperature goes above the critical temperature threshold $\overline{EVENT}$ de-asserts immediately when temperature drops below the critical temperature.
  - Competitor devices: If the $\overline{EVENT}$ output is not cleared before or when the temperature is in the critical temperature threshold, $\overline{EVENT}$ will remain asserted after the temperature drops below the critical temperature until a Clear $\overline{EVENT}$ command.

- Work-around: Always clear the $\overline{\text{EVENT}}$ output before temperature exceeds the critical temperature.
- SE97B will keep $\overline{\text{EVENT}}$ asserted after the temperature drops below the critical temperature until a Clear $\overline{\text{EVENT}}$ command de-asserts $\overline{\text{EVENT}}$.

7.4 Conversion rate

The conversion time is the amount of time required for the ADC to complete a temperature measurement for the local temperature sensor. The conversion rate is the inverse of the conversion period which describes the number of cycles the temperature measurement completes in one second—the faster the conversion rate, the faster the temperature reading is updated. The SE97's conversion rate is at least 8 Hz or 125 ms.

7.4.1 What temperature is read when conversion is in progress

The SE97 has been designed to ensure a valid temperature is always available. When a read to the temperature register is initiated through the SMBus, the device checks to see if the temperature conversion process (Analog-to-Digital conversion) is complete and a new temperature is available:

- If the temperature conversion process is complete, then the new temperature value is sent out on the SMBus.
- If the temperature conversion process in **not** complete, then the previous temperature value is sent out on the SMBus.

It is possible that while SMBus Master is reading the temperature register, a new temperature conversion completes. However, this will not affect the data (MSB or LSB) that is being shifted out. On the next read of the temperature register, the new temperature value will be shifted out.

7.5 Power-up default condition

After power-on, the SE97 is initialized to the following default condition:

- Starts monitoring local sensor
- $\overline{\text{EVENT}}$ register is cleared; $\overline{\text{EVENT}}$ output is pulled HIGH by external pull-ups
- $\overline{\text{EVENT}}$ hysteresis is defaulted to 0 °C
- Command pointer is defaulted to '00h'
- Critical Temp, Alarm Temperature Upper and Lower Boundary Trip register are defaulted to 0 °C
- Capability register is defaulted to '0017h' for the B grade
- Operational mode: comparator
- SMBus register is defaulted to '00h'

7.6 Device initialization

SE97 temperature sensors have programmable registers, which, upon power-up, default to zero. The open-drain $\overline{\text{EVENT}}$ output is default to being disabled, comparator mode and active LOW. The alarm trigger registers default to being unprotected. The configuration registers, upper and lower alarm boundary registers and critical temperature window are defaulted to zero and need to be programmed to the desired values. SMBus TIMEOUT

feature defaults to being enabled and can be programmed to disable. These registers are required to be initialized before the device can properly function. Except for the SPD, which does not have any programmable registers, and does not need to be initialized.

Table 4 shows the default values and the example value to be programmed to these registers.

Table 4. Registers to be initialized

Register	Default value	Example value	Description
01h	0000h	0209h	Configuration register • hysteresis = 1.5 °C • $\overline{\text{EVENT}}$ output = Interrupt mode • $\overline{\text{EVENT}}$ output is enabled
02h	0000h	0550h	Upper Boundary Alarm Trip register = 85 °C
03h	0000h	1F40h	Lower Boundary Alarm Trip register = –20 °C
04h	0000h	05F0h	Critical Alarm Trip register = 95 °C
22h	0000h	0000h	SMBus register = no change

7.7 SMBus time-out

The SE97 supports SMBus time-out feature. If the host holds SCL LOW between 25 ns and 35 ms, the SE97 would reset its internal state machine to the bus IDLE state to prevent the system bus hang-up. This feature is turned on by default. The SMBus time-out is disabled by writing a ‘1’ to bit 7 of register 22h.

Remark: When SMBus time-out is enabled, the I^2C-bus minimum bus speed is limited by the SMBus time-out specification limit of 10 kHz.

The SE97 has no SCL driver, so it cannot hold the SCL line LOW.

Remark: SMBus time-out works over the entire supply range of 1.7 V to 3.6 V unless the shutdown bit (SHMD) is set and turns off the oscillator.

7.8 SMBus Alert Response Address (ARA)

The SE97 supports SMBus ALERT when it is programmed for the Interrupt mode and when the $\overline{\text{EVENT}}$ polarity bit is set to ‘0’. The $\overline{\text{EVENT}}$ pin can be ANDed with other $\overline{\text{EVENT}}$ or interrupt signals from other slave devices to signal their intention to communicate with the host controller. When the host detects $\overline{\text{EVENT}}$ or other interrupt signal LOW, it issues an ARA to which a slave device would respond with its address. When there are multiple slave devices generating an ALERT the SE97 performs bus arbitration with the other slaves. If it wins the bus, it responds to the ARA and then clears the $\overline{\text{EVENT}}$ pin.

Remark: Either in comparator mode or when the SE97 crosses the critical temperature, the host must also read the $\overline{\text{EVENT}}$ status bit and provide remedy to the situation by bringing the temperature to within the alarm window or below the critical temperature if that bit is set. Otherwise, the $\overline{\text{EVENT}}$ pin will not get de-asserted.

Remark: In the SE97 the ARA is set to default ON. However, in the SE97B the ARA will be set to default OFF since ARA is not anticipated to be used in DDR3 DIMM applications.

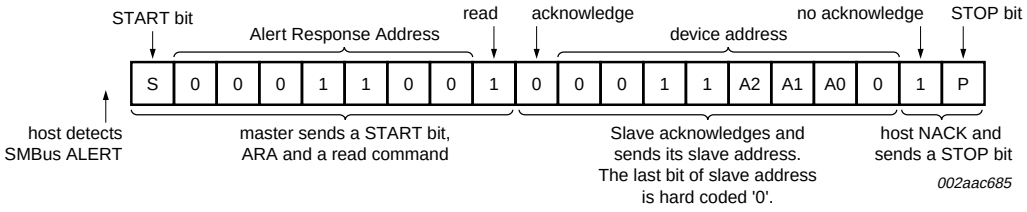


Fig 8. How SE97 responds to SMBus Alert Response Address

7.9 SMBus/I²C-bus interface

The data registers in this device are selected by the Pointer register. At power-up, the Pointer register is set to ‘00h’, the location for the Capability register. The Pointer register latches the last location to which it was set. Each data register falls into one of three types of user accessibility:

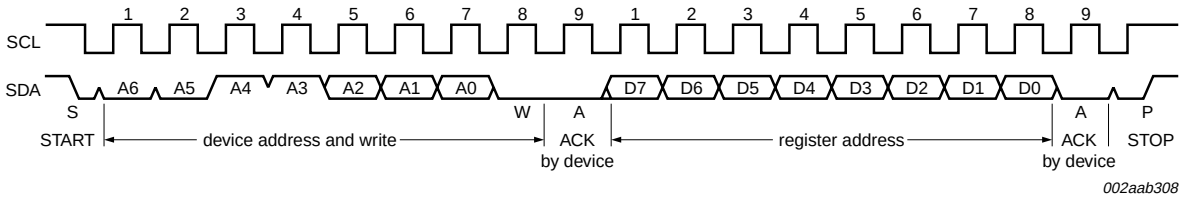
- Read only
- Write only
- Write/Read same address

A ‘write’ to this device will always include the address byte and the pointer byte. A write to any register other than the Pointer register requires two data bytes.

Reading this device can take place either of two ways:

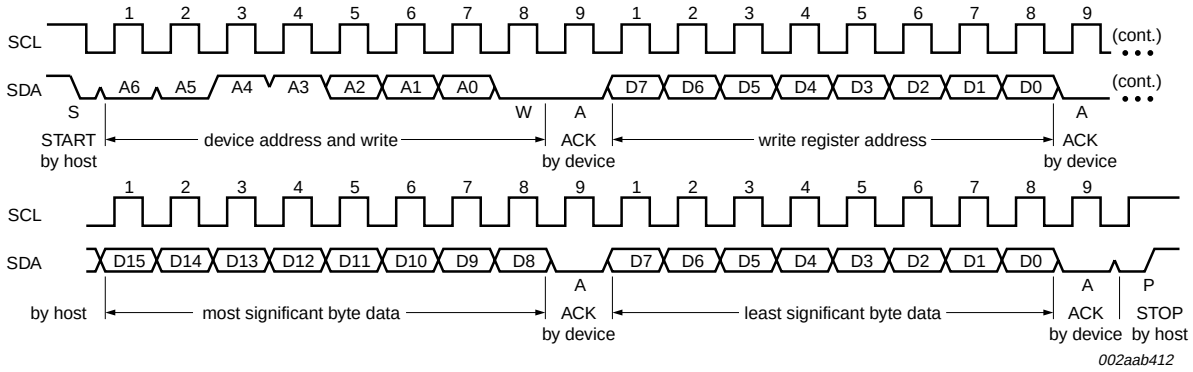
- If the location latched in the Pointer register is correct (most of the time it is expected that the Pointer register will point to one of the Temperature register (as it will be the data most frequently read), then the read can simply consist of an address byte, followed by retrieving the two data bytes.
- If the Pointer register needs to be set, then an address byte, pointer byte, repeat START, and another address byte will accomplish a read.

The data byte has the most significant bit first. At the end of a read, this device can accept either Acknowledge (ACK) or No Acknowledge (NACK) from the Master (No Acknowledge is typically used as a signal for the slave that the Master has read its last byte). It takes this device 125 ms to measure the temperature. Refer to timing diagrams Figure 9 to Figure 12 for how to program the device.



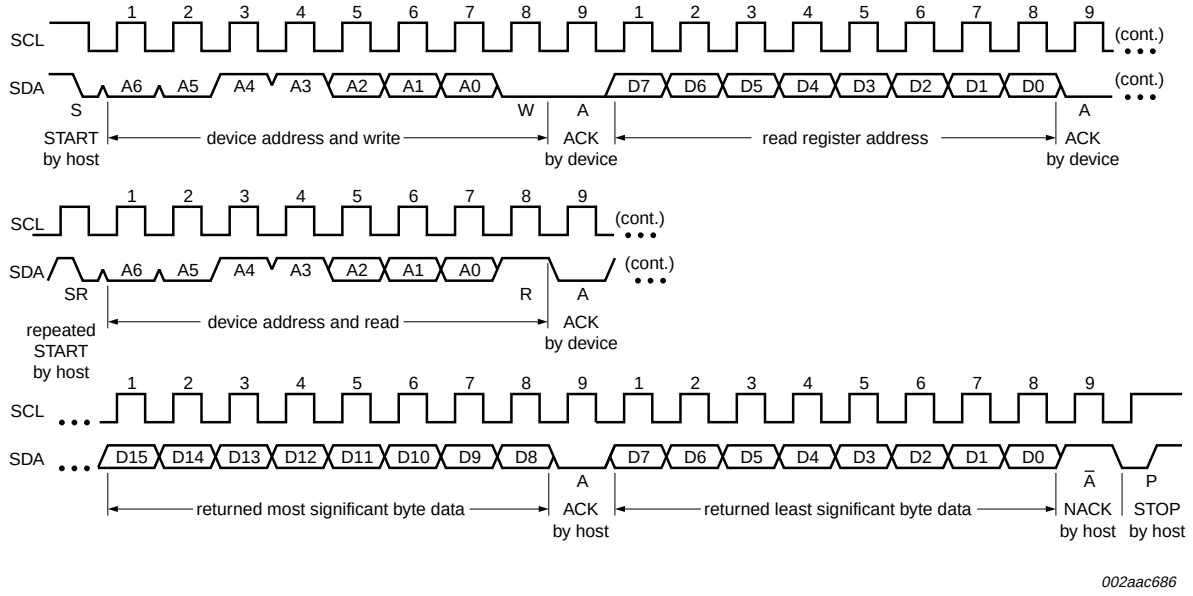
A = ACK = Acknowledge bit. W = Write bit = 0. R = Read bit = 1.

Fig 9. SMBus/I²C-bus write to the Pointer register



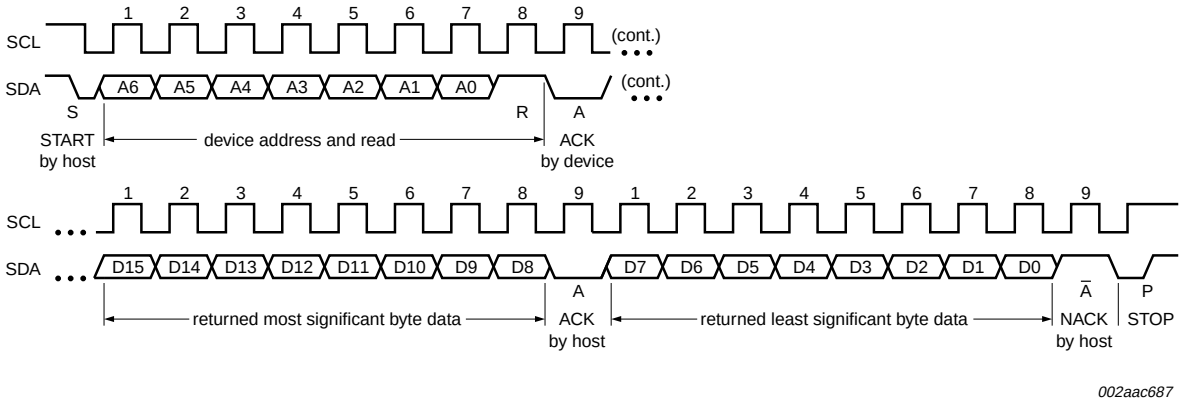
A = ACK = Acknowledge bit. W = Write bit = 0. R = Read bit = 1.

Fig 10. SMBus/I²C-bus write to the Pointer register followed by a write data word



A = ACK = Acknowledge bit. $\overline{A}$ = NACK = No Acknowledge bit. W = Write bit = 0. R = Read bit = 1.

Fig 11. SMBus/I²C-bus write to Pointer register followed by a repeated START and an immediate data word read



A = ACK = Acknowledge bit. $\overline{A}$ = NACK = No Acknowledge bit. W = Write bit = 0. R = Read bit = 1.

Fig 12. SMBus/I²C-bus word read from register with a pre-set pointer

7.10 EEPROM operation

The 2-kbit EEPROM is organized as either 256 bytes of 8 bits each (byte mode), or 16 pages of 16 bytes each (page mode). Accessing the EEPROM in byte mode or page mode is automatic; partial page write of 2 bytes, 4 bytes, or 8 bytes is also supported. Communication with the EEPROM is via the 2-wire serial I^2C-bus or SMBus. Figure 13 provides an overview of the EEPROM partitioning.

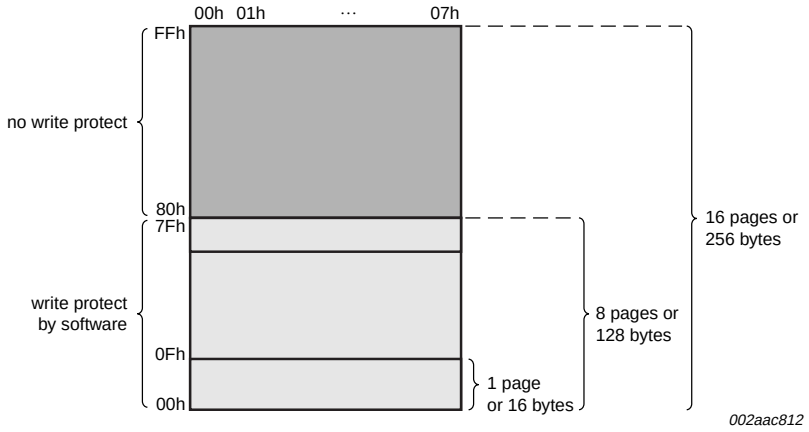


Fig 13. EEPROM partitioning

The EEPROM can be read over voltage range 1.7 V to 3.6 V, but all write operations must be done 3.0 V to 3.6 V.

7.10.1 Write operations

7.10.1.1 Byte Write

In Byte Write mode the master creates a START condition and then broadcasts the slave address, byte address, and data to be written. The slave acknowledges all 3 bytes by pulling down the SDA line during the ninth clock cycle following each byte. The master creates a STOP condition after the last ACK from the slave, which then starts the internal write operation (see Figure 14). During internal write, the slave will ignore any read/write request from the master.

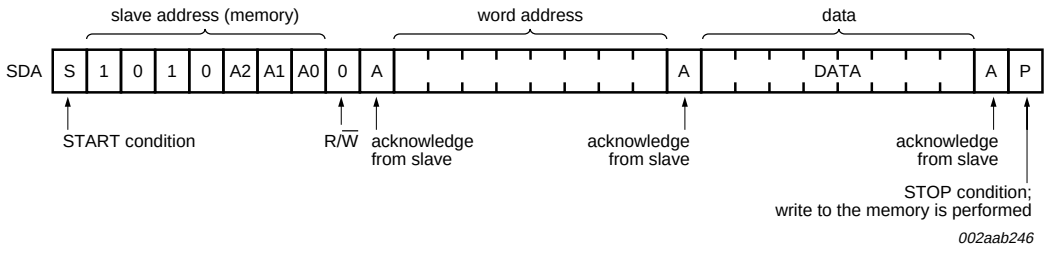


Fig 14. Byte Write timing

7.10.1.2 Page Write

The SE97 contains 256 bytes of data, arranged in 16 pages of 16 bytes each. The page is selected by the four Most Significant Bits (MSB) of the address byte presented to the device after the slave address, while the four Least Significant Bits (LSB) point to the byte within the page. By loading more than one data byte into the device, up to an entire page can be written in one write cycle (see Figure 15). The internal byte address counter will increment automatically after each data byte. If the master transmits more than 16 data bytes, then earlier bytes will be overwritten by later bytes in a wrap-around fashion within the selected page. The internal write cycle is started following the STOP condition created by the master.

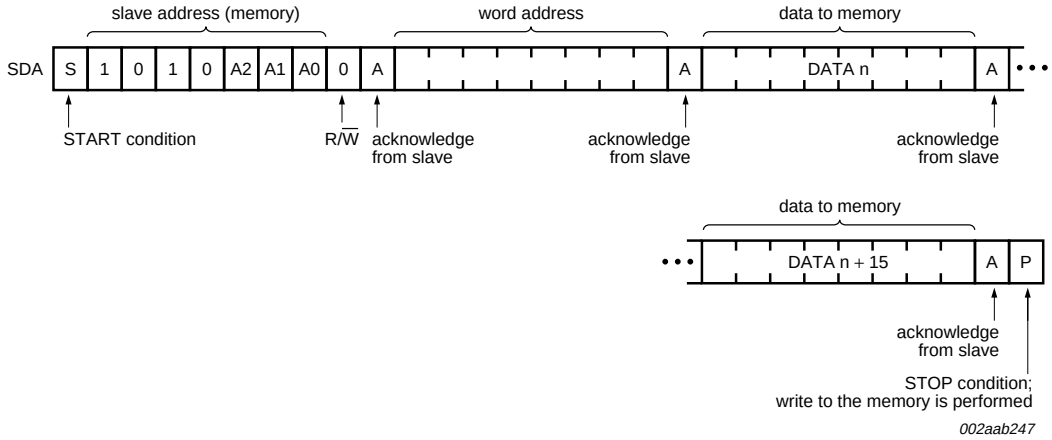


Fig 15. Page Write timing

7.10.1.3 Acknowledge polling

Acknowledge polling can be used to determine if the SE97 is busy writing or is ready to accept commands. Polling is implemented by sending a 'Selective Read' command (described in Section 7.10.3 "Read operations") to the device. The SE97 will not acknowledge the slave address as long as internal write is in progress.

7.10.2 Memory protection

The lower half (the first 128 bytes) of the memory can be write protected by special EEPROM commands without an external control pin. The SE97 features three types of memory write protection instructions, and three respective read Protection instructions. The level of write-protection (set or clear) that has been defined using these instructions remained defined even after power cycle.

The memory protection commands are:

- Permanent Write Protection (PWP)
- Reversible Write Protection (RWP)
- Clear Write Protection (CWP)
- Read Permanent Write Protection (RPWP)
- Read Reversible Write Protection (RRWP)
- Read Clear Write Protection (RCWP)

Table 5 is the summary for normal and memory protection instructions.

Table 5. EEPROM commands summary

Command	Fixed address				Hardware selectable address			R/$\overline{W}$
	Bit 7[1]	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Normal EEPROM read/write	1	0	1	0	A2	A1	A0	R/$\overline{W}$
Reversible Write Protection (RWP)	0	1	1	0	V_{SS}	V_{SS}	$V_{I(ov)}$[3]	0
Clear Reversible Write Protection (CRWP)	0	1	1	0	V_{SS}	V_{DD}	$V_{I(ov)}$[3]	0
Permanent Write Protection (PWP)[2]	0	1	1	0	A2	A1	A0	0
Read RWP	0	1	1	0	V_{SS}	V_{SS}	$V_{I(ov)}$[3]	1
Read CRWP	0	1	1	0	V_{SS}	V_{DD}	$V_{I(ov)}$[3]	1
Read PWP	0	1	1	0	A2	A1	A0	1

[1] The most significant bit, bit 7, is sent first.

[2] A0, A1, and A2 are compared against the respective external pins on the SE97.

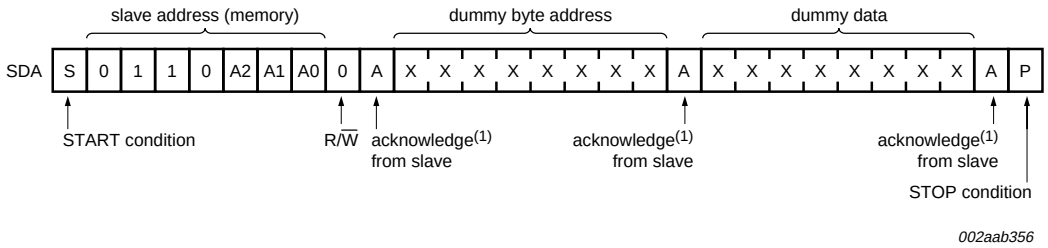
[3] $V_{I(ov)}$ ranges from 7.8 V to 10 V.

This special EEPROM command consists of a unique 4-bit fixed address (0110b) and the voltage level applied on the 3-bit hardware address. Normally, to address the memory array, the 4-bit fixed address is '1010b'. To access the memory protection settings, the 4-bit fixed address is '0110b'. Figure 16 and Figure 17 show the write and read protection sequence, respectively.

Up to eight memory devices can be connected on a single I^2C-bus. Each one is given a 3-bit on the hardware selectable address (A2, A1, A0) inputs. The device only responds when the 4-bit fixed and hardware selectable bits are matched. The 8th bit is the read/write bit. This bit is set to 1 or 0 for read and write protection, respectively.

The corresponding device acknowledges during the ninth bit time when there is a match on the 7-bit address.

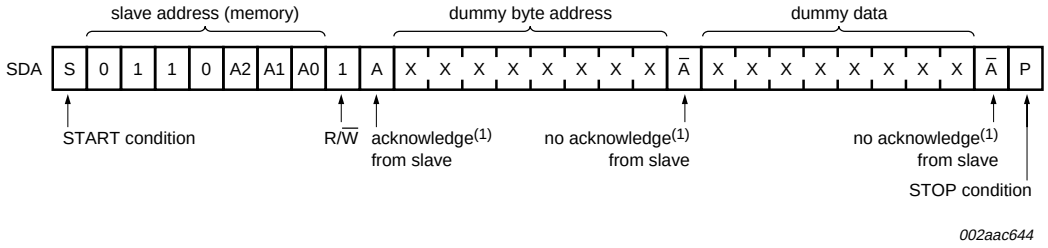
The device does not acknowledge when there is no match on the 7-bit address or when the device is already in permanent write protection mode and is programmed with any write protection instructions (i.e., PWP, RWP, CWP).



X = Don't Care

(1) Refer to Table 6 regarding the exact state of the acknowledge bit.

Fig 16. Software Write Protect (write)



X = Don't Care

(1) Refer to Table 7 regarding the exact state of the acknowledge bit.

Fig 17. Software Write Protect (read)

7.10.2.1 Permanent Write Protection (PWP)

If the software write-protection has been set with the PWP instruction, the first 128 bytes of the memory are permanently write-protected. This write-protection cannot be cleared by any instruction, or by power-cycling the device. Also, once the PWP instruction has been successfully executed, the device no longer acknowledges any instruction (with 4-bit fixed address of 0110b) to access the write-protection settings.

7.10.2.2 Reversible Write Protection (RWP) and Clear Reversible Write Protection (CRWP)

If the software write-protection has been set with the RWP instruction, it can be cleared again with a CRWP instruction.

The two instructions, RWP and CRWP have the same format as a Byte Write instruction, but with a different setting for the hardware address pins (as shown in Table 5). Like the Byte Write instruction, it is followed by an address byte and a data byte, but in this case the contents are all 'Don't Care' (Figure 16). Another difference is that the voltage, $V_{I(ov)}$, must be applied on the A0 pin, and specific logical levels must be applied on the other two (A1 and A2), as shown in Table 5.

Table 6. Acknowledge when writing data or defining write protection

Instructions with R/$\overline{W}$ bit = 0.

Status	Instruction	ACK	Address	ACK	Data byte	ACK	Write cycle ($T_{cy(W)}$)
Permanently protected	PWP, RWP or CRWP	NACK	not significant	NACK	not significant	NACK	no
	page or byte write in lower 128 bytes	ACK	address	ACK	data	NACK	no
Protected with RWP	RWP	NACK	not significant	NACK	not significant	NACK	no
	CRWP	ACK	not significant	ACK	not significant	ACK	yes
	PWP	ACK	not significant	ACK	not significant	ACK	yes
	page or byte write in lower 128 bytes	ACK	address	ACK	data	NACK	no
Not protected	PWP or RWP	ACK	not significant	ACK	not significant	ACK	yes
	CRWP	ACK	not significant	ACK	not significant	ACK	no
	page or byte write	ACK	address	ACK	data	ACK	yes

7.10.2.3 Read Permanent Write Protection (RPWP), Read Reversible Write Protection (RRWP), and Read Clear Reversible Write Protection (RCRWP)

Read PWP, RWP, and CRWP allow the SE97 to be read in write protection mode. The instruction format is the same as that of the write protection except that the 8th bit, R/$\overline{W}$, is set to 1. Figure 17 shows the instruction format, while Table 7 shows the responses when the instructions are issued.

Table 7. Acknowledge when reading the write protection

Instructions with R/$\overline{W}$ bit = 1.

Status	Instruction	ACK	Address	ACK	Data byte	ACK
Permanently protected	RPWP, RRWP or RCRWP	NACK	not significant	NACK	not significant	NACK
Protected with RWP	RRWP	NACK	not significant	NACK	not significant	NACK
	RCRWP	ACK	not significant	NACK	not significant	NACK
	RPWP	ACK	not significant	NACK	not significant	NACK
Not protected	RPWP, RRWP or RCRWP	ACK	not significant	NACK	not significant	NACK

7.10.3 Read operations

7.10.3.1 Current address read

In Standby mode, the SE97 internal address counter points to the data byte immediately following the last byte accessed by a previous operation. If the 'previous' byte was the last byte in memory, then the address counter will point to the first memory byte, and so on. If the SE97 decodes a slave address with a '1' in the R/$\overline{W}$ bit position (Figure 18), it will issue an Acknowledge in the ninth clock cycle and will then transmit the data byte being pointed at by the address counter. The master can then stop further transmission by issuing a No Acknowledge on the ninth bit then followed by a STOP condition.

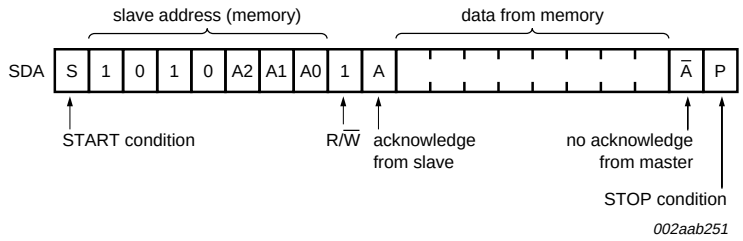


Fig 18. Current address read timing

7.10.3.2 Selective read

The read operation can also be started at an address different from the one stored in the address counter. The address counter can be 'initialized' by performing a 'dummy' write operation (Figure 19). The START condition is followed by the slave address (with the R/$\overline{W}$ bit set to '0') and the desired byte address. Instead of following-up with data, the master then issues a second START, followed by the 'Current Address Read' sequence, as described in Section 7.10.3.1.

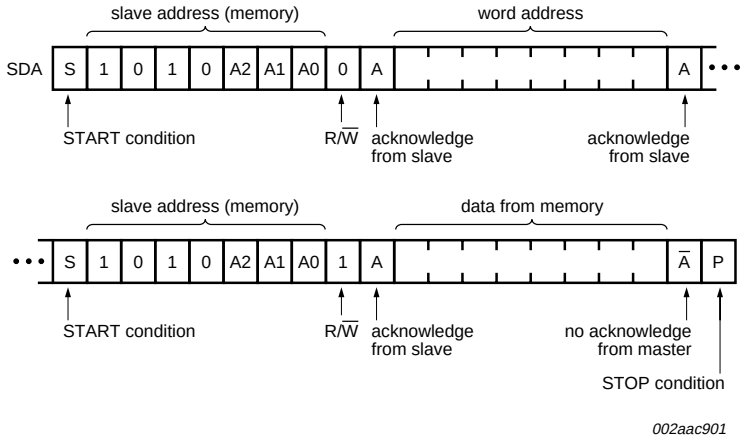


Fig 19. Selective read timing

7.10.3.3 Sequential read

If the master acknowledges the first data byte transmitted by the SE97, then the device will continue transmitting as long as each data byte is acknowledged by the master (Figure 20). If the end of memory is reached during sequential Read, the address counter will 'wrap around' to the beginning of memory, and so on. Sequential Read works with either 'Immediate Address Read' or 'Selective Read', the only difference being the starting byte address.

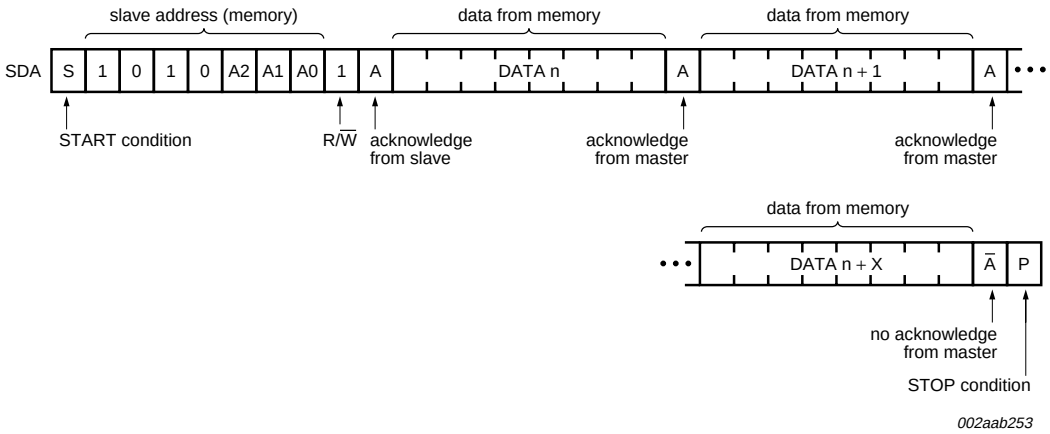


Fig 20. Sequential read timing

7.11 Hot plugging

The SE97 can be used in hot plugging applications. Internal circuitry prevents damaging current backflow through the device when it is powered down, but with the I²C-bus, $\overline{\text{EVENT}}$ or address pins still connected. The open-drain SDA and $\overline{\text{EVENT}}$ pins (SCL and address pins are input only) effectively places the outputs in a high-impedance state during power-up and power-down, which prevents driver conflict and bus contention. The 50 ns noise filter will filter out any insertion glitches from the state machine, which is very robust and not prone to false operation.

The device needs a proper power-up sequence to reset itself, not only for the device I²C-bus and I/O initial states, but also to load specific pre-defined data or calibration data into its operational registers. The power-up sequence should occur correctly with a fast ramp rate and the I²C-bus active. The SE97 might not respond immediately after power-up, but it should not damage the part if the power-up sequence is abnormal. If the SCL line is held LOW, the part will not exit the power-on reset mode since the part is held in reset until SCL is released.

8. Register descriptions

8.1 Register overview

This section describes all the registers used in the SE97. The registers are used for latching the temperature reading, storing the low and high temperature limits, configuring, the hysteresis threshold and the ADC, as well as reporting status. The device uses the pointer register to access these registers. Read registers, as the name implies, are used for read only, and the write registers are for write only. Any attempt to read from a write-only register will result in reading ‘0’s. Writing to a read-only register will have no effect on the read even though the write command is acknowledged. The Pointer register is an 8-bit register. All other registers are 16-bit.

Table 8. Register summary

Address (hex)	Default state (hex)	Register name
n/a	n/a	Pointer register
00h	0017h	Capability register (B grade = 0017h)
01h	0000h	Configuration register
02h	0000h	Upper Boundary Alarm Trip register
03h	0000h	Lower Boundary Alarm Trip register
04h	0000h	Critical Alarm Trip register
05h	n/a	Temperature register
06h	1131h	Manufacturer ID register
07h	A200h	Device ID/Revision register
08h to 21h	0000h	reserved registers
22h	0000h	SMBus register
23h to FFh	0000h	reserved registers

A write to reserved registers my cause unexpected results which may result in requiring a reset by removing and re-applying its power.

8.2 Capability register (00h, 16-bit read-only)

Table 9. Capability register (address 00h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	RFU							
Default	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	RFU		VHV	TRES		WRNG	HACC	BCAP
Default	0	0	0[1]	1	0	1	1	1
Access	R	R	R	R	R	R	R	R

[1] The SE97 A0 pin can support up to 10 V, but the final die was already taped out before the JC42.4 ballot 1435.00 register change could be implemented. Bit 5 is changed from '0' to '1' on the future 1.7 V to 3.6 V SE97B.

Table 10. Capability register (address 00h) bit description

Bit	Symbol	Description
15:6	RFU	Reserved for future use; must be zero.
5	VHV	High voltage standoff for pin A0. 0 — default 1 — This part can support a voltage up to 10 V on the A0 pin to support JC42.4 ballot 1435.00.
4:3	TRES	Temperature resolution. 10 — 0.125 °C LSB (11-bit)
2	WRNG	Wider range. 1 — can read temperatures below 0 °C and set sign bit accordingly
1	HACC	Higher accuracy (set during manufacture). 1 — B grade accuracy
0	BCAP	Basic capability. 1 — has Alarm and Critical Trips interrupt capability

8.3 Configuration register (01h, 16-bit read/write)

Table 11. Configuration register (address 01h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	RFU					HEN		SHMD
Default	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CTLB	AWLB	CEVNT	ESTAT	EOCTL	CVO	EP	EMD
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 12. Configuration register (address 01h) bit description

Bit	Symbol	Description
15:11	RFU	reserved for future use; must be ‘0’.
10:9	HEN	Hysteresis Enable. 00 — disable hysteresis (default) 01 — enable hysteresis at 1.5 °C 10 — enable hysteresis at 3 °C 11 — enable hysteresis at 6 °C When enabled, hysteresis is applied to temperature movement around trigger points. For example, consider the behavior of the ‘Above Alarm Window’ bit (bit 14 of the Temperature register) when the hysteresis is set to 3 °C. As the temperature rises, bit 14 will be set to ‘1’ (temperature is above the alarm window) when the Temperature register contains a value that is greater than the value in the Alarm Temperature Upper Boundary register. If the temperature decreases, bit 14 will remain set until the measured temperature is less than or equal to the value in the Alarm Temperature Upper Boundary register minus 3 °C. (Refer to Figure 7 and Table 13). Similarly, the ‘Below Alarm Window’ bit (bit 13 of the Temperature register) will be set to ‘0’ (temperature is equal to or above the Alarm Window Lower Boundary Trip register) when the value in the Temperature register is equal to or greater than the value in the Alarm Temperature Lower Boundary register. As the temperature decreases, bit 13 will be set to ‘1’ when the value in the Temperature register is equal to or less than the value in the Alarm Temperature Lower Boundary register minus 3 °C. Note that hysteresis is also applied to $\overline{\text{EVENT}}$ pin functionality. When either of the Critical Trip or Alarm Window lock bits is set, these bits cannot be altered until unlocked.

Table 12. Configuration register (address 01h) bit description *...continued*

Bit	Symbol	Description
8	SHMD	Shutdown Mode. 0 — enabled Temperature Sensor (default) 1 — disabled Temperature Sensor When shut down, the thermal sensor diode and ADC are disabled to save power, no events will be generated. When either of the Critical Trip or Alarm Window lock bits is set, this bit cannot be set until unlocked. However, it can be cleared at any time. **Remark:** SMBus Time-out works over the entire supply range of 1.7 V to 3.6 V unless the shutdown bit (SHMD) is set and turns off the oscillator. • The EEPROM read works over the entire supply range of 1.7 V to 3.6 V whether or not SHMD is set because it does not need oscillator to function. There is no undervoltage lockout, the device no longer responds at some voltage below 1.7 V. • EEPROM write works over the supply range of 3.0 V to 3.6 V, but not if SHMD is set since the oscillator is needed to write to EEPROM. There is an undervoltage lockout around 2.7 V that disables the RRPROM write operation. • Thermal sensor is operational over the supply range of 3.0 V to 3.6 V, but not if SHMD is set since the oscillator is needed. There is an undervoltage lockout around 2.7 V that disables the temp sensor. **Thermal sensor auto turn-off feature:** It was determined during testing of the SE97TP on 5 May 2008 that the Thermal Sensor auto turn-off feature was not compatible with the JEDEC power supply maximum ramp rate of 70 ms to 100 ms (slowest ramp rate) and this feature was disabled for all SE97 samples/production devices tested after 6 May (wk 0818 date code is when the devices were assembled). If there is a slow ramp rate on the supply voltage to 3.3 V the SE97 would be EE read only and not Thermal Sensor. This is due to a feature integrated into the device to automatically turn off the oscillator and place the thermal sensor in shutdown if the SE97 was being used in SO-DIMM in notebook applications at 1.8 V to reduce the power consumption on the battery. The feature counts for 30 ms (± 5 ms) after the oscillator starts working (around 1.2 V to 1.7 V) and if at 30 ms the voltage is greater than 2.4 V, the oscillator is left on and the Thermal Sensor functions as normal. But if the voltage is less than 2.4 V at 30 ms, the oscillator is turned off and the SE97 will think the part is in SPD only mode defaulting to the oscillator and Thermal Sensor disabled (SHMD Shutdown Mode bit 8 = 1). The oscillator and Thermal Sensor can be re-enabled by writing a logic 0 to SHMD. It is important in RDIMM/server applications that the Thermal Sensor is working as the default condition since the Thermal Sensor needs to be compatible with the JEDEC power supply ramp rate (maximum ramp rate is 70 ms to 100 ms) so the Thermal Sensor auto turn-off feature was disabled starting on 6 May 2008 by changing a programmable bit on the device during final test. There is no change in performance of the SE97 with this feature turned off and was verified during characterization. There is no way to read the SE97 registers via the I^2C-bus to determine if the Thermal Sensor auto turn-off feature is enabled or disabled. This is set in a factory only register. You need to check the date code or do an operational test (e.g., run up to < 2.4 V, hold, then go to 3.3 V, then read SHMD bit 8 in the Configuration register to see if it is set to logic 0 (e.g., oscillator running = feature disabled) or logic 1 (e.g., oscillator turned off = feature enabled)). The Thermal Sensor auto turn-off feature is active in all package options prior to wk 0818. The SE97TP and SE97TL were not yet released to production so there is a clear line at release/orderable devices versus samples with this feature disabled in all production devices.

Table 12. Configuration register (address 01h) bit description *...continued*

Bit	Symbol	Description
7	CTLB	Critical Trip Lock bit. 0 — Critical Alarm Trip register is not locked and can be altered (default) 1 — Critical Alarm Trip register settings cannot be altered This bit is initially cleared. When set, this bit will return a '1', and remains locked until cleared by internal Power-on reset. This bit can be written with a single write and do not require double writes.
6	AWLB	Alarm Window Lock bit. 0 — Upper and Lower Alarm Trip registers are not locked and can be altered (default) 1 — Upper and Lower Alarm Trip registers setting cannot be altered This bit is initially cleared. When set, this bit will return a '1' and remains locked until cleared by internal power-on reset. This bit can be written with a single write and does not require double writes.
5	CEVNT	Clear $\overline{\text{EVENT}}$ (write only). 0 — no effect (default) 1 — clears active $\overline{\text{EVENT}}$ in Interrupt mode. Writing to this register has no effect in Comparator mode. When read, this register always returns zero.
4	ESTAT	$\overline{\text{EVENT}}$ Status (read only). 0 — $\overline{\text{EVENT}}$ output condition is not being asserted by this device (default) 1 — $\overline{\text{EVENT}}$ output pin is being asserted by this device due to Alarm Window or Critical Trip condition The actual event causing the event can be determined from the Read Temperature register. Interrupt Events can be cleared by writing to the 'Clear $\overline{\text{EVENT}}$' bit (CEVNT). Writing to this bit will have no effect.
3	EOCTL	$\overline{\text{EVENT}}$ Output Control. 0 — $\overline{\text{EVENT}}$ output disabled (default) 1 — $\overline{\text{EVENT}}$ output enabled When either of the Critical Trip or Alarm Window lock bits is set, this bit cannot be altered until unlocked.
2	CVO	Critical Event Only. 0 — $\overline{\text{EVENT}}$ output on Alarm or Critical temperature event (default) 1 — $\overline{\text{EVENT}}$ only if temperature is above the value in the critical temperature register When the Critical Trip or Alarm Window lock bit is set, this bit cannot be altered until unlocked. • **Advisory note:** – JEDEC specification requires only the Alarm Window lock bit to be set. – Work-around: Clear both Critical Trip and Alarm Window lock bits. – Future 1.7 V to 3.6 V SE97B will require only the Alarm Window lock bit to be set.
1	EP	$\overline{\text{EVENT}}$ Polarity. 0 — active LOW (default) 1 — active HIGH. When either of the Critical Trip or Alarm Window lock bits is set, this bit cannot be altered until unlocked.

Table 12. Configuration register (address 01h) bit description *...continued*

Bit	Symbol	Description
0	EMD	$\overline{\text{EVENT}}$ Mode. 0 — comparator output mode (default) 1 — interrupt mode When either of the Critical Trip or Alarm Window lock bits is set, this bit cannot be altered until unlocked.

Table 13. Hysteresis enable

Action	Below Alarm Window bit (bit 13)		Above Alarm Window bit (bit 14)		Above Critical Trip bit (bit 15)	
	Temperature slope	Threshold temperature	Temperature slope	Threshold temperature	Temperature slope	Threshold temperature
sets	falling	$T_{trip(l)} - T_{hys}$	rising	$T_{trip(u)}$	rising	$T_{th(crit)}$
clears	rising	$T_{trip(l)}$	falling	$T_{trip(u)} - T_{hys}$	falling	$T_{th(crit)} - T_{hys}$

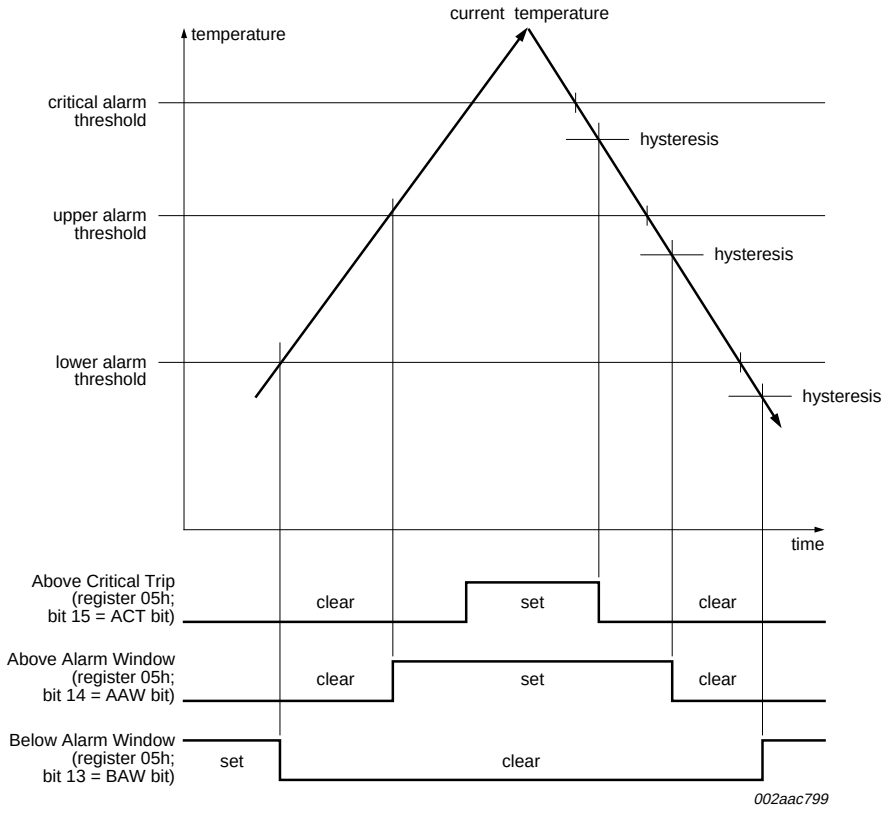


Fig 21. Hysteresis: how it works

8.4 Temperature format

The temperature data from the temperature read back register is an 11-bit 2's complement word with the least significant bit (LSB) equal to 0.125 °C (resolution).

- A value of 019Ch will represent 25.75 °C
- A value of 07C0h will represent 124 °C
- A value of 1E64h will represent –25.75 °C.

The unused LSB (bit 0) is set to '0'. Bit 11 will have a resolution of 128 °C.

The upper 3 bits of the temperature register indicate Trip Status based on the current temperature, and are not affected by the status of the $\overline{\text{EVENT}}$ output.

Table 14 lists the examples of the content of the temperature data register for positive and negative temperature for two scenarios of status bits: status bits = 000b and status bits = 111b.

Table 14. Degree Celsius and Temperature Data register

Temperature	Content of Temperature Data register			
	Status bits = 000b		Status bits = 111b	
	Binary	Hex	Binary	Hex
+125 °C	000 0 01111101 000 0	07D0h	111 0 01111101 000 0	E7D0h
+25 °C	000 0 00011001 000 0	0190h	111 0 00011001 000 0	E190h
+1 °C	000 0 00000001 000 0	0010h	111 0 00000001 000 0	E010h
+0.25 °C	000 0 00000000 010 0	0004h	111 0 00000000 010 0	E004h
+0.125 °C	000 0 00000000 001 0	0002h	111 0 00000000 001 0	E002h
0 °C	000 0 00000000 000 0	0000h	111 0 00000000 000 0	E000h
–0.125 °C	000 1 11111111 111 0	1FFEh	111 1 11111111 111 0	FFFEh
–0.25 °C	000 1 11111111 110 0	1FFCh	111 1 11111111 110 0	FFFCh
–1 °C	000 1 11111111 000 0	1FF0h	111 1 11111111 000 0	FFF0h
–20 °C	000 1 11110100 000 0	1F40h	111 1 11110100 000 0	FF40h
–25 °C	000 1 11100111 000 0	1E70h	111 1 11100111 000 0	FE70h
–55 °C	000 1 11001001 000 0	1C90h	111 1 11001001 000 0	FC90h

8.5 Temperature Trip Point registers

8.5.1 Upper Boundary Alarm Trip register (16-bit read/write)

The value is the upper threshold temperature value for Alarm mode. The data format is 2's complement with bit 2 = 0.25 °C. 'RFU' bits will always report zero. Interrupts will respond to the presently programmed boundary values. If boundary values are being altered in-system, it is advised to turn off interrupts until a known state can be obtained to avoid superfluous interrupt activity.

Table 15. Upper Boundary Alarm Trip register bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	RFU			SIGN	UBT			
Default	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	UBT						RFU	
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Table 16. Upper Boundary Alarm Trip register bit description

Bit	Symbol	Description
15:13	RFU	reserved; always '0'
12	SIGN	Sign (MSB)
11:2	UBT	Upper Boundary Alarm Trip Temperature (LSB = 0.25 °C)
1:0	RFU	reserved; always '0'

8.5.2 Lower Boundary Alarm Trip register (16-bit read/write)

The value is the lower threshold temperature value for Alarm mode. The data format is 2's complement with bit 2 = 0.25 °C. RFU bits will always report zero. Interrupts will respond to the presently programmed boundary values. If boundary values are being altered in-system, it is advised to turn off interrupts until a known state can be obtained to avoid superfluous interrupt activity.

Table 17. Lower Boundary Alarm Trip register bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	RFU			SIGN	LBT			
Default	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	LBT						RFU	
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Table 18. Lower Boundary Alarm Trip register bit description

Bit	Symbol	Description
15:13	RFU	reserved; always '0'
12	SIGN	Sign (MSB)
11:2	LBT	Lower Boundary Alarm Trip Temperature (LSB = 0.25 °C)
1:0	RFU	reserved; always '0'

8.5.3 Critical Alarm Trip register (16-bit read/write)

The value is the critical temperature. The data format is 2's complement with bit 2 = 0.25 °C. RFU bits will always report zero.

Table 19. Lower Boundary Alarm Trip register bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	RFU			SIGN	CT			
Default	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CT						RFU	
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Table 20. Critical Alarm Trip register bit description

Bit	Symbol	Description
15:13	RFU	reserved; always '0'
12	SIGN	Sign (MSB)
11:2	CT	Critical Alarm Trip Temperature (LSB = 0.25 °C)
1:0	RFU	reserved; always '0'

8.6 Temperature register (16-bit read-only)

Table 21. Temperature register bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	ACT	AAW	BAW	SIGN	TEMP			
Default	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	TEMP							RFU
Default	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 22. Temperature register bit description

Bit	Symbol	Description
15	ACT	Above Critical Trip. Increasing T_{amb}: 0 — $T_{amb} < T_{th(crit)}$ 1 — $T_{amb} \geq T_{th(crit)}$ Decreasing T_{amb}: 0 — $T_{amb} < T_{th(crit)} - T_{hys}$ 1 — $T_{amb} \geq T_{th(crit)} - T_{hys}$
14	AAW	Above Alarm Window. Increasing T_{amb}: 0 — $T_{amb} \leq T_{trip(u)}$ 1 — $T_{amb} > T_{trip(u)}$ Decreasing T_{amb}: 0 — $T_{amb} \leq T_{trip(u)} - T_{hys}$ 1 — $T_{amb} > T_{trip(u)} - T_{hys}$
13	BAW	Below Alarm Window. Increasing T_{amb}: 0 — $T_{amb} \geq T_{trip(l)}$ 1 — $T_{amb} < T_{trip(l)}$ Decreasing T_{amb}: 0 — $T_{amb} \geq T_{trip(l)} - T_{hys}$ 1 — $T_{amb} < T_{trip(l)} - T_{hys}$
12	SIGN	Sign bit. 0 — positive temperature value 1 — negative temperature value
11:1	TEMP	Temperature Value (2's complement). (LSB = 0.125 °C)
0	RFU	reserved; always '0'

8.7 Manufacturer's ID register (16-bit read-only)

The SE97 Manufacturer's ID register is intended to match NXP Semiconductors PCI SIG (1131h).

Table 23. Manufacturer's ID register bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	Manufacturer ID							
Default	0	0	0	1	0	0	0	1
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	(continued)							
Default	0	0	1	1	0	0	0	1
Access	R	R	R	R	R	R	R	R

8.8 Device ID register

The SE97 device ID is A1h. The device revision varies by device.

Table 24. Device ID register bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	Device ID							
Default	1	0	1	0	0	0	1	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	Device revision							
Default	0	0	0	0	0	0	[1]	[1]
Access	R	R	R	R	R	R	R	R

[1] 00 for SE97PW, SE97TK (original).
01 for SE97TL, SE97TP (improved V_{POR} and $\overline{EVENT}$ I_{OL}).

8.9 SMBus register

Table 25. SMBus Time-out register bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	RFU							
Default	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	STMOUT	RFU						SALRT
Default	0	0	0	0	0	0	0	0
Access	R/W	R	R	R	R	R	R	R/W

Table 26. SMBus Time-out register bit description

Bit	Symbol	Description
15:8	RFU	reserved; always ‘0’
7	STMOUT	SMBus time-out. 0 — SMBus time-out is enabled (default) 1 — disable SMBus time-out When either of the Critical Trip or Alarm Window lock bits is set, this bit cannot be altered until unlocked.
6:1	RFU	reserved; always ‘0’
0	SALRT	SMBus Alert Response Address (ARA). 0 — SMBus ARA is enabled (default) 1 — disable SMBus ARA When either of the Critical Trip or Alarm Window lock bits is set, this bit cannot be altered until unlocked.

9. Application design-in information

In a typical application, the SE97 behaves as a slave device and interfaces to a bus master (or host) via the SCL and SDA lines. The $\overline{\text{EVENT}}$ output is monitored by the host, and asserts when the temperature reading exceeds the programmed values in the alarm registers. The A0, A1 and A2 pins are directly connected to V_{DD} or V_{SS} without any pull-up resistors. The SDA and SCL serial interface pins are open-drain I/Os that require pull-up resistors, and are able to sink a maximum of 3 mA with a voltage drop less than 0.4 V. Typical pull-up values for SCL and SDA are 10 kΩ, but the resistor values can be changed in order to meet the rise time requirement if the capacitance load is too large due to routing, connectors, or multiple components sharing the same bus.

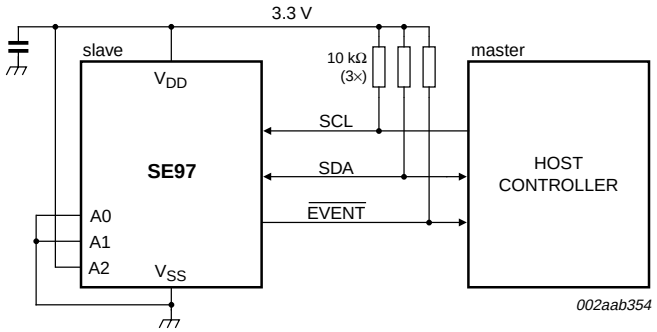


Fig 22. Typical application showing SE97 interfacing with 3.3 V host

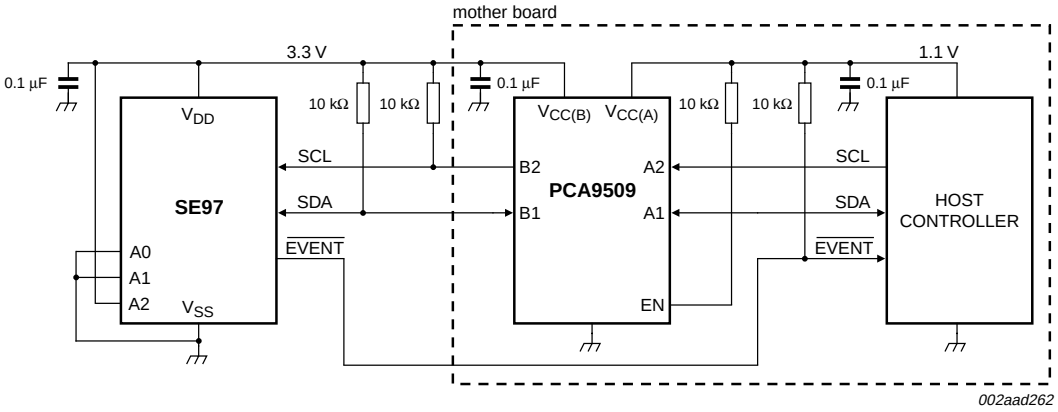


Fig 23. SE97 interfacing with 1.1 V host controller

9.1 SE97 in memory module application

Figure 24 shows the SE97 being placed in the memory module application. The SE97 is centered in the memory module to monitor the temperature of the DRAM and also to provide a 2-kbit EEPROM as the Serial Presence Detect (SPD). In the event of overheating, the SE97 triggers the $\overline{\text{EVENT}}$ output and the memory controller throttles the memory bus to slow the DRAM. The memory controller can also read the SE97 and watch the DRAM thermal behavior, taking preventive measures when necessary.

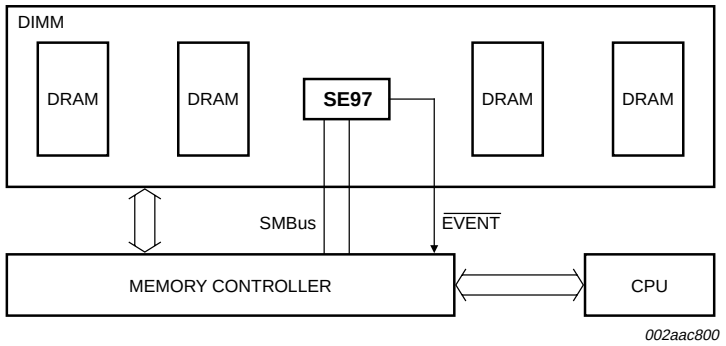


Fig 24. System application

9.2 Layout consideration

The SE97 does not require any additional components other than the host controller to read its temperature. It is recommended that a 0.1 µF bypass capacitor between the V_{DD} and V_{SS} pins is located as close as possible to the power and ground pins for noise protection.

9.3 Thermal considerations

In general, self-heating is the result of power consumption and not a concern, especially with the SE97, which consumes very low power. In the event the SDA and $\overline{\text{EVENT}}$ pins are heavily loaded with small pull-up resistor values, self-heating affects temperature accuracy by approximately 0.5 °C.

Equation 1 is the formula to calculate the effect of self-heating:

$$\Delta T = R_{th(j\text{-}a)} \times [(V_{DD} \times I_{DD(AV)}) + (V_{OL(SDA)} \times I_{OL(sink)(SDA)}) + (V_{OL(EVENT)} \times I_{OL(sink)EVENT})] \quad (1)$$

where:

$\Delta T = T_j - T_{amb}$

T_j = junction temperature

T_{amb} = ambient temperature

$R_{th(j\text{-}a)}$ = package thermal resistance

V_{DD} = supply voltage

$I_{DD(AV)}$ = average supply current

$V_{OL(SDA)}$ = LOW-level output voltage on pin SDA

$V_{OL(EVENT)}$ = LOW-level output voltage on pin $\overline{EVENT}$

$I_{OL(sink)(SDA)}$ = SDA output current LOW

$I_{OL(sink)EVENT}$ = $\overline{EVENT}$ output current LOW

Calculation example:

T_{amb} (typical temperature inside the notebook) = 50 °C

$I_{DD(AV)}$ = 400 µA

V_{DD} = 3.6 V

Maximum $V_{OL(SDA)}$ = 0.4 V

$I_{OL(sink)(SDA)}$ = 1 mA

$V_{OL(EVENT)}$ = 0.4 V

$I_{OL(sink)EVENT}$ = 3 mA

$R_{th(j-a)}$ of HVSON8 = 56 °C/W

$R_{th(j-a)}$ of TSSOP8 = 160 °C/W

Self heating due to power dissipation for HVSON8 is:

$$\Delta T = 56 \times [(3.6 \times 0.4) + (0.4 \times 3) + (0.4 \times 1)] = 56\ °C/W \times 3.04\ mW = 0.17\ °C \quad (2)$$

Self heating due to power dissipation for TSSOP8 is:

$$\Delta T = 160 \times [(3.6 \times 0.4) + (0.4 \times 3) + (0.4 \times 1)] = 160\ °C/W \times 3.04\ mV = 0.49\ °C \quad (3)$$

10. Limiting values

Table 27. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.3	+4.2	V
V_n	voltage on any other pin	SDA, SCL, $\overline{EVENT}$ pins	–0.3	+4.2	V
V_{A0}	voltage on pin A0	overvoltage input; A0 pin	–0.3	+12.5	V
I_{sink}	sink current	at SDA, SCL, $\overline{EVENT}$ pins	–1	+50.0	mA
$T_{j(max)}$	maximum junction temperature		-	150	°C
T_{stg}	storage temperature		–65	+165	°C

11. Characteristics

Table 28. SE97 thermal sensor characteristics

V_{DD} = 3.0 V to 3.6 V; T_{amb} = −40 °C to +125 °C; unless otherwise specified.

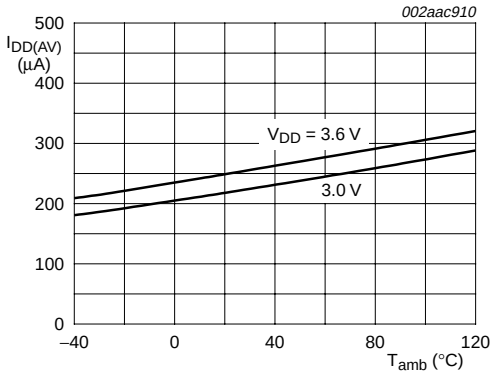
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{lim(acc)}$	temperature limit accuracy	B grade; V_{DD} = 3.3 V ± 10 %				
		T_{amb} = 75 °C to 95 °C	−1.0	< ±0.5	+1.0	°C
		T_{amb} = 40 °C to 125 °C	−2.0	< ±1.0	+2.0	°C
		T_{amb} = −40 °C to +125 °C	−3.0	< ±2	+3.0	°C
T_{res}	temperature resolution		-	0.125	-	°C
T_{conv}	conversion period	conversion time from STOP bit to conversion complete	-	100	120	ms
$E_{f(conv)}$	conversion rate error	percentage error in programmed data	−30	-	+30	%

Table 29. DC characteristics

V_{DD} = 1.7 V to 3.6 V; T_{amb} = −40 °C to +125 °C; unless otherwise specified. These specifications are guaranteed by design.

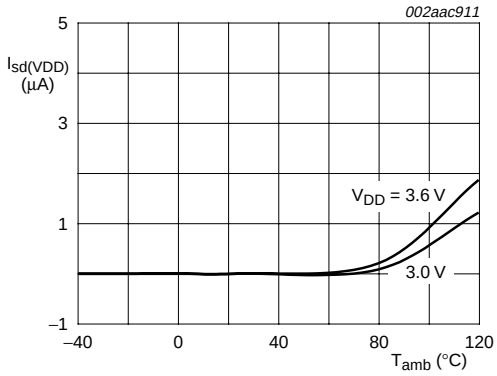
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{DD(AV)}$	average supply current	SMBus inactive		-	250	400	µA
$I_{sd(VDD)}$	supply voltage shutdown mode current	SMBus inactive		-	0.1	5.0	µA
V_{IH}	HIGH-level input voltage	SCL, SDA; V_{DD} = 3.0 V to 3.6 V		0.7 × V_{DD}	-	V_{DD} + 1	V
V_{IL}	LOW-level input voltage	SCL, SDA; V_{DD} = 3.0 V to 3.6 V		-	-	0.3 × V_{DD}	V
V_{OL1}	LOW-level output voltage 1	V_{DD} = 3.0 V; I_{OL} = 3 mA		-	-	0.4	V
V_{OL2}	LOW-level output voltage 2	V_{DD} = 1.7 V; I_{OL} = 1.5 mA		-	-	0.5	V
$V_{I(ov)}$	overvoltage input voltage	pin A0; $V_{I(ov)} - V_{DD}$ > 4.8 V	[1]	7.8	-	10	V
V_{POR}	power-on reset voltage	power supply rising		-	-	1.7	V
		power supply falling					
		SE97PW, SE97TK		0.1	-	-	V
		SE97TL, SE97TP		0.6	-	-	V
$I_{OL(sink)EVENT}$	LOW-level output sink current on pin $\overline{EVENT}$	V_{OL1} = 0.4 V					
		SE97PW, SE97TK		2	-	-	mA
		SE97TL, SE97TP		6	-	-	mA
$I_{OL(sink)(SDA)}$	LOW-level output sink current on pin SDA	V_{OL2} = 0.5 V		3	-	-	mA
I_{LOH}	HIGH-level output leakage current	$\overline{EVENT}$; $V_{OH} = V_{DD}$		−1.0	-	+1.0	µA
I_{LIH}	HIGH-level input leakage current	SDA, SCL; $V_I = V_{DD}$		−1.0	-	+1.0	µA
I_{LIL}	LOW-level input leakage current	SDA, SCL; $V_I = V_{SS}$		−1.0	-	+1.0	µA
		A0, A1, A2; $V_I = V_{SS}$		−1.0	-	+1.0	µA
$C_{i(SCL/SDA)}$	SCL and SDA input capacitance			-	5	10	pF
I_L	leakage current	on A0, A1, A2		-	1	-	µA
I_{pd}	pull-down current	internal; A0, A1, A2 pins; V_I = 0.3V_{DD} to V_{DD}		-	-	4.0	µA
Z_{IL}	LOW-level input impedance	pins A0, A1, A2; V_I < 0.3V_{DD}		30	-	-	kΩ
Z_{IH}	HIGH-level input impedance	pins A0, A1, A2		800	-	-	kΩ

[1] High-voltage input voltage applied to pin A0 during RWP and CRWP operations. The JEDEC specification is 7 V (min.) and 10 V (max.), but since the SE97 EEPROM write works only down to 3.0 V, the condition of $V_{I(ov)}$ > 4.8 V + V_{DD} or > 4.8 V + 3.0 V was applied and the minimum voltage changed to 7.8 V. If V_{DD} is 3.6 V then the minimum voltage is 8.4 V.



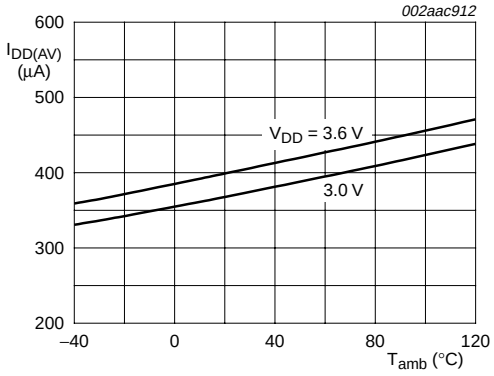
I^2C-bus and EEPROM inactive.

Fig 25. Average supply current



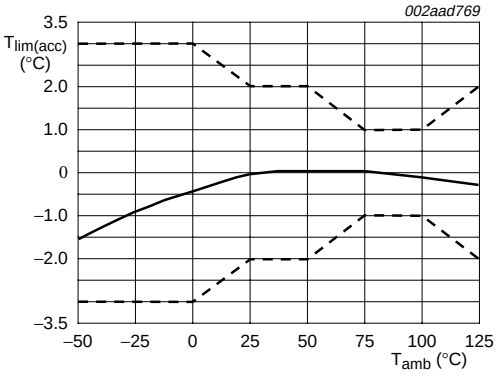
I^2C-bus, temp sensor and EEPROM inactive.

Fig 26. Shutdown supply current



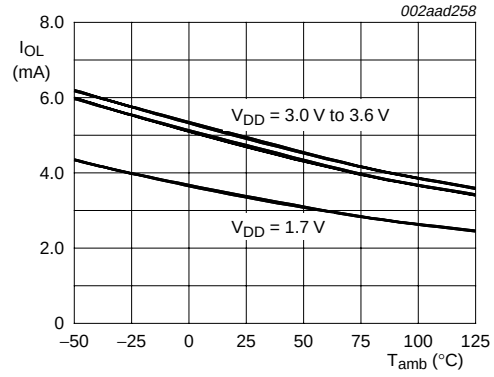
Temp sensor and EEPROM active.

Fig 27. Average supply current during EEPROM write



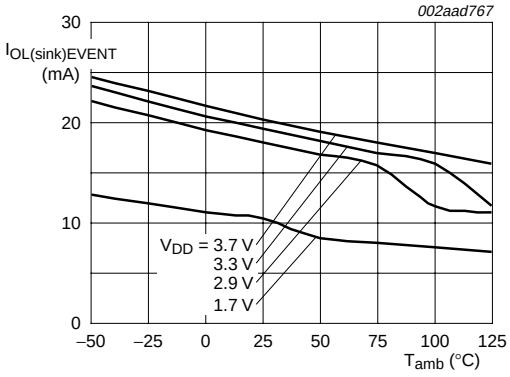
V_{DD} = 3.0 V to 3.6 V.

Fig 28. Typical temperature accuracy



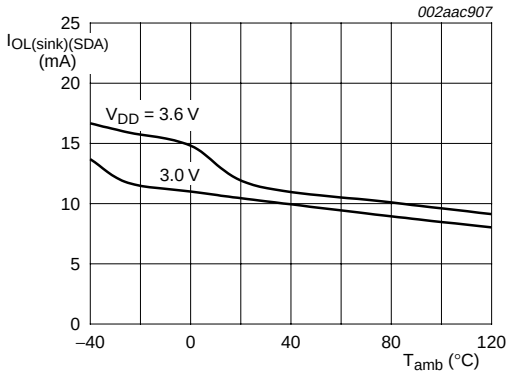
V_{OL1} = 0.4 V.

Fig 29. $\overline{EVENT}$ output current SE97PW, SE97TK



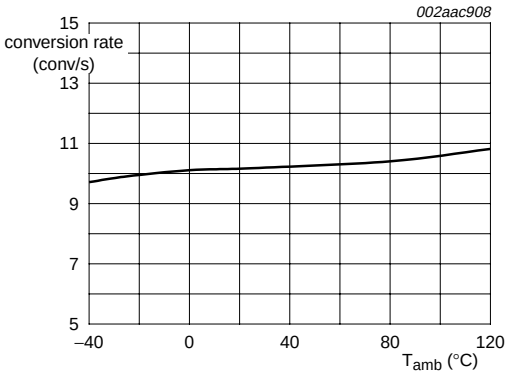
V_{OL1} = 0.4 V.

Fig 30. $\overline{EVENT}$ output current SE97TL, SE97TP



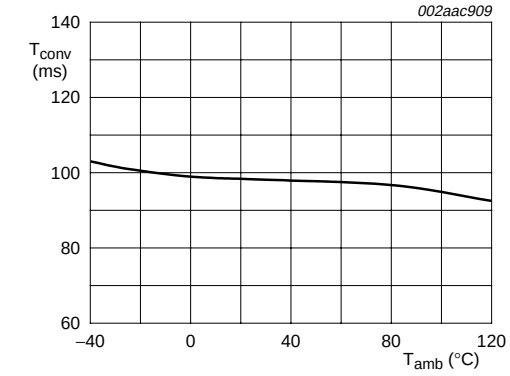
V_{OL2} = 0.6 V.

Fig 31. SDA output current



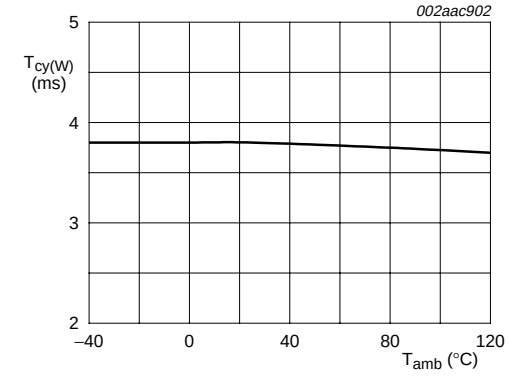
V_{DD} = 3.0 V to 3.6 V.

Fig 32. Conversion rate



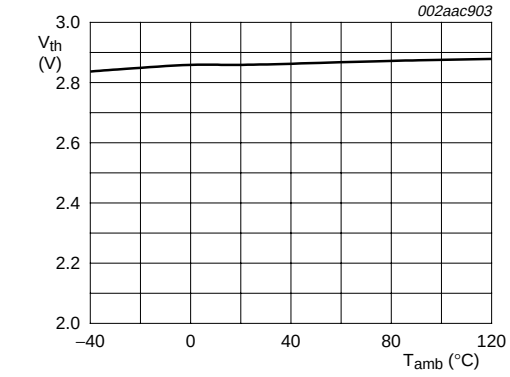
V_{DD} = 3.0 V to 3.6 V.

Fig 33. Conversion period



V_{DD} = 3.0 V to 3.6 V.

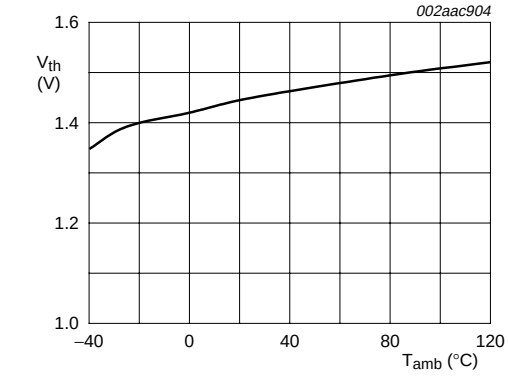
Fig 34. EEPROM write cycle time



For temp sensor conversion.

V_{DD} = 3.0 V to 3.6 V.

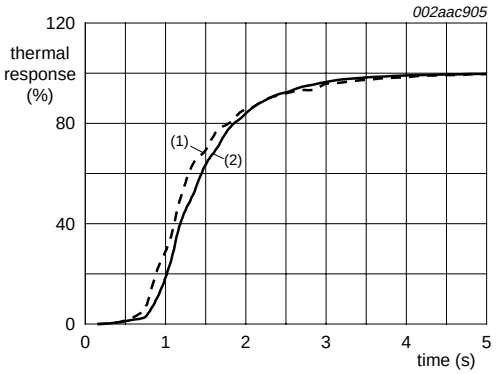
Fig 35. Average power-on threshold voltage



For EEPROM read operation.

V_{DD} = 1.7 V to 3.6 V.

Fig 36. Average power-on threshold voltage



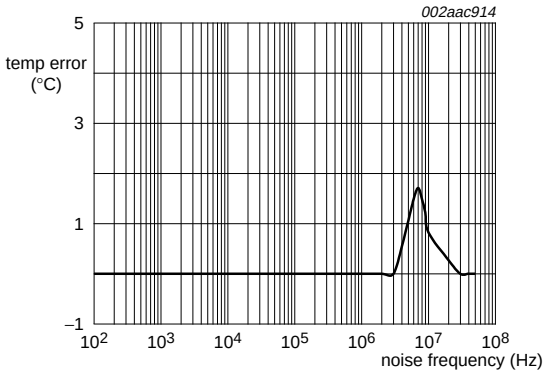
V_{DD} = 3.0 V to 3.6 V.

From 25 °C (air) to 120 °C (oil bath).

(1) TSSOP8

(2) HVSON8, HWSON8, HXSON8

Fig 37. Package thermal response



V_{DD} = 3.3 V + 150 mV (p-p); 0.1 µF AC coupling capacitor; no decoupling capacitor; T_{amb} = 25 °C.

Fig 38. Temperature error versus power supply noise frequency

Table 30. SMBus AC characteristics

V_{DD} = 1.7 V to 3.6 V; T_{amb} = −40 °C to +125 °C; unless otherwise specified. These specifications are guaranteed by design. The AC specifications fully meet or exceed SMBus 2.0 specifications, but allow the bus to interface with the I^2C-bus from DC to 400 kHz.

Symbol	Parameter	Conditions		Standard mode		Fast mode		Unit
				Min	Max	Min	Max	
f_{SCL}	SCL clock frequency			10[1]	100	10[1]	400	kHz
t_{HIGH}	HIGH period of the SCL clock	70 % to 70 %		4000	-	600	-	ns
t_{LOW}	LOW period of the SCL clock	30 % to 30 %		4700	-	1300	-	ns
$t_{to(SMBus)}$	SMBus time-out time	LOW period to reset SMBus		25	35	25	35	ms
t_r	rise time of both SDA and SCL signals			-	1000	20	300	ns
t_f	fall time of both SDA and SCL signals			-	300	-	300	ns
$t_{SU;DAT}$	data set-up time			250	-	100	-	ns
$t_{h(i)(D)}$	data input hold time		[2][3]	0	-	0	-	ns
$t_{HD;DAT}$	data hold time		[4]	200	3450	200	900	ns
$t_{SU;STA}$	set-up time for a repeated START condition		[5]	4700	-	600	-	ns
$t_{HD;STA}$	hold time (repeated) START condition	30 % of SDA to 70 % of SCL	[6]	4000	-	600	-	ns
$t_{SU;STO}$	set-up time for STOP condition			4000	-	600	-	ns
t_{BUF}	bus free time between a STOP and START condition		[2]	4700	-	1300	-	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter			-	50	-	50	ns
$t_{VD;DAT}$	data valid time	from clock		200	-	200	-	ns
$t_{f(o)}$	output fall time			-	-	-	250	ns
t_{POR}	power-on reset pulse time	power supply falling		0.5	-	0.5	-	µs
EEPROM power-up timing[7]								
$t_{pu(R)}$	read power-up time		[8]	-	1	-	1	ms
$t_{pu(W)}$	write power-up time		[8]	-	1	-	1	ms
Write cycle limits								
$T_{cy(W)}$	write cycle time		[9]	-	10	-	10	ms

[1] Minimum clock frequency is 0 kHz if SMBus Time-out is disabled.

[2] Delay from SDA STOP to SDA START.

[3] A device must internally provide a hold time of at least 200 ns for SDA signal (referenced to the $V_{IH(min)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[4] Delay from SCL HIGH-to-LOW transition to SDA edges.

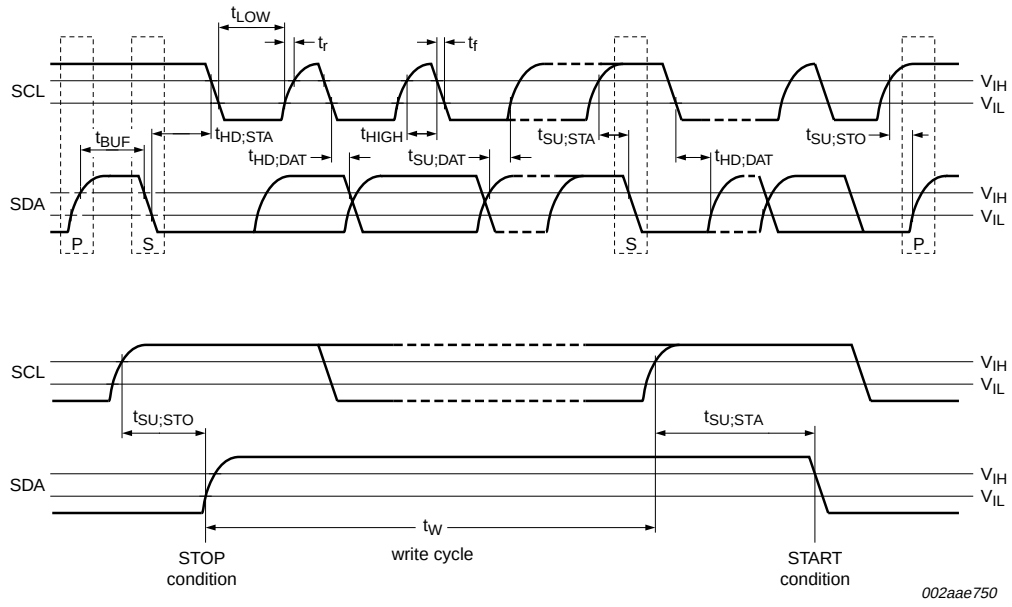
[5] Delay from SCL LOW-to-HIGH transition to restart SDA.

[6] Delay from SDA START to first SCL HIGH-to-LOW transition.

[7] These parameters tested initially and after a design or process change that affects the parameter.

[8] $t_{pu(R)}$ and $t_{pu(W)}$ are the delays required from the time V_{DD} is stable until the specified operation can be initiated.

[9] The write cycle time is the time elapsed between the STOP command (following the write instruction) and the completion of the internal write cycle. During the internal write cycle, SDA is released by the slave and the device does not acknowledge external commands.



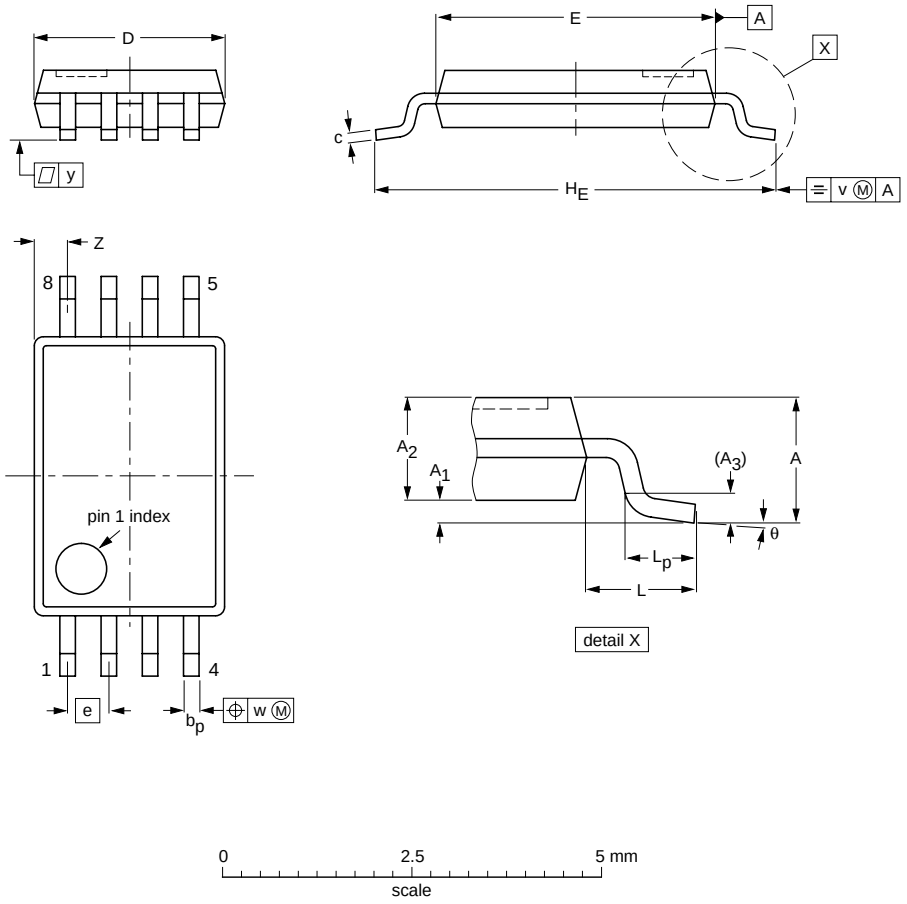
S = START condition

P = STOP condition

Fig 39. AC waveforms

12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 4.4 mm **SOT530-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.85	0.25	0.30 0.19	0.20 0.13	3.1 2.9	4.5 4.3	0.65	6.5 6.3	0.94	0.7 0.5	0.1	0.1	0.1	0.70 0.35	8° 0°

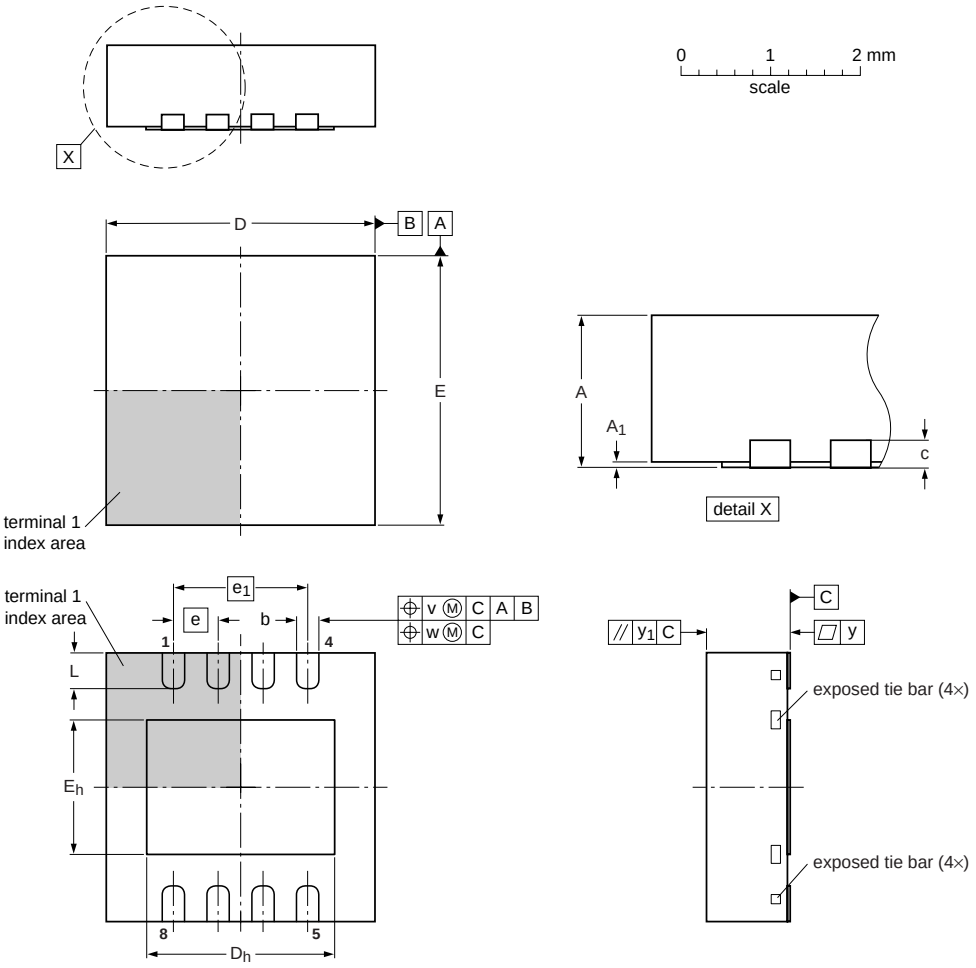
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT530-1		MO-153				~~00-02-24~~ 03-02-18

Fig 40. Package outline SOT530-1 (TSSOP8)

HVSON8: plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 x 3 x 0.85 mm **SOT908-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.3 0.2	0.2	3.1 2.9	2.25 1.95	3.1 2.9	1.65 1.35	0.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

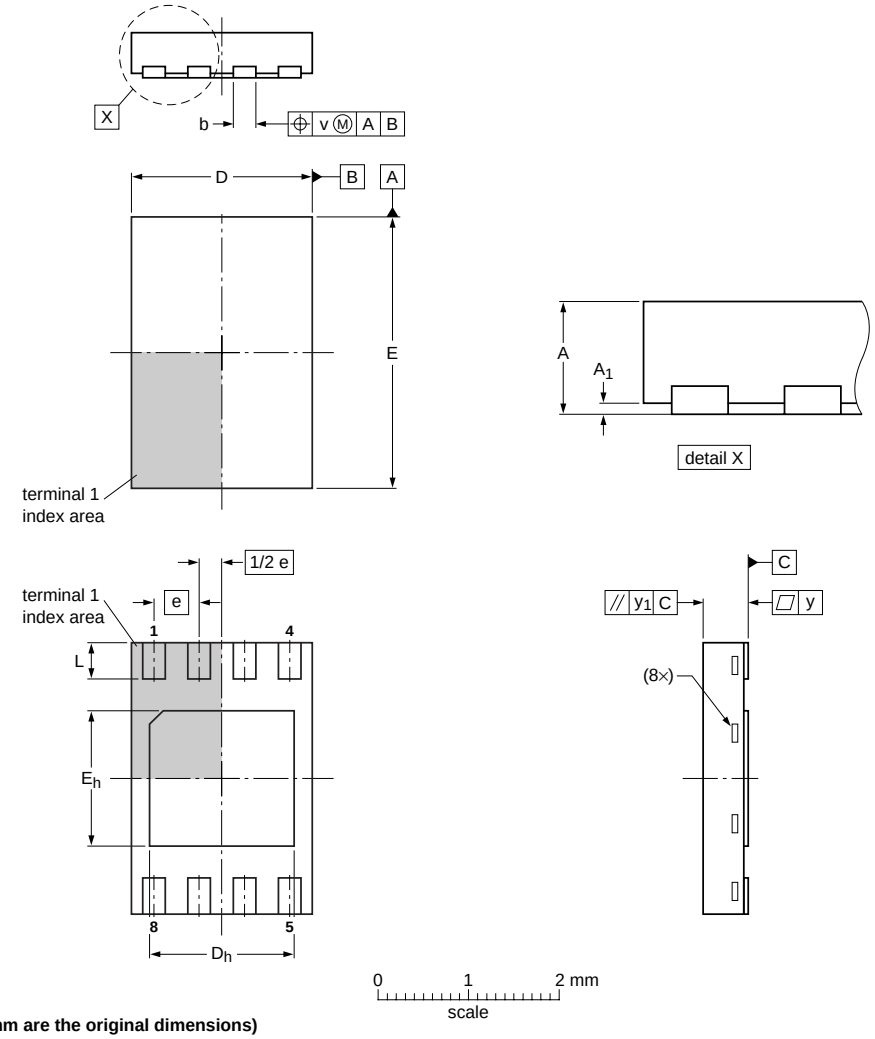
Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT908-1		MO-229				~~05-09-26~~ 05-10-05

Fig 41. Package outline SOT908-1 (HVSON8)

HXSON8: plastic thermal enhanced extremely thin small outline package; no leads; 8 terminals; body 2 x 3 x 0.5 mm **SOT1052-1**



DIMENSIONS (mm are the original dimensions)

UNIT		A(1)	A_1	b	D	D_1	E	E_1	e	L	v	y	y_1
mm	max	0.5	0.04	0.3	2.1	1.6	3.1	1.6		0.45			
	nom				2.0		3.0		0.5		0.1	0.05	0.05
	min			0.2	1.9	1.4	2.9	1.4		0.35			

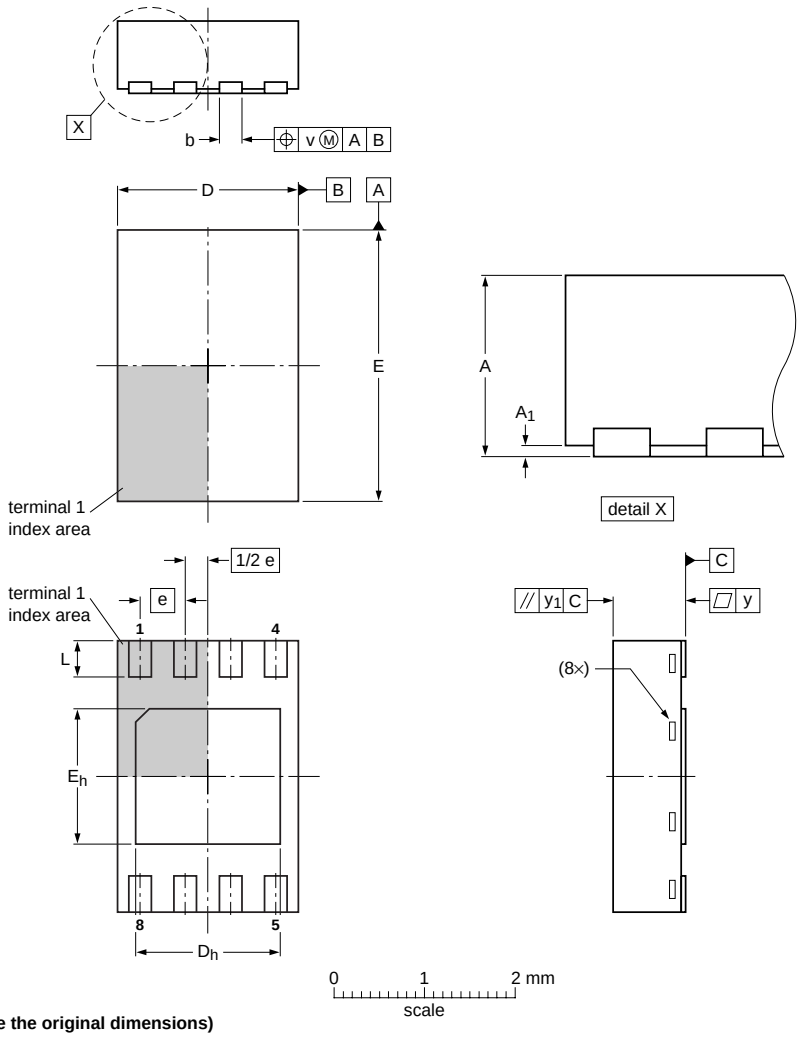
Note

1. Dimension A is including plating thickness. The package footprint is compatible with JEDEC MO229

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT1052-1		MO-229				~~08-01-11~~ 08-03-11

Fig 42. Package outline SOT1052-1 (HXSON8)

HWSON8: plastic thermal enhanced very very thin small outline package; no leads; 8 terminals; body 2 x 3 x 0.8 mm **SOT1069-1**



DIMENSIONS (mm are the original dimensions)

UNIT		A(1)	A_1	b	D	D_1	E	E_1	e	L	v	y	y_1
mm	max	0.8	0.04	0.3	2.1	1.6	3.1	1.6		0.45			
	nom				2.0		3.0		0.5		0.1	0.05	0.05
	min			0.2	1.9	1.4	2.9	1.4		0.35			

Note

1. Dimension A is including plating thickness. The package footprint is compatible with JEDEC MO229

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT1069-1		MO-229				~~08-06-11~~ 08-07-10

Fig 43. Package outline SOT1069-1 (HWSON8)

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 44) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 31 and 32

Table 31. SnPb eutectic process (from J-STD-020C)

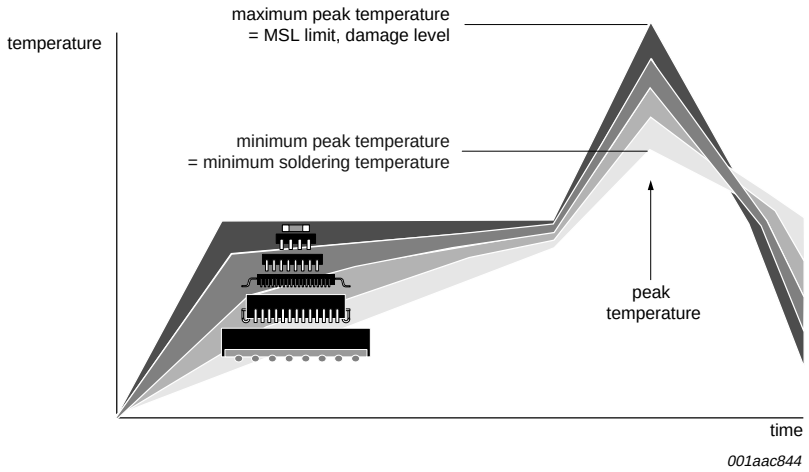
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 32. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 44.



MSL: Moisture Sensitivity Level

Fig 44. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Abbreviations

Table 33. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
ARA	Alert Response Address
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
DDR	Double Data Rate
DIMM	Dual In-line Memory Module
DRAM	Dynamic Random Access Memory
ECC	Error-Correcting Code
EEPROM	Electrically Erasable Programmable Read-Only Memory
ESD	ElectroStatic Discharge
HBM	Human Body Model
I^2C-bus	Inter-Integrated Circuit bus
LSB	Least Significant Bit
MM	Machine Model
MSB	Most Significant Bit
PC	Personal Computer
PCB	Printed-Circuit Board
POR	Power-On Reset

Table 33. Abbreviations *...continued*

Acronym	Description
RDIMM	Registered Dual In-line Memory Module
SMBus	System Management Bus
SO-DIMM	Small Outline Dual In-line Memory Module
SPD	Serial Presence Detect

15. Revision history

Table 34. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SE97_5	20090806	Product data sheet	-	SE97_4

Modifications:

- Section 1 “General description”, 7th paragraph: deleted 5th sentence
- Section 2.1 “General features”:
  - 1st bullet item: changed from “SO-DIMM” to “TSE 2002B3 DIMM ± 0.5 °C (typ.) between 75 °C and 95 °C”
  - 3rd bullet item: changed from “3.0 µA (max.)” to “5.0 µA (max.)”
  - 8th bullet item: appended “(JEDEC PSON8 VCED-3)”
- Table 1 “Ordering information”, Table note [2] re-written
- Section 7.3.2.1 “Alarm window”:
  - 1st Advisory notification, Competitor device: appended “(CEVNT)” to end of phrase
  - 1st Advisory notification, Work-around: appended “(CEVNT)” to end of phrase
  - 2nd Advisory notification, Competitor devices: changed from “... when new UPPER or LOWER and Event bit 3 (EOCTL) are set ... “ to “when new UPPER or LOWER Alarm Windows and the $\overline{\text{EVENT}}$ output are set ...”
  - 2nd Advisory notification, Work-around: appended “(EOCTL = 1)” to end of phrase
- Section 7.3.2.2 “Critical trip”
  - 1st paragraph, last sentence: changed from “... through the Clear $\overline{\text{EVENT}}$ bit ...” to “... through the Clear $\overline{\text{EVENT}}$ bit (CEVNT) ...
  - Advisory notification, Competitor devices: re-written
  - Advisory notification, Work-around: changed from “Wait at least 125 ms before enabling $\overline{\text{EVENT}}$ output, Intel will change Nehalem BIOS so that $T_{th(crit)}$ is set for more than 125 ms before Event bit 3 (EOCTL) is enabled and Event value is checked.” to “Wait at least 125 ms before enabling $\overline{\text{EVENT}}$ output (EOCTL = 1), Intel will change Nehalem BIOS so that $T_{th(crit)}$ is set for more than 125 ms before $\overline{\text{EVENT}}$ output is enabled and Event value is checked.
- Section 7.7 “SMBus time-out”:
  - 1st paragraph, 2nd sentence changed from “... holds SCL LOW more than 35 ms” to “... holds SCL LOW between 25 ns and 35 ns”
  - added 2nd “Remark”
- Section 7.8 “SMBus Alert Response Address (ARA)”: added 2nd “Remark”
- Table 12 “Configuration register (address 01h) bit description”, bit 8, SHMD: added “Remark” and 3 bullet items
- Table 29 “DC characteristics”:
  - $I_{DD(AV)}$: removed condition “V_{DD} = 3.0 V to 3.6 V”
  - $I_{DD(AV)}$: removed sub-row with condition “V_{DD} = 1.7 V”
  - $I_{sd(VDD)}$: changed Max value from “3 µA” to “5.0 µA”

Table 34. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications: (continued)	• Table 30 “SMBus AC characteristics” replaced in its entirety • (old) Figure 39 “Definition of timing for F/S-mode devices on the I^2C-bus” replaced with (new) Figure 39 “AC waveforms”			
SE97_4	20090130	Product data sheet	-	SE97_3
SE97_3	20080715	Product data sheet	-	SE97_2
SE97_2	20071012	Product data sheet	-	SE97_1
SE97_1	20070524	Objective data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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