



**n PIN DESCRIPTIONS**

Name	Function
<b>A0 to A19 Address Input (word mode)</b>	These 20 address inputs select one of the 1,024K x 16 bit in the RAM, if $\overline{\text{BYTE}}$ is HIGH
<b>A0 to A20 Address Input (byte mode) (TSOP only)</b>	These 21 address inputs select one of the 2,048K x 8 bit in the RAM, If $\overline{\text{BYTE}}$ is LOW
<b>CE1 Chip Enable 1 Input CE2 Chip Enable 2 Input</b>	$\overline{\text{CE1}}$ is active LOW and CE2 is active HIGH. Both chip enables must be active when data read from or write to the device. If either chip enable is not active, the device is deselected and is in standby power mode. The DQ pins will be in the high impedance state when the device is deselected.
<b><math>\overline{\text{WE}}</math> Write Enable Input</b>	The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{\text{WE}}$ is HIGH and $\overline{\text{OE}}$ is LOW, output data will be present on the DQ pins; when $\overline{\text{WE}}$ is LOW, the data present on the DQ pins will be written into the selected memory location.
<b><math>\overline{\text{OE}}</math> Output Enable Input</b>	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{\text{OE}}$ is inactive.
<b><math>\overline{\text{LB}}</math> and <math>\overline{\text{UB}}</math> Data Byte Control Input</b>	Lower byte and upper byte data input/output control pins.
<b><math>\overline{\text{BYTE}}</math> Byte Enable Input (TSOP only)</b>	This input selects the organization of the SRAM. 1,024K x 16-bit configuration is selected if $\overline{\text{BYTE}}$ is HIGH. 2,048K x 8-bit configuration is selected if $\overline{\text{BYTE}}$ is LOW
<b>DQ0-DQ15 Data Input/Output Ports</b>	16 bi-directional ports are used to read data from or write data into the RAM.
<b>V<sub>CC</sub></b>	Power Supply
<b>V<sub>SS</sub></b>	Ground

**n TRUTH TABLE**
**Byte Mode (TSOP only)**

MODE	$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	$\overline{BYTE}$	DQ0~DQ7	DQ8~DQ14	DQ15	V <sub>CC</sub> CURRENT
Chip De-selected (Power Down)	H	X	X	X	X	X	L	High Z	High Z	High Z	I <sub>CCSB</sub> , I <sub>CCSB1</sub>
	X	L	X	X	X	X	L	High Z	High Z	High Z	I <sub>CCSB</sub> , I <sub>CCSB1</sub>
Output Disabled	L	H	H	H	X	X	L	High Z	High Z	High Z	I <sub>CC</sub>
Read (byte mode)	L	H	H	L	X	X	L	D <sub>OUT</sub>	High Z	A20	I <sub>CC</sub>
Write (byte mode)	L	H	L	X	X	X	L	D <sub>IN</sub>	X	A20	I <sub>CC</sub>

**Word Mode**

MODE	$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	$\overline{BYTE}$	DQ0~DQ7	DQ8~DQ14	DQ15	V <sub>CC</sub> CURRENT
Chip De-selected (Power Down)	H	X	X	X	X	X	H	High Z	High Z	High Z	I <sub>CCSB</sub> , I <sub>CCSB1</sub>
	X	L	X	X	X	X	H	High Z	High Z	High Z	I <sub>CCSB</sub> , I <sub>CCSB1</sub>
	X	X	X	X	H	H	H	High Z	High Z	High Z	I <sub>CCSB</sub> , I <sub>CCSB1</sub>
Output Disabled	L	H	H	H	X	X	H	High Z	High Z	High Z	I <sub>CC</sub>
Read (word mode)	L	H	H	L	L	L	H	D <sub>OUT</sub>	D <sub>OUT</sub>	D <sub>OUT</sub>	I <sub>CC</sub>
					H	L	H	High Z	D <sub>OUT</sub>	D <sub>OUT</sub>	I <sub>CC</sub>
					L	H	H	D <sub>OUT</sub>	High Z	High Z	I <sub>CC</sub>
Write (word mode)	L	H	L	X	L	L	H	D <sub>IN</sub>	D <sub>IN</sub>	D <sub>IN</sub>	I <sub>CC</sub>
					H	L	H	X	D <sub>IN</sub>	D <sub>IN</sub>	I <sub>CC</sub>
					L	H	H	D <sub>IN</sub>	X	X	I <sub>CC</sub>

NOTES: H means V<sub>IH</sub>; L means V<sub>IL</sub>; X means don't care (Must be V<sub>IH</sub> or V<sub>IL</sub> state)  
48BGA ignore  $\overline{BYTE}$  condition.

**n ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>**

SYMBOL	PARAMETER	RATING	UNITS
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 <sup>(2)</sup> to 4.6V	V
T <sub>BIAS</sub>	Temperature Under Bias	-40 to +125	°C
T <sub>STG</sub>	Storage Temperature	-60 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	W
I <sub>OUT</sub>	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. -2.0V in case of AC pulse width less than 30 ns

**n OPERATING RANGE**

RANG	AMBIENT TEMPERATURE	V <sub>CC</sub>
Industrial	-40°C to + 85°C	1.65V ~ 3.6V

**n CAPACITANCE <sup>(1)</sup> (T<sub>A</sub> = 25°C, f = 1.0MHz)**

SYMBOL	PAMAMETER	CONDITIONS	MAX.	UNITS
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	pF
C <sub>IO</sub>	Input/Output Capacitance	V <sub>IO</sub> = 0V	8	pF

1. This parameter is guaranteed and not 100% tested.

**n DC ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = -40°C to +85°C)**

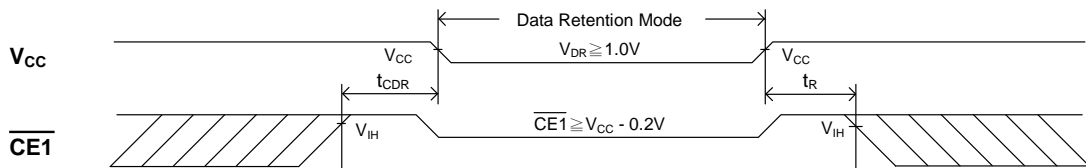
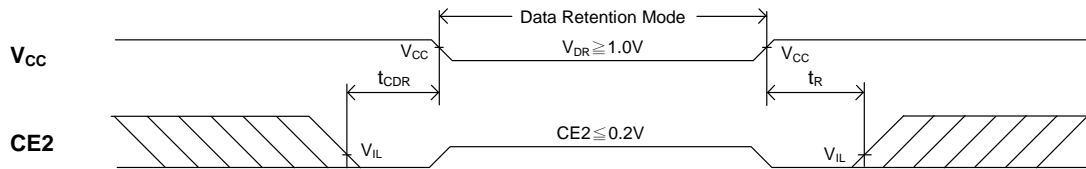
PARAMETER NAME	PARAMETER	TEST CONDITIONS	MIN.	TYP. <sup>(1)</sup>	MAX.	UNITS
V <sub>CC</sub>	Power Supply		1.65	--	3.6	V
V <sub>IL</sub>	Input Low Voltage	V <sub>CC</sub> =1.8V	-0.3 <sup>(2)</sup>	--	0.4	V
		V <sub>CC</sub> =3.6V			0.8	
V <sub>IH</sub>	Input High Voltage	V <sub>CC</sub> =1.8V	1.4	--	V <sub>CC</sub> +0.3 <sup>(3)</sup>	V
		V <sub>CC</sub> =3.6V	2.2			
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> = 0V to V <sub>CC</sub> , CE1 = V <sub>IH</sub> or CE2 = V <sub>IL</sub>	--	--	1	uA
I <sub>LO</sub>	Output Leakage Current	V <sub>IO</sub> = 0V to V <sub>CC</sub> , CE1 = V <sub>IH</sub> or CE2 = V <sub>IL</sub> or OE = V <sub>IH</sub> or UB = LB = V <sub>IH</sub>	--	--	1	uA
V <sub>OL</sub>	Output Low Voltage	V <sub>CC</sub> = Max, I <sub>OL</sub> = 0.2mA	V <sub>CC</sub> =1.8V	--	0.2	V
		V <sub>CC</sub> = Max, I <sub>OL</sub> = 2.0mA	V <sub>CC</sub> =3.6V		0.4	
V <sub>OH</sub>	Output High Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = -0.1mA	V <sub>CC</sub> =1.8V	V <sub>CC</sub> -0.2	--	V
		V <sub>CC</sub> = Min, I <sub>OH</sub> = -1.0mA	V <sub>CC</sub> =3.6V	2.4		
I <sub>CC</sub>	Operating Power Supply Current	CE1 = V <sub>IL</sub> and CE2 = V <sub>IH</sub> , I <sub>DQ</sub> = 0mA, f = F <sub>MAX</sub> <sup>(4)</sup>	V <sub>CC</sub> =1.8V	--	6	mA
			V <sub>CC</sub> =3.6V		8	
I <sub>CC1</sub>	Operating Power Supply Current	CE1 = V <sub>IL</sub> and CE2 = V <sub>IH</sub> , I <sub>DQ</sub> = 0mA, f = 1MHz	V <sub>CC</sub> =1.8V	--	1.0	mA
			V <sub>CC</sub> =3.6V		1.5	
I <sub>CCSB</sub>	Standby Current – TTL	CE1 = V <sub>IH</sub> , or CE2 = V <sub>IL</sub> , I <sub>DQ</sub> = 0mA	V <sub>CC</sub> =1.8V	--	0.5	mA
			V <sub>CC</sub> =3.6V		1.0	
I <sub>CCSB1</sub>	Standby Current – CMOS	CE1 ≥ V <sub>CC</sub> -0.2V or CE2 ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> -0.2V or V <sub>IN</sub> ≤ 0.2V	V <sub>CC</sub> =1.8V	--	4.0	uA
			V <sub>CC</sub> =3.6V		5.0 <sup>(5)</sup>	

1. Typical characteristics are at T<sub>A</sub>=25°C and not 100% tested.
2. Undershoot: -1.0V in case of pulse width less than 20 ns.
3. Overshoot: V<sub>CC</sub>+1.0V in case of pulse width less than 20 ns.
4. F<sub>MAX</sub>=1/tr<sub>C</sub>.
5. V<sub>CC</sub>=3.0V

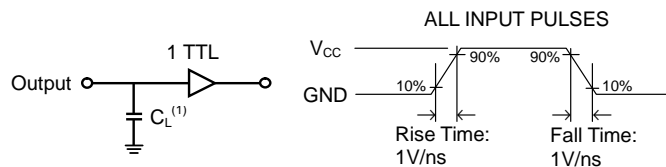
**n DATA RETENTION CHARACTERISTICS (T<sub>A</sub> = -40°C to +85°C)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP. <sup>(1)</sup>	MAX.	UNITS
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention	$\overline{CE1} \geq V_{CC}-0.2V$ or $CE2 \leq 0.2V$ , $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$	1.0	--	--	V
I <sub>CCDR</sub>	Data Retention Current	$\overline{CE1} \geq V_{CC}-0.2V$ or $CE2 \leq 0.2V$ , $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$	--	1.5	15	μA
t <sub>CDR</sub>	Chip Deselect to Data Retention Time	See Retention Waveform	0	--	--	ns
t <sub>R</sub>	Operation Recovery Time		t <sub>RC</sub> <sup>(2)</sup>	--	--	ns

1. Typical characteristics are at T<sub>A</sub>=25°C and not 100% tested.
2. t<sub>RC</sub> = Read Cycle Time.



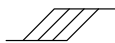


**n LOW V<sub>CC</sub> DATA RETENTION WAVEFORM (1) ( $\overline{CE1}$  Controlled)**

**n LOW V<sub>CC</sub> DATA RETENTION WAVEFORM (2) (CE2 Controlled)**

**n AC TEST CONDITIONS  
(Test Load and Input/Output Reference)**

Input Pulse Levels	V <sub>CC</sub> / 0V
Input Rise and Fall Times	1V/ns
Input and Output Timing Reference Level	0.5V <sub>CC</sub>
Output Load	t <sub>CLZ1</sub> , t <sub>CLZ2</sub> , t <sub>BE</sub> , t <sub>OLZ</sub> , t <sub>CHZ1</sub> , t <sub>CHZ2</sub> , t <sub>BDO</sub> , t <sub>OHZ</sub> , t <sub>WHZ</sub> , t <sub>OW</sub>
	Others



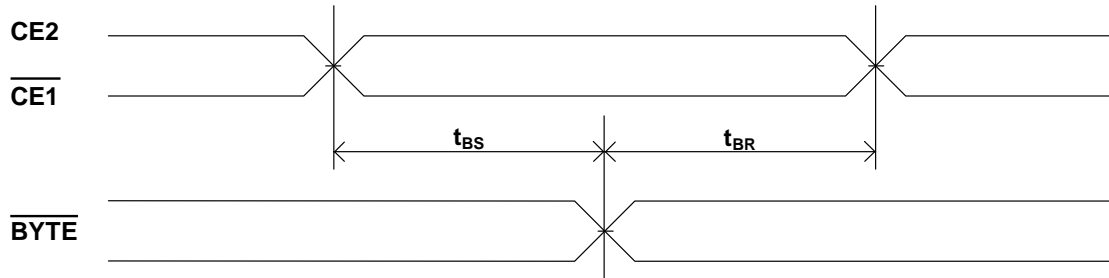
1. Including jig and scope capacitance.

**n KEY TO SWITCHING WAVEFORMS**

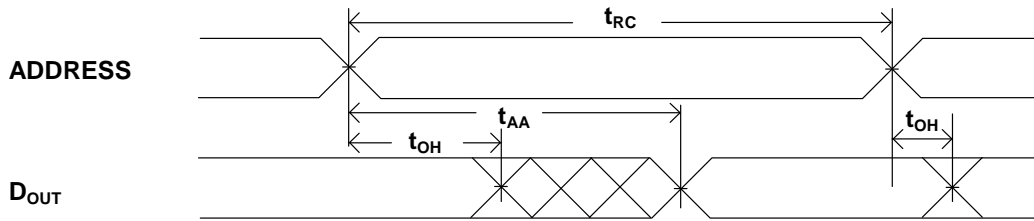
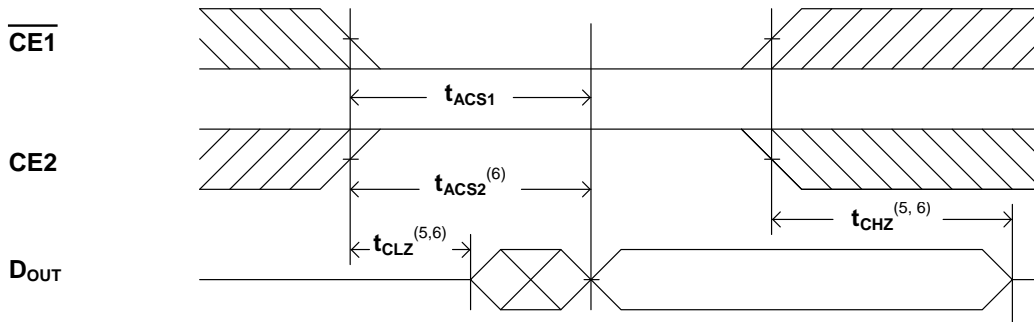
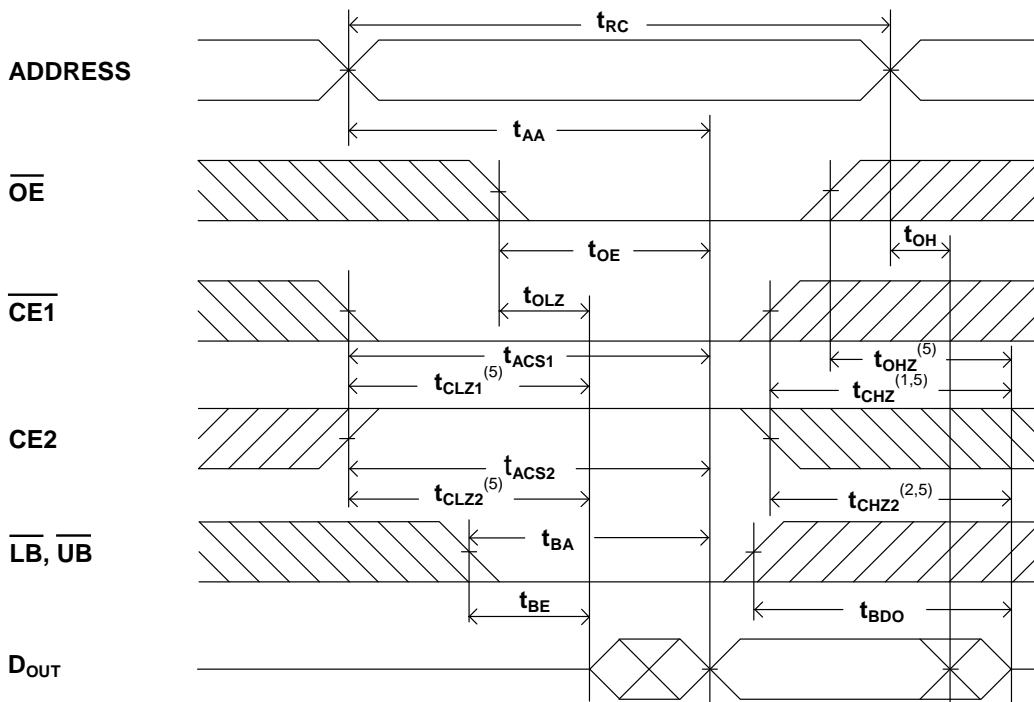
WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM "H" TO "L"	WILL BE CHANGE FROM "H" TO "L"
	MAY CHANGE FROM "L" TO "H"	WILL BE CHANGE FROM "L" TO "H"
	DON'T CARE ANY CHANGE PERMITTED	CHANGE : STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

**n BYTE FUNCTION**

PARAMETER NAME	PARAMETER	MIN.	MAX.	UNITS
$t_{BS}$	BYTE Setup Time	5	--	ms
$t_{BR}$	BYTE Recovery Time	5	--	ms


**n AC ELECTRICAL CHARACTERISTICS ( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )**
**READ CYCLE**

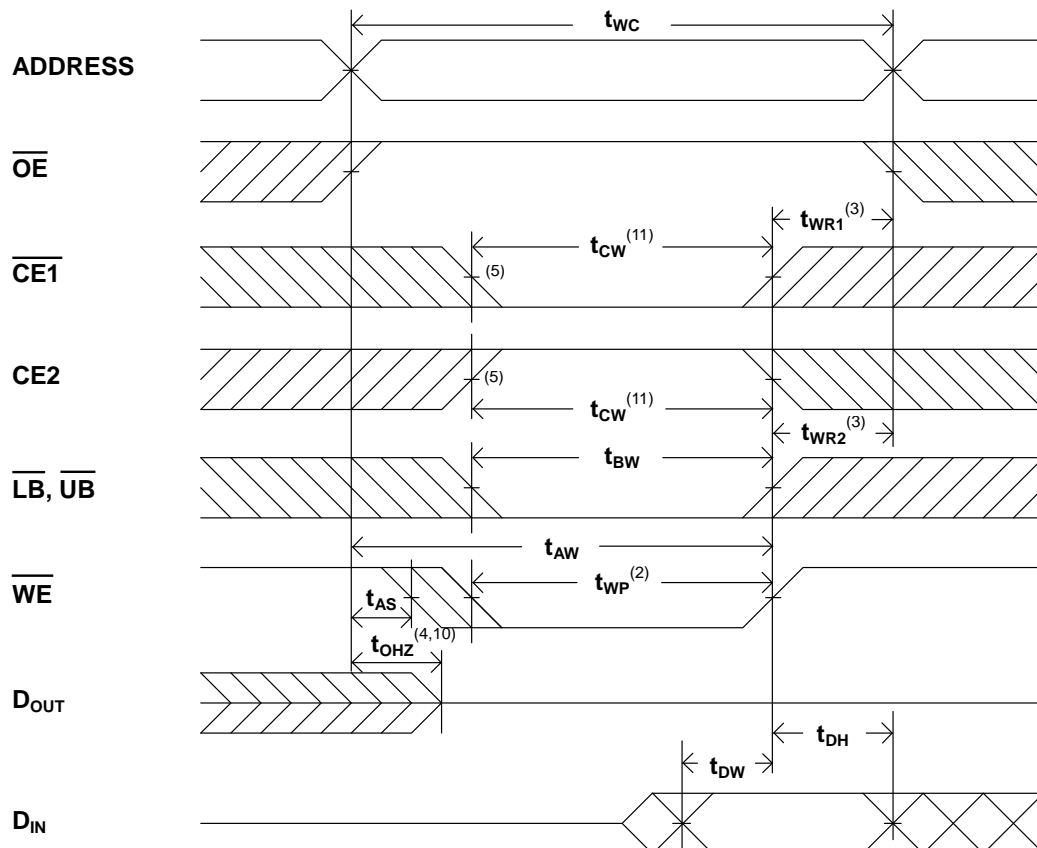
JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	CYCLE TIME : 55ns			CYCLE TIME : 70ns			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
$t_{AVAX}$	$t_{RC}$	Read Cycle Time	55	--	--	70	--	--	ns
$t_{AVQX}$	$t_{AA}$	Address Access Time	--	--	55	--	--	70	ns
$t_{E1LQV}$	$t_{ACS1}$	Chip Select Access Time (CE1)	--	--	55	--	--	70	ns
$t_{E2LQV}$	$t_{ACS2}$	Chip Select Access Time (CE2)	--	--	55	--	--	70	ns
$t_{BLQV}$	$t_{BA}$	Data Byte Control Access Time (LB, UB)	--	--	55	--	--	70	ns
$t_{GLQV}$	$t_{OE}$	Output Enable to Output Valid	--	--	25	--	--	35	ns
$t_{E1LQX}$	$t_{CLZ1}$	Chip Select to Output Low Z (CE1)	10	--	--	10	--	--	ns
$t_{E2LQX}$	$t_{CLZ2}$	Chip Select to Output Low Z (CE2)	10	--	--	10	--	--	ns
$t_{BLQX}$	$t_{BE}$	Data Byte Control to Output Low Z (LB, UB)	10	--	--	10	--	--	ns
$t_{GLQX}$	$t_{OLZ}$	Output Enable to Output Low Z	5	--	--	5	--	--	ns
$t_{E1HQZ}$	$t_{CHZ1}$	Chip Deselect to Output High Z (CE1)	--	--	25	--	--	35	ns
$t_{E2HQZ}$	$t_{CHZ2}$	Chip Deselect to Output High Z (CE2)	--	--	25	--	--	35	ns
$t_{BHQZ}$	$t_{BDO}$	Data Byte Control to Output High Z (LB, UB)	--	--	25	--	--	35	ns
$t_{GHQZ}$	$t_{OHZ}$	Output Disable to Output High Z	--	--	25	--	--	30	ns
$t_{AVQX}$	$t_{OH}$	Data Hold from Address Change	10	--	--	10	--	--	ns

**n SWITCHING WAVEFORMS (READ CYCLE)**
**READ CYCLE 1** <sup>(1,2,4)</sup>

**READ CYCLE 2** <sup>(1,3,4)</sup>

**READ CYCLE 3** <sup>(1,4)</sup>

**NOTES:**

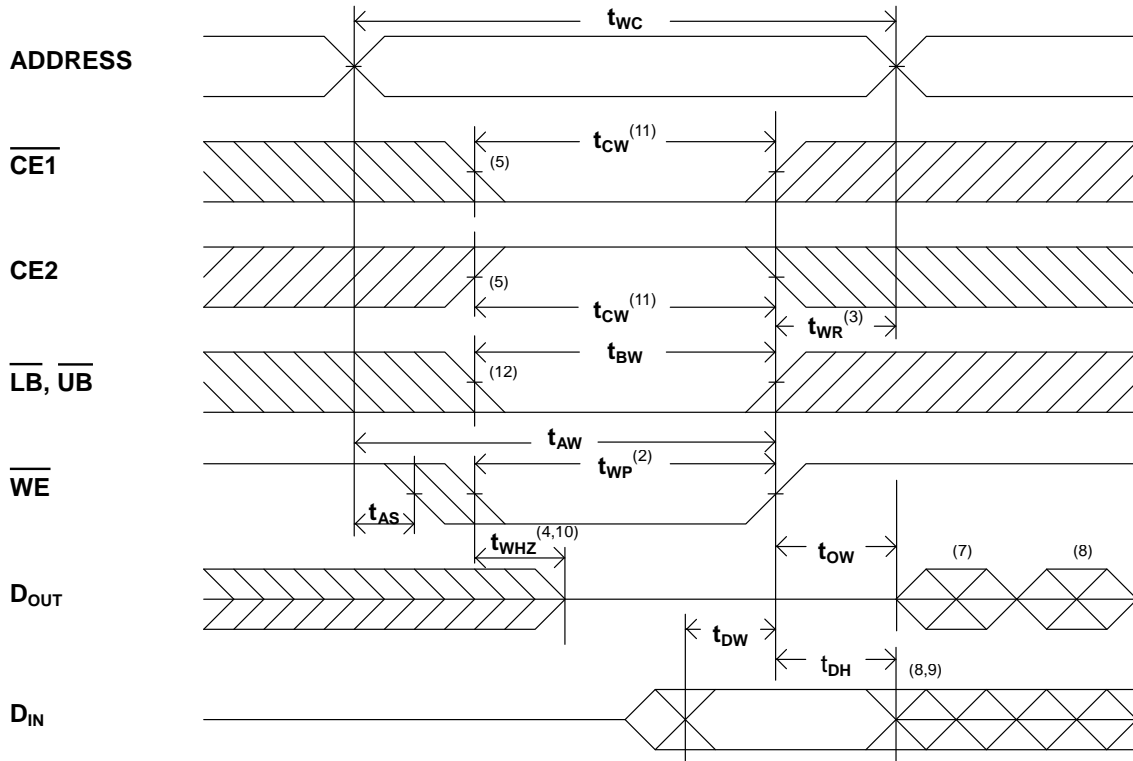
1. WE is high in read Cycle.
2. Device is continuously selected when  $\overline{CE1} = V_{IL}$  and  $CE2 = V_{IH}$ .
3. Address valid prior to or coincident with  $\overline{CE1}$  transition low and/or  $CE2$  transition high.
4.  $\overline{OE} = V_{IL}$ .
5. Transition is measured  $\pm 500\text{mV}$  from steady state with  $C_L = 5\text{pF}$ .  
The parameter is guaranteed but not 100% tested.

**n AC ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = -40°C to +85°C)**
**WRITE CYCLE**

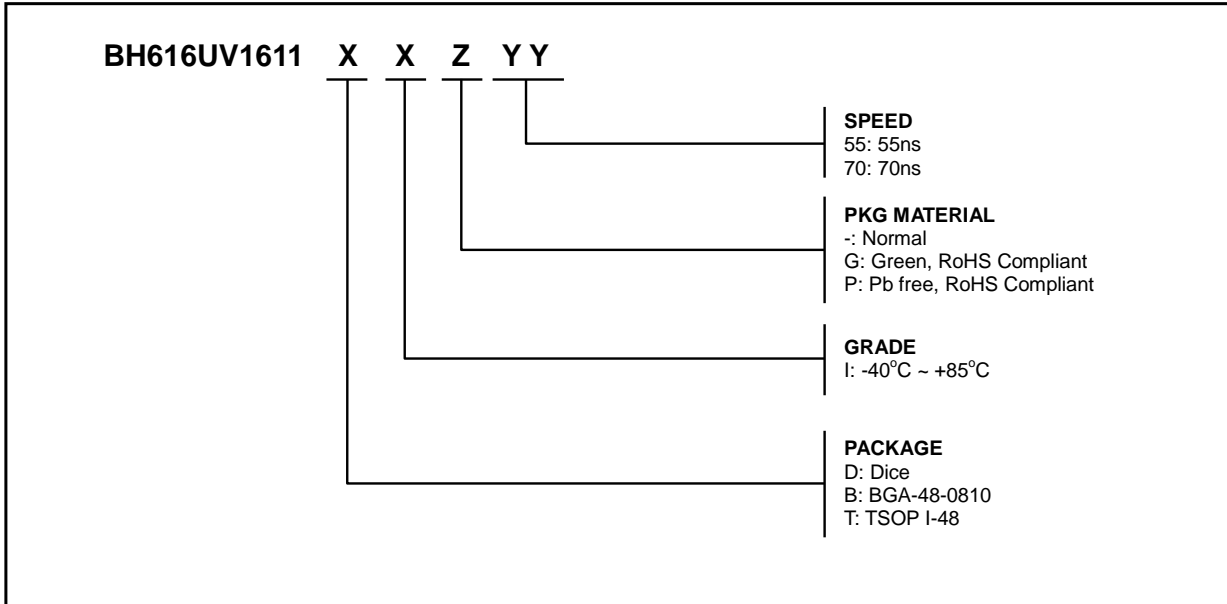
JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	CYCLE TIME : 55ns			CYCLE TIME : 70ns			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
t <sub>AVAX</sub>	t <sub>wc</sub>	Write Cycle Time	55	--	--	70	--	--	ns
t <sub>AVWL</sub>	t <sub>AS</sub>	Address Set up Time	0	--	--	0	--	--	ns
t <sub>AVWH</sub>	t <sub>AW</sub>	Address Valid to End of Write	40	--	--	60	--	--	ns
t <sub>ELWH</sub>	t <sub>cw</sub>	Chip Select to End of Write	40	--	--	60	--	--	ns
t <sub>BLWH</sub>	t <sub>BW</sub>	Data Byte Control to End of Write (LB, UB)	40	--	--	60	--	--	ns
t <sub>WLWH</sub>	t <sub>WP</sub>	Write Pulse Width	30	--	--	35	--	--	ns
t <sub>WHAX</sub>	t <sub>WR1</sub>	Write Recovery Time (CE1, WE)	0	--	--	0	--	--	ns
t <sub>E2LAX</sub>	t <sub>WR2</sub>	Write Recovery Time (CE2)	0	--	--	0	--	--	ns
t <sub>WLQZ</sub>	t <sub>WHZ</sub>	Write to Output High Z	--	--	20	--	--	30	ns
t <sub>DVWH</sub>	t <sub>DW</sub>	Data to Write Time Overlap	25	--	--	30	--	--	ns
t <sub>WHDX</sub>	t <sub>DH</sub>	Data Hold from Write Time	0	--	--	0	--	--	ns
t <sub>GHQZ</sub>	t <sub>OHZ</sub>	Output Disable to Output in High Z	--	--	25	--	--	30	ns
t <sub>WHQX</sub>	t <sub>OW</sub>	End of Write to Output Active	5	--	--	5	--	--	ns

**n SWITCHING WAVEFORMS (WRITE CYCLE)**
**WRITE CYCLE 1 <sup>(1)</sup>**


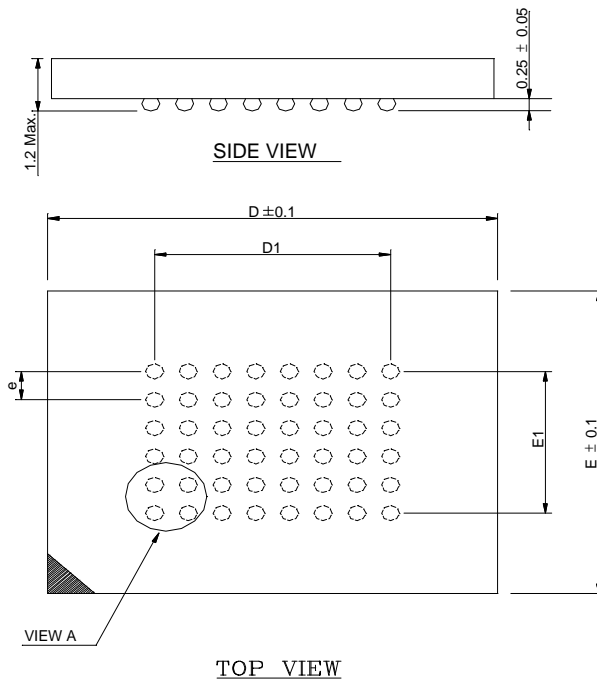


**WRITE CYCLE 2** <sup>(1,6)</sup>

**NOTES:**

1.  $\overline{WE}$  must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of  $\overline{CE1}$  and  $\overline{CE2}$  active and  $\overline{WE}$  low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3.  $t_{WR}$  is measured from the earlier of  $\overline{CE1}$  or  $\overline{WE}$  going high or  $\overline{CE2}$  going low at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the  $\overline{CE1}$  low transition or the  $\overline{CE2}$  high transition occurs simultaneously with the  $\overline{WE}$  low transitions or after the  $\overline{WE}$  transition, output remain in a high impedance state.
6.  $\overline{OE}$  is continuously low ( $\overline{OE} = V_{IL}$ ).
7.  $D_{OUT}$  is the same phase of write data of this write cycle.
8.  $D_{OUT}$  is the read data of next address.
9. If  $\overline{CE1}$  is low and  $\overline{CE2}$  is high during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured  $\pm 500\text{mV}$  from steady state with  $C_L = 5\text{pF}$ .  
The parameter is guaranteed but not 100% tested.
11.  $t_{CW}$  is measured from the later of  $\overline{CE1}$  going low or  $\overline{CE2}$  going high to the end of write.

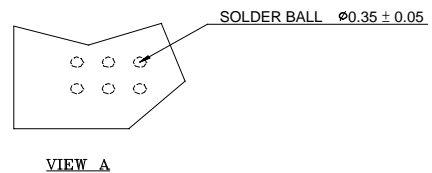
**n ORDERING INFORMATION**

**Note:**

Brilliance Semiconductor Inc. (BSI) assumes no responsibility for the application or use of any product or circuit described herein. BSI does not authorize its products for use as critical components in any application in which the failure of the BSI product may be expected to result in significant injury or death, including life-support systems and critical medical instruments.

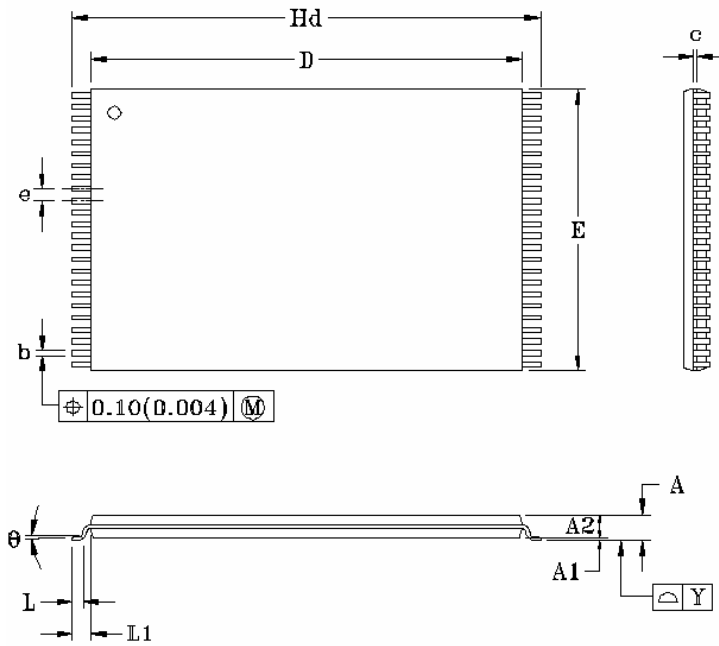
**n PACKAGE DIMENSIONS**

**NOTES:**

- 1: CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
- 2: PIN#1 DOT MARKING BY LASER OR PAD PRINT.
- 3: SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.

N	D	E	D1	E1	e
48	10.0	8.0	5.25	3.75	0.75



*48 mini-BGA (8 x 10mm)*

**n PACKAGE DIMENSIONS**


SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.17	0.20	0.23	0.007	0.008	0.009
c	0.10	0.125	0.18	0.004	0.005	0.008
D	18.30	18.40	18.50	0.720	0.724	0.728
E	11.90	12.00	12.10	0.468	0.472	0.476
Hd	19.80	20.00	20.20	0.780	0.787	0.795
e		0.50			0.020	
L	0.40	0.50	0.60	0.016	0.020	0.024
L1		0.80			0.031	
Y	0.00		0.10	0.000		0.004
θ	1°	3°	5°	1°	3°	5°

*TSOP I-48 Pin (12mm x 20mm)*

**n Revision History**

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
1.0	Initial Production Version	May 10,2006	Initial
1.1	Change I-grade operation temperature range - from -25°C to -40°C	May 25, 2006	
1.2	Add Part Number for 70ns	July 21, 2006	
1.3	Add DICE form and 48 TSOP-I package type Change BGA package dimension for single chip solution - form 6x8 mm to 8x10mm Improve Spec. - $I_{CC(MAX.)}$ from 12mA to 10mA for $V_{CC}=3.6V$ - $I_{CCsb1(TYP.)}$ from 5.0uA to 4.0uA for $V_{CC}=1.8V$ - $I_{CCDR(TYP.)}$ from 2.5uA to 1.5uA for $V_{CC}=1.2V$ - $t_{OE(MIN.)}$ from 30ns to 25ns - $t_{AW(MIN.)}$ from 45ns to 40ns - $t_{CW(MIN.)}$ from 45ns to 40ns - $t_{BW(MIN.)}$ from 45ns to 40ns	Otc 22, 2006	