MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

TDA3301B
TDA3303

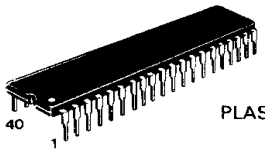
TV COLOR PROCESSOR

These devices will accept a PAL or NTSC composite video signal and output the three color signals, needing only a simple driver amplifier to interface to the picture tube. The provision of high bandwidth on-screen display inputs makes them suitable for text display, TV games, cameras, etc. The TDA3301B differs from the TDA3303 in its user control laws, and also a phase shift control which operates in PAL, as well as NTSC.

- Automatic Black Level Setup
- Beam Current Limiting
- Uses Inexpensive 4.43/3.58 MHz Crystal
- No Oscillator Adjustment Required
- Three OSD Inputs Plus Fast Blanking Input
- Four DC, High Impedance User Controls
- Interfaces with TDA3030B SECAM Adaptor
- Single 12 V Supply
- Low Dissipation, Typically 600 mW

TV COLOR PROCESSOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 711

FN SUFFIX
PLASTIC PACKAGE
CASE 777
(PLCC-44)

FIGURE 1 — PIN ASSIGNMENT

Chroma Input	1 (1)	(44) 40	Hue Control/NTSC Switch
ACC Capacitor	2 (2)	(43) 39	+ 12 V
Chroma DL Driver, Emitter	3 (3)	(42) 38	Ground
Chroma DL Driver, Collector	4 (4)	(41) 37	1.0 V Composite Video Input
Saturation Control	5 (5)	(40) 36	Delayed Luma Input
Identification Capacitor	6 (6)	(39) 35	Luma DL Drive and 3.0 Inverted Output
V Input	7 (10)	(38) 34	Luma Emitter Load
U Input	8 (11)	(37) 33	Luma Collector Load
90° Loop Capacitor	9 (12)	(36) 32	Contrast Control
Oscillator Loop Filter	10 (13)	(35) 31	Black Level Clamp
Crystal Drive	11 (14)	(34) 30	Brightness Control
Crystal Feedback	12 (15)	(33) 29	Peak Beam Limit Adjust
Ground	13 (16)	(32) 28	Frame Pulse Input
Blue Output	14 (18)	(31) 27	Sandcastle Pulse Input
Blue Output Clamp Capacitor	15 (19)	(30) 26	OSD Input Green
Blue Output Feedback	16 (20)	(29) 25	OSD Input Red
Green Output	17 (21)	(28) 24	OSD Input Blue
Green Output Clamp Capacitor	18 (22)	(27) 23	OSD Input Fast Blanking
Green Output Feedback	19 (23)	(26) 22	Red Output Feedback
Red Output	20 (24)	(25) 21	Red Output Clamp Capacitor

*( ) PLCC Pin Assignment

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MAXIMUM RATINGS (T_A = +25°C unless otherwise stated)

Rating	Pin	Value	Unit
Supply Voltage	39	14	Vdc
Operating Temperature Range		0 to +70	°C
Storage Temperature Range		−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 12 V)

Characteristic	Pin	Min	Typ	Max	Unit
Supply Voltage	39	10.8	12	13.2	V
Supply Current		—	45	60	mA
Composite Video Input	37	—	1.0	—	Vp-p
Video Input Resistance		13	18	23	kΩ
Video Gain to Pin 35		2.7	3.2	3.6	Vp-p
Input Window		0.8–3	0.7–3.2	—	V
Chroma Input (Burst)	1	10	100	200	mVp-p
Input Resistance	1	—	5.0	—	kΩ
ACC Effectiveness	4	—	1.2	3.0	dB
OSD Input	24,25,26	0.5	0.7	1.0	V
OSD Drive Impedance		—	—	180	Ω
OSD Frequency Response (−3.0 dB)		9.0	—	—	MHz
OSD Max Gain		—	7.2	—	MHz
Gain Difference Between Any Two		—	—	15	%
Beam Current Ref. Threshold	16,19,22	1.7	2.0	2.3	V
Differential Voltage		—	—	20	mV
Beam Current Ref. Input Current		—	—	+1.5/−0.5	μA
Differential Current		—	—	1.0	μA
Luminance Gain Between Pin 36 and Outputs (depends on R_{33} and R_{34})		—	4.7	—	
Luminance Bandwidth (−3.0 dB)	14,17,20	9.0	—	—	MHz
Output Resistance		120	170	300	Ω
Residual Carrier (4.43 Mc/s)		—	30	150	mVp-p
PAL Offset (H/2)		—	—	50	mVp-p
Difference in Gain Between Y Input and any RGB o/p		—	5.0	—	%
U Input Sensitivity for 5.0 V Blue Output	8	—	340	—	mVp-p
Matrix Error	14,17,20	—	—	10	%
Oscillator Capture Range		350	—	—	Hz
U Ref. Phase Error		—	—	5.0	Degrees
V Ref. Phase Error		—	—	5.0	Degrees
Color Kill Attenuation	14,17,20	50	—	—	dB
Contrast Tracking OSD/Luma/Chroma	14,17,20	—	—	—	dB
OSD Contrast Tracking	14,17,20	—	—	±2.0	dB
OSD Enable Slice Level	23	—	0.7	—	V
Sandcastle Slice Level	27				
Burst Gate		6.5	7.2	8.0	V
Line Blanking		2.0	2.6	3.0	V
R Input V_{27} > 7.0 V		—	5.0	—	kΩ
V_{27} < 7.0 V		—	22	—	kΩ
Frame Slice Level	28	2	2.8	3.6	V
R Input			15	—	kΩ
Peak Beam Limiter Threshold (I_{29} Min = 250 μA)		3.4 x I_{29}	4 x I_{29}	4.6 x I_{29}	
Pin 29 Input Resistance	29	—	5.0	—	kΩ
Pin 29 Open Circuit Voltage	29	—	10.6	—	V

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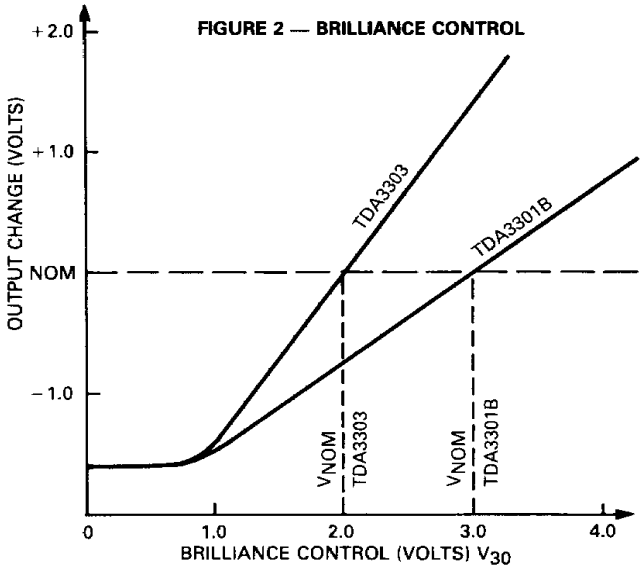
INPUT/OUTPUT FUNCTIONS

FIGURE 2 — BRILLIANCE CONTROL

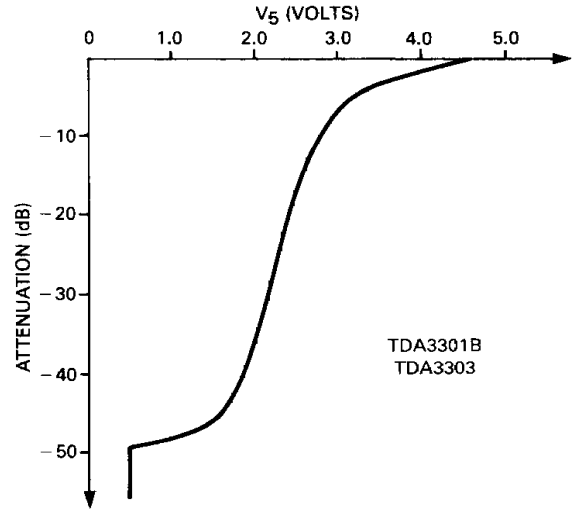


The brilliance control operates by adding a pedestal to the output signals. The amplitude of the pedestal is controlled by Pin 30.

During CRT beam current sampling a standard pedestal is substituted, its value being equivalent to the value given by V_{30} Nom. Brightness at black level with V_{30} Nom is given by the sum of three gun currents at the sampling level, i.e. 3 x 20 μA with 100 k reference resistors on Pins 16, 19, and 22.

During picture blanking the brilliance pedestal is zero; therefore the output voltage during blanking is always the minimum brilliance black level (Note: Signal channels are also gain blanked).

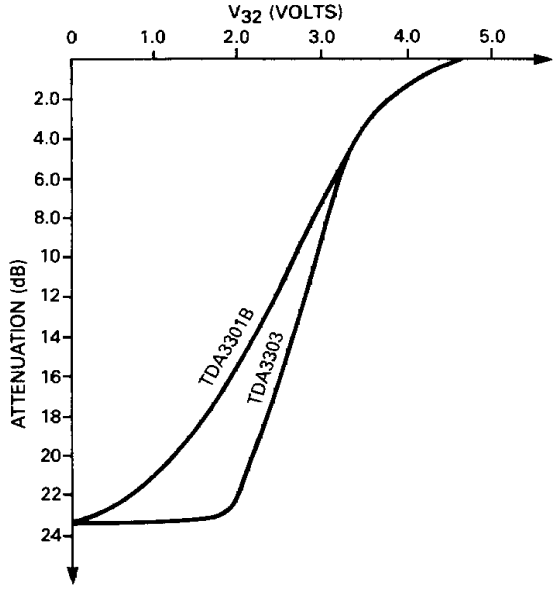
FIGURE 3 — SATURATION CONTROL VOLTAGE



Pin 5 is automatically pulled to ground with a misidentified PAL signal.

Note: Nominal 100% saturation point is given by choice of R_2 which sets ACC operating point.

FIGURE 4 — CONTRAST CONTROL



Note: Pin 32 is pulled down by the operation of the peak beam limiter.

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FIGURE 5 — BLOCK DIAGRAM

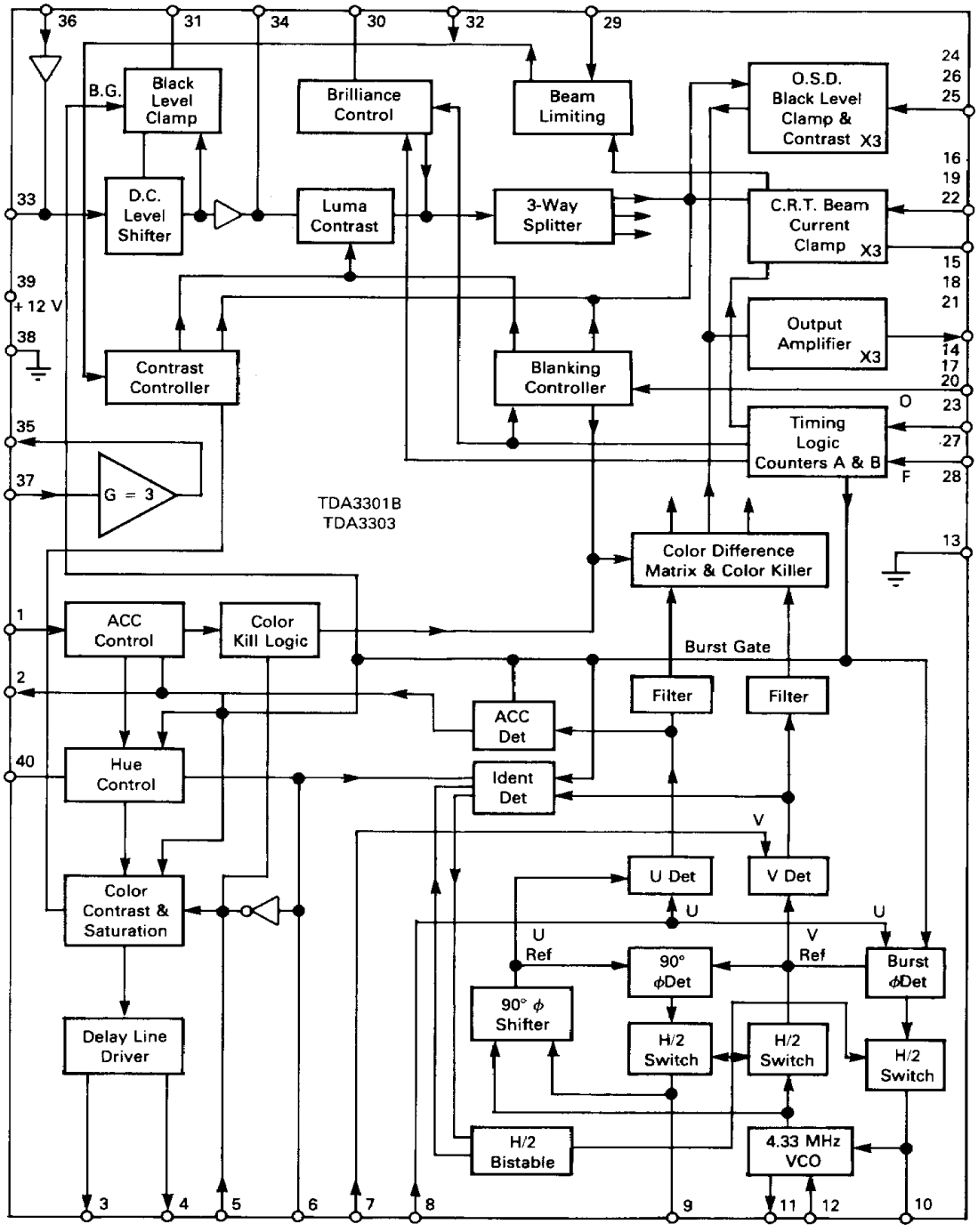
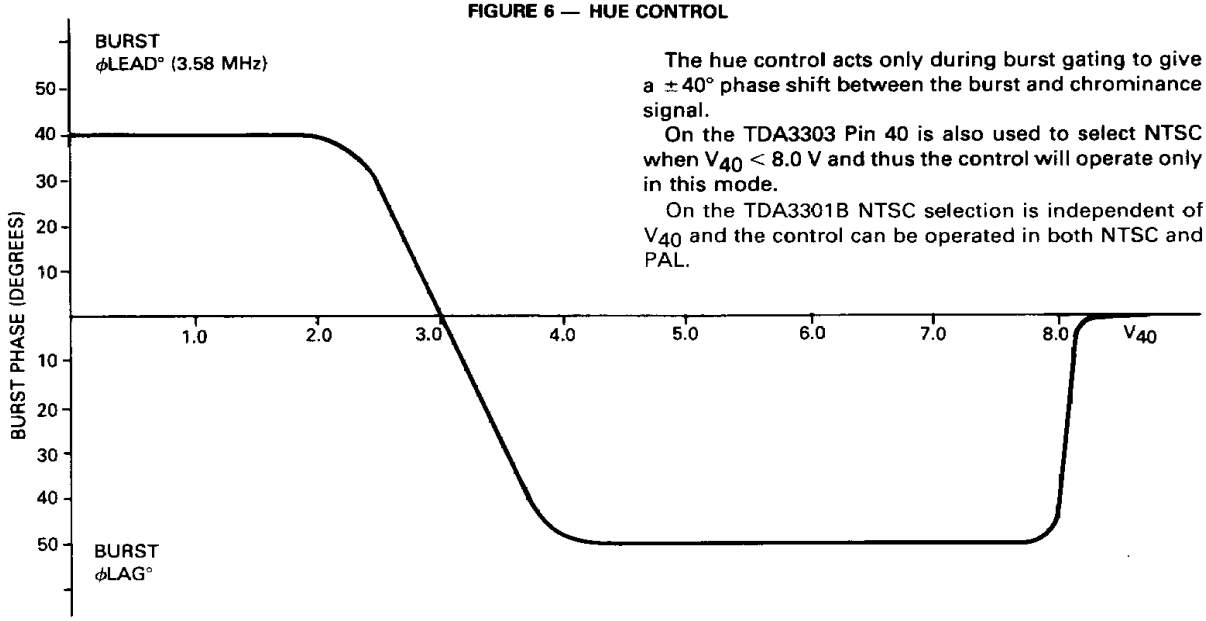


FIGURE 6 — HUE CONTROL



The hue control acts only during burst gating to give a ±40° phase shift between the burst and chrominance signal.

On the TDA3303 Pin 40 is also used to select NTSC when $V_{40} < 8.0$ V and thus the control will operate only in this mode.

On the TDA3301B NTSC selection is independent of V_{40} and the control can be operated in both NTSC and PAL.

CIRCUIT OPERATION

CHROMINANCE DECODER SECTION

The chrominance decoder section of the TDA3301B consists of the following blocks:

Phase-locked reference oscillator — Figures 7, 8 and 9
Phase-locked 90 degree servo loop — Figures 9 and 10
U and V axis decoders
ACC detector and identification detector — Figure 11
Identification circuits and PAL bistable — Figure 12
Color difference filters and matrixes with fast blanking circuits.

The major design considerations apart from optimum performance were:

— a minimum number of factory adjustments
— a minimum number of external components
— compatibility with the SECAM adapter TDA3030B
— low dissipation
— use of a standard 4.433618 MHz Crystal rather than a 2.0 fc Crystal with divider.

REFERENCE REGENERATION

The crystal VCO is of the phase shift variety in which the frequency is controlled by varying the phase of the feedback. A great deal of care was taken to ensure that the oscillator loop gain and the crystal loading impedance were held constant in order to ensure that the circuit functions well with low grade crystal (crystals having high magnitude spurious responses can cause bad phase jitter). It is also necessary to ensure that the gain at third harmonic is low enough to ensure absence of oscillation at this frequency.

FIGURE 7 — VOLTAGE CONTROLLED OSCILLATOR (VCO)

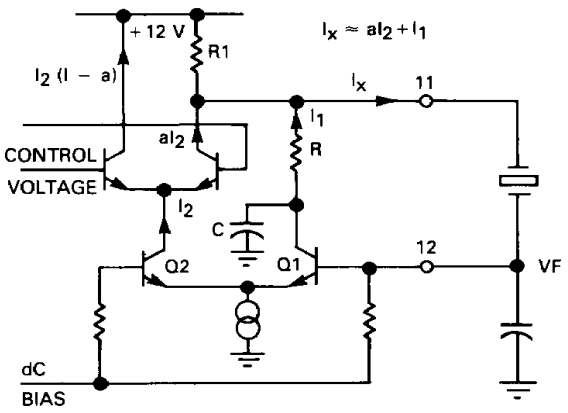
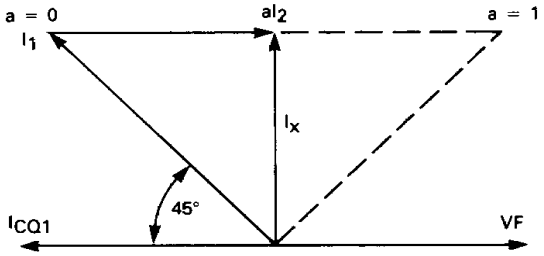


FIGURE 8 — VECTOR DIAGRAM FOR VCO



By referring to Figures 7 and 8 it can be seen that the necessary ±45° phase shift is obtained by variable addition of two currents I_1 and I_2 which are then fed into the load resistance of the crystal tuned circuit R_1. Feedback is taken from the crystal load capacitance which gives a voltage VF lagging the crystal current by 90°.

The RC network in T_1 collector causes I_1 to lag the collector current of T_1 by 45°.

For SECAM operation the currents I_1 and I_2 are added together in a fixed ratio giving a frequency close to nominal.

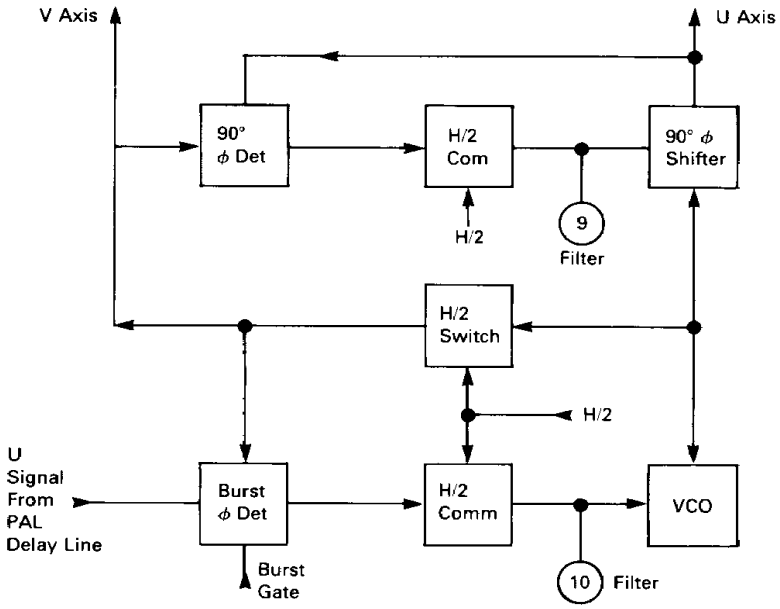
When decoding PAL there are two departures from normal chroma reference regeneration practice:

a) The loop is locked to the burst entering from the PAL delay line matrix U channel and hence there is no alternating component. A small improvement in signal noise ratio is gained but more important is that the loop filter is not compromised by the 7.8 kHz component normally required at this point for PAL identification.

b) The H/2 switching of the oscillator phase is carried out before the phase detector. This implies any error signal from the phase detector is a signal at 7.8 kHz and not dc. A commutator at the phase detector output also driven from the PAL bistable converts this ac signal to a dc prior to the loop filter. The purpose of this is that constant offsets in the phase detector are converted by the commutator to a signal at 7.8 kHz which is integrated to zero and does not give a phase error.

When used for decoding NTSC the bistable is inhibited, and slightly less accurate phasing is achieved; however, as a hue control is used on NTSC this cannot be considered to be a serious disadvantage.

FIGURE 9 — BLOCK DIAGRAM OF REFERENCE SECTION



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90° REFERENCE GENERATION

To generate the U axis reference a variable all-pass network is utilized in a servo loop. The output of the all-pass network is compared with the oscillator output with a phase detector of which the output is filtered and corrects the operating point of the variable all-pass network (see Figure 10).

As with the reference loop the oscillator signal is taken after the H/2 phase switch and a commutator inserted before the filter so that constant phase detector errors are cancelled.

For SECAM operation the loop filter is grounded causing near zero phase shift so that the two synchronous detectors work in phase and not in quadrature.

The use of a 4.4 MHz oscillator and a servo loop to generate the required 90° reference signal allows the use of a standard, high volume, low cost crystal and gives an extremely accurate 90° which may be easily switched to 0° for decoding AM SECAM generated by the TDA3030B adapter.

FIGURE 10 — VARIABLE ALL-PASS NETWORK

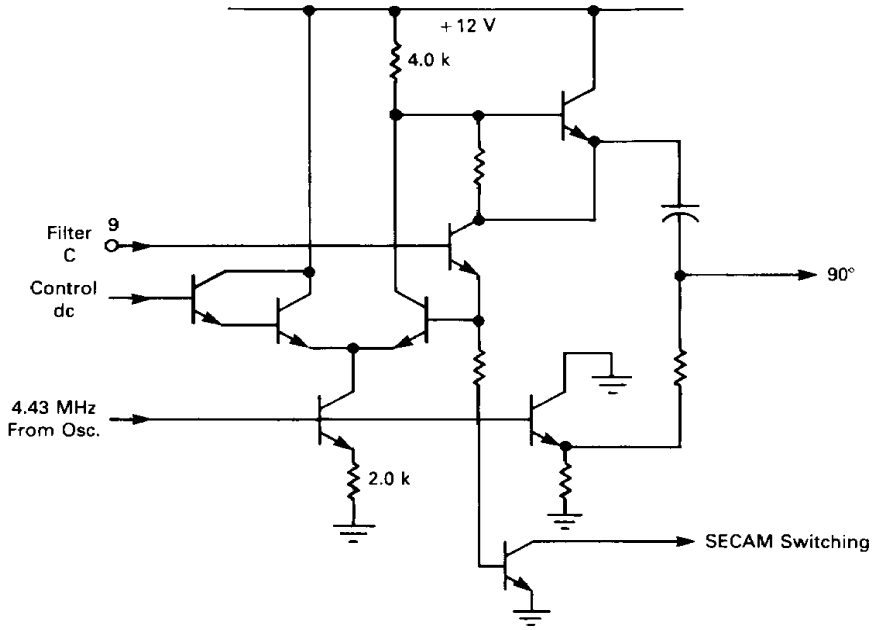
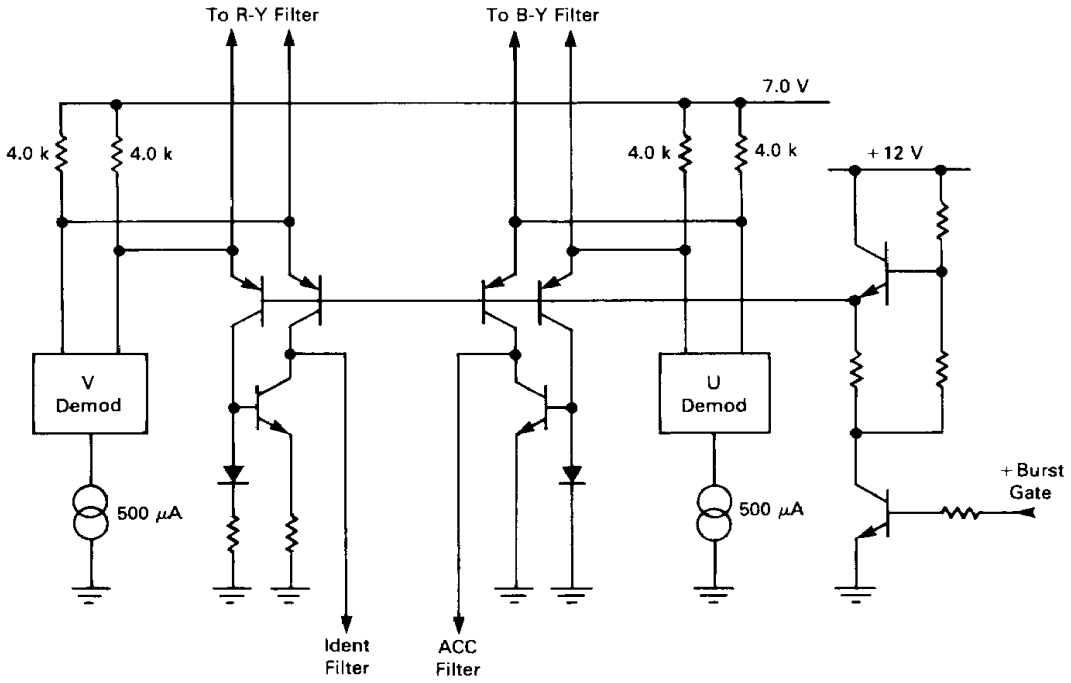


FIGURE 11 — ACC AND IDENTIFICATION DETECTORS



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ACC AND IDENTIFICATION DETECTORS

During burst gate time the output components of the U and also the V demodulators are steered into PNP emitters. One collector current of each PNP pair is mirrored and balanced against its twin giving push-pull current sources for driving the ACC and the identification filter capacitors.

The identification detector is given an internal offset by making the NPN current mirror emitter resistors unequal. The resistors are offset by 5% such that the identification detector pulls up on its filter capacitor with zero signal.

IDENTIFICATION

See Figure 12 for definitions.

Monochrome	$I_1 > I_2$
PAL ident. OK	$I_1 < I_2$
PAL ident. X	$I_1 > I_2$
NTSC	$I_3 > I_2$

Only for correctly identified PAL signal is the capacitor voltage held low since I_2 is then greater than I_1.

For monochrome and incorrectly identified PAL signals $I_1 > I_2$ hence voltage V_C rises with each burst gate pulse.

When $V_{ref}1$ is exceeded by 0.7 V latch 1 is made conducting which increases rate of voltage rise on C. Maximum current is limited by R_1.

When V_{ref} 2 is exceeded by 0.7 V then latch 2 is made conducting until C is completely discharged and the current drops to a value insufficient to hold on latch 2.

As latch 2 turns on latch 1 must turn off.

Latch 2 turning on gives extra trigger pulse to bistable to correct identification.

The inhibit line on latch 2 restricts latch 2 conduction to alternate lines as controlled by the bistable. This function allows the SECAM switching line to inhibit the bistable operation by firing latch 2 in the correct phase for SECAM. For NTSC latch 2 is fired by current injected on Pin 6.

If the voltage on C is greater than 1.4 V then the saturation is held down. Only for SECAM/NTSC with latch 2 on or correctly identified PAL can the saturation control be anywhere but minimum.

NTSC SWITCH

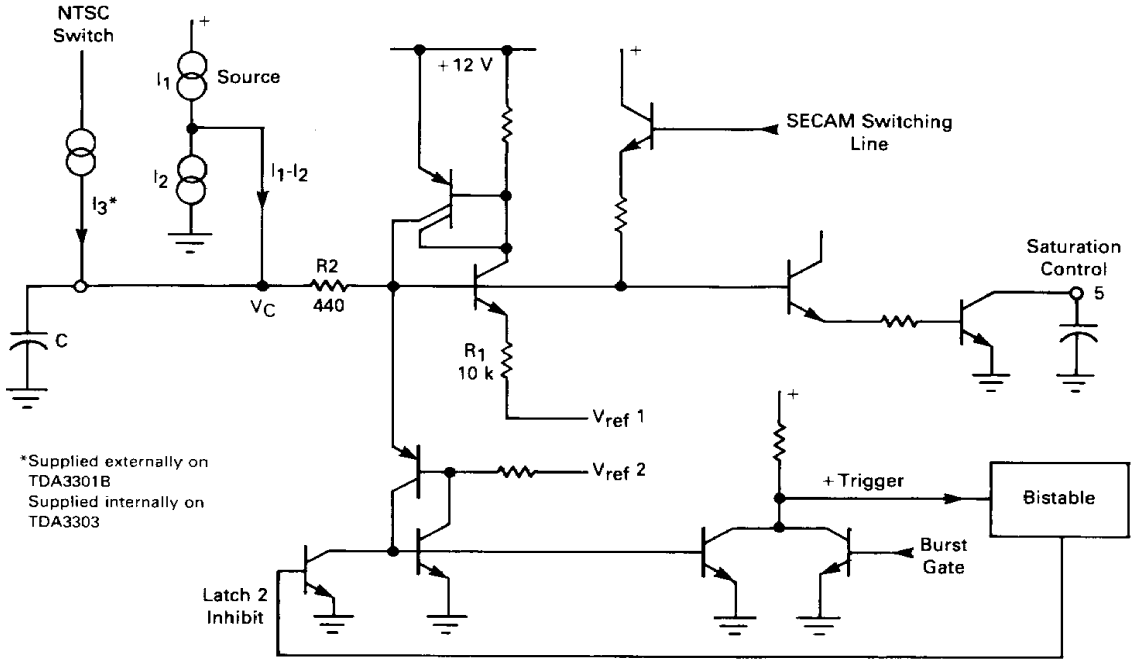
NTSC operation is selected when current (I_3) is injected into Pin 6.

On the TDA3301B this current must be derived externally by connecting Pin 6 to +12 V via a 27 k resistor (as on TDA3300B).

On the TDA3303 I_3 is supplied internally when V_{40} falls below 8.0 V;

For normal PAL operation on both versions Pin 40 should be connected to +12 V and Pin 6 to the filter capacitor.

FIGURE 12 — IDENTIFICATION CIRCUIT



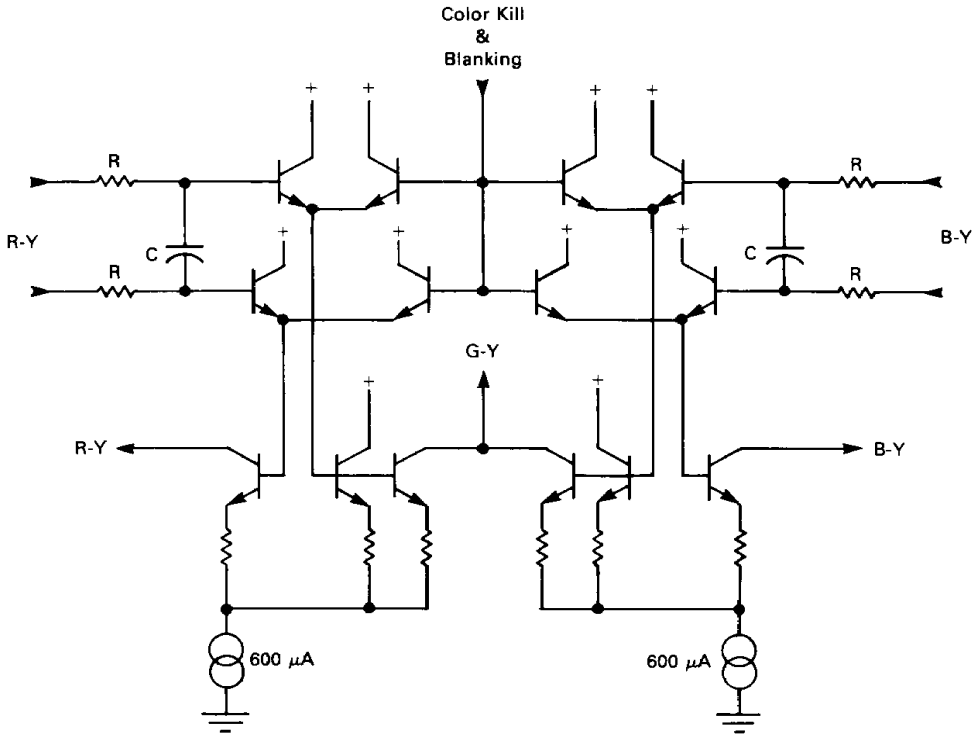
COLOR DIFFERENCE MATRIXING, COLOR KILLING, AND CHROMA BLANKING

During picture time the two demodulators feed simple RC filters with emitter follower outputs. Color killing and blanking is performed by lifting these outputs to a voltage above the maximum value that the color difference signal could supply.

The color difference matrixing is performed by 2 differential amplifiers each with one side split to give the correct values of the −(B-Y) and −(R-Y) signals. These are added to give the (G-Y) signal.

The 3 color difference signals are then taken to the virtual earths of the video output stages together with luminance signal.

FIGURE 13 — COLOR DIFFERENCE STAGES



SANDCASTLE SELECTION

The TDA3301B/3303 may be used with a two level sandcastle and a separate frame pulse to Pin 28, or with only a 3 level (super) sandcastle. In the latter case a resistor of 1 MΩ is necessary from +12 volts to Pin 28 and a 470 pF capacitor from Pin 28 to ground.

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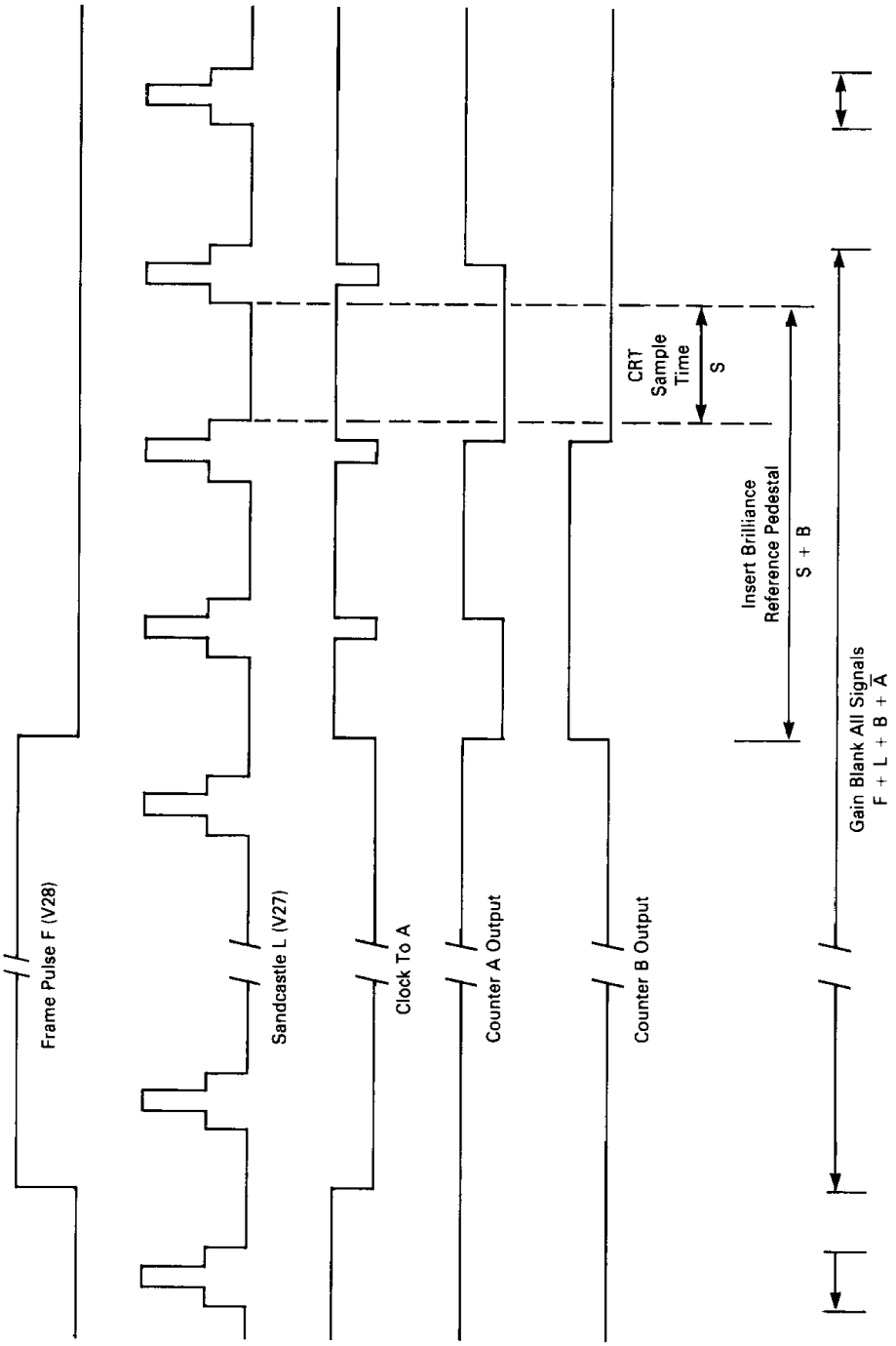

FIGURE 14 — TIMING DIAGRAM

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TIMING COUNTER FOR SAMPLE CONTROL

In order to control the beam current sampling at the beginning of each frame scan two edge triggered flip-flops are used.

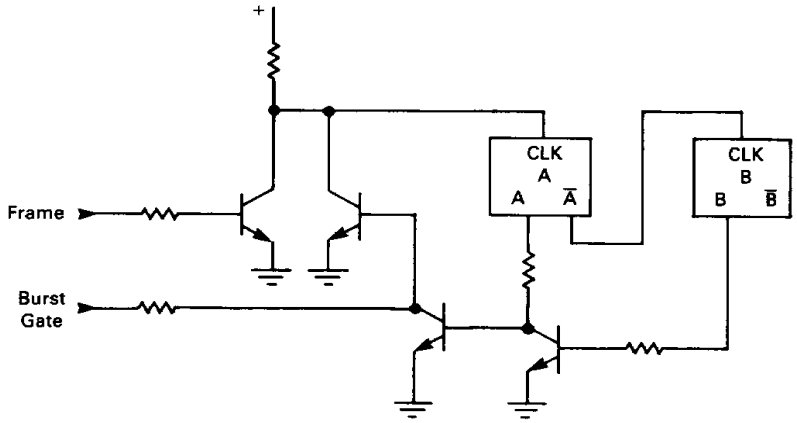
The output $\overline{A}$ of the first flip-flop A is used to clock the second flip-flop B. Clocking of A by the burst gate is inhibited by a count of $A.\overline{B}$.

The count sequence can only by initiated by the trailing edge of the frame pulse. In order to provide control signals for:

Luma/Chroma blanking,
Beam current sampling,
On-screen display blanking,
Brilliance control.

The appropriate flip-flop outputs are matrixed with sandcastle and frame signals by an emitter follower matrix.

FIGURE 15 — TIMING COUNTER



ON-SCREEN DISPLAY INPUTS

Each section of the OSD stages consists of a common emitter input stage feeding a diversion gate controlled by the contrast control. During burst gate time a feedback loop is activated which clamps the signal at the input coupling capacitor. This ensures that the current in the diversion gate is zero at black level and makes the OSD black level insensitive to contrast control, also the inputs ignore signals below black, e.g. sync, pulses.

FIGURE 16 — OSD STAGE

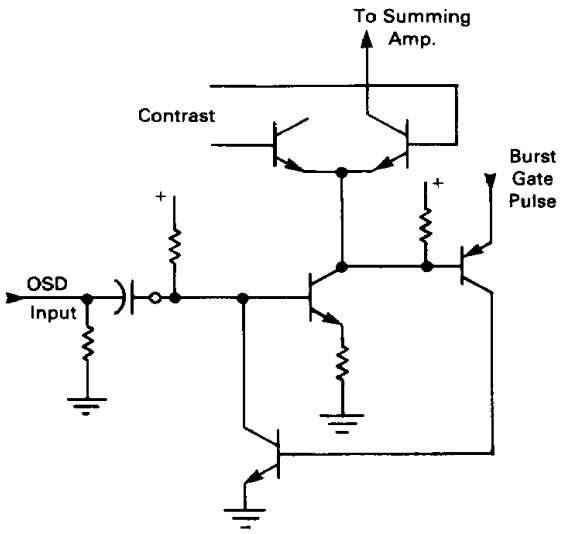


FIGURE 17 — VIDEO OUTPUT SECTION

Each video output stage consists of a feedback amplifier in which the input signal is a current drive to the virtual earth from the luminance, color difference and on-screen display stages.

A further drive current is used to control the dc operating point; this is derived from the sample and hold stage which samples the beam current after frame flyback.

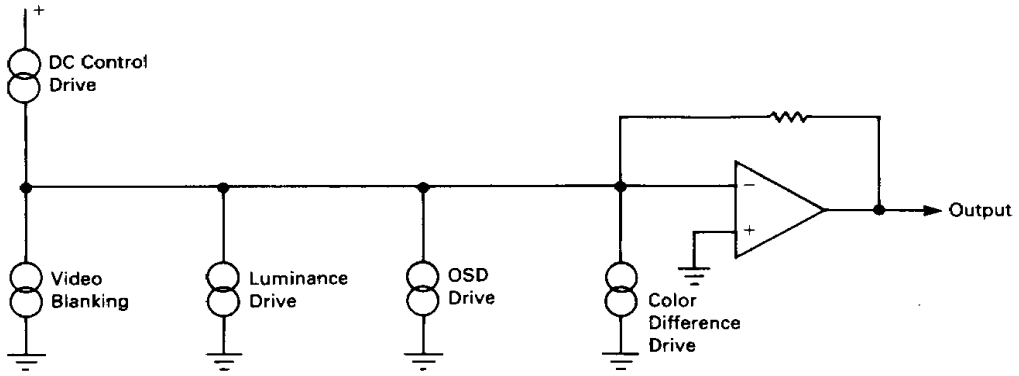


FIGURE 18 — COMPLETE VIDEO OUTPUT SECTIONS

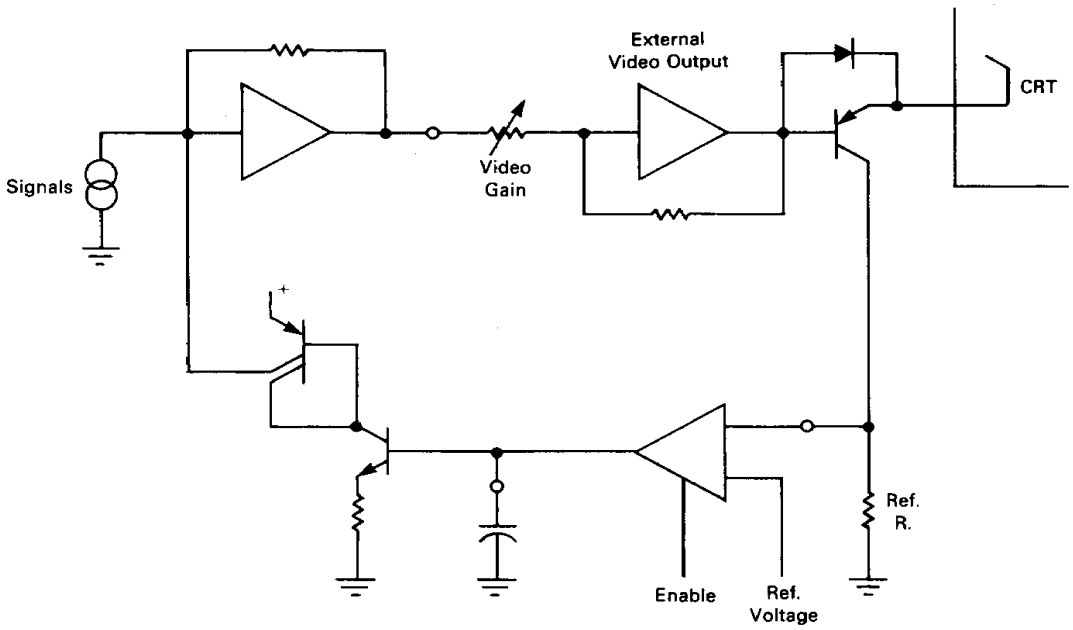


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FIGURE 19 — TYPICAL VIDEO OUTPUT STAGE

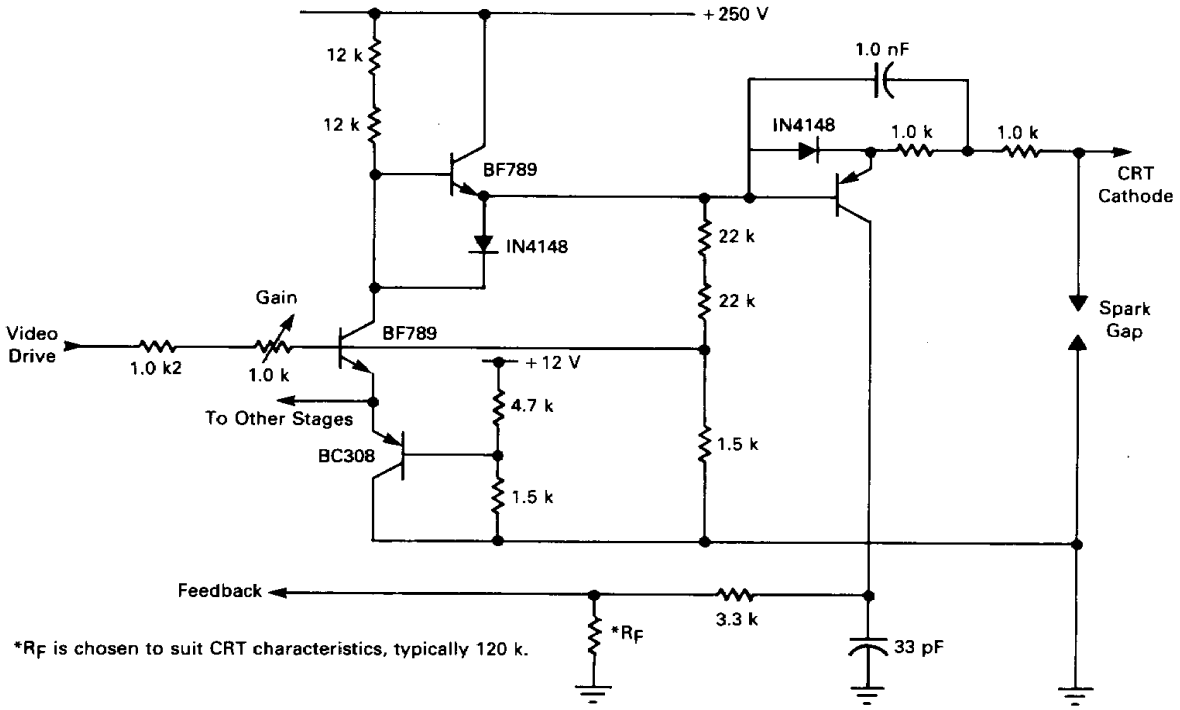
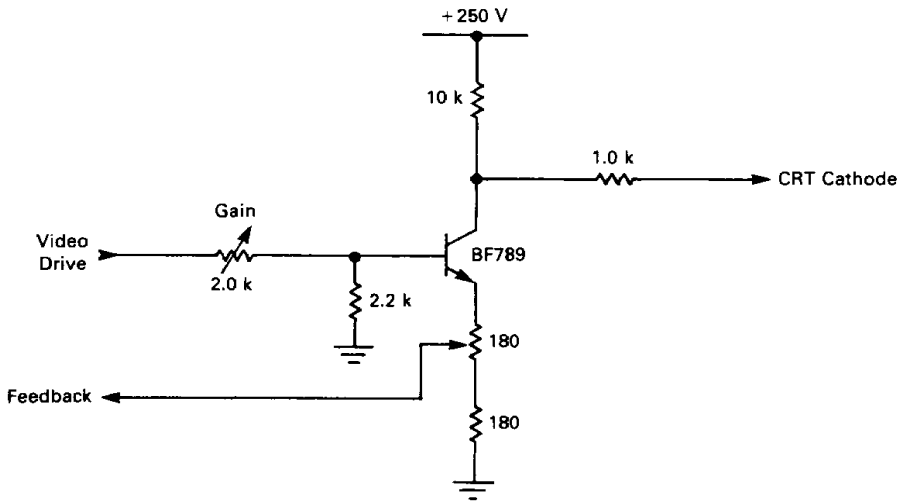


FIGURE 20 — CLASS A VIDEO OUTPUT STAGE WITH DIRECT FEEDBACK



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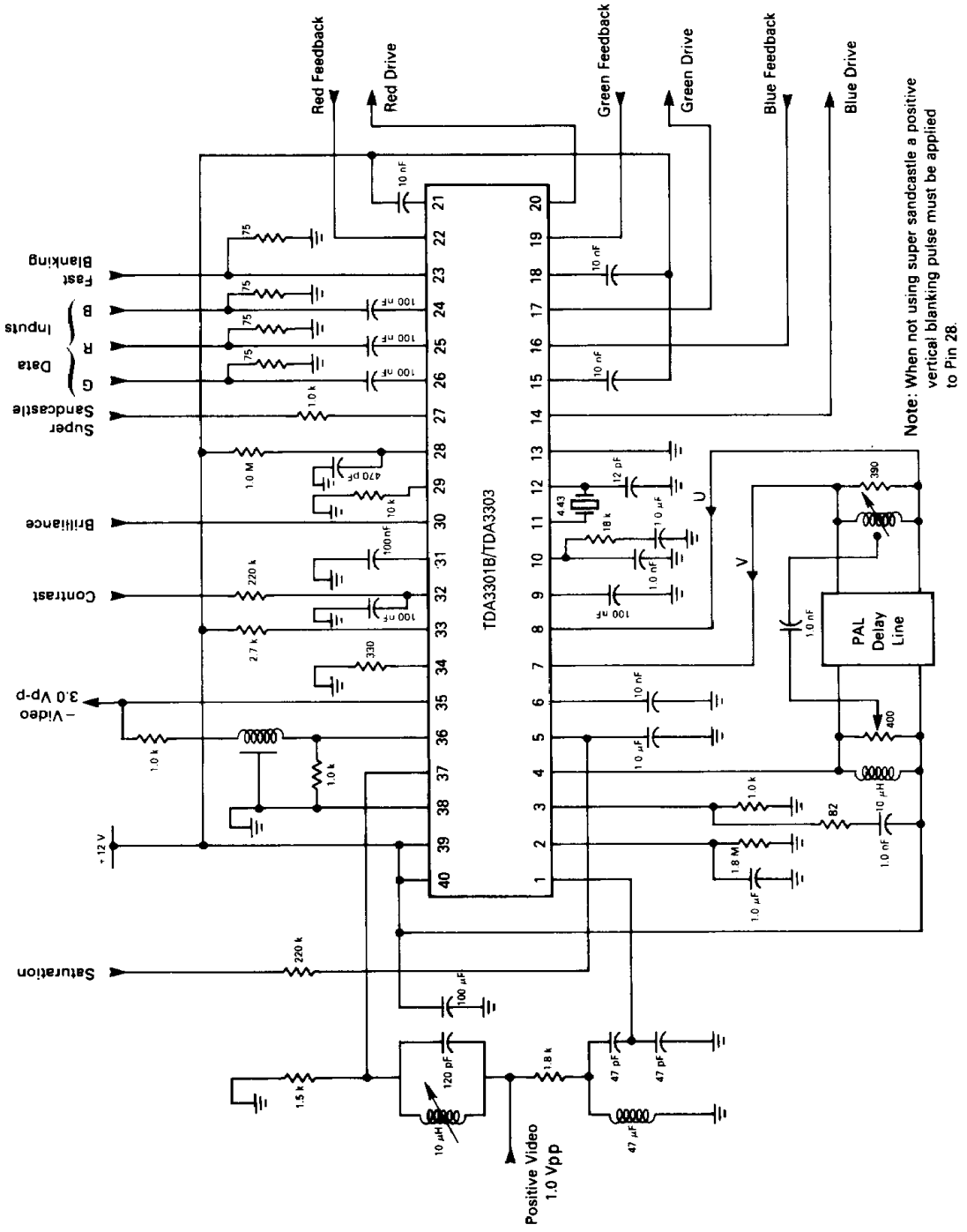

FIGURE 21 — TYPICAL PAL APPLICATION

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