MC1458S
MC1558S

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ORDERING INFORMATION

Device	Temperature Range	Package
MC1458SD	0°C to +70°C	SO-8
MC1458SG	0°C to +70°C	Metal Can
MC1458SP1	0°C to +70°C	Plastic DIP
MC1458SU	0°C to +70°C	Ceramic DIP
MC1558SG	−55°C to +125°C	Metal Can
MC1558SU	−55°C to +125°C	Ceramic DIP

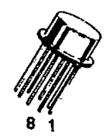
DUAL HIGH SLEW RATE INTERNALLY-COMPENSATED OPERATIONAL AMPLIFIERS

The MC1558S is functionally equivalent, pin compatible, and possesses the same ease of use as the popular MC1558 circuit, yet offers 20 times higher slew rate and power bandwidth. This device is ideally suited for D/A converters due to its fast settling time and high slew rate.

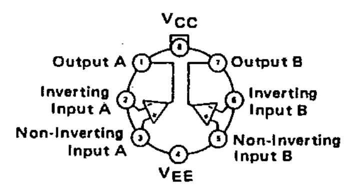
- High Slew Rate — 10 V/μs Guaranteed Minimum (for inverting unity gain only)
- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch-Up

DUAL OPERATIONAL AMPLIFIERS

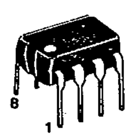
SILICON MONOLITHIC INTEGRATED CIRCUIT



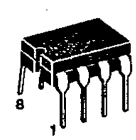
G SUFFIX
METAL PACKAGE
CASE 601-04



(Top View)

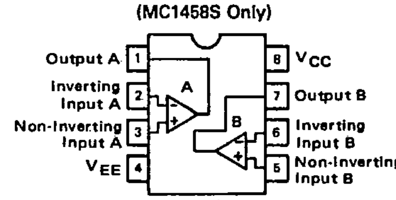


P1 SUFFIX
PLASTIC PACKAGE
CASE 626-05
(MC1458S Only)



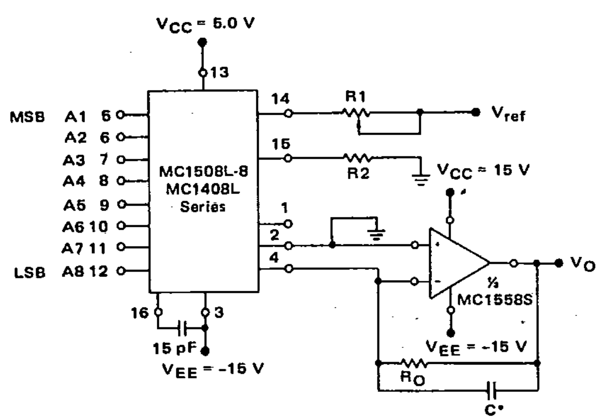
U SUFFIX
CERAMIC PACKAGE
CASE 693-02

D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8
(MC1458S Only)



(Top View)

TYPICAL APPLICATION OUTPUT CURRENT TO VOLTAGE TRANSFORMATION FOR A D-TO-A CONVERTER



Settling time to within 1/2 LSB (±19.5 mV) is approximately 4.0 μs from the time that all bits are switched.

*The value of C may be selected to minimize overshoot and ringing (C ≈ 68 pF).

Theoretical V_O

$$V_O = \frac{V_{ref}}{R1}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

Adjust V_{ref}, R1 or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

$$V_{ref} = 2.0\ \text{Vdc}$$
$$R1 = R2 \cong 1.0\ k\Omega$$
$$R_O = 5.0\ k\Omega$$

$$V_O = \frac{2\ V}{1\ k}(5\ k)\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right] = 10\ V\left[\frac{255}{256}\right] = 9.961\ V$$

MC1458S, MC1558S

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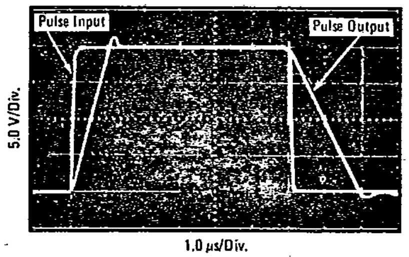
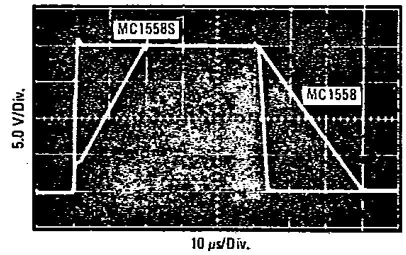
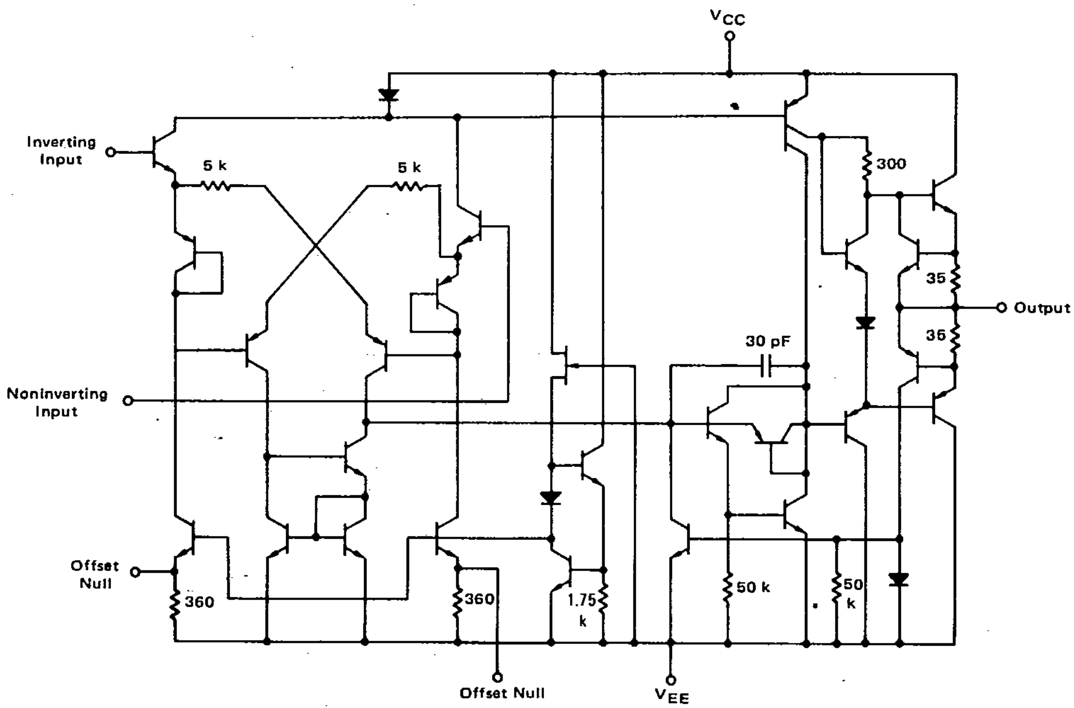
MC1558S LARGE-SIGNAL TRANSIENT RESPONSE
(Inverting Mode)



STANDARD MC1558 versus MC1558S RESPONSE COMPARISON
(Inverting Mode)



½ REPRESENTATIVE CIRCUIT SCHEMATIC



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	MC1558S	MC1458S	Unit
Power Supply Voltage	V_{CC} V_{EE}	+22 -22	+18 -18	Vdc
Input Differential Voltage Range ①	V_{IDR}	±30		Volts
Input Common-Mode Voltage Range ②	V_{ICR}	±15		Volts
Output Short Circuit Duration	t_S	Continuous		
Operating Ambient Temperature Range	T_A	-55 to +125	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C
Junction Temperature — Ceramic and Metal Package Plastic Package	T_J	175 150	175 150	°C °C

Note 1. For supply voltages less than ±15 Vdc, the absolute maximum input voltage is equal to the supply voltage.
Note 2. Supply voltage equal to or less than 15 Vdc.

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ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1558S Min	MC1558S Typ	MC1558S Max	MC1458S Min	MC1458S Typ	MC1458S Max	Unit
Power Bandwidth (See Figure 3) A_v = 1, R_L = 2.0 kΩ, THD = 5%, V_O = 20 V(p-p)	BW_p	150	200	–	150	200	–	kHz
Large-Signal Transient Response								
Slew Rate (Figures 10 and 11)	SR							
V(–) to V(+)		10	20	–	10	20	–	V/µs
V(+) to V(–)		10	12	–	10	12	–	
Settling Time (Figures 10 and 11) (to within 0.1%)	t_{setlg}	–	3.0	–	–	3.0	–	µs
Small-Signal Transient Response (Gain = 1, E_{in} = 20 mV, see Figures 7 and 8)								
Rise Time	t_{TLH}	–	0.25		–	0.25	–	µs
Fall Time	t_{THL}	–	0.25	–	–	0.25	–	µs
Propagation Delay Time	t_{PLH}, t_{PHL}	–	0.25	–	–	0.25	–	µs
Overshoot	OS	–	20	–	–	20	–	%
Short-Circuit Output Currents	I_{OS}	±10	–	±45	±10	–	±45	mA
Open-Loop Voltage Gain (R_L ≥ 2.0 kΩ) (See Figure 4) V_O = ±10 V	A_{VOL}	50,000	200,000	–	20,000	100,000	–	–
Output Impedance (f = 20 Hz)	z_o	–	75	–	–	75	–	Ω
Input Impedance (f = 20 Hz)	z_i	0.3	1.0	–	0.3	1.0	–	MΩ
Output Voltage Swing	V_O							V_{pk}
R_L = 10 kΩ		±12	±14	–	±12	±14	–	
R_L = 2.0 kΩ		±10	±13	–	±10	±13	–	
Input Common-Mode Voltage Swing	V_{ICR}	±12	±13	–	±12	±13	–	V_{pk}
Common-Mode Rejection Ratio (f = 20 Hz)	CMRR	70	90	–	70	90	–	dB
Input Bias Current (See Figure 2)	I_{IB}	–	200	500	–	200	500	nA
Input Offset Current	$\lvert I_{IO} \rvert$	–	30	200	–	30	200	nA
Input Offset Voltage (R_S ≤ 10 kΩ)	$\lvert V_{IO} \rvert$	–	1.0	5.0	–	2.0	6.0	mV
DC Power Consumption (See Figure 9) (Power Supply = ±15 V, V_O = 0)	P_C	–	70	150	–	70	170	mW
Positive Voltage Supply Sensitivity (V_{EE} constant)	PSS+	–	2.0	150	–	2.0	150	µV/V
Negative Voltage Supply Sensitivity (V_{CC} constant)	PSS-	–	10	150	–	10	150	µV/V

**Plastic package offered in limited temperature range device only.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = –15 Vdc, T_A = –55 to +125°C for MC1558S and T_A = 0 to 70°C for MC1458S, unless otherwise noted.)

Characteristic	Symbol	MC1558S Min	MC1558S Typ	MC1558S Max	MC1458S Min	MC1458S Typ	MC1458S Max	Unit
Open Loop Voltage Gain V_O = ±10 V	A_{VOL}	25,000	–	–	15,000	–	–	V/V
Output Voltage Swing	V_O							V_{pk}
R_L = 10 kΩ		±12	–	–	±12	–	–	
R_L = 2 kΩ		±10	–	–	±10	–	–	
Input Common-Mode Voltage Range	V_{ICR}	±12	–	–	–	–	–	V_{pk}
Common-Mode Rejection Ratio (f = 20 Hz)	CMRR	70	–	–	–	–	–	dB
Input Bias Current	I_{IB}							nA
T_A = 125°C		–	200	500	–	–	–	
T_A = -55°C		–	500	1500	–	–	–	
T_A = 0 to 70°C		–	–	–	–	–	800	
Input Offset Current	I_{IO}							nA
T_A = 125°C		–	30	200	–	–	–	
T_A = -55°C		–	–	500	–	–	–	
T_A = 0 to 70°C		–	–	–	–	–	300	
Input Offset Voltage R_S ≤ 10 kΩ	V_{IO}	–	–	6.0	–	–	7.5	mV
DC Power Consumption V_O = 0 V	P_C	–	–	200	–	–	–	mW
Positive Power Supply Sensitivity V_{EE} = -15 V	P_{SS+}	–	–	150	–	–	–	µV/V
Negative Power Supply Sensitivity V_{CC} = 15 V	P_{SS-}	–	–	150	–	–	–	µV/V

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 1 — OFFSET ADJUST CIRCUIT

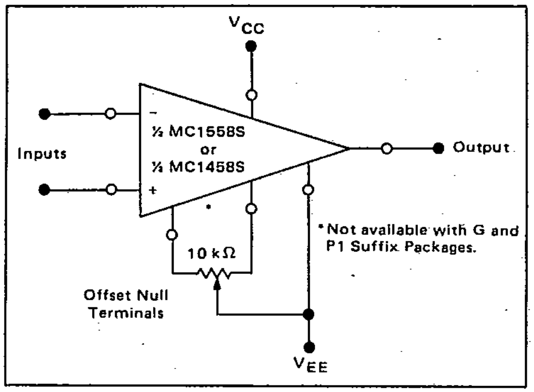


FIGURE 2 — INPUT BIAS CURRENT versus TEMPERATURE

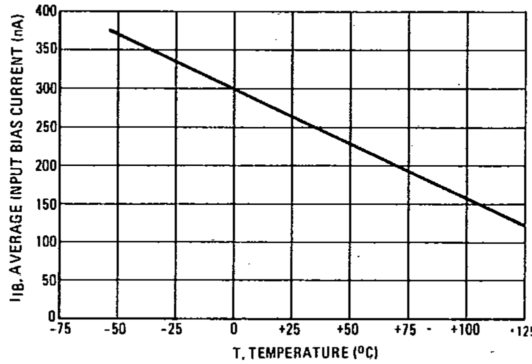


FIGURE 3 — POWER BANDWIDTH — NONDISTORTED OUTPUT VOLTAGE versus FREQUENCY

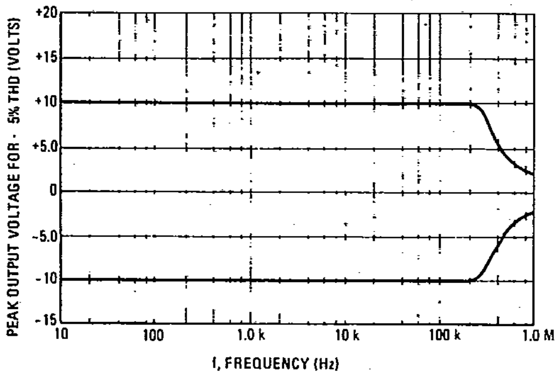


FIGURE 4 — OPEN-LOOP FREQUENCY RESPONSE

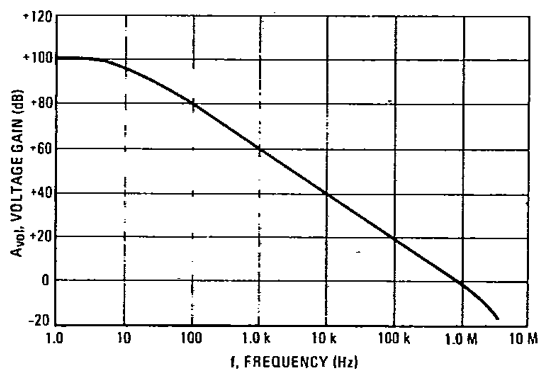
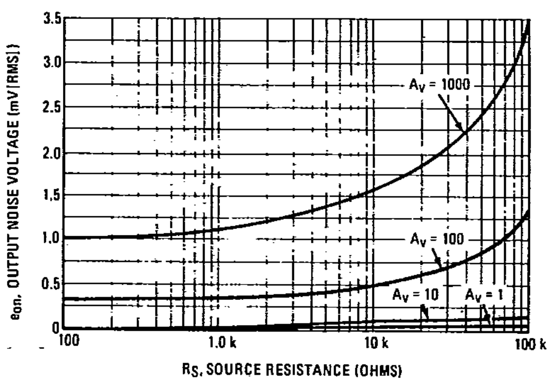


FIGURE 5 — OUTPUT NOISE versus SOURCE RESISTANCE



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TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 6 — SMALL-SIGNAL TRANSIENT RESPONSE DEFINITIONS

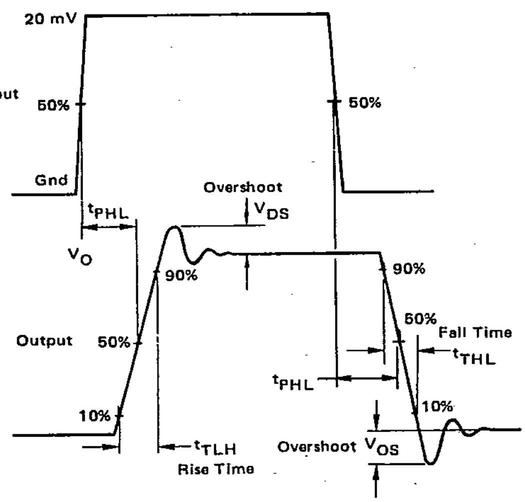


FIGURE 7 — SMALL-SIGNAL TRANSIENT RESPONSE

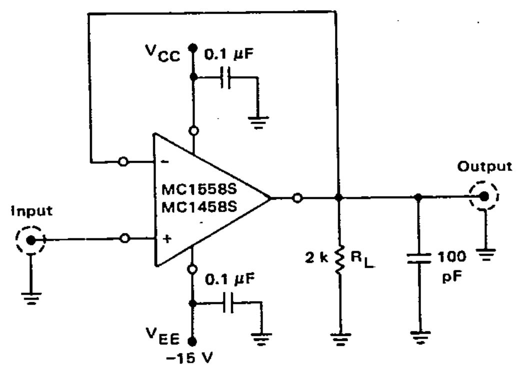


FIGURE 8 — POWER CONSUMPTION versus POWER SUPPLY VOLTAGES

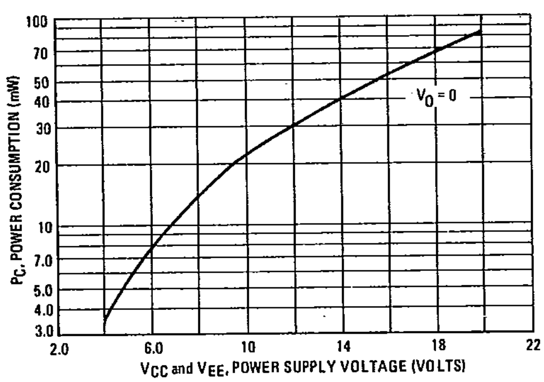


FIGURE 9 — LARGE-SIGNAL TRANSIENT WAVEFORMS

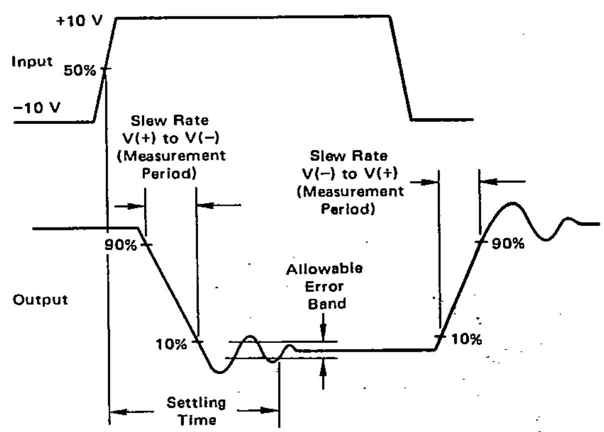
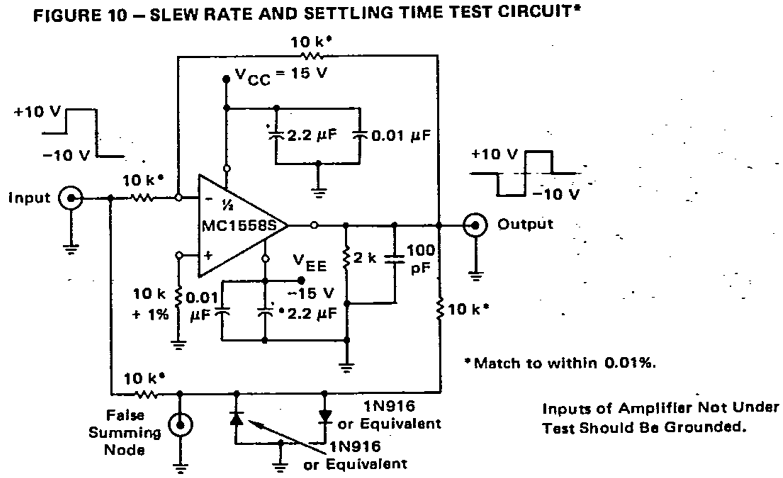


FIGURE 10 — SLEW RATE AND SETTLING TIME TEST CIRCUIT*



*Match to within 0.01%.

Inputs of Amplifier Not Under Test Should Be Grounded.

SETTLING TIME

In order to properly utilize the high slew rate and fast settling time of an operational amplifier, a number of system considerations must be observed. Capacitance at the summing node and at the amplifier output must be minimal and circuit board layout should be consistent with common high-frequency considerations. Both power supply connections should be adequately bypassed as close as possible to the device pins. In bypassing, both low and high-frequency components should be considered to avoid the possibility of excessive ringing. In order to achieve optimum damping, the selection of a capacitor in parallel with the feedback resistor may be necessary. A value too small could result in excessive ringing while a value too large will degrade slew rate and settling time.

SETTLING TIME MEASUREMENT

In order to accurately measure the settling time of an operational amplifier, it is suggested that the "false" summing junction approach be taken as shown in Figure 11. This is necessary since it is difficult to determine when the waveform at the output of the operational amplifier settles to within 0.1% of it's final value. Because the output and input voltages are effectively subtracted from each other at the amplifier inverting input, this seems like an ideal node for the measurement. However, the probe capacitance at this critical node can greatly affect the accuracy of the actual measurement.

FIGURE 11 — WAVEFORM AT FALSE SUMMING NODE
(Inverting Mode)

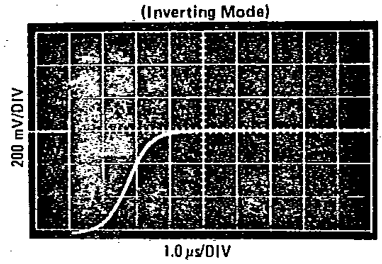
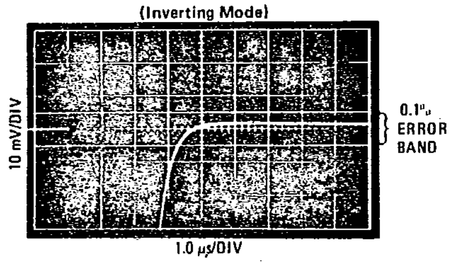


FIGURE 12 — EXPANDED WAVEFORM AT FALSE SUMMING NODE
(Inverting Mode)



The solution to these problems is the creation of a second or "false" summing node. The addition of two diodes at this node clamps the error voltage to limit the voltage excursion to the oscilloscope. Because of the voltage divider effect, only one-half of the actual error appears at this node. For extremely critical measurements, the capacitance of the diodes and the oscilloscope, and the settling time of the oscilloscope must be considered. The expression

$$t_{setlg} = \sqrt{x^2 + y^2 + z^2}$$

can be used to determine the actual amplifier settling time, where

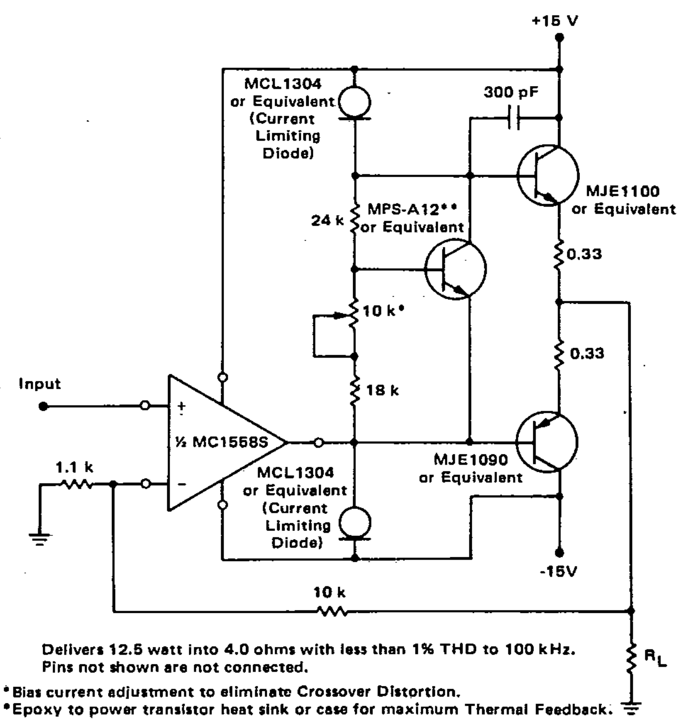
t_{setlg} = observed settling time
x = amplifier settling time (to be determined)
y = false summing junction settling time
z = oscilloscope settling time

It should be remembered that to settle within ±0.1% requires 7RC time constants.

The ±0.1% factor was chosen for the MC1558S settling time as it is compatible with the ±1/2 LSB accuracy of the MC1508L-8 digital-to-analog converter. This D-to-A converter features ±0.19% maximum error.

TYPICAL APPLICATION

FIGURE 13 — 12.5-WATT WIDEBAND POWER AMPLIFIER



Delivers 12.5 watt into 4.0 ohms with less than 1% THD to 100 kHz.
Pins not shown are not connected.
*Bias current adjustment to eliminate Crossover Distortion.
**Epoxy to power transistor heat sink or case for maximum Thermal Feedback.