

# NTGD4161P

## Power MOSFET

-30 V, -2.3 A, Dual P-Channel, TSOP-6

### Features

- Fast Switching Speed
- Low Gate Charge
- Low  $R_{DS(on)}$
- Independently Connected Devices to Provide Design Flexibility
- This is a Pb-Free Device

### Applications

- Load Switch
- Battery Protection
- Portable Devices Like PDAs, Cellular Phones and Hard Drives

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	$V_{DSS}$	-30	V	
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V	
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$ -2.1	A
		$T_A = 85^\circ\text{C}$	-1.5	
		$t \leq 5$ s	$T_A = 25^\circ\text{C}$	
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	$P_D$ 1.1	W
		$t \leq 5$ s	1.3	
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$ -1.5	A
		$T_A = 85^\circ\text{C}$	-1.1	
Power Dissipation (Note 2)		$T_A = 25^\circ\text{C}$	$P_D$ 0.6	W
Pulsed Drain Current	$t_p = 10$ $\mu\text{s}$	$I_{DM}$	-10	A
Operating Junction and Storage Temperature	$T_J, T_{STG}$	-55 to 150		$^\circ\text{C}$
Source Current (Body Diode)	$I_S$	-0.8		A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260		$^\circ\text{C}$

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	115	$^\circ\text{C}/\text{W}$
Junction-to-Ambient - Steady State (Note 2)		225	
Junction-to-Ambient - $t \leq 5$ s (Note 1)		95	
Junction-to-Case - Steady State (Note 1)	$R_{\theta JC}$	40	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. When surface mounted to an FR4 board using 1 in. pad size (Cu. area = 1.2 in<sup>2</sup> [1 oz] including traces)
2. When surface mounted to an FR4 board using minimum recommended pad size (Cu. area = 0.047 in<sup>2</sup>)

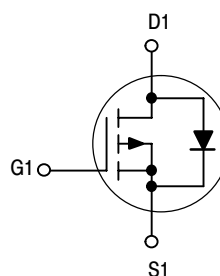


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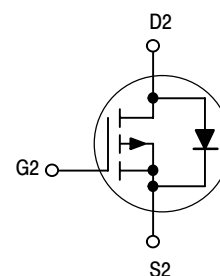
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ Max
-30 V	160 m $\Omega$ @ -10 V
	280 m $\Omega$ @ -4.5 V

P-Channel (MOSFET1)



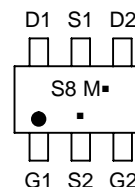
P-Channel (MOSFET2)



### MARKING DIAGRAM



TSOP-6  
CASE 318G  
STYLE 13



S8 = Specific Device Code  
M = Date Code\*  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation may vary depending upon manufacturing location.

### ORDERING INFORMATION

Device	Package	Shipping†
NTGD4161PT1G	TSOP-6 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTGD4161P

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub>=25°C unless otherwise stated)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA	-30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>			22		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -24 V	T <sub>J</sub> = 25°C		-1.0	μA
			T <sub>J</sub> = 125°C		-10	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -250 μA	-1.0	-1.9	-3.0	V
Gate Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>			-4.7		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -2.1 A		105	160	mΩ
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -1.6 A		190	280	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = -5.0 V, I <sub>D</sub> = -2.1 A		2.7		S

### CHARGES AND CAPACITANCES

Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> = -15 V, f = 1.0 MHz, V <sub>GS</sub> = 0 V		281		pF
Output Capacitance	C <sub>OSS</sub>			50		
Reverse Transfer Capacitance	C <sub>RSS</sub>			28		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = -10 V, V <sub>DS</sub> = -5.0 V, I <sub>D</sub> = -2.1 A		5.6	7.1	nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			0.65		
Gate-to-Source Charge	Q <sub>GS</sub>			1.2		
Gate-to-Drain Charge	Q <sub>GD</sub>			0.90		

### SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = -4.5 V, V <sub>DD</sub> = -15 V, I <sub>D</sub> = -1.0 A, R <sub>G</sub> = 6.0 Ω		7.6	14	ns
Rise Time	t <sub>r</sub>			9.2	23	
Turn-Off Delay Time	t <sub>d(off)</sub>			12.5	20	
Fall Time	t <sub>f</sub>			4.5	12	

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -0.8 A	T <sub>J</sub> = 25°C		-0.79	-1.2	V
			T <sub>J</sub> = 125°C		-0.65		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = -0.8 A		8.0		ns	
Charge Time	t <sub>a</sub>			5.7			
Discharge Time	t <sub>b</sub>			2.3			
Reverse Recovery Charge	Q <sub>RR</sub>			3			nC

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

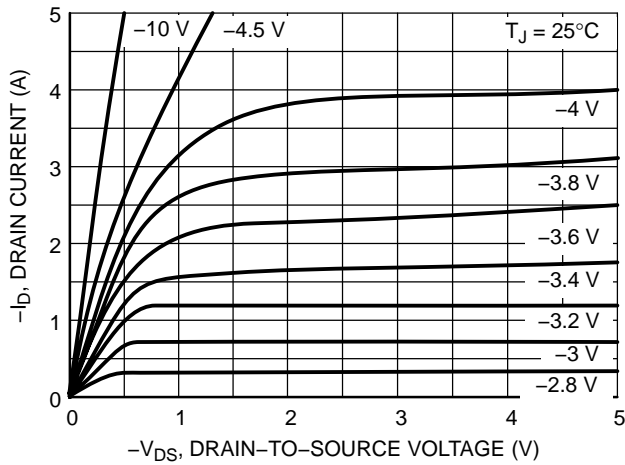


Figure 1. On-Region Characteristics

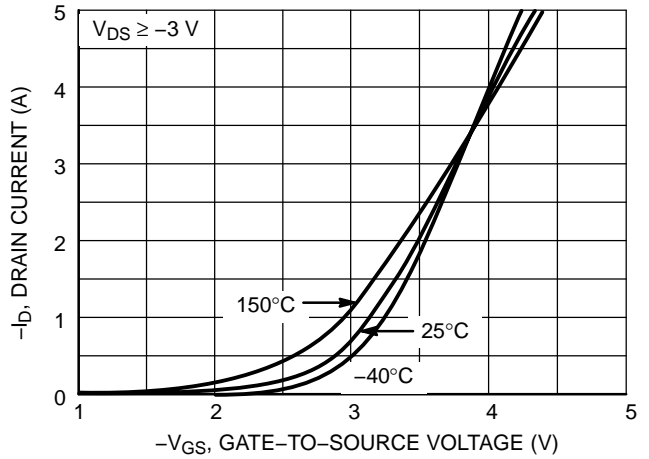


Figure 2. Transfer Characteristics

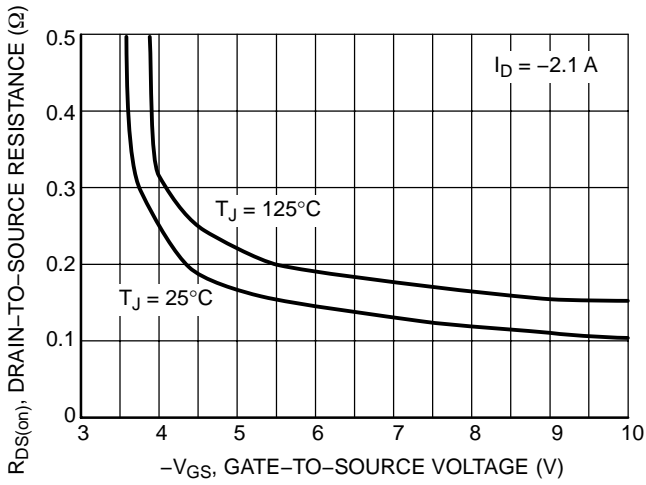


Figure 3. On-Resistance versus Gate-to-Source Voltage

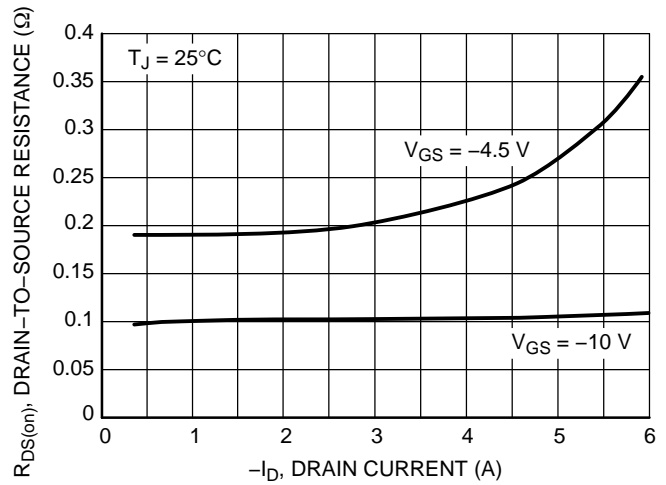


Figure 4. On-Resistance versus Drain Current and Temperature

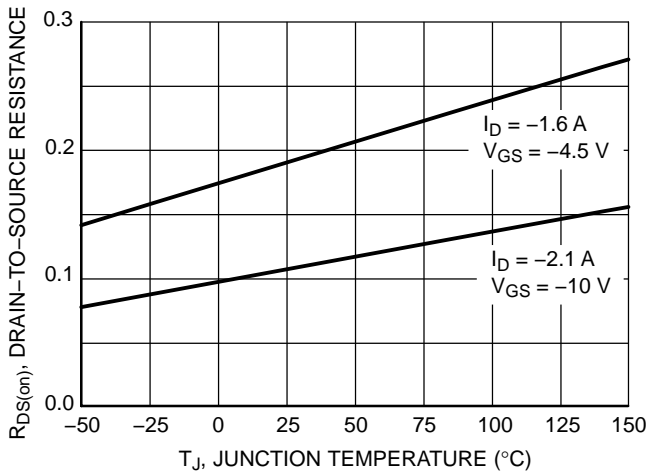


Figure 5. On-Resistance Variation with Temperature

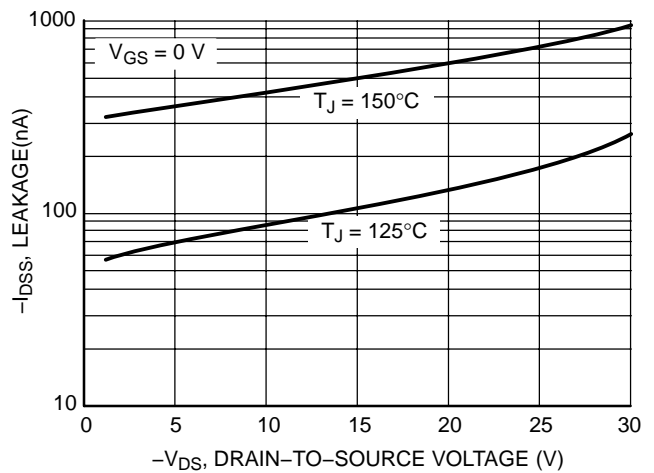


Figure 6. On-Resistance Variation with Temperature

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## TYPICAL PERFORMANCE CURVES

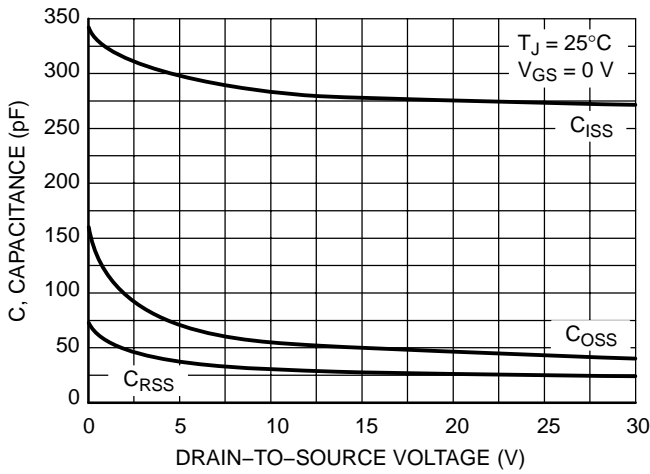


Figure 7. Capacitance Variation

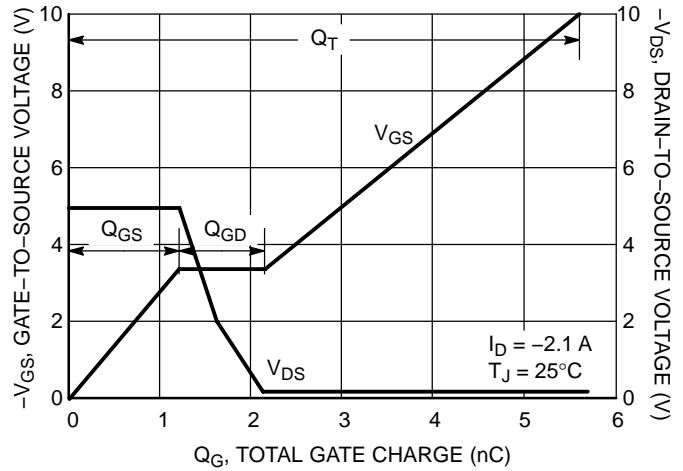


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

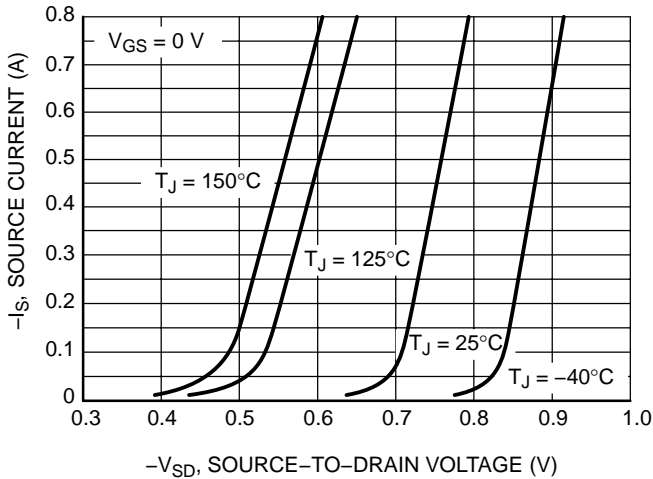


Figure 9. Diode Forward Voltage versus Current

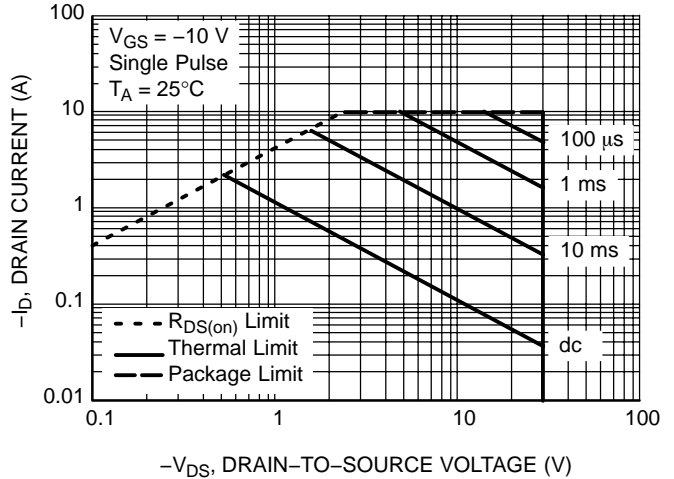


Figure 10. Maximum Rated Forward Biased Safe Operating Area

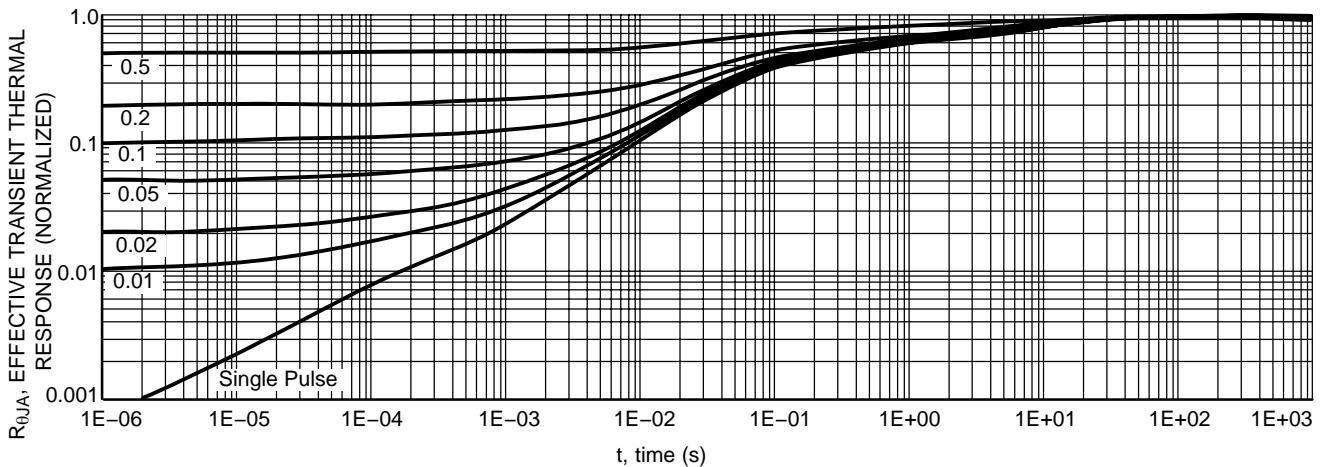
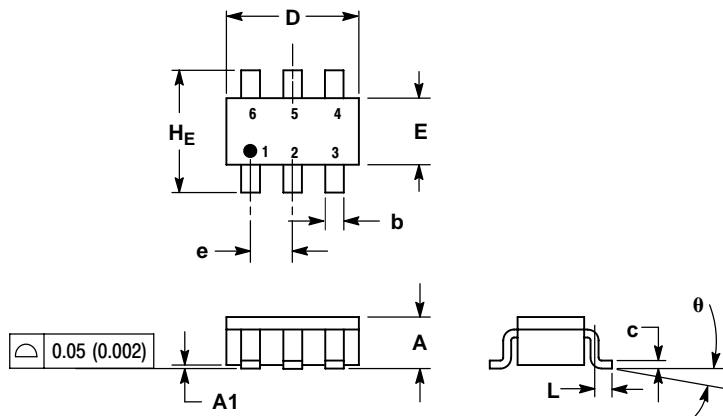


Figure 11. FET Thermal Response

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## PACKAGE DIMENSIONS

### TSOP-6 CASE 318G-02 ISSUE S



#### NOTES:

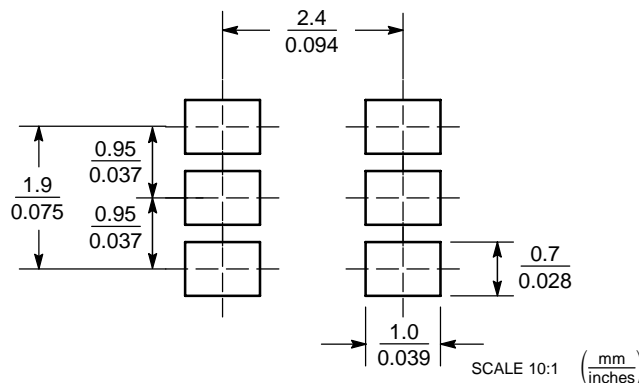
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.38	0.50	0.010	0.014	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
HE	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	-	10°	0°	-	10°

#### STYLE 13:

- PIN 1. GATE 1
- SOURCE 2
- GATE 2
- DRAIN 2
- SOURCE 1
- DRAIN 1

#### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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