

1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2114

General Description

The AP2114 is CMOS process low dropout linear regulator with enable function, the regulator delivers a guaranteed 1A (Min.) continuous load current.

The AP2114 features low power consumption.

The AP2114 is available in 1.2V, 1.8V, 2.5V and 3.3V regulator output, and available in excellent output accuracy 1.5%, it is also available in an excellent load regulation and line regulation performance.

The AP2114 is available in standard packages of SOT-223, TO-252-2 (1), TO-252-2 (3), TO-263-3, SOIC-8 and PSOP-8.

Features

- Output Voltage Accuracy: $\pm 1.5\%$
- Output Current: 1A (Min.)
- Fold-back Short Current Protection: 50mA
- Low Dropout Voltage (3.3V): 450mV (Typ.) @ $I_{OUT}=1A$
- Stable with 4.7 μF Flexible Cap: Ceramic, Tantalum and Aluminum Electrolytic
- Excellent Line Regulation: 0.02%/V (Typ.), 0.1%/V (Max.) @ $I_{OUT}=30mA$
- Excellent Load Regulation: 0.2% @ $I_{OUT}=0A$ to 1A
- Low Quiescent Current: 60 μA (1.2V/1.8V/2.5V)
- Low Output Noise: 30 $\mu VRMS$
- PSRR: 68dB @ Freq=1KHz (1.2V/1.8V)
- OTSD Protection
- Operating Temperature Range: -40°C to 85°C
- ESD: MM 400V, HBM 4000V

Applications

- LCD Monitor
- LCD TV
- STB

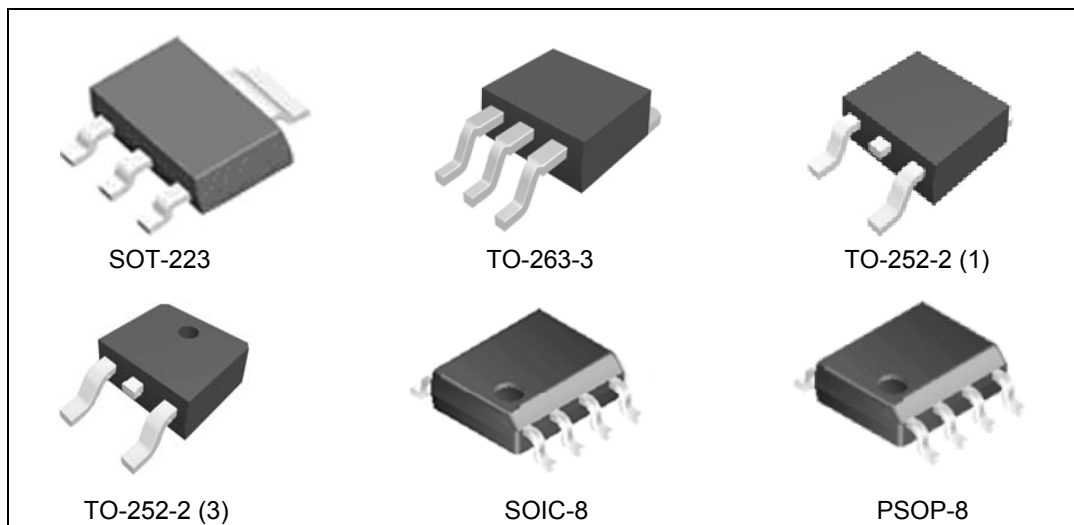


Figure 1. Package Types of AP2114

1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2114

Pin Configuration

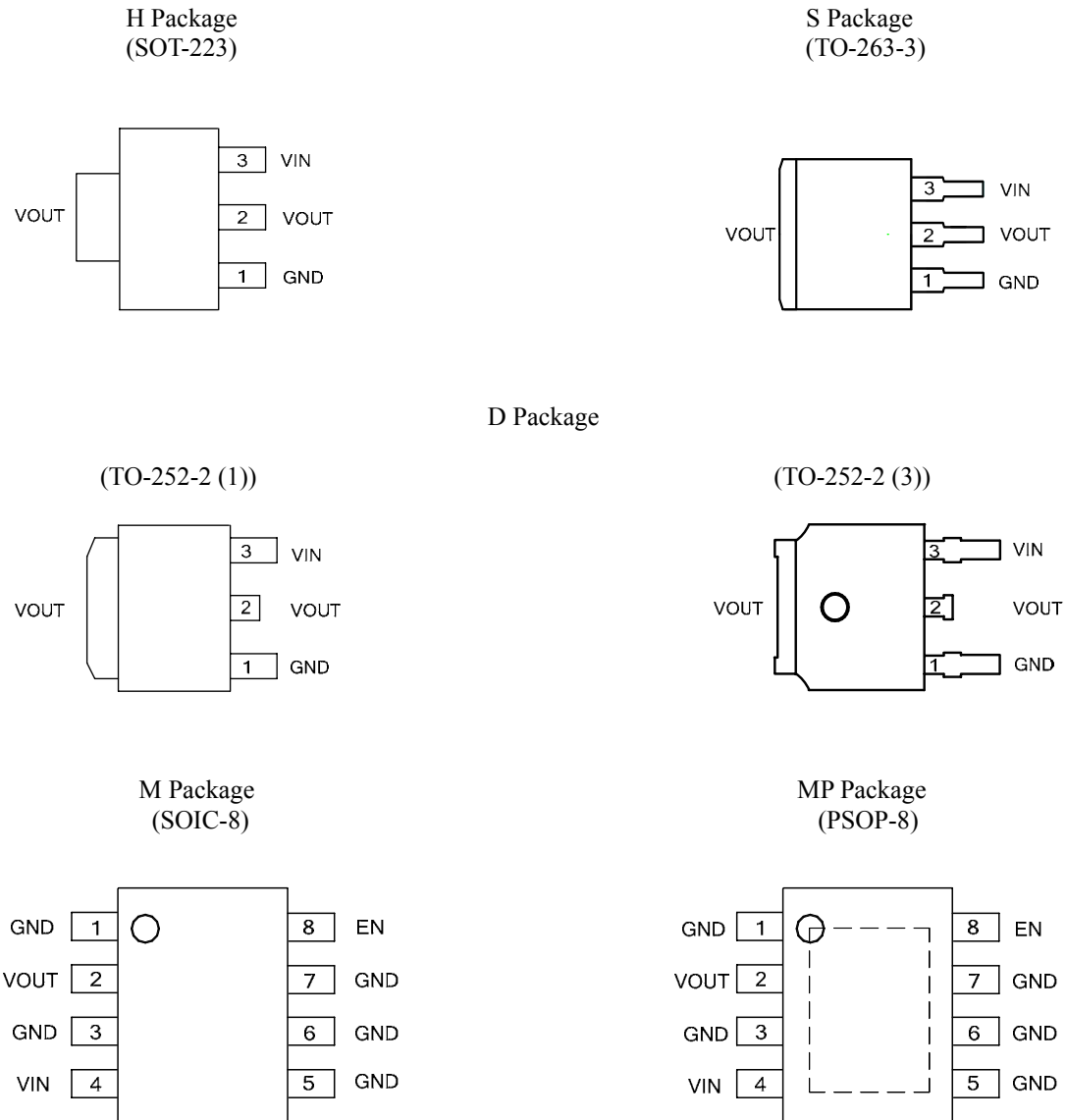


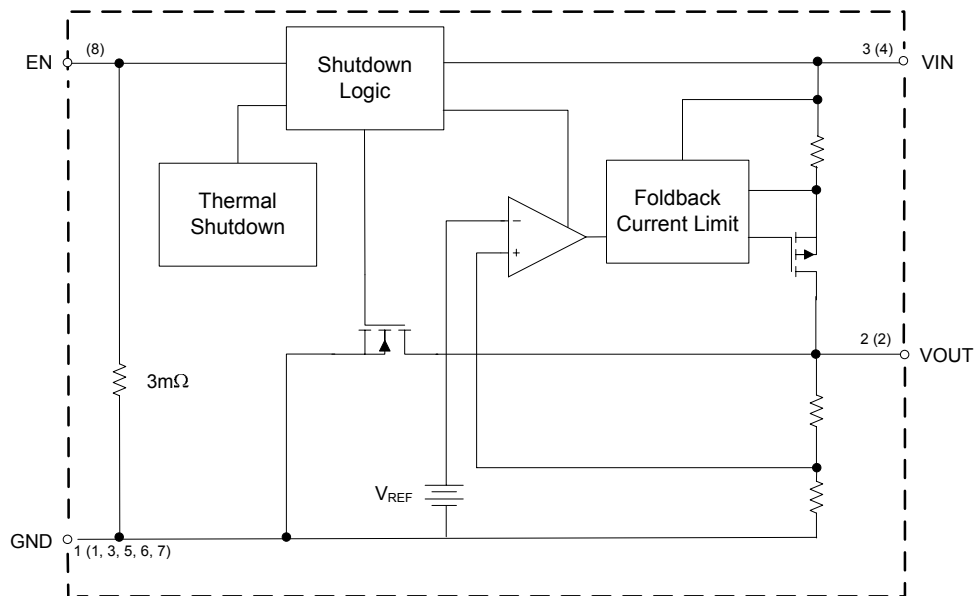
Figure 2. Pin Configuration of AP2114 (Top View)

1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2114

Pin Descriptions

Pin Number		Pin Name	Function
SOT-223, TO-263-3, TO-252-2 (1) / (3)	SOIC-8/PSOP-8		
1	1, 3, 5, 6, 7,	GND	Ground
2	2	VOUT	Regulated Output
3	4	VIN	Input Voltage Pin
	8	EN	Chip Enable, H – normal work, L – shutdown output

Functional Block Diagram



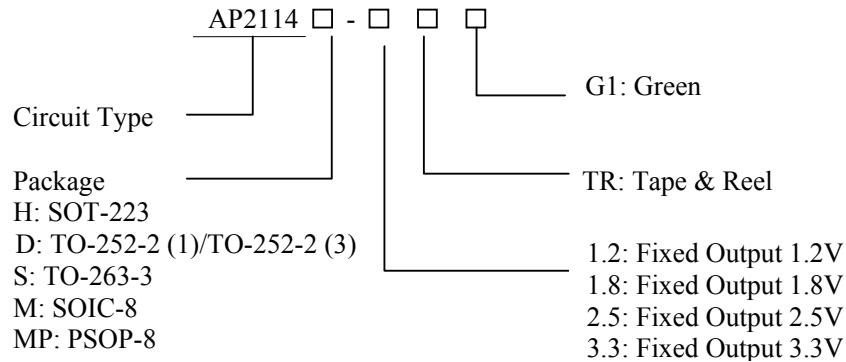
A (B)
 A: SOT-223, TO-263-3, TO-252-2 (1)/(3)
 B: SOIC-8, PSOP-8

Figure 3. Functional Block Diagram of AP2114



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Ordering Information



Package	Temperature Range	Part Number	Marking ID	Packing Type
SOT-223	-40 to 85°C	AP2114H-1.2TRG1	GH12C	Tape & Reel
		AP2114H-1.8TRG1	GH12D	Tape & Reel
		AP2114H-2.5TRG1	GH14C	Tape & Reel
		AP2114H-3.3TRG1	GH12E	Tape & Reel
TO-252-2 (1)/ TO-252-2 (3)	-40 to 85°C	AP2114D-1.2TRG1	AP2114D-1.2G1	Tape & Reel
		AP2114D-1.8TRG1	AP2114D-1.8G1	Tape & Reel
		AP2114D-2.5TRG1	AP2114D-2.5G1	Tape & Reel
		AP2114D-3.3TRG1	AP2114D-3.3G1	Tape & Reel
TO-263-3	-40 to 85°C	AP2114S-1.2TRG1	AP2114S-1.2G1	Tape & Reel
		AP2114S-1.8TRG1	AP2114S-1.8G1	Tape & Reel
		AP2114S-2.5TRG1	AP2114S-2.5G1	Tape & Reel
		AP2114S-3.3TRG1	AP2114S-3.3G1	Tape & Reel
SOIC-8	-40 to 85°C	AP2114M-1.2TRG1	2114M-1.2G1	Tape & Reel
		AP2114M-1.8TRG1	2114M-1.8G1	Tape & Reel
		AP2114M-2.5TRG1	2114M-2.5G1	Tape & Reel
		AP2114M-3.3TRG1	2114M-3.3G1	Tape & Reel
PSOP-8	-40 to 85°C	AP2114MP-1.2TRG1	2114MP-1.2G1	Tape & Reel
		AP2114MP-1.8TRG1	2114MP-1.8G1	Tape & Reel
		AP2114MP-2.5TRG1	2114MP-2.5G1	Tape & Reel
		AP2114MP-3.3TRG1	2114MP-3.3G1	Tape & Reel

BCD Semiconductor's Pb-free products, as designated with "G1" suffix in the part number, are RoHS compliant and Green.

**1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2114****Absolute Maximum Ratings (Note 1)**

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{IN}	6.5	V
Operating Junction Temperature Range	T_J	150	°C
Storage Temperature Range	T_{STG}	-65 to 150	°C
Lead Temperature (Soldering, 10sec)	T_{LEAD}	260	°C
ESD (Machine Model)		400	V
ESD (Human Body Model)		4000	V

Note 1: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{IN}	2.5	6.0	V
Operating Ambient Temperature Range	T_A	-40	85	°C



1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2114

Electrical Characteristics

AP2114-1.2 Electrical Characteristics (Note 2)

($V_{IN}=2.5V$, $C_{IN}=4.7\mu F$ (Ceramic), $C_{OUT}=4.7\mu F$ (Ceramic), Typical $T_A = 25^\circ C$, **Bold** typeface applies over $-40^\circ C \leq T_A \leq 85^\circ C$ ranges, unless otherwise specified (Note 3))

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_{OUT}	$V_{IN}=2.5V$, $1mA \leq I_{OUT} \leq 30mA$	$V_{OUT} \times 98.5\%$	1.2	$V_{OUT} \times 101.5\%$	V
Input Voltage	V_{IN}				6.0	V
Maximum Output Current	$I_{OUT(MAX)}$	$V_{IN}=2.5V$, $V_{OUT}=1.182V$ to $1.218V$	1			A
Load Regulation	$\frac{\Delta V_{OUT}/V_{OUT}}{\Delta I_{OUT}}$	$V_{IN}=2.5V$, $1mA \leq I_{OUT} \leq 1A$		0.2	1	%/A
Line Regulation	$\frac{\Delta V_{OUT}/V_{OUT}}{\Delta V_{IN}}$	$2.5V \leq V_{IN} \leq 6V$, $I_{OUT}=30mA$		0.02	± 0.1	%/V
Dropout Voltage	V_{DROP}	$I_{OUT}=1.0A$		1200	1300	mV
Quiescent Current	I_Q	$V_{IN}=2.5V$, $I_{OUT}=0mA$		60	75	μA
Power Supply Rejection Ratio	PSRR	Ripple 1Vp-p $V_{IN}=2.5V$, $I_{OUT}=100mA$	$f=100Hz$	68		dB
			$f=1KHz$	68		
Output Voltage Temperature Coefficient	$\frac{\Delta V_{OUT}/V_{OUT}}{\Delta T}$	$I_{OUT}=30mA$, $T_A = -40^\circ C$ to $85^\circ C$		± 30		ppm/ $^\circ C$
Short Current Limit	I_{SHORT}	$V_{OUT}=0V$		50		mA
RMS Output Noise	V_{NOISE}	$10Hz \leq f \leq 100kHz$ (No Load)		30		μV_{RMS}
V_{EN} High Voltage	V_{IH}	Enable logic high, regulator on	1.5			V
V_{EN} Low Voltage	V_{IL}	Enable logic low, regulator off			0.4	
Standby Current	I_{STD}	$V_{IN}=3.5V$, V_{EN} in OFF mode		0.01	1.0	μA
Start-up Time	T_S	No Load		20		μs
EN Pull Down Resistor	RPD			3.0		m Ω
V_{OUT} Discharge Resistor	R_{DCHG}	Set EN pin at Low		60		Ω
Thermal Shutdown Temperature	T_{OTSD}			160		$^\circ C$
Thermal Shutdown Hysteresis	T_{HYOTSD}			25		
Thermal Resistance (Junction to Case)	θ_{JC}	SOIC-8		74.6		$^\circ C/W$
		PSOP-8		43.7		
		SOT-223		50.9		
		TO-252-2 (1) / TO-252-2 (3)		35		
		TO-263-3		22		

Note 2: To prevent the Short Circuit Current protection feature from being prematurely activated, the input voltage must be applied before a current source load is applied.

Note 3: Production testing at $T_A=25^\circ C$. Over temperature specifications guaranteed by design only.



1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2114

Electrical Characteristics (Continued)

AP2114-1.8 Electrical Characteristics (Note 2)

($V_{IN}=2.8V$, $C_{IN}=4.7\mu F$ (Ceramic), $C_{OUT}=4.7\mu F$ (Ceramic), Typical $T_A = 25^\circ C$, **Bold** typeface applies over $-40^\circ C \leq T_A \leq 85^\circ C$ ranges, unless otherwise specified (Note 3))

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_{OUT}	$V_{IN}=2.8V$, $1mA \leq I_{OUT} \leq 30mA$	$V_{OUT} \times 98.5\%$	1.8	$V_{OUT} \times 101.5\%$	V
Maximum Output Current	$I_{OUT(MAX)}$	$V_{IN}=2.8V$, $V_{OUT}=1.773V$ to $1.827V$	1.0			A
Load Regulation	$\frac{\Delta V_{OUT}/V_{OUT}}{\Delta I_{OUT}}$	$V_{IN}=2.8V$, $1mA \leq I_{OUT} \leq 1A$		0.2	1.0	%/A
Line Regulation	$\frac{\Delta V_{OUT}/V_{OUT}}{\Delta V_{IN}}$	$2.8V \leq V_{IN} \leq 6V$, $I_{OUT}=30mA$		0.02	± 0.1	%/V
Dropout Voltage	V_{DROP}	$I_{OUT}=1.0A$		500	700	mV
Quiescent Current	I_Q	$V_{IN}=2.8V$, $I_{OUT}=0mA$		60	75	μA
Power Supply Rejection Ratio	PSRR	Ripple 1Vp-p $V_{IN}=2.8V$, $I_{OUT}=100mA$	f=100Hz	68		dB
			f=1KHz	68		
Output Voltage Temperature Coefficient	$\frac{\Delta V_{OUT}/V_{OUT}}{\Delta T}$	$I_{OUT}=30mA$, $T_A = -40^\circ C$ to $85^\circ C$		± 30		ppm/ $^\circ C$
Short Current Limit	I_{SHORT}	$V_{OUT}=0V$		50		mA
RMS Output Noise	V_{NOISE}	$10Hz \leq f \leq 100kHz$ (No load)		30		μV_{RMS}
V_{EN} High Voltage	V_{IH}	Enable logic high, regulator on	1.5			V
V_{EN} Low Voltage	V_{IL}	Enable logic low, regulator off			0.4	
Standby Current	I_{STD}	$V_{IN}=3.5V$, V_{EN} in OFF mode		0.01	1.0	μA
Start-up Time	T_S	No Load		20		μs
EN Pull Down Resistor	RPD			3.0		m Ω
V_{OUT} Discharge Resistor	R_{DCHG}	Set EN pin at Low		60		Ω
Thermal Shutdown Temperature	T_{OTSD}			160		$^\circ C$
Thermal Shutdown Hysteresis	T_{HYOTSD}			25		
Thermal Resistance (Junction to Case)	θ_{JC}	SOIC-8		74.6		$^\circ C / W$
		PSOP-8		43.7		
		SOT-223		50.9		
		TO-252-2 (1) / TO-252-2 (3)		35		
		TO-263-3		22		

Note 2: To prevent the Short Circuit Current protection feature from being prematurely activated, the input voltage must be applied before a current source load is applied.

Note 3: Production testing at $T_A=25^\circ C$. Over temperature specifications guaranteed by design only.



1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2114

Electrical Characteristics (Continued)

AP2114-2.5 Electrical Characteristics (Note 2)

($V_{IN}=3.5V$, $C_{IN}=4.7\mu F$ (Ceramic), $C_{OUT}=4.7\mu F$ (Ceramic), Typical $T_A = 25^\circ C$, **Bold** typeface applies over $-40^\circ C \leq T_A \leq 85^\circ C$ ranges, unless otherwise specified (Note 3))

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_{OUT}	$V_{IN}=3.5V$, $1mA \leq I_{OUT} \leq 30mA$	$\frac{V_{OUT}}{\times 98.5\%}$	2.5	$\frac{V_{OUT}}{\times 101.5\%}$	V
Maximum Output Current	$I_{OUT(MAX)}$	$V_{IN}=3.5V$, $V_{OUT}=2.463V$ to $2.537V$	1.0			A
Load Regulation	$\frac{\Delta V_{OUT}/V_{OUT}}{\Delta I_{OUT}}$	$V_{out}=2.5V$, $V_{IN}=V_{out}+1V$ $1mA \leq I_{OUT} \leq 1A$		0.2	1.0	%/A
Line Regulation	$\frac{\Delta V_{OUT}/V_{OUT}}{\Delta V_{IN}}$	$3.5V \leq V_{IN} \leq 6V$, $I_{OUT}=30mA$		0.02	± 0.1	%/V
Dropout Voltage	V_{DROP}	$I_{OUT}=1A$		450	750	mV
Quiescent Current	I_Q	$V_{IN}=3.5V$, $I_{OUT}=0mA$		60	80	μA
Power Supply Rejection Ratio	PSRR	Ripple 1Vp-p $V_{IN}=3.5V$, $I_{OUT}=100mA$	$f=100Hz$	65		dB
			$f=1KHz$	65		
Output Voltage Temperature Coefficient	$\frac{\Delta V_{OUT}/V_{OUT}}{\Delta T}$	$I_{OUT}=30mA$		± 30		ppm/ $^\circ C$
Short Current Limit	I_{SHORT}	$V_{OUT}=0V$		50		mA
RMS Output Noise	V_{NOISE}	$10Hz \leq f \leq 100kHz$		30		μV_{RMS}
V_{EN} High Voltage	V_{IH}	Enable logic high, regulator on	1.5			V
V_{EN} Low Voltage	V_{IL}	Enable logic low, regulator off			0.4	
Standby Current	I_{STD}	$V_{IN}=3.5V$, V_{EN} in OFF mode		0.01	1.0	μA
Start-up Time	T_S	No Load		20		μs
EN Pull Down Resistor	RPD			3.0		m Ω
V_{OUT} Discharge Resistor	R_{DCHG}	Set EN pin at Low		60		Ω
Thermal Shutdown Temperature	T_{OTSD}			160		$^\circ C$
Thermal Shutdown Hysteresis	T_{HYOTSD}			25		
Thermal Resistance (Junction to Case)	θ_{JC}	SOIC-8		74.6		$^\circ C / W$
		PSOP-8		43.7		
		SOT-223		50.9		
		TO-252-2 (1) / TO-252-2 (3)		35		
		TO-263-3		22		

Note 2: To prevent the Short Circuit Current protection feature from being prematurely activated, the input voltage must be applied before a current source load is applied.

Note 3: Production testing at $T_A=25^\circ C$. Over temperature specifications guaranteed by design only.



1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2114

Electrical Characteristics (Continued)

AP2114-3.3 Electrical Characteristics (Note 2)

($V_{IN}=4.3V$, $C_{IN}=4.7\mu F$ (Ceramic), $C_{OUT}=4.7\mu F$ (Ceramic), Typical $T_A = 25^\circ C$, **Bold** typeface applies over $-40^\circ C \leq T_A \leq 85^\circ C$ ranges, unless otherwise specified (Note 3))

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_{OUT}	$V_{IN}=4.3V$, $1mA \leq I_{OUT} \leq 30mA$	$V_{OUT} \times 98.5\%$	3.3	$V_{OUT} \times 101.5\%$	V
Maximum Output Current	$I_{OUT(MAX)}$	$V_{IN}=4.3V$, $V_{OUT}=3.25V$ to $3.35V$	1.0			A
Load Regulation	$\frac{\Delta V_{OUT}/V_{OUT}}{\Delta I_{OUT}}$	$V_{IN}=4.3V$, $1mA \leq I_{OUT} \leq 1A$		0.2	1.0	%/A
Line Regulation	$\frac{\Delta V_{OUT}/V_{OUT}}{\Delta V_{IN}}$	$4.3V \leq V_{IN} \leq 6V$, $I_{OUT}=30mA$		0.02	± 0.1	%/V
Dropout Voltage	V_{DROP}	$I_{OUT}=1A$		450	750	mV
Quiescent Current	I_Q	$V_{IN}=4.3V$, $I_{OUT}=0mA$		65	90	μA
Power Supply Rejection Ratio	PSRR	Ripple 1Vp-p $V_{IN}=4.3V$, $I_{OUT}=100mA$	$f=100Hz$	65		dB
			$f=1KHz$	65		
Output Voltage Temperature Coefficient	$\frac{\Delta V_{OUT}/V_{OUT}}{\Delta T}$	$I_{OUT}=30mA$		± 30		ppm/ $^\circ C$
Short Current Limit	I_{SHORT}	$V_{OUT}=0V$		50		mA
RMS Output Noise	V_{NOISE}	$10Hz \leq f \leq 100kHz$ (No load)		30		μV_{RMS}
V_{EN} High Voltage	V_{IH}	Enable logic high, regulator on	1.5			V
V_{EN} Low Voltage	V_{IL}	Enable logic low, regulator off			0.4	
Standby Current	I_{STD}	$V_{IN}=3.5V$, V_{EN} in OFF mode		0.01	1.0	μA
Start-up Time	T_S	No Load		20		μs
EN Pull Down Resistor	RPD			3.0		m Ω
V_{OUT} Discharge Resistor	R_{DCHG}	Set EN pin at Low		60		Ω
Thermal Shutdown Temperature	T_{OTSD}			160		$^\circ C$
Thermal Shutdown Hysteresis	T_{HYOTSD}			25		
Thermal Resistance (Junction to Case)	θ_{JC}	SOIC-8		74.6		$^\circ C / W$
		PSOP-8		43.7		
		SOT-223		50.9		
		TO-252-2 (1) / TO-252-2 (3)		35		
		TO-263-3		22		

Note 2: To prevent the Short Circuit Current protection feature from being prematurely activated, the input voltage must be applied before a current source load is applied.

Note 3: Production testing at $T_A=25^\circ C$. Over temperature specifications guaranteed by design only.



1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2114

Typical Performance Characteristics

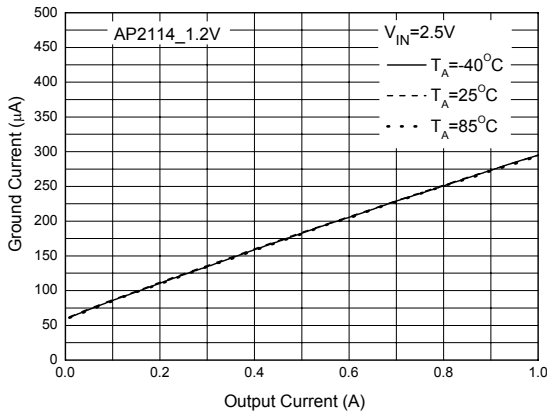


Figure 4. Ground Current vs. Output Current

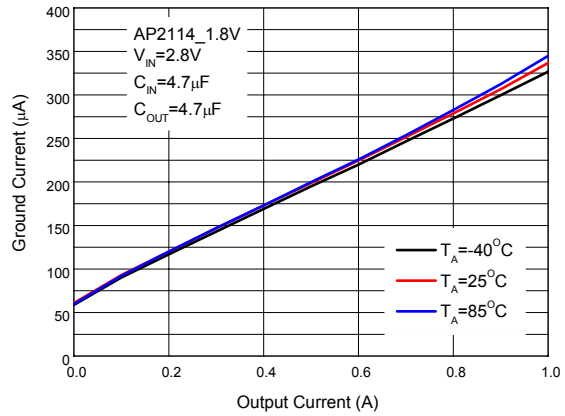


Figure 5. Ground Current vs. Output Current

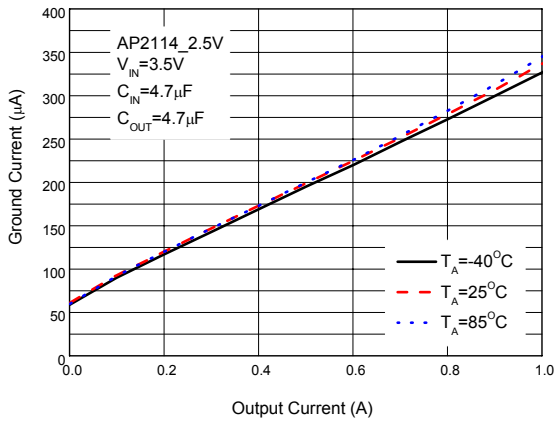


Figure 6. Ground Current vs. Output Current

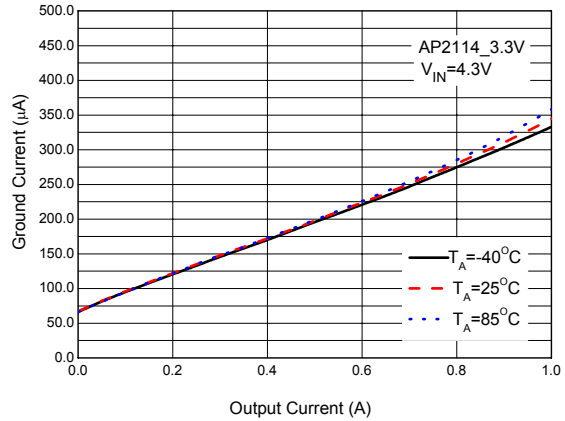


Figure 7. Ground Current vs. Output Current



1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2114

Typical Performance Characteristics (Continued)

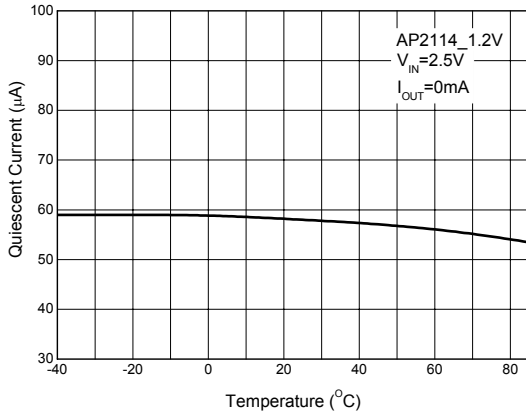


Figure 8. Quiescent Current vs. Temperature

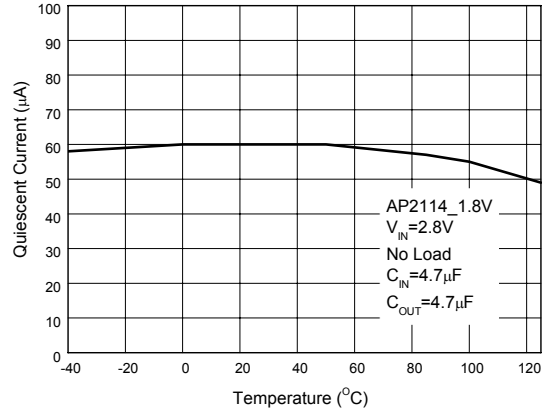


Figure 9. Quiescent Current vs. Temperature

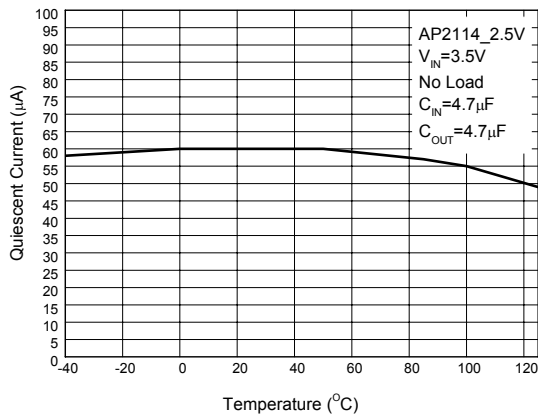


Figure 10. Quiescent Current vs. Temperature

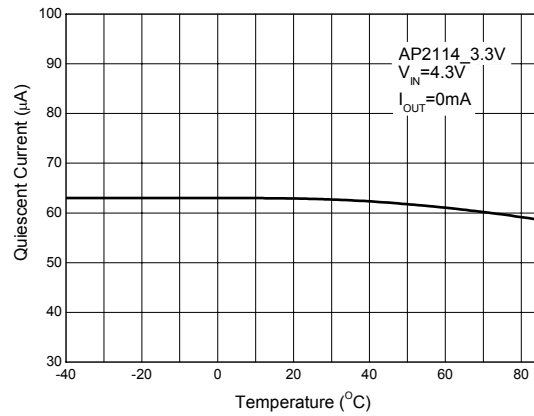


Figure 11. Quiescent Current vs. Temperature



1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2114

Typical Performance Characteristics (Continued)

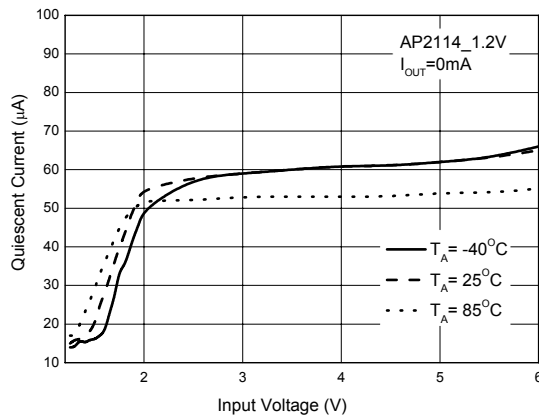


Figure 12. Quiescent Current vs. Input Voltage

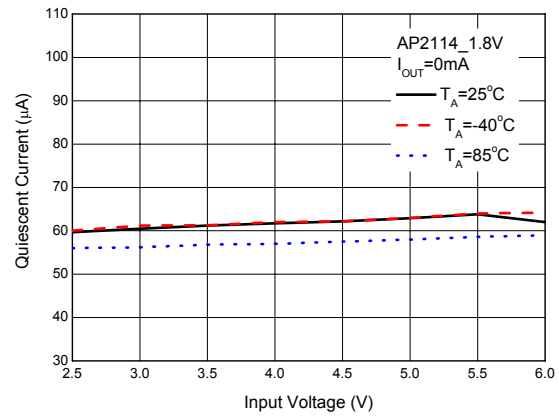


Figure 13. Quiescent Current vs. Input Voltage

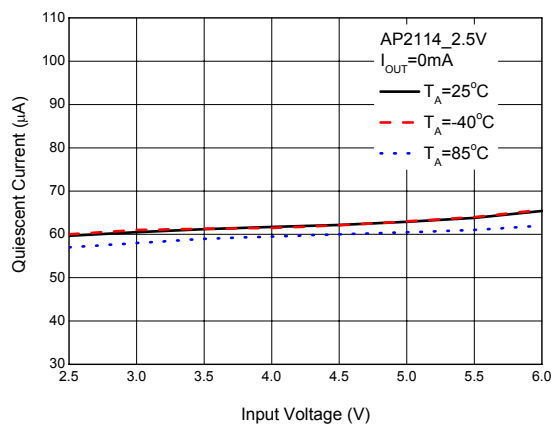


Figure 14. Quiescent Current vs. Input Voltage

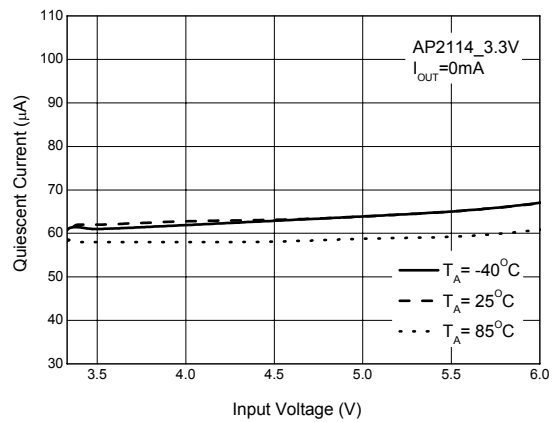


Figure 15. Quiescent Current vs. Input Voltage



1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2114

Typical Performance Characteristics (Continued)

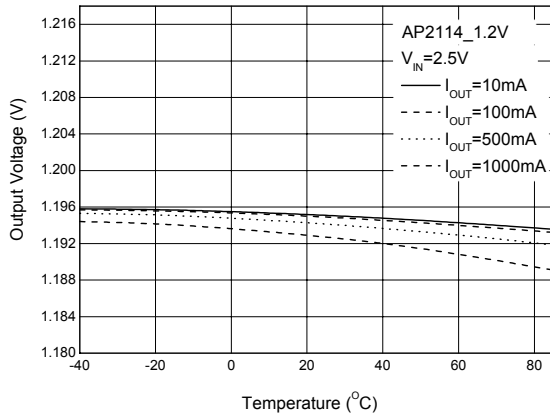


Figure 16. Output Voltage vs. Temperature

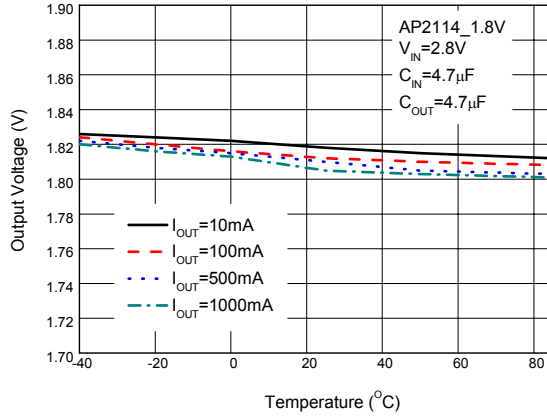


Figure 17. Output Voltage vs. Temperature

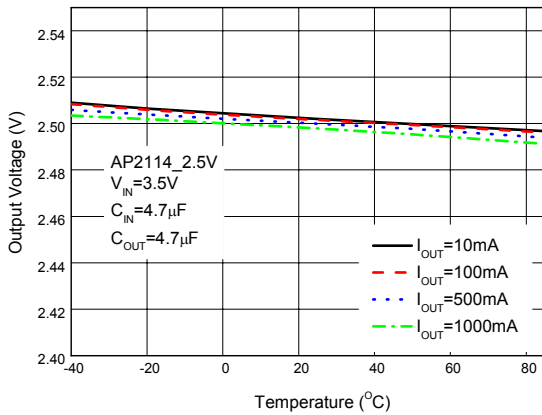


Figure 18. Output Voltage vs. Temperature

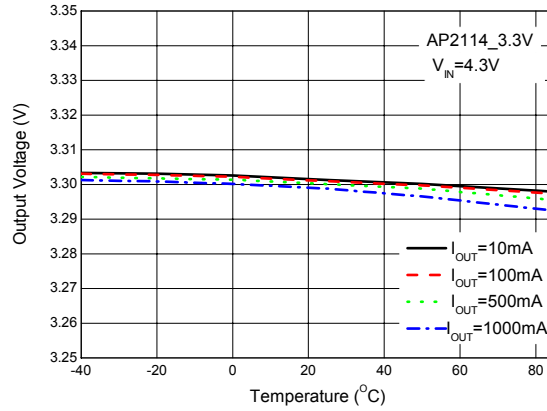


Figure 19. Output Voltage vs. Temperature

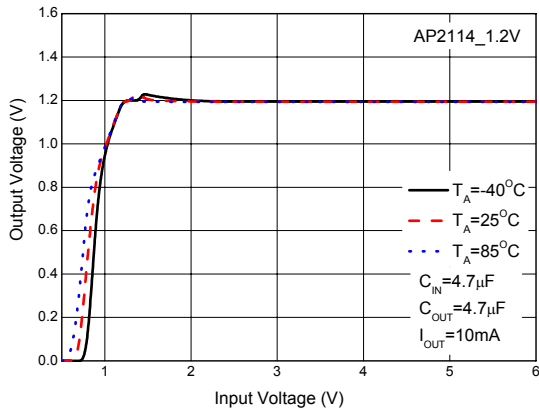
1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2114
Typical Performance Characteristics (Continued)


Figure 20. Output Voltage vs. Input Voltage

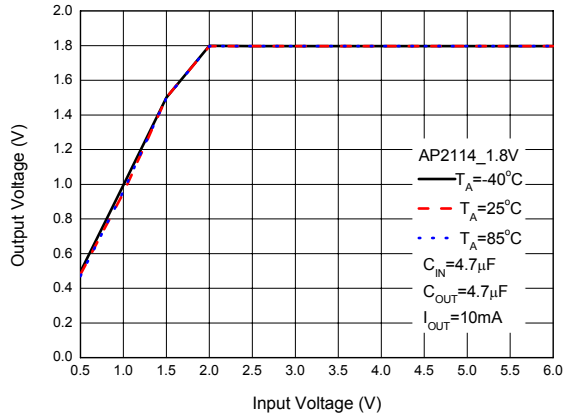


Figure 21. Output Voltage vs. Input Voltage

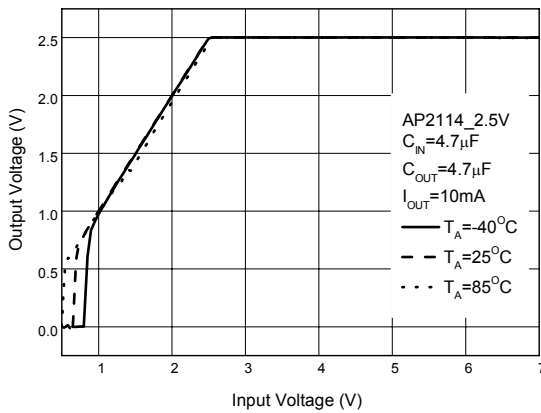


Figure 22. Output Voltage vs. Input Voltage

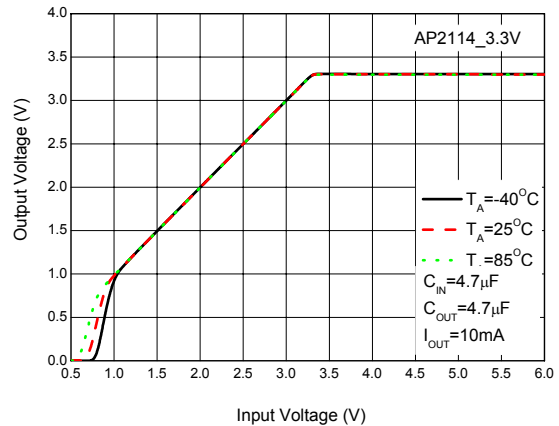


Figure 23. Output Voltage vs. Input Voltage



1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2114

Typical Performance Characteristics (Continued)

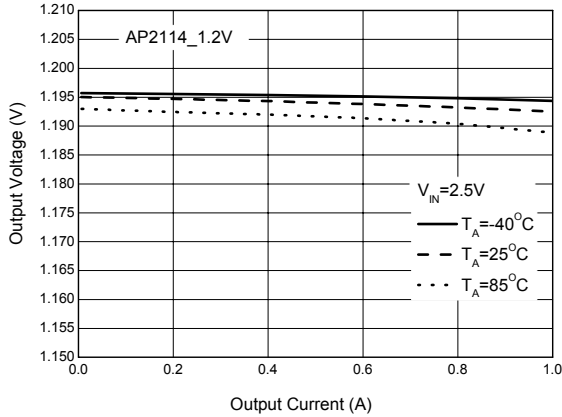


Figure 24. Output Voltage vs. Output Current

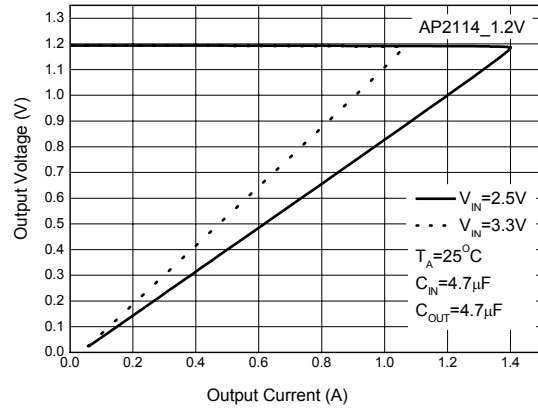


Figure 25. Output Voltage vs. Output Current

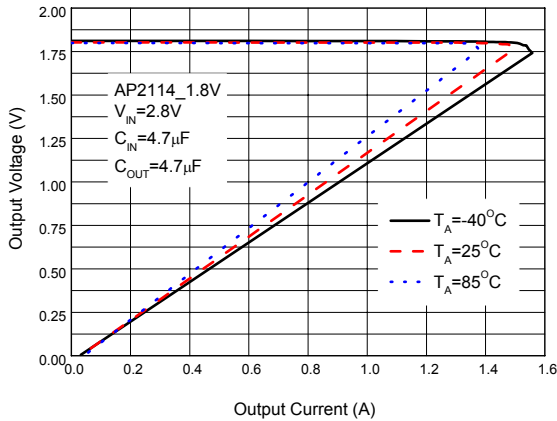


Figure 26. Output Voltage vs. Output Current

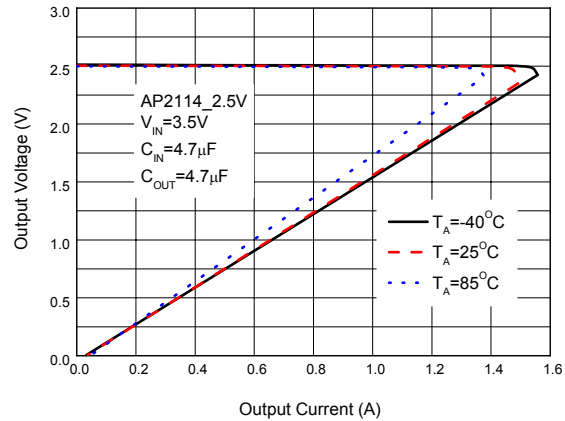


Figure 27. Output Voltage vs. Output Current



1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2114

Typical Performance Characteristics (Continued)

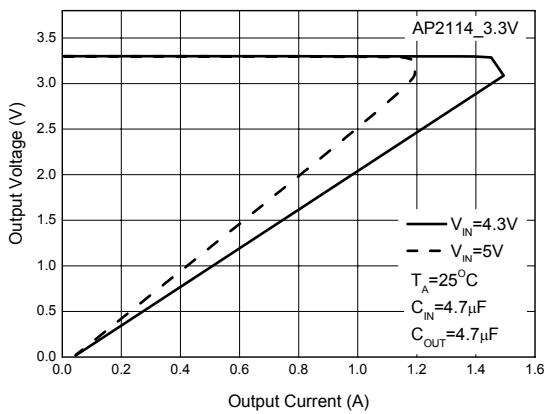


Figure 28. Output Voltage vs. Output Current

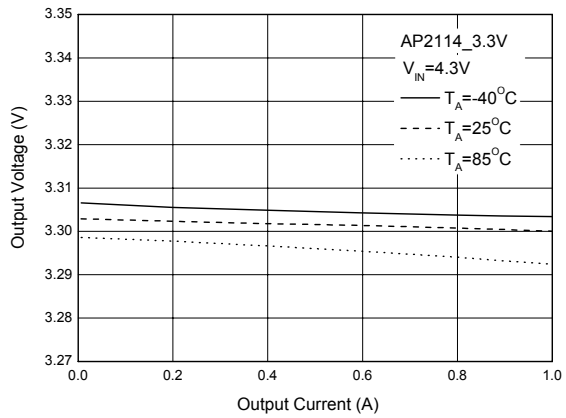


Figure 29. Output Voltage vs. Output Current

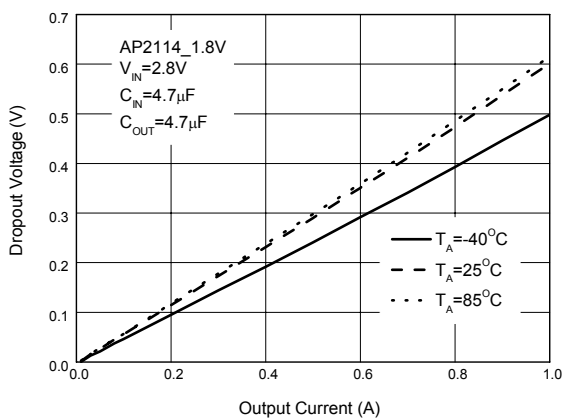


Figure 30. Dropout Voltage vs. Output Current

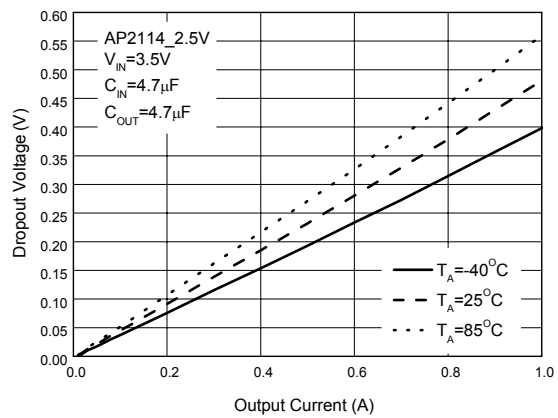


Figure 31. Dropout Voltage vs. Output Current



1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2114

Typical Performance Characteristics (Continued)

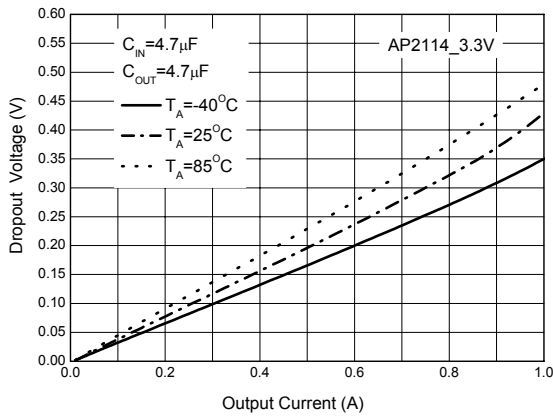


Figure 32. Dropout Voltage vs. Output Current

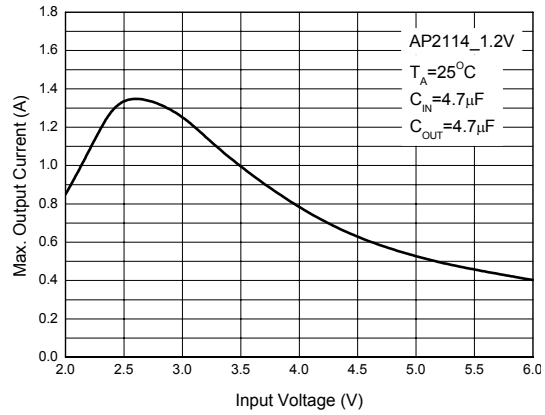


Figure 33. Max. Output Current vs. Input Voltage

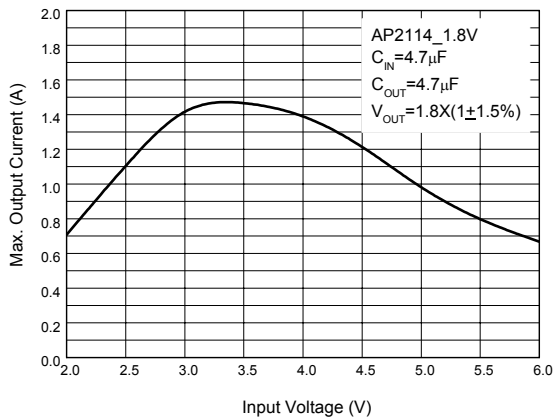


Figure 34. Max. Output Current vs. Input Voltage

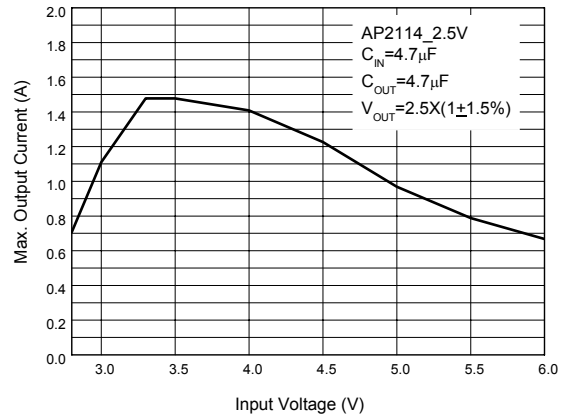


Figure 35. Max. Output Current vs. Input Voltage



1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2114

Typical Performance Characteristics (Continued)

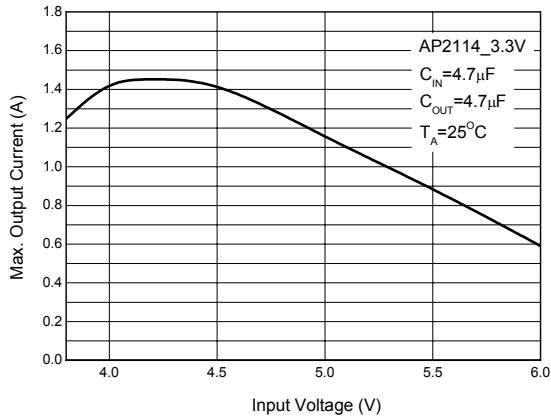


Figure 36. Max. Output Current vs. Input Voltage

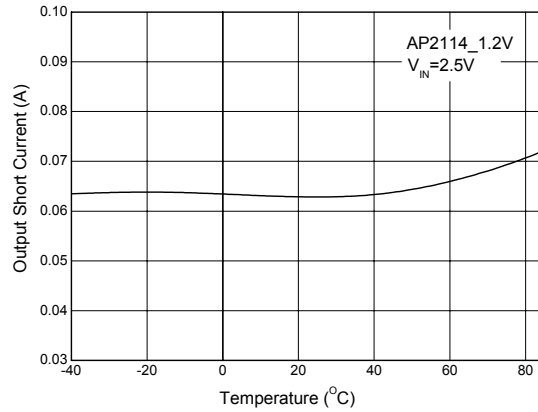


Figure 37. Output Short Current vs. Temperature

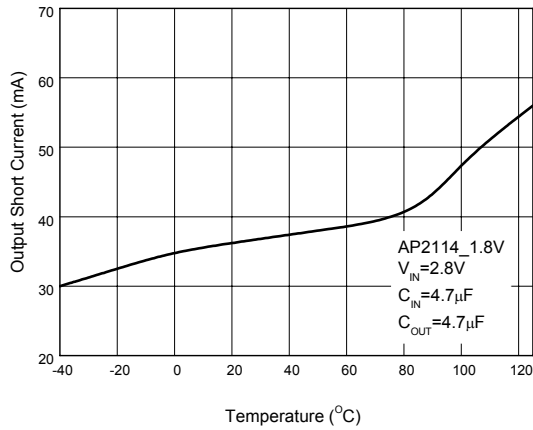


Figure 38. Output Short Current vs. Temperature

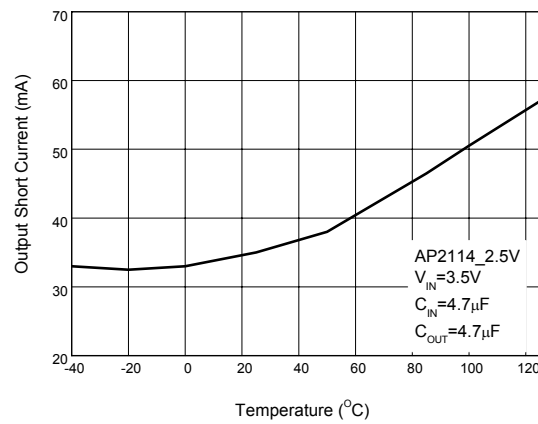


Figure 39. Output Short Current vs. Temperature



1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2114

Typical Performance Characteristics (Continued)

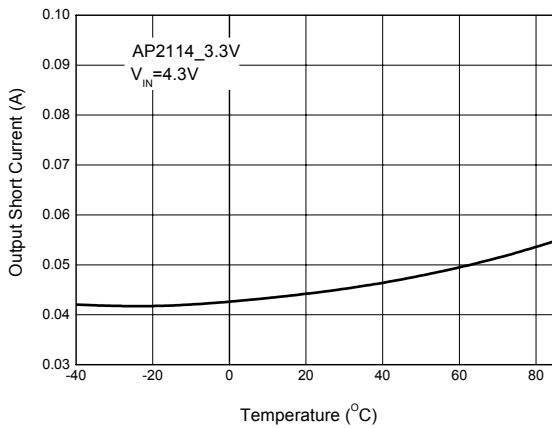


Figure 40. Output Short Current vs. Temperature

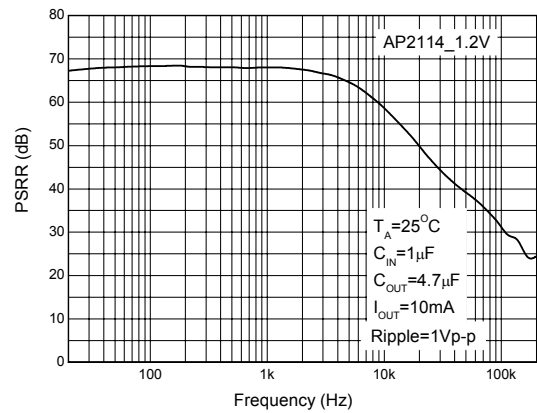


Figure 41. PSRR vs. Frequency

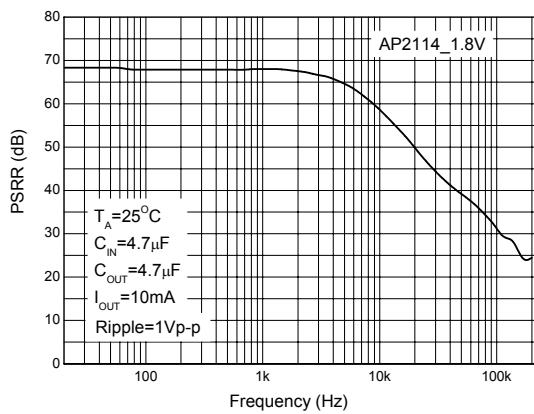


Figure 42. PSRR vs. Frequency

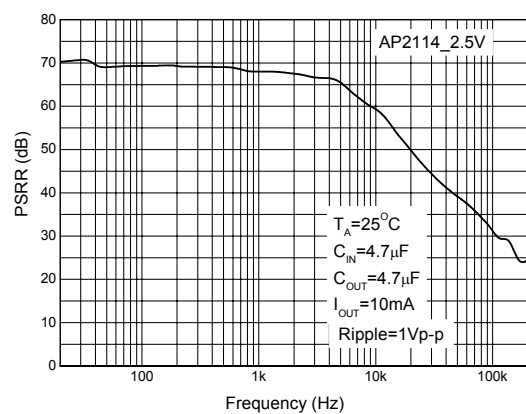


Figure 43. PSRR vs. Frequency

1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2114

Typical Performance Characteristics (Continued)

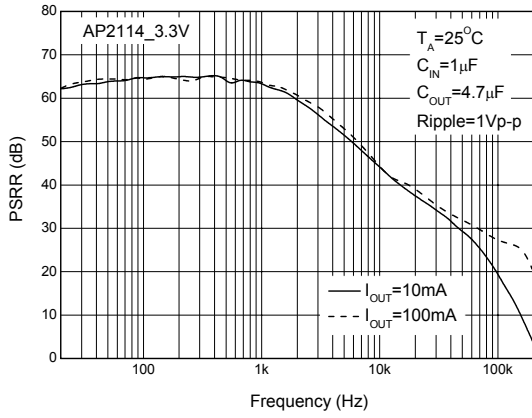


Figure 44. PSRR vs. Frequency

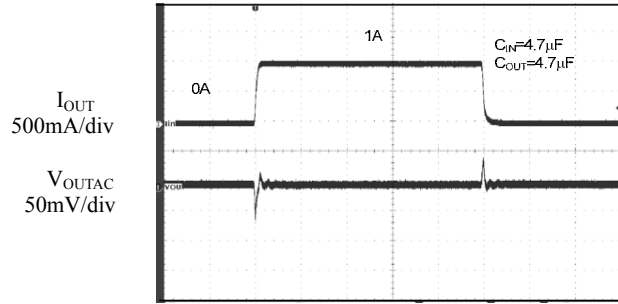


Figure 45. Load Transient

1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2114

Typical Application

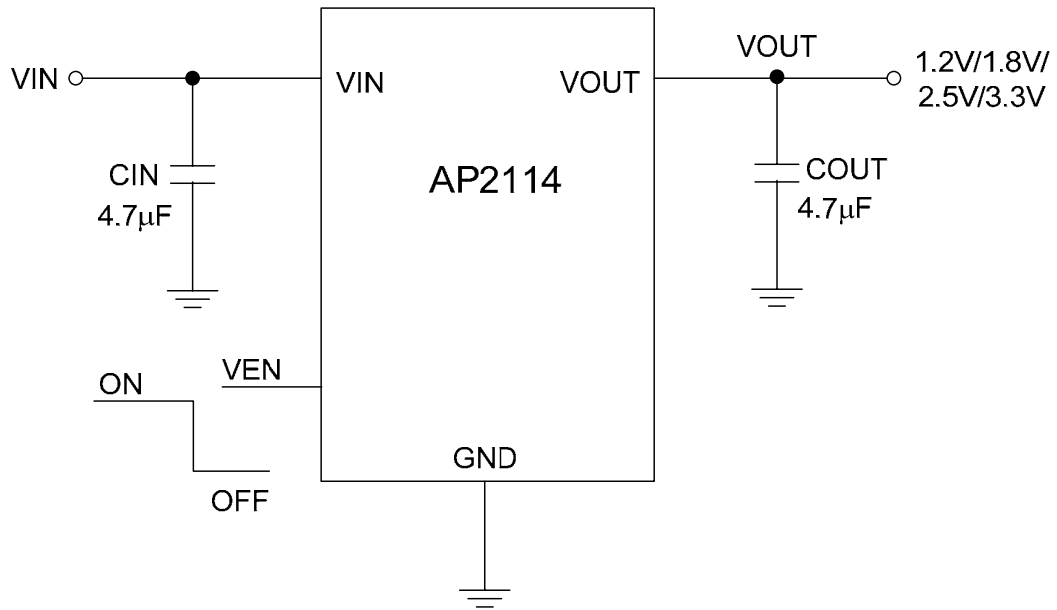


Figure 46. Typical Application of AP2114

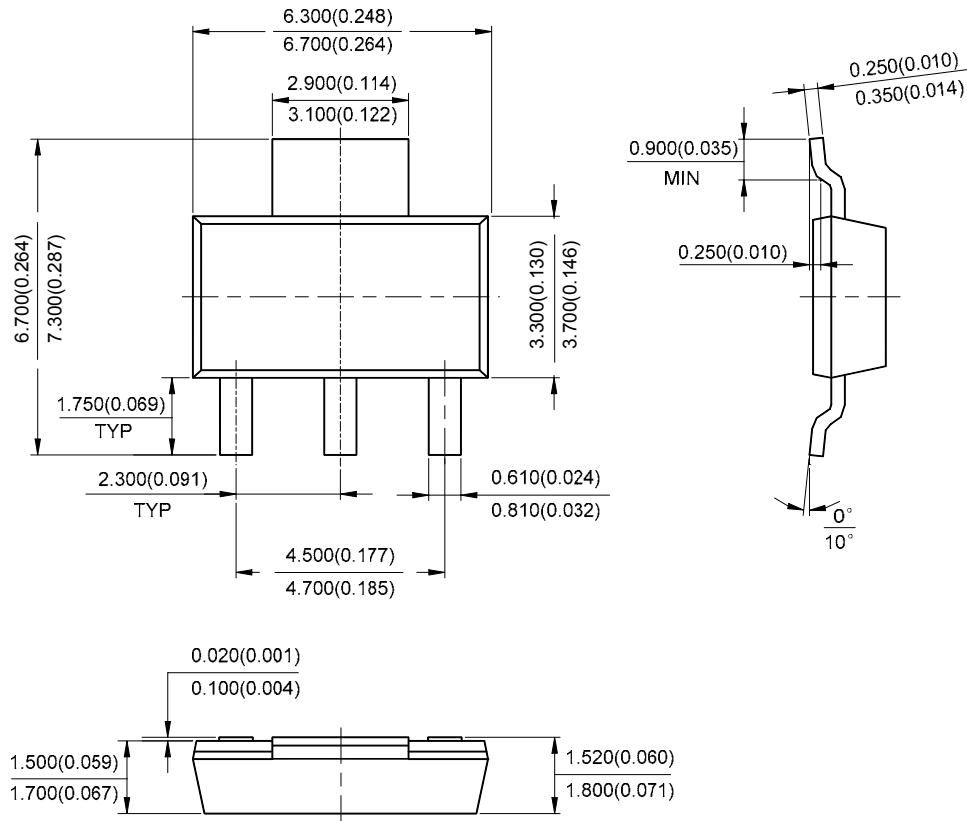


1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2114

Mechanical Dimensions

SOT-223

Unit: mm(inch)



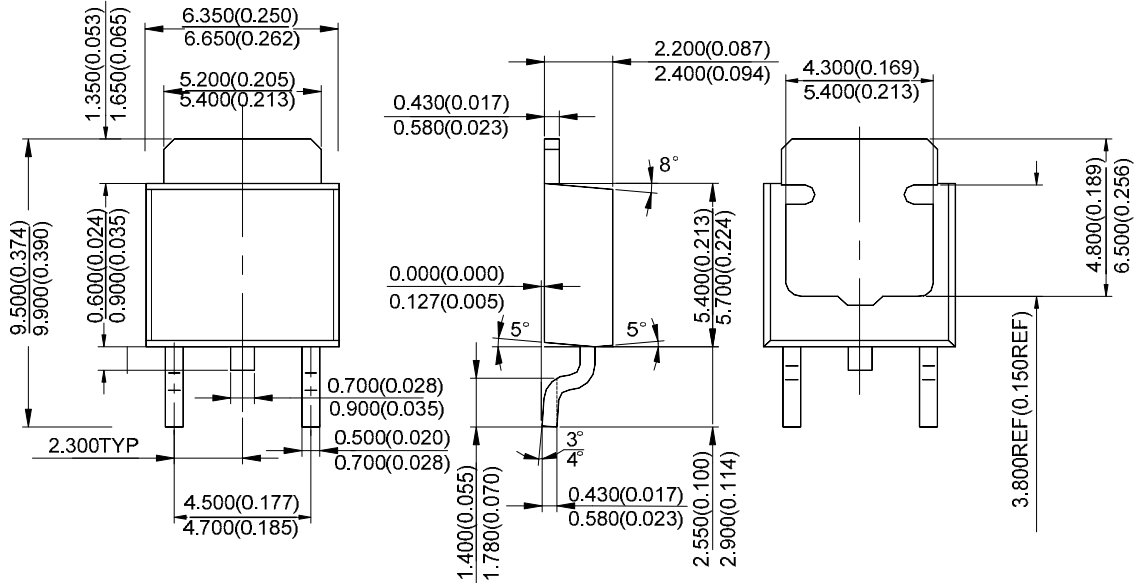


1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2114

Mechanical Dimensions (Continued)

TO-252-2 (1)

Unit: mm(inch)



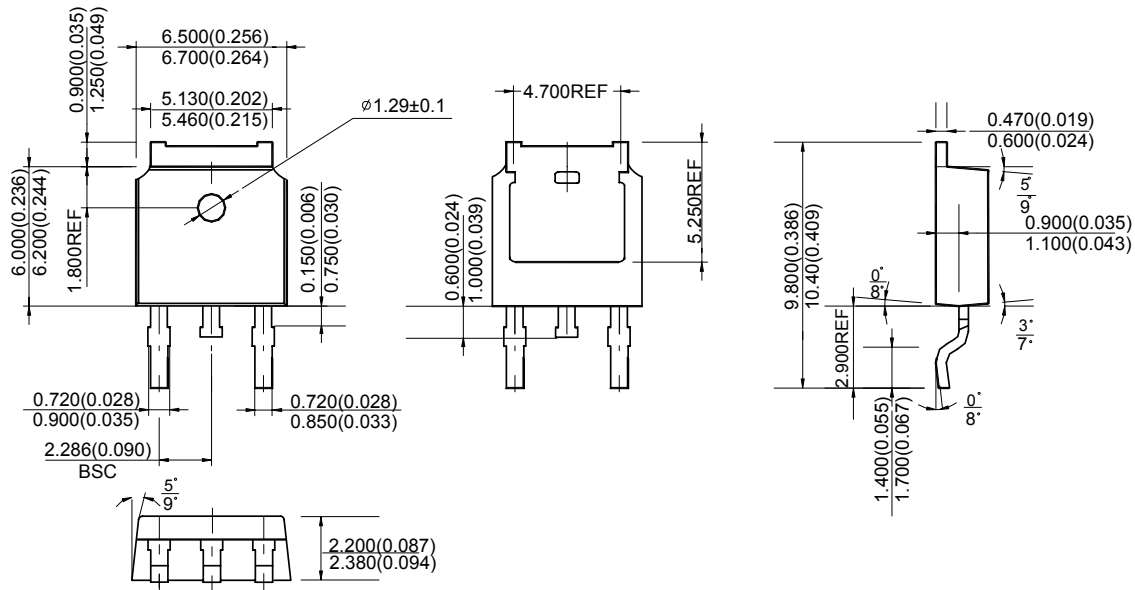


1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2114

Mechanical Dimensions (Continued)

TO-252-2 (3)

Unit: mm(inch)



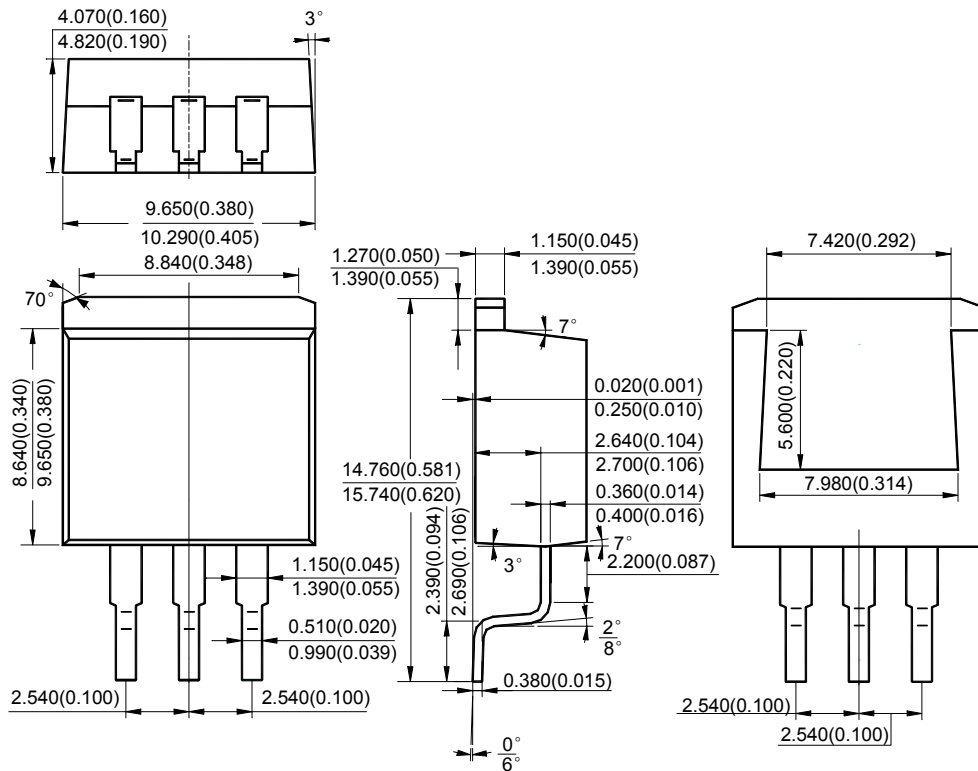


1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2114

Mechanical Dimensions (Continued)

TO-263-3

Unit: mm(inch)

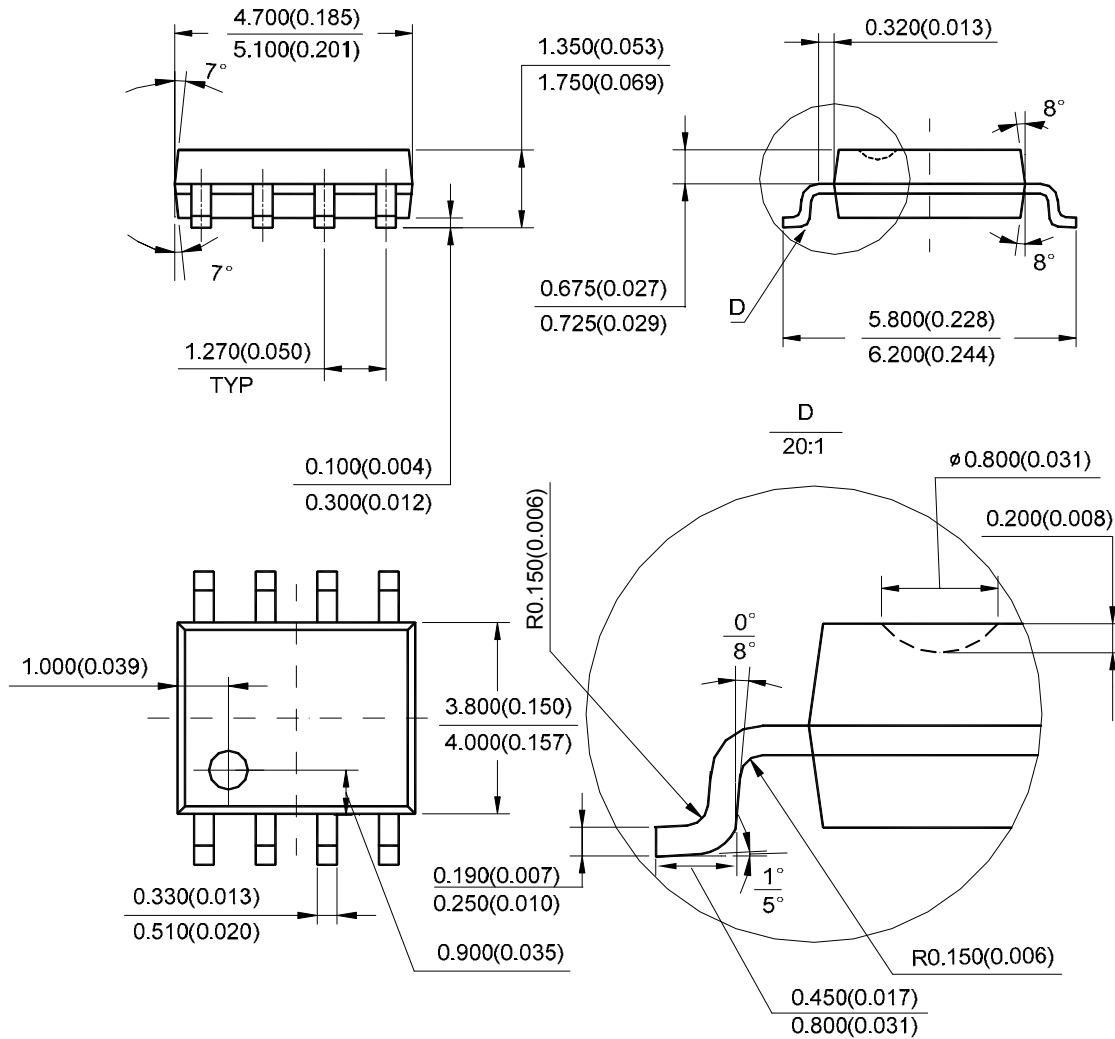


1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2114

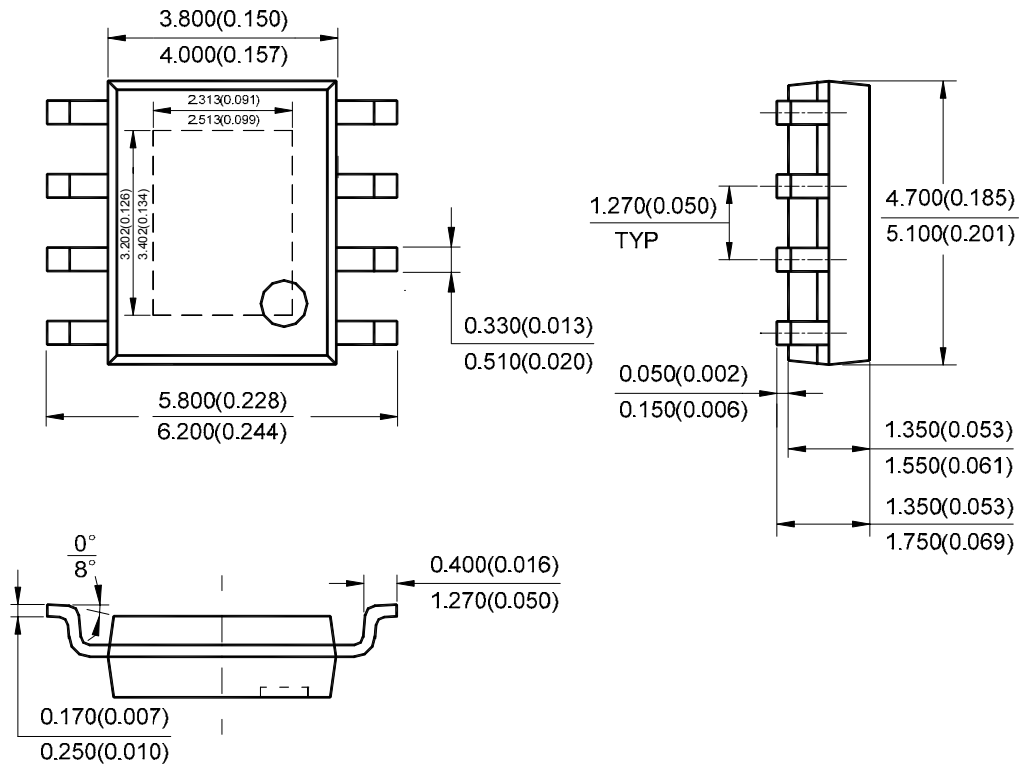
Mechanical Dimensions (Continued)

SOIC-8

Unit: mm(inch)



Note: Eject hole, oriented hole and mold mark is optional.

1A LOW NOISE CMOS LDO REGULATOR WITH ENABLE AP2114
Mechanical Dimensions (Continued)
PSOP-8
Unit: mm(inch)


Note: Eject hole, oriented hole and mold mark is optional.



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