FAIRCHILD SEMICONDUCTOR®

May 2008

SG6932
PFC / Forward PWM Controller

Features

- Interleaved PFC/PWM Switching
- Low Operating Current
- Innovative Switching-Charge Multiplier-divider
- Multi-vector Control for Improved PFC Output Transient Response
- Average Current Mode for Input-current Shaping
- PFC Over-voltage and Under-voltage Protections
- PFC and PWM Feedback Open-loop Protection
- Cycle-by-cycle Current Limiting for PFC/PWM
- Slope Compensation for PWM
- Selectable PWM Maximum Duty Cycle: 50%, 65%
- Brownout Protection
- Power-on Sequence Control and Soft-start

Applications

- Switch-mode Power Supplies with Active PFC
- Servo-system Power Supplies
- PC-ATX Power Supplies

Description

The highly integrated SG6932 is designed for power supplies with boost PFC and forward PWM. It requires very few external components to achieve versatile protections and compensation. It is available in 16-pin DIP and SOP packages.

The proprietary interleave-switching feature synchronizes the PFC and PWM stages and reduces switching noise. At light load, the switching frequency is continuously decreased to reduce power consumption.

For PFC stage, the proprietary multi-vector control scheme provides a fast transient response in a low-bandwidth PFC loop; in which the overshoot and undershoot of the PFC voltage are clamped. If the feedback loop is broken, SG6932 shuts off to prevent extra-high voltage on output.

For the forward PWM stage, the synchronized slope compensation ensures the stability of the current loop under continuous-conduction-mode (CCM) operation. Hiccup operation during output overloading is guaranteed. The soft-start and programmable maximum duty cycle ensure safe operation.

SG6932 provides complete protection functions, such as brownout protection and RI open/short latch off.

Ordering Information

Part Number	Operating Temperature Range	Package	Eco Status	Packing Method
SG6932DZ	-40°C to +85°C	16-pin Dual In-Line Package (DIP)	RoHS	Tube
SG6932SZ	-40°C to +85°C	16-pin Small Outline Package (SOP)	RoHS	Tape & Reel

For Fairchild's definition of "green" Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Application Diagram

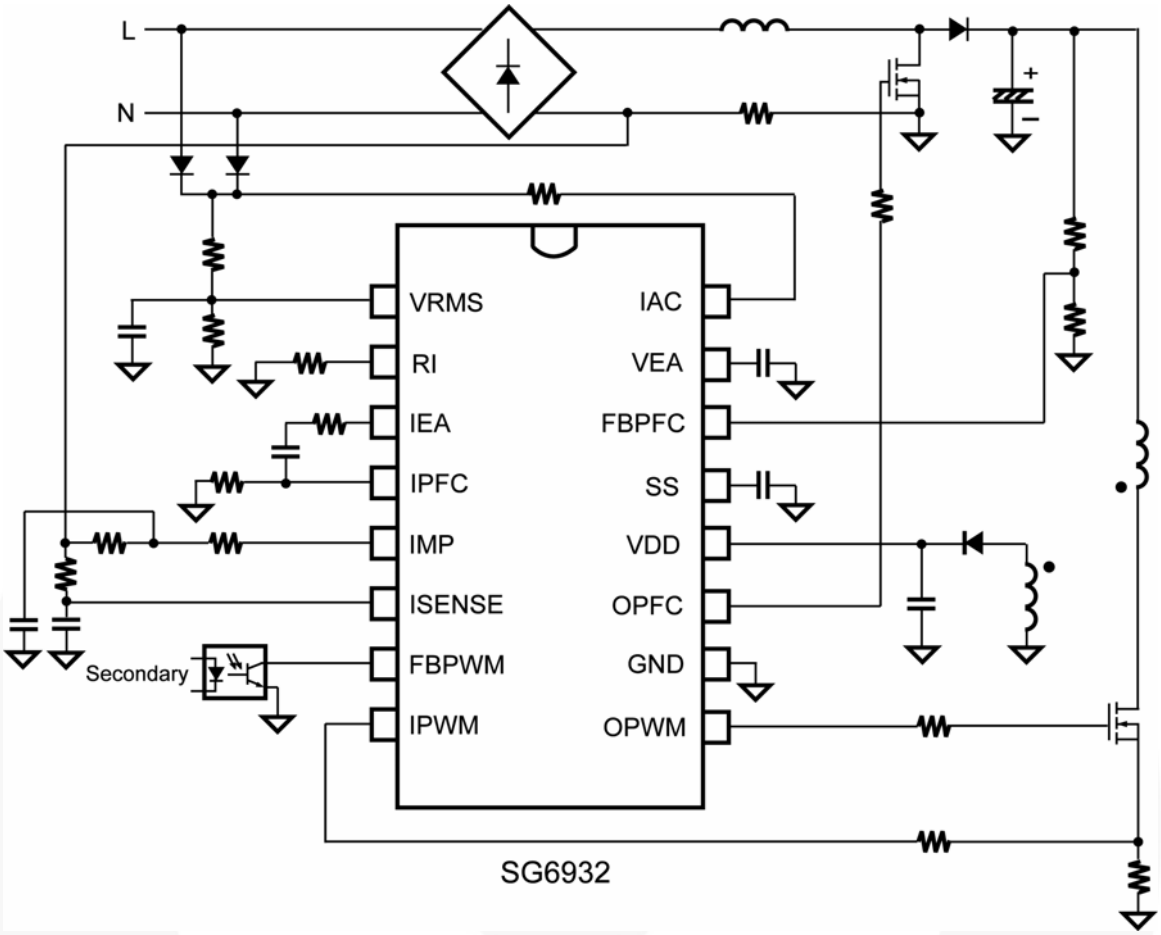


Figure 1. Typical Application

Block Diagram

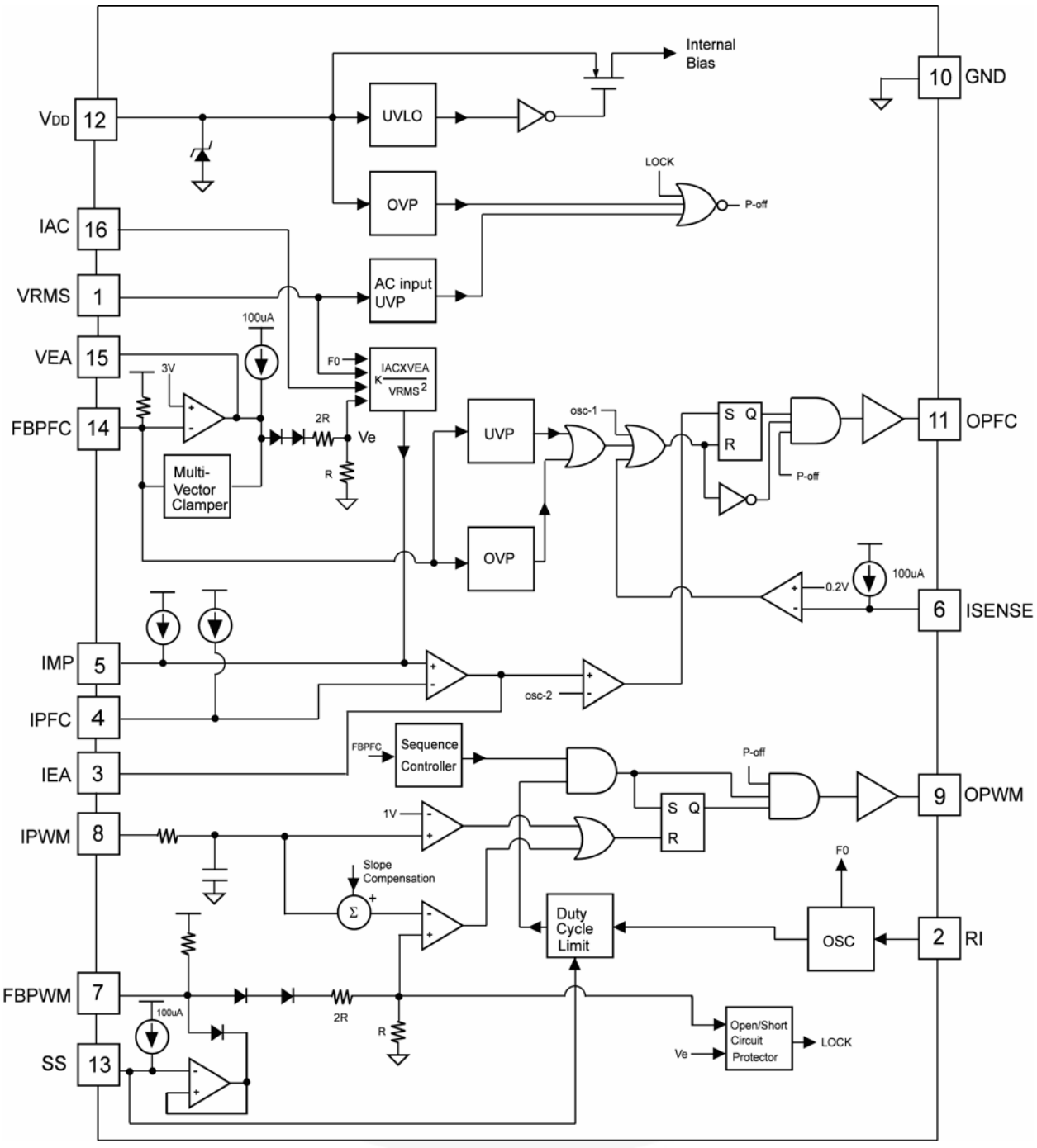
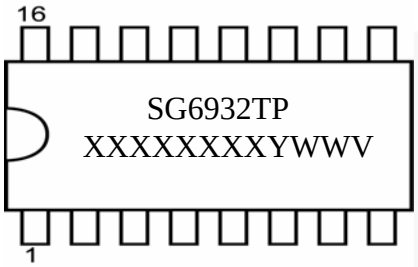


Figure 2. Function Block Diagram

Marking Information



T: D=DIP, S=SOP
P : Z =Lead Free + ROHS Compatible
XXXXXXXX: Wafer Lot
Y: Year; WW: Week
V: Assembly Location

Figure 3. Top Mark

Pin Configuration

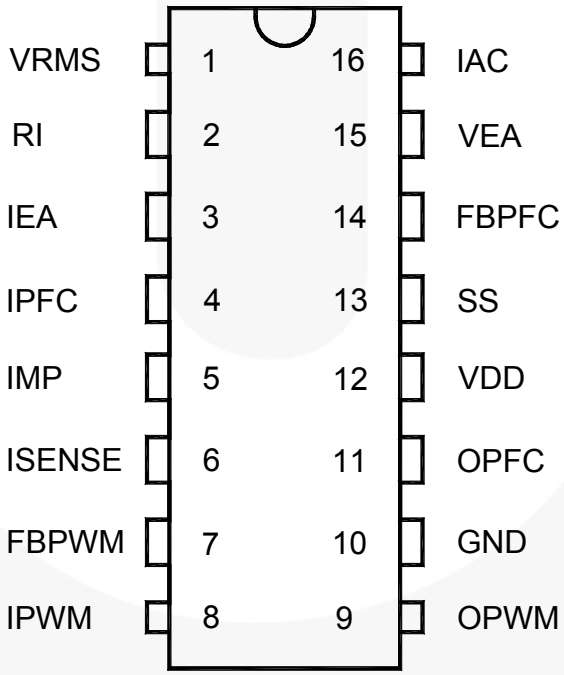


Figure 4. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	VRMS	**Line-Voltage Detection**. The pin is used for PFC multiplier and brownout protection.
2	RI	**Oscillator Setting**. One resistor connected between RI and ground determines the switching frequency. A resistor with resistance between 12 ~ 47kΩ is recommended. The switching frequency is equal to [1560 / R_I]kHz, where R_I is in kΩ. For example, if R_I is 24kΩ, the switching frequency is 65kHz.
3	IEA	**Output of PFC Current Amplifier**. The signal from this pin is compared with an internal sawtooth to determine the pulsewidth for PFC gate drive.
4	IPFC	**Inverting Input of PFC Current Amplifier**. Proper external compensation circuits result in excellent input power factor via average-current-mode control.
5	IMP	**Non-inverting Input of PFC Current Amplifier and Output of Multiplier**. Proper external compensation circuits result in excellent input power factor via average-current-mode control.
6	ISENSE	**Peak Current Limit Setting for PFC**.
7	FBPWM	**PWM Feedback Input**. The control input for voltage-loop feedback of PWM stage. It is internally pulled HIGH through a 6.5kΩ resistor. An external opto-coupler from the secondary feedback circuit is usually connected to this pin.
8	IPWM	**PWM Current Sense**. The current sense input for the PWM stage. Via a current sense resistor, this pin provides the control input for peak-current-mode control and cycle-by-cycle current limiting.
9	OPWM	**PWM Gate Drive**. The totem-pole output drive for PWM MOSFET. This pin is internally clamped under 18V to protect the MOSFET.
10	GND	**Ground.** The power ground.
11	OPFC	**PFC Gate Drive**. The totem-pole output drive for the PFC MOSFET. This pin is internally clamped under 18V to protect the MOSFET.
12	VDD	**Supply**. The power supply pin. The threshold voltages for start-up and turn-off are 14V and 10V, respectively. The operating current is lower than 10mA.
13	SS	**PWM Soft-Start**. During startup, the SS pin charges an external capacitor with a 50μA constant current source. The voltage on FBPWM is clamped by SS during startup. In the event of a protection condition occurring and/or PWM being disabled, the SS pin is quickly discharged. The voltage of SS pin can be used to select 50% or 65% maximum duty cycle.
14	FBPFC	**Voltage Feedback Input for PFC**. The feedback input for PFC voltage loop. The inverting input of PFC error amplifier. This pin is connected to the PFC output through a divider network.
15	VEA	**Error Amplifier Output for PFC Voltage Feedback Loop**. A compensation network (usually a capacitor) is connected between this pin and ground. A large capacitor value results in a narrow bandwidth and improves the power factor.
16	IAC	**Input AC Current**. For normal operation, this input is used to provide current reference for the multiplier. The suggested maximum I_{AC} is 360μA.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. All voltage values, except differential voltage, are given with respect to GND pin. Stresses beyond those listed under “absolute maximum ratings “may cause permanent damage to the device.

Symbol	Parameter		Min.	Max.	Unit
V_{DD}	DC Supply Voltage			25	V
I_{AC}	Input AC Current			2	mA
V_{HIGH}	OPWM, OPFC, IAC		-0.5	25.0	V
V_{LOW}	Others		-0.5	7.0	V
P_D	Power Dissipation (T_A<50°C)			0.8	W
T_J	Operating Junction Temperature		-40	+125	°C
T_{STG}	Storage Temperature Range		-55	+150	°C
θ_{JC}	Thermal Resistance (Junction-to-Case)	DIP		33.64	°C/W
		SOP		41.95	
T_L	Lead Temperature (Wave Soldering, 10 Seconds)			+260	°C
ESD	Electrostatic Discharge Capability, Human Body Model: JESD22-A114			4.5	KV
	Electrostatic Discharge Capability, Machine Model: JESD22-A115			250	V

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Ambient Temperature	-40		+85	°C

Electrical Characteristics

V_{DD}=15V, T_A= 25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD} Section						
V_{DD-OP}	Continuously Operating Voltage				20	V
$I_{DD\ ST}$	Start-Up Current	V_{DD} – 0.16V		10	20	µA
I_{DD-OP}	Operating Current	V_{DD} = 15V; OPFC OPWM open		6	10	mA
V_{TH-ON}	Start Threshold Voltage		13	14	15	V
V_{DD-min}	Minimum Operating Voltage		9	10	11	V
V_{DD-OVP}	V_{DD} OVP1 (Turn Off PWM with Delay)		23.4	24.5	25.5	V
$t_{VDD-OVP}$	Delay Time of V_{DD} OVP1	R_I=24kΩ	8		25	µs
Oscillator						
V_{RI}	RI Voltage		1.176	1.200	1.224	V
f_{OSC}	PWM Frequency	R_I=24kΩ	62	65	68	kHz
RI	RI Range		12		47	kΩ
RI_{OPEN}	RI Pin Open Protection	If RI > RI_{OPEN}, PWM Turned Off		200		kΩ
RI_{SHORT}	RI Pin Short Protection	If RI > RI_{SHORT}, PWM Turned Off		2		kΩ
V_{RMS} for UVP and ON/OFF						
$V_{RMS-UVP-1}$	RMS AC Voltage Under-Voltage Threshold to Turn Off PFC (with T_{UVP} Delay) for UVP Mode1		0.75	0.80	0.85	V
$V_{RMS-UVP-2}$	Recovery Level on V_{RMS} for UVP		$V_{RMS-UVP-1}$ +0.17	$V_{RMS-UVP-1}$ +0.19	$V_{RMS-UVP-1}$ +0.21	V
t_{UVP}	Under-Voltage Protection to Turn Off PFC Delay Time (No Delay for Start-up)	R_I=24kΩ	150	195	240	ms
PFC Stage						
Voltage Error Amplifier						
V_{REF}	Reference Voltage		2.95	3.00	3.05	V
A_V	Open-Loop Gain			60		dB
Z_o	Output Impedance			110		kΩ
OVP_{FBPFC}	PFC Over-Voltage Protection		3.20	3.25	3.30	V
△ OVP_{FBPFC}	PFC Feedback Voltage Protection Hysteresis		60	90	120	mV
$V_{FBPFC-H}$	Clamp-High Feedback Voltage		3.10	3.15	3.20	V
$G_{FBPFC-H}$	Clamp-High Gain			0.5		mA/V
$V_{FBPFC-L}$	Clamp-Low Feedback Voltage		2.75	2.85	2.90	V
$G_{FBPFC-L}$	Clamp-Low Gain			6.5		mA/V
$I_{FBPFC-L}$	Maximum Source Current		1.5	2.0		mA
$I_{FBPFC-H}$	Maximum Sink Current		70	110		µA
UVP_{VFB}	PFC Feedback Under-Voltage Protection		0.35	0.40	0.45	V
$V_{OFF-FBPFC}$	Voltage Level on FBPFC to Disable OPWM		2.15	2.20	2.25	V

Continued on following page…

Electrical Characteristics (Continued)

V_{DD}=15V, T_A= 25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{FBHIGH}	Output High Voltage on V_{EA}		6	7	8	V
$V_{RD-FBPFC}$	Voltage Level on FBPFC to Enable OPWM During Start-up		2.6	2.7	2.8	V
t_{UVP_PFC}	Debounce Time of PFC UVP		40	70	120	μs
Current Error Amplifier						
V_{OFFSET}	Input Offset Voltage ((-) > (+))			8		mV
A_I	Open-loop Gain			60		dB
BW	Unit Gain Bandwidth			1.5		MHz
CMRR	Common-Mode Rejection Ratio	V_{CM}=0~1.5V		70		dB
$V_{OUT-HIGH}$	Output HIGH Voltage		3.2			V
$V_{OUT-LOW}$	Output LOW Voltage				0.2	V
I_{MR1}, I_{MR2}	Reference Current Source	R_I=24kΩ (I_{MR}=20+I_{RI}•0.8)	50		70	μA
I_L	Maximum Source Current			3		mA
I_H	Maximum Sink Current			0.25		mA
Peak Current Limit						
I_P	Constant Current Output	R_I=24kΩ	90	100	110	μA
V_{pk}	Peak Current Limit Threshold Voltage Cycle-by-Cycle Limit (V_{sense} < V_{pk})	V_{RMS}=1.05V	0.15	0.20	0.25	V
		V_{RMS}=3V	0.35	0.40	0.45	
t_{pkD}	Propagation Delay				200	ns
t_{Bnk}	Leading-Edge Blanking Time		270	350	450	ns
Multiplier						
I_{AC}	Input AC Current	Multiplier Linear Range	0		360	μA
I_{MO-max}	Maximum Multiplier Current Output	R_I=24kΩ		230		μA
I_{MO-1}	Multiplier Current Output (Low-Line, High-Power)	V_{RMS}=1.05V; I_{AC}=90μA; V_{EA}=7.5V; R_I=24kΩ	200	230	280	μA
I_{MO-2}	Multiplier Current Output (High-Line, High-Power)	V_{RMS}=3V; I_{AC}=264μA; V_{EA}=7.5V; R_I=24kΩ	65	85		μA
V_{IMP}	Voltage of IMP Open		3.4	3.9	4.4	V
PFC Output Driver						
V_{Z-PFC}	Output Voltage Maximum (Clamp)	V_{DD}=20V		16	18	V
V_{OL-PFC}	Output Voltage Low	V_{DD}=15V; I_O=100mA			1.5	V
V_{OH-PFC}	Output Voltage High	V_{DD}=13V; I_O=100mA	8			V
t_{R-PFC}	Rising Time	V_{DD}=15V; C_L=5nF; O/P= 2V to 9V	40	70	120	ns
t_{F-PFC}	Falling Time	V_{DD}=15V; C_L=5nF; O/P= 9V to 2V	40	60	110	ns
DC_{MAX}	Maximum Duty Cycle		93		97	%

Continued on following page…

Electrical Characteristics (Continued)

V_{DD}=15V, T_A= 25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
PWM Stage						
FBPWM						
A_V	FB to current Comparator Attenuation		2.2	2.7	3.2	V/V
Z_{FB}	Input Impedance		4	5	7	kΩ
$FB_{OPEN-LOOP}$	PWM Open-Loop Protection Voltage		4.2	4.5	4.8	V
$t_{OPEN-PWM-Hiccup}$	Interval of PWM Open-Loop Protection Reset	R_I=24kΩ	500	600	700	ms
$t_{OPEN-PWM}$	PWM Open-Loop Protection Delay Time	R_I=24kΩ	80	95	120	ms
V_N	Frequency Reduction Threshold on FBPWM		1.9	2.1	2.3	V
PWM Current Sense						
t_{PD-PWM}	Propagation Delay to Output – V_{LIMIT} Loop	V_{DD}=15V, OPWM Drops to 9V	60		120	ns
V_{LIMIT}	Peak Current Limit Threshold Voltage		0.65	0.70	0.75	V
$t_{Bnk-PWM}$	Leading-Edge Blanking Time		270	350	450	ns
$\triangle V_{SLOPE}$	Slope Compensation $\triangle V_S = \triangle V_{SLOPE}(t_{on}/t)$ $\triangle V_S$: Compensation Voltage Added to Current Sense		0.40	0.45	0.55	V
Output Driver						
V_{Z-PWM}	Output Voltage Maximum (Clamp)	V_{DD}=20V		16	18	V
V_{OL-PWM}	Output Voltage Low	V_{DD}=15V; I_O=100mA			1.5	V
V_{OH-PWM}	Output Voltage High	V_{DD}=13V; I_O=100mA	8			V
t_{R-PWM}	Rising Time	V_{DD}=15V; C_L=5nF; O/P=2V to 9V	30	60	120	ns
t_{F-PWM}	Falling Time	V_{DD}=15V; C_L=5nF; O/P=9V to 2V	30	50	110	ns
Maximum Duty Cycle						
$DC_{SS=6V}$	Maximum Duty Cycle for SS=6V	R_I=24kΩ	62		66	%
$DC_{SS=5V}$	Maximum Duty Cycle for SS=5V	R_I=24kΩ	46		50	%
Soft Start						
I_{SS}	Constant Current Output for Soft-Start	R_I=24kΩ	44	50	56	μA
$V_{DC-MAX-50\%}$	Voltage of SS for 50% Maximum Duty Cycle				5	V
$V_{DC-MAX-65\%}$	Voltage of SS for 65% Maximum Duty Cycle		6			V
R_D	Discharge Resistance			470		Ω

Typical Characteristics

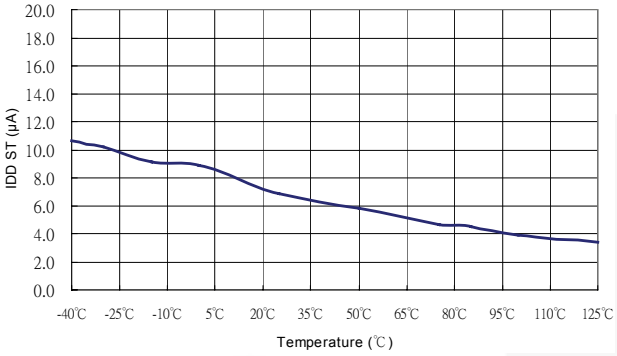


Figure 5. Startup (I_{DD-ST}) vs. Temperature

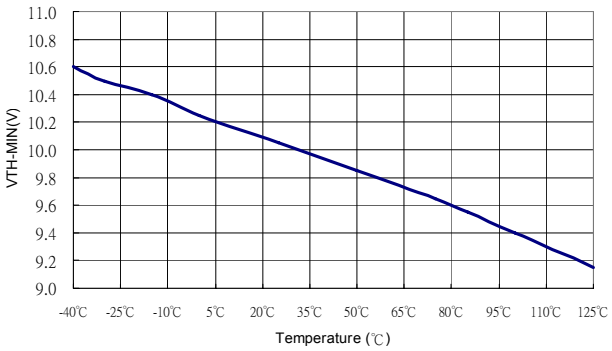


Figure 6. Minimum Operation Voltage (V_{DD-MIN}) vs. Temperature

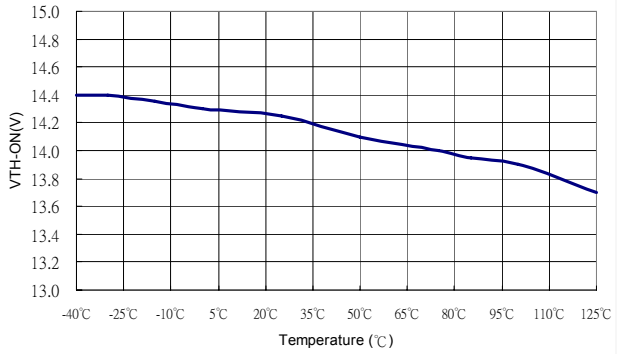


Figure 7. Start Threshold Voltage (V_{TH-ON}) vs. Temperature

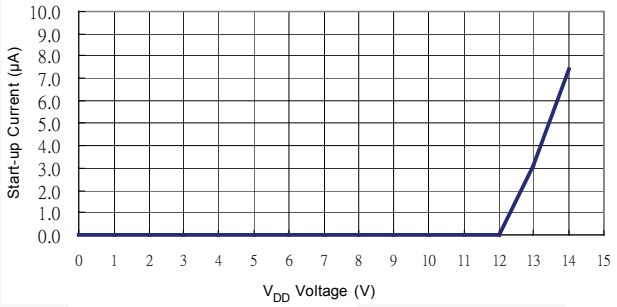


Figure 8. Startup Current vs. V_{DD} Voltage

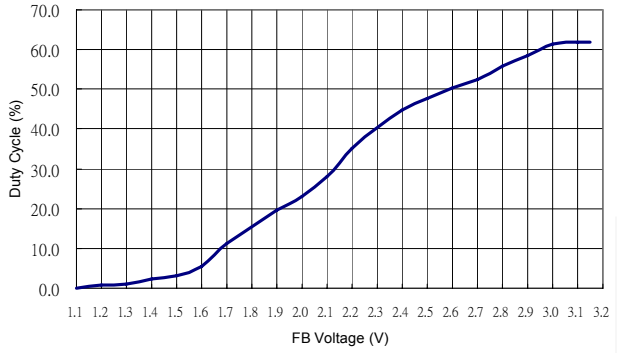


Figure 9. Duty Cycle vs. FB Voltage

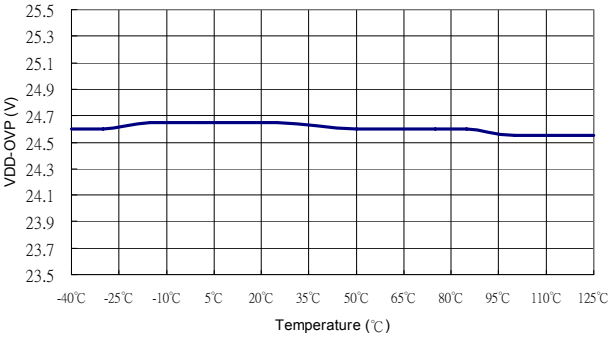


Figure 10. V_{DD} OVP Threshold vs. Temperature

Typical Characteristics (Continued)

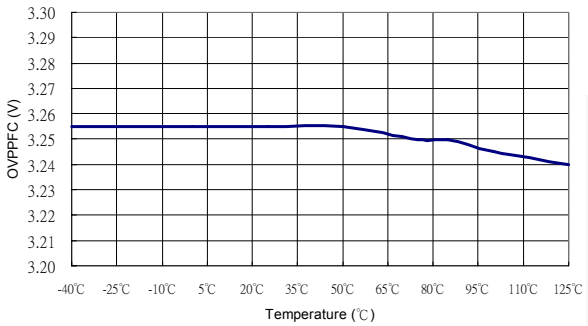


Figure 11. PFC Over-voltage Protection vs. Temperature

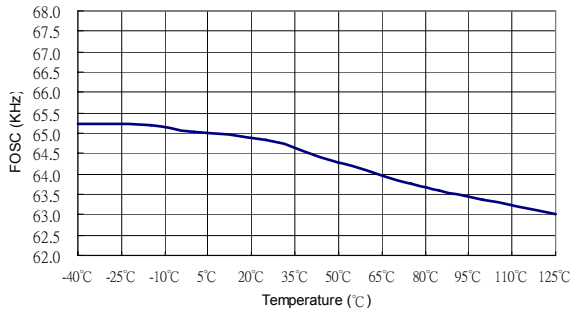


Figure 12. PWM Frequency (f_{OSC}) vs. Temperature

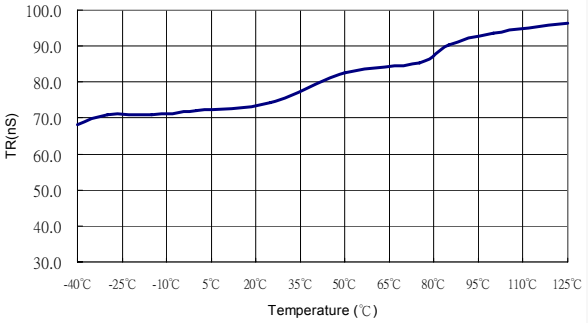


Figure 13. Rising Time vs. Temperature

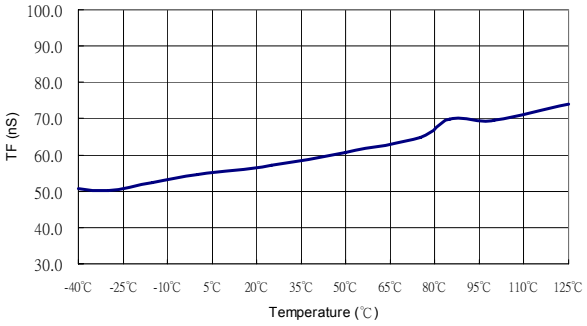


Figure 14. Falling Time vs. Temperature

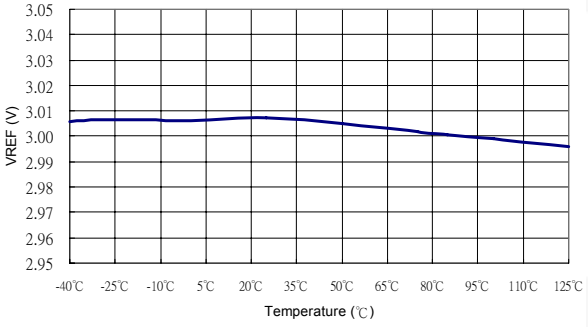


Figure 15. Reference Voltage vs. Temperature

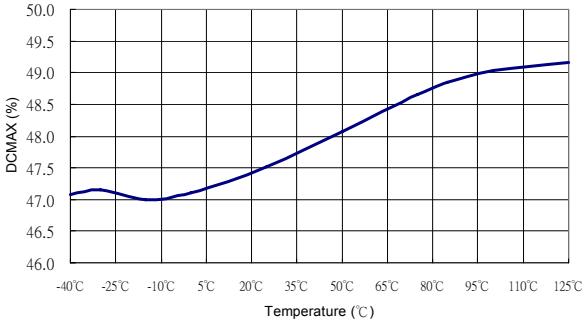


Figure 16. Maximum Duty Cycle (SS=5V) vs. Temperature

Typical Characteristics (Continued)

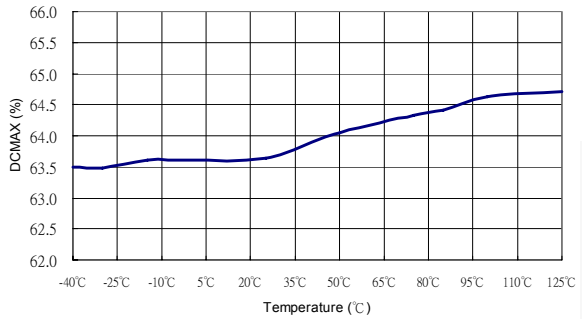


Figure 17. Maximum Duty Cycle (SS=6V) vs. Temperature

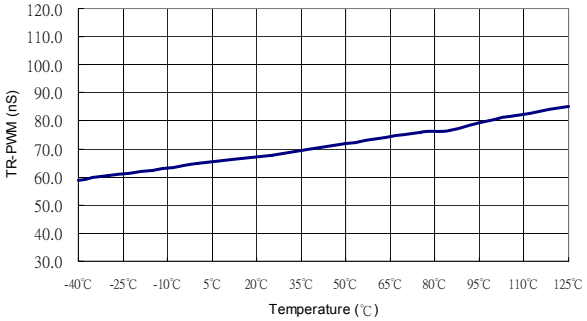


Figure 18. Rising Time vs. Temperature

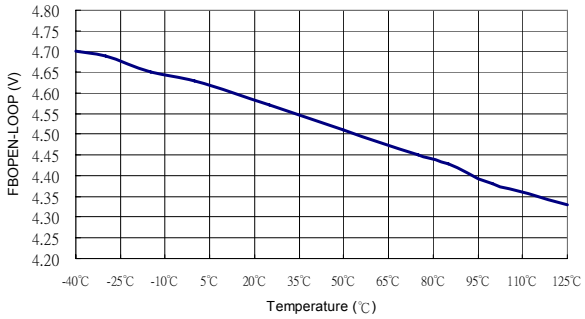


Figure 19. PWM Open-Loop Protection Voltage vs. Temperature

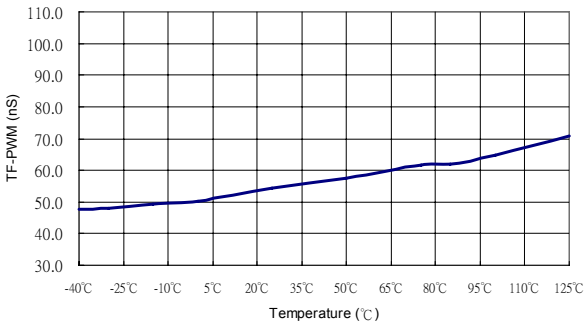


Figure 20. Fall Time vs. Temperature

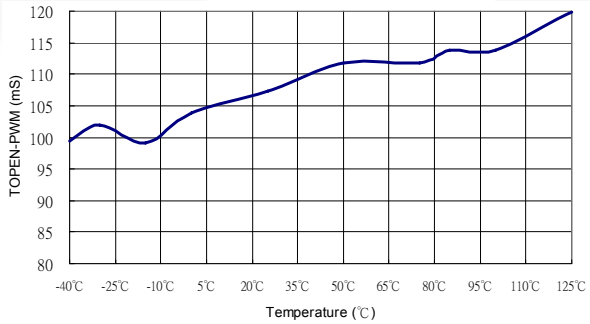


Figure 21. PWM Open-Loop Protection Delay Time vs. Temperature

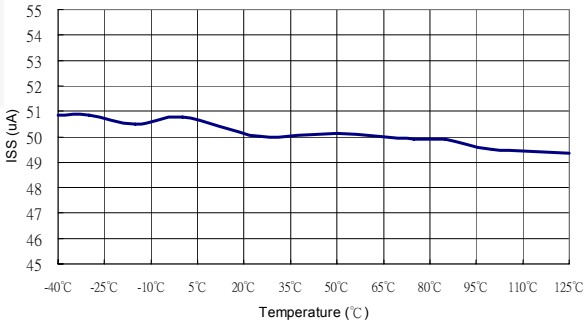


Figure 22. Constant Current Output for Soft-start vs. Temperature

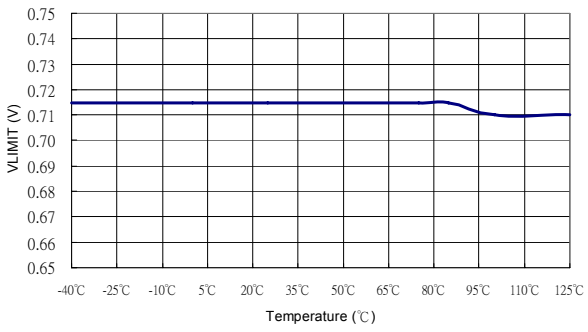


Figure 23. Peak Current Limit Threshold Voltage vs. Temperature

Functional Description

The highly integrated SG6932 is designed for power supplies with boost PFC and forward PWM. It requires very few external components to achieve versatile protections and compensation.

The proprietary interleave-switching feature synchronizes the PFC and PWM stages and reduces switching noise. At light load, the switching frequency is linearly decreased to reduce power consumption.

The PFC function is implemented by average-current-mode control. The proprietary switching charge multiplier-divider provides a high degree of noise immunity for the PFC circuit. This enables the PFC circuit to operate over a much wider region. The proprietary multi-vector output voltage control scheme provides a fast transient response in a low-bandwidth PFC loop; in which the overshoot and undershoot of the PFC voltage are clamped. If the feedback loop; is broken, the SG6932 shuts off PFC to prevent extra-high voltage on output.

For the forward PWM, the synchronized slope compensation ensures the stability of the current loop under continuous-mode operation. Hiccup operation during output overloading is guaranteed. To prevent the power supply from drawing large current during start-up, the start-up for PWM stage is delayed 4ms after the PFC output voltage reaches its set value.

SG6932 provides complete protection functions, such as brownout protection and built-in latch for over-voltage and RI open/short.

I_{AC} Signal

Figure 24 shows the IAC pin connected to input voltage by a resistor and the current, $I_{AC,}$ is the input for PFC multiplier. For the linear range of I_{AC} 0~360μA, the range input voltage should be connected to a resistance over 1.2MΩ.

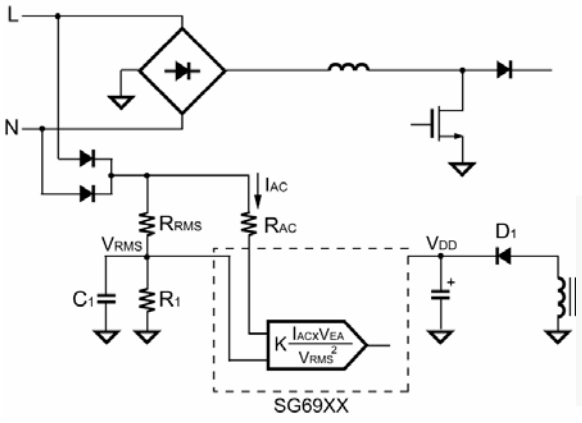


Figure 24. Input Voltage Detection

Switching Frequency / Current Sources

The switching frequency can be programmed by the resistor R_I connected between the RI and GND pins. The relationship is:

$$f_{PWM} = \frac{1560}{R_I(k\Omega)}(kHz) \quad (1)$$

For example, a 24kΩ resistor R_I results in a 65kHz switching frequency. Accordingly, constant current I_T flows through R_I:

$$I_T = \frac{1.2V}{R_I(k\Omega)}(mA) \quad (2)$$

I_T is used to generate internal current reference.

Line Voltage Detection (VRMS)

Figure 25 shows a resistive divider with low-pass filtering for line-voltage detection on the VRMS pin. The V_{RMS} voltage is used for the PFC multiplier and brownout protection. For brownout protection, when the V_{RMS} voltage drops below 0.8V, OPFC turns off.

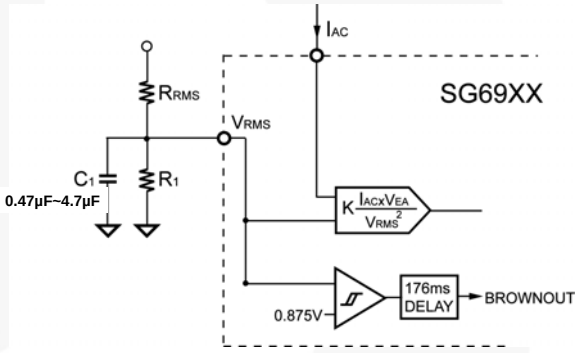


Figure 25. Line-Voltage Detection on VRMS Pin

Interleave Switching

The SG6932 uses interleaved switching to synchronize the PFC and PWM stages. This reduces switching noise and spreads the EMI emissions. Figure 26 shows off-time (t_{OFF}) inserted between the turn-off of the PFC gate drives and the turn-on of the PWM.

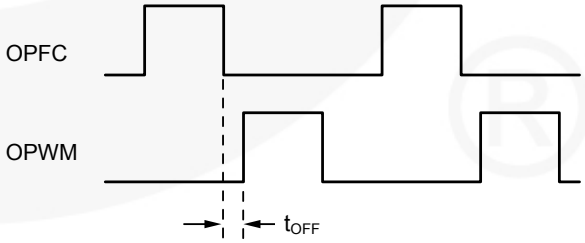


Figure 26. Interleaved Switching

PFC Operation

The purpose of a boost active power factor corrector (PFC) is to shape the input current of a power supply. The input current waveform and phase follow that of the input voltage. Average-current-mode control is utilized for continuous-current-mode operation for the PFC booster. With the innovative multi-vector control for voltage loop and switching charge multiplier-divider for current reference, excellent input power factor is achieved with good noise immunity and transient response. Figure 27 shows the control loop for the average-current-mode control circuit.

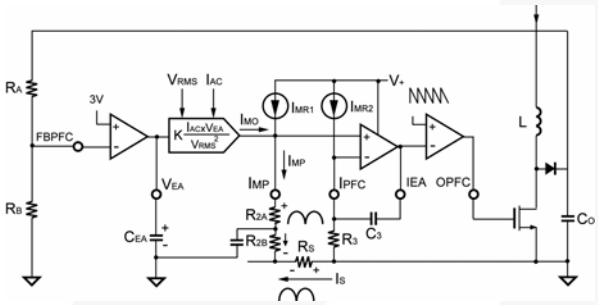


Figure 27. Control Loop of PFC Stage

The current source output from the switching charge multiplier-divider can be expressed as:

$$I_{MO} = K \times \frac{I_{AC} \times V_{EA}}{V_{RMS}^2} (\mu A) \quad (3)$$

I_{MP}, the current output from IMP pin, is the summation of I_{MO} and I_{MR1}. I_{MR1} and I_{MR2} are identical, fixed-current sources. R_2 and R_3 are also identical and are used to pull HIGH the operating point of the IMP and IPFC pins when the voltage across R_S goes negative with respect to ground.

Through the differential amplification of the signal across R_S, better noise immunity is achieved. The output of IEA is compared with an internal sawtooth and the pulsewidth for PFC is determined. Through the average-current-mode control loop, the input current I_S is proportional to I_{MO}:

$$I_{MO} \times R_2 = I_S \times R_S \quad (4)$$

According to Equation 4, the minimum value of R_2 and maximum of R_S can be determined because I_{MO} should not exceed the specified maximum value.

There are different considerations in determining the value of the sense resistor R_S. The value of R_S should be small enough to reduce power consumption, but large enough to maintain the resolution. A current transformer (CT) may be used to improve the efficiency of high-power converters.

To achieve good power factor, the voltage for V_{RMS} and V_{EA} should be kept as DC as possible, according to Equation 3. Good RC filtering for V_{RMS} and narrow bandwidth (lower than the line frequency) for voltage loop are suggested for better input current shaping.

The transconductance error amplifier has output impedance R_O (>90kΩ) and a capacitor C_{EA} (1μF ~ 10μF) connected to ground (as shown in Figure 28). This establishes a dominant pole f_1 for the voltage loop:

$$f_1 = \frac{1}{2\pi \times R_O \times C_{EA}} \quad (5)$$

The average total input power can be expressed as:

$$\begin{aligned} P_{IN} &= V_{IN}(rms) \times I_{IN}(rms) \\ &\propto V_{RMS} \times I_{MO} \\ &\propto V_{RMS} \times \frac{I_{AC} \times V_{EA}}{V_{RMS}^2} \\ &\propto V_{RMS} \times \frac{\frac{V_{IN}}{R_{AC}} \times V_{EA}}{V_{RMS}^2} \propto V_{EA} \end{aligned} \quad (6)$$

From Equation 6, V_{EA}, the output of the voltage error amplifier, actually controls the total input power and the power delivered to the load.

Multi-vector Error Amplifier

The voltage-loop error amplifier is transconductance, which has high output impedance (> 90kΩ). A capacitor C_{EA} (1μF ~ 10μF) connected from VEA to ground provides a dominant pole for the voltage loop. Although the PFC stage has a low bandwidth voltage loop for better input power factor, the innovative multi-vector error amplifier provides a fast transient response to clamp the overshoot and undershoot of the PFC output voltage.

Figure 28 shows the block diagram of the multi-vector error amplifier. When the variation of the feedback voltage exceeds ±5% of the reference voltage, the transconductance error amplifier adjusts its output impedance to increase the loop response. If R_A is opened, SG6932 shuts off immediately to prevent extra-high voltage on the output capacitor.

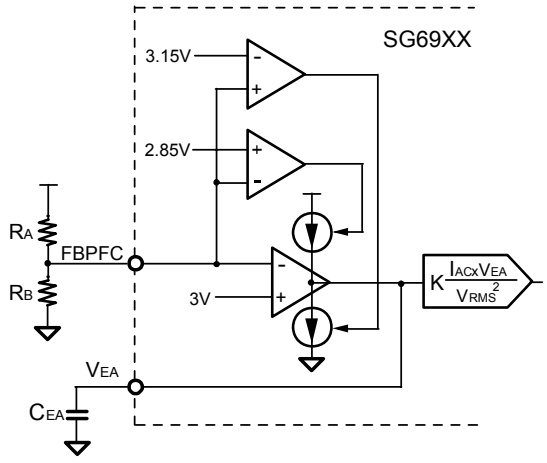


Figure 28. Multi-Vector Error Amplifier

Cycle-by-Cycle Current Limiting

SG6932 provides cycle-by-cycle current limiting for both PFC and PWM stages. Figure 29 shows the peak current limit for the PFC stage. The PFC gate drive is terminated once the voltage on the ISENSE pin goes below V_{PK}.

The V_{RMS} voltage determines the V_{PK} voltage. The relationship between V_{PK} and V_{RMS} is shown in Figure 29.

The amplitude of the constant current, $I_{P,}$ is determined by the internal current reference, I_T, according to the following equation:

$$I_P = 2 \times I_T = 2 \times \frac{1.2(V)}{R_I} \quad (7)$$

Therefore, the peak current of the I_S is given by (V_{RMS}<1.05V):

$$I_{S\_peak} = \frac{(I_P \times R_P) - 0.2(V)}{R_S} \quad (8)$$

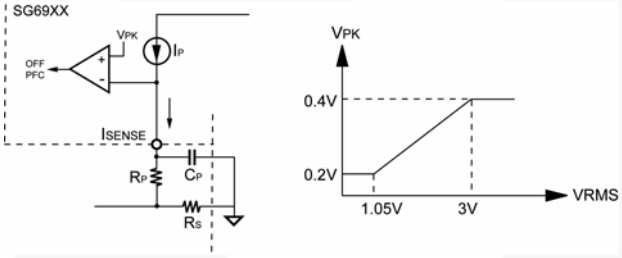


Figure 29. Current Limit

Power-On Sequence and Soft-Start

The SG6932 is enabled whenever the line voltage is higher than the brownout threshold. Once the SG6932 is active, the PFC stage is enabled first. The PWM stage is enabled following a 4ms delay time after FBPFC voltage exceeds 2.7V. During start-up of PWM stage, the SS pin charges an external capacitor with a constant current source. The voltage on FBPWM is clamped by SS during start-up. In the event of a protection condition occurring and/or PWM being disabled, the SS pin is quickly discharged.

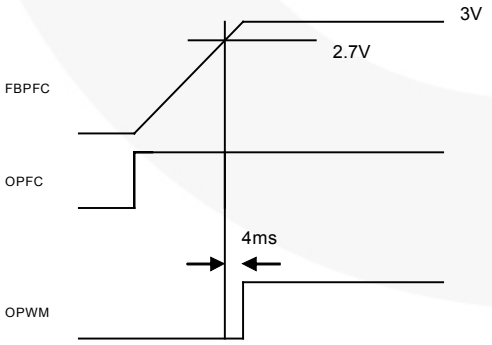


Figure 30. Power-On Sequence

Forward PWM and Slope Compensation

The PWM stage is designed for forward power converters. Peak-current-mode control is used to optimize system performance. Slope compensation is added to stabilize the current loop. The SG6932 inserts a synchronized, positively sloped ramp at each switching cycle. The positively sloped ramp is represented by the voltage signal $V_{s\text{-}comp}$. In this example, the voltage of the ramp signal is 0.55V.

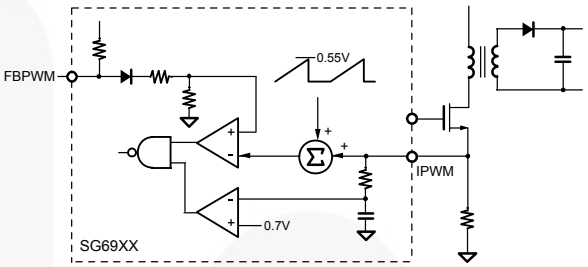


Figure 31. Slope Compensation

Limited Power Control

Every time the output of power supply is shorted or overloaded, the FBPWM voltage increases. If the FB voltage is higher than a designed threshold of 4.2V for longer than 95ms, the PWM output is turned off.

Gate Drivers

SG6932 output stages are fast totem-pole gate drivers. The output driver is clamped by an internal 18V Zener diode to protect the power MOSFET.

Protections

The SG6932 provides full protection functions to prevent the power supply and the load from being damaged. The protection features include:

PFC Feedback Over-Voltage Protection. When the PFC feedback voltage exceeds the over-voltage threshold, SG6932 inhibits the PFC switching signal. This protection prevents the PFC power converter from operating abnormally while the FBPFC pin is open.

Second PFC Over-Voltage Protection (OVP_PFC). The PFC stage over-voltage input. The comparator disables the PFC output driver if this input exceeds 3.25V. This pin can be connected to the FBPFC pin or the PFC boost output through a divider network. This pin provides an extra input for PFC over-voltage protection.

PFC Feedback Under-Voltage Protection. The SG6932 stops the PFC switching signal whenever the PFC feedback voltage drops below the under-voltage threshold. This protection feature prevents the PFC power converter from experiencing abnormal conditions while the FBPFC pin is shorted to ground.

V_{DD} Over-Voltage Protection. The PFC and PWM stages are disabled whenever the V_{DD} voltage exceeds the over-voltage threshold.

RI Pin Open / Short Protection. The RI pin is used to set the switching frequency and internal current reference. The PFC and PWM stages of SG6932 are disabled whenever the RI pin is short or open.

PCB Layout

SG6932 has a single ground pin, which prevents high sink currents in the output being returned separately. Good high-frequency or RF layout practices should be followed. Avoid long PCB traces and component leads. Locate decoupling capacitors near the SG6932. A resistor (5 ~ 20Ω) is recommended, connected in series from the output to the gate of the MOSFET.

Isolating the interference between the PFC and PWM stages is also important. Figure 32 shows an example of the PCB layout. The *ground trace 1* is connected from the ground pin to the decoupling capacitor, which should be low impedance and as short as possible. The *ground trace 2* provides a signal ground and should be connected directly to the decoupling capacitor C_{DD} and/or to the ground pin. The *ground trace 3* is independently tied from the decoupling capacitor to the PFC output capacitor C_O.

The ground in the output capacitor C_O is the major ground reference for power switching. To provide a good ground reference and reduce the switching noise of both the PFC and PWM stages, the *ground traces 6 and 7* should be located very near and be low impedance.

The IPFC pin is connected directly to R_S through R_3 to improve noise immunity. **Do not incorrectly connect to the ground trace 2**. The IMP and ISENSE pins should also be connected directly via the resistors R_2 and R_P to another terminal of R_S.

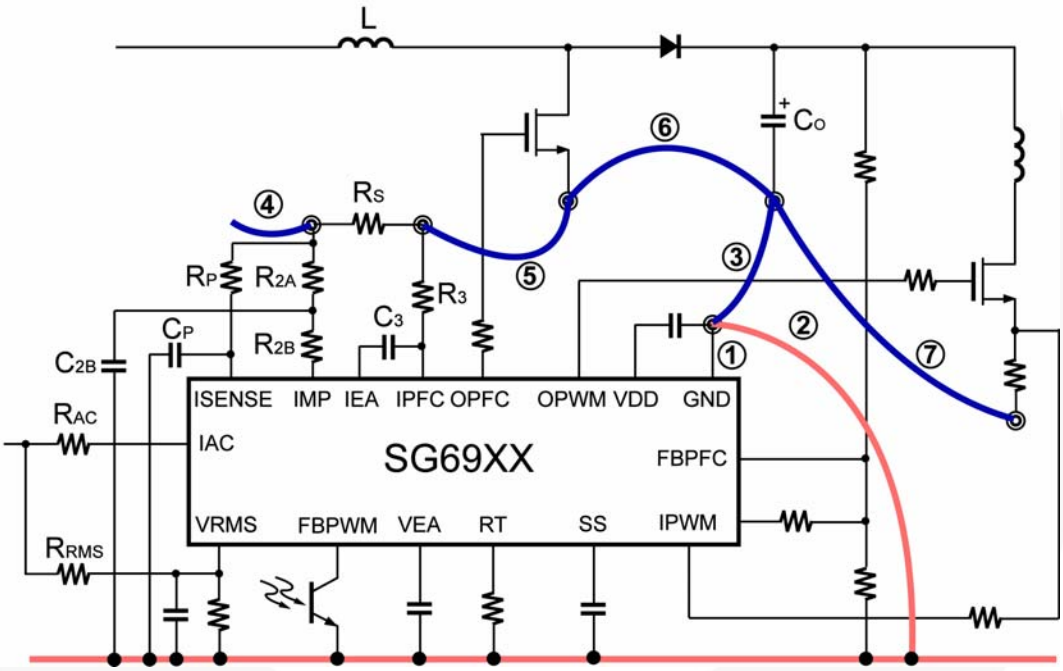


Figure 32. PCB Layout

Reference Circuit

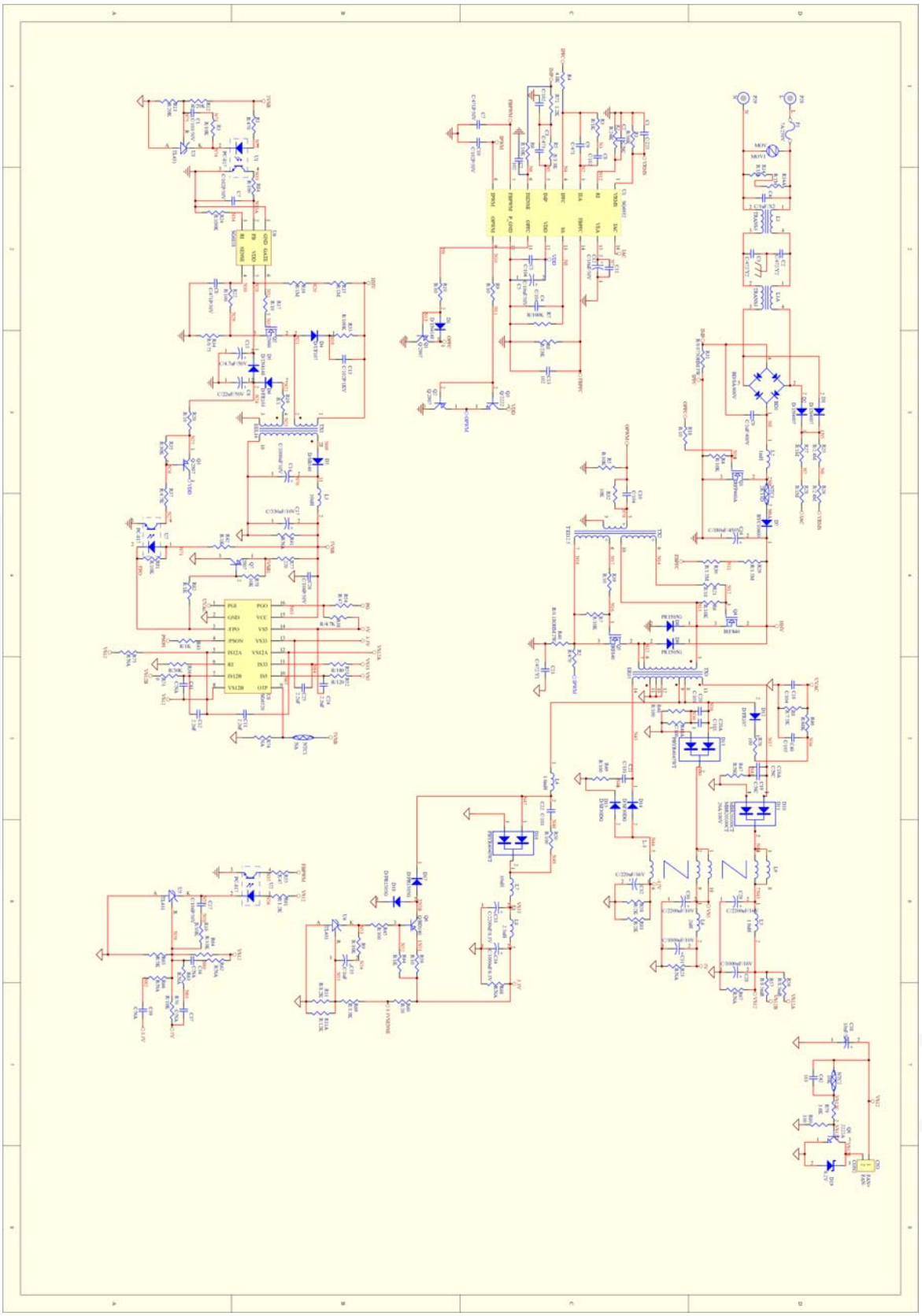
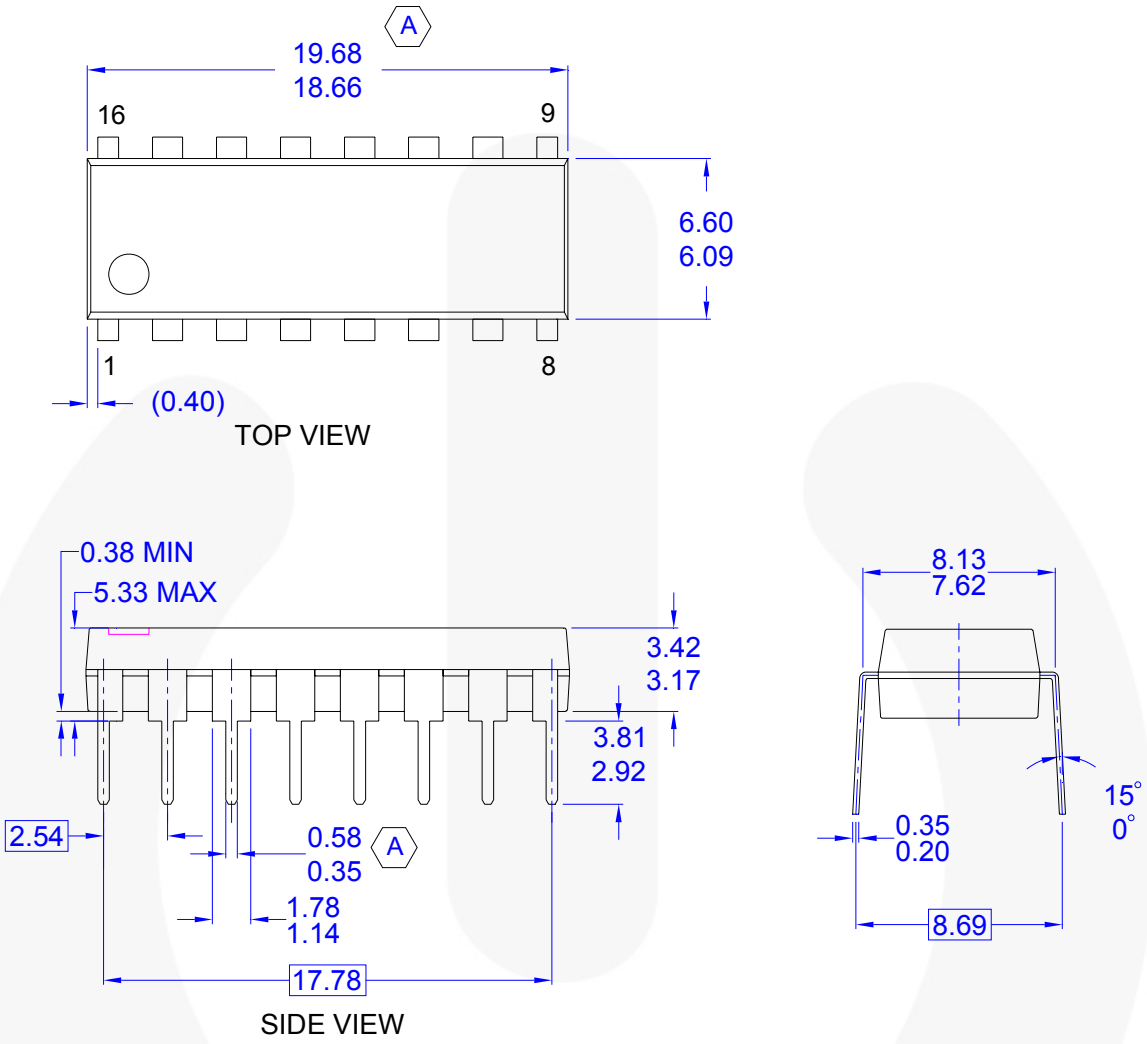


Figure 33. Reference Circuit

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MS-001 VARIATION BB

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR PROTRUSIONS

D) CONFORMS TO ASME Y14.5M-1994

E) DRAWING FILE NAME: N16EREV1

Figure 34. 16-pin Dual In-Line Package (DIP)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
http://www.fairchildsemi.com/packaging/

Physical Dimensions (Continued)

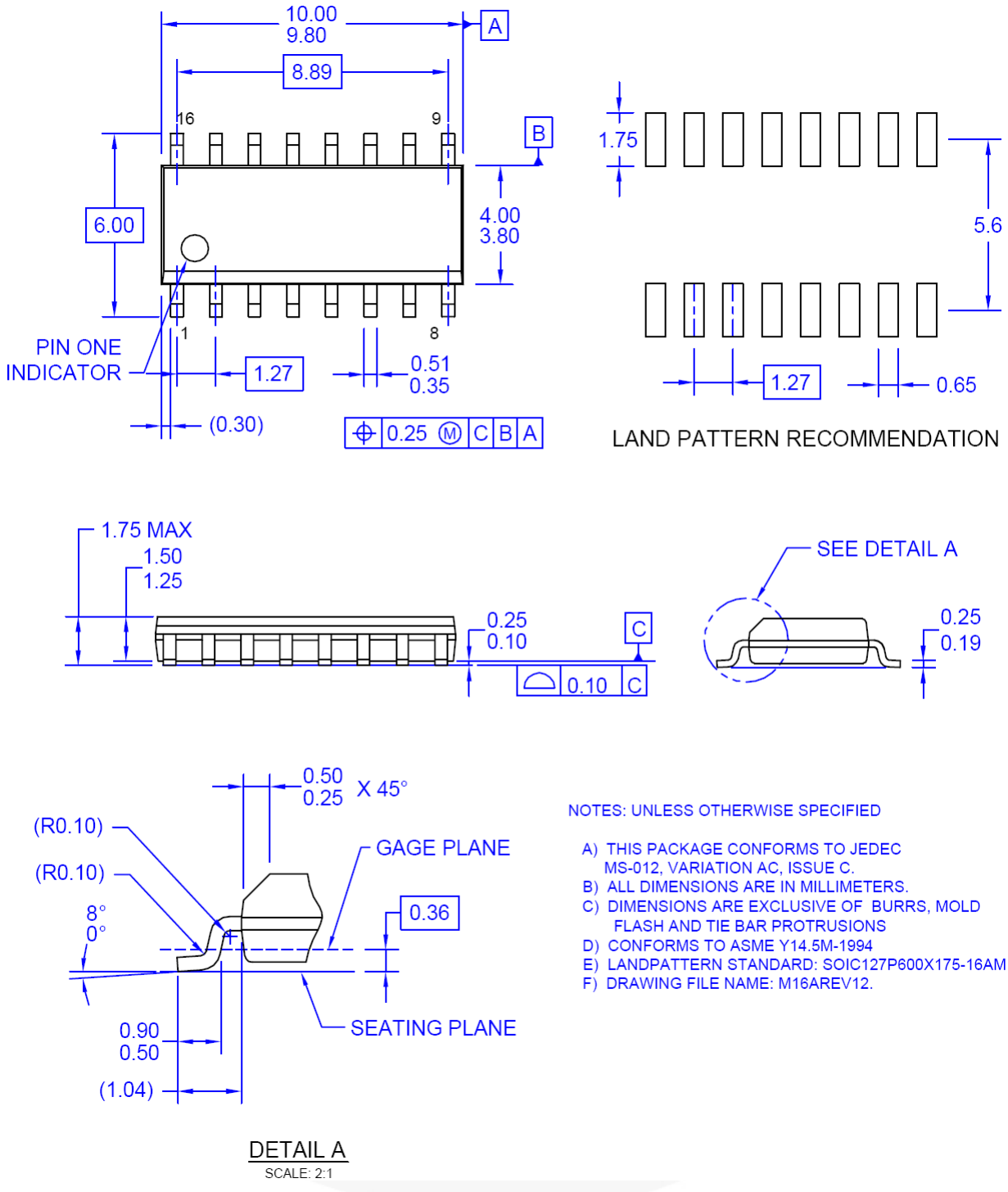


Figure 35. 16-Pin Small Outline Package (SOIC)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
http://www.fairchildsemi.com/packaging/

FAIRCHILD SEMICONDUCTOR®

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

ACEx®
Build it Now™
CorePLUS™
CorePOWER™
CROSSVOLT™
CTL™
Current Transfer Logic™
EcoSPARK®
EfficentMax™
EZSWITCH™ *
E²™
ƒ®
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FlashWriter®*
FPS™
F-PFS™
FRFET®
Global Power Resource℠
Green FPS™
Green FPS™ e-Series™
GTO™
IntelliMAX™
ISOPLANAR™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MillerDrive™
MotionMax™
Motion-SPM™
OPTOLOGIC®
OPTOPLANAR®
PDP SPM™
Power-SPM™
PowerTrench®
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
Saving our world, 1mW at a time™
SmartMax™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS™
SyncFET™
SYSTEM GENERAL®
The Power Franchise®
the power franchise
TinyBoost™
TinyBuck™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
µSerDes™
µSerDes
UHC®
Ultra FRFET™
UniFET™
VCX™
VisualMax™

* EZSWITCH™ and FlashWriter® are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I34