ROHM SEMICONDUCTOR

Datasheet

For air-conditioner fan motor

Three phase brushless fan motor controller

BD62013FS

● **General Description**

This controller synthesizes the optimal driving signal from hall sensor signals, and outputs the synthesized signal to control the external level shifter and power transistor. The replacement is also easy because of the almost pin compatible with BD62011FS, BD62012FS and BD62014FS, and this controller provides optimum motor drive for a wide variety of applications, and enables motor unit standardization.

● **Key Specifications**

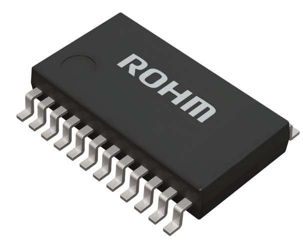
■ Supply voltage range:	10V to 18V
■ Duty control voltage range:	2.1V to 5.4V
■ Phase control range:	0° to 30°
■ Operating temperature:	-40°C to 110°
■ Power dissipation:	1.0W

● **Features**

- ■ 150° commutation logic
- ■ PWM control (Upper arm switching)
- ■ Phase control supported from 0° to +30° at 1° intervals
- ■ Rotational direction switch
- ■ FG signal output (12 pulses)
- ■ VREG output (5V/30mA)
- ■ Protection circuits provided: OCP, TSD, UVLO, MLP and the external fault input (FIB)

● **Package** W(Typ.) x D(Typ.) x H(Max.)

SSOP-A24 10.00mm x 7.80mm x 2.10mm



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● **Applications**

- ■ Air conditioners; air cleaners; water pumps; dishwashers; washing machines
- ■ General OA equipment

● **Typical Application Circuit**

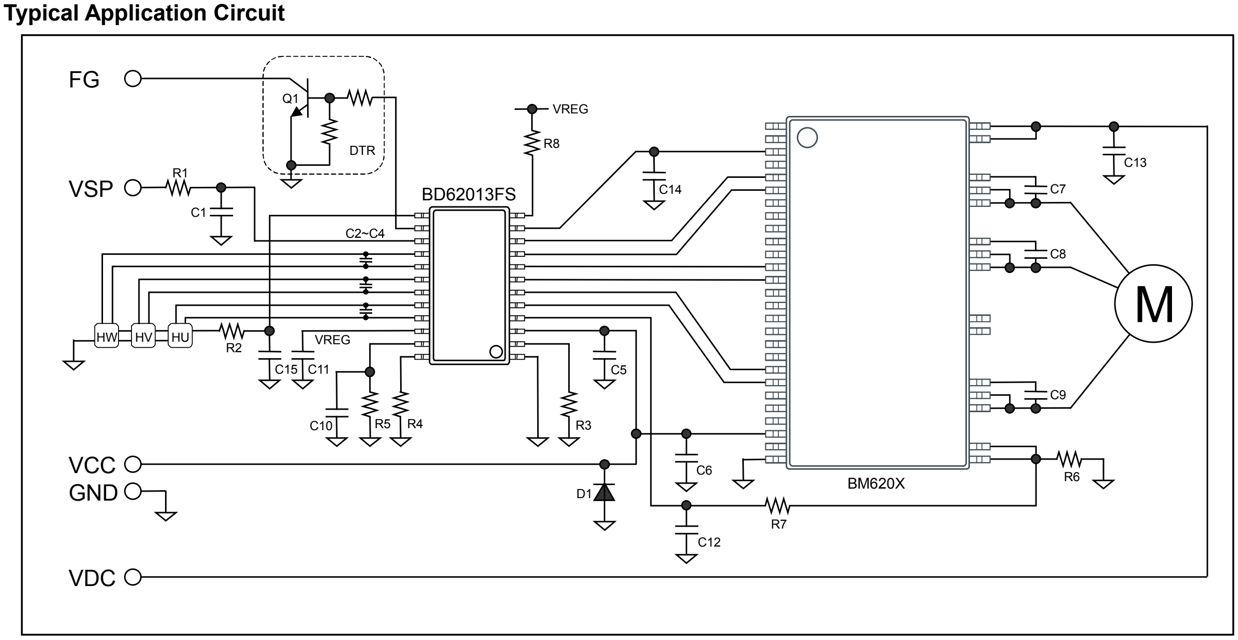


Fig.1 Application circuit example - BD62013FS & BM620X

○Product structure : Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays

● Block diagram and pin configuration

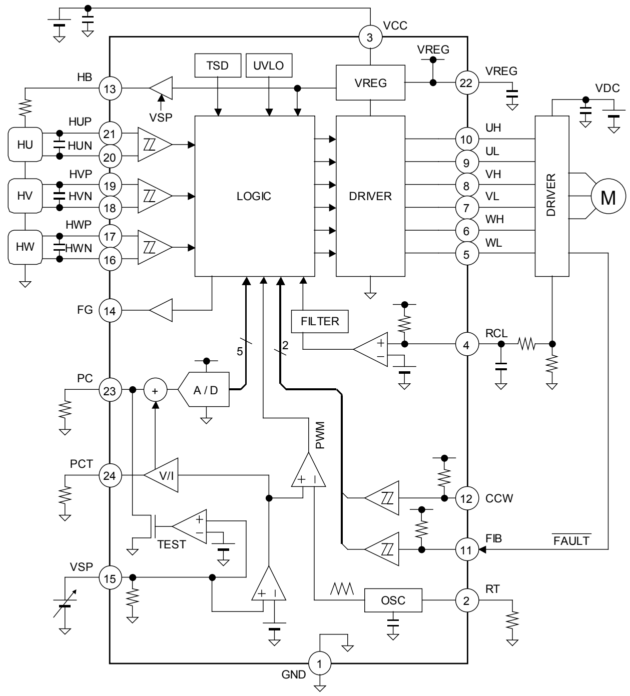


Fig.2 Block diagram

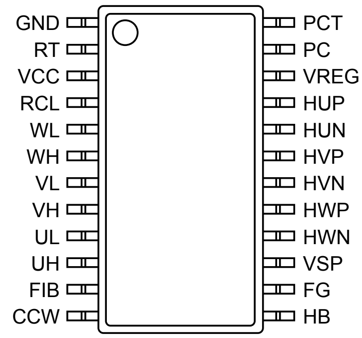


Fig.3 Pin configuration

● Pin descriptions

Pin	Name	Function	Pin	Name	Function
1	GND	Signal ground	24	PCT	VSP offset voltage output pin
2	RT	Carrier frequency setting pin	23	PC	Phase control input pin
3	VCC	Power supply	22	VREG	Regulator output
4	RCL	Over current sense pin	21	HUP	Hall input pin phase U+
5	WL	Low side driver output phase W	20	HUN	Hall input pin phase U-
6	WH	High side driver output phase W	19	HVP	Hall input pin phase V+
7	VL	Low side driver output phase V	18	HVN	Hall input pin phase V-
8	VH	High side driver output phase V	17	HWP	Hall input pin phase W+
9	UL	Low side driver output phase U	16	HWN	Hall input pin phase W-
10	UH	High side driver output phase U	15	VSP	Duty control voltage input pin
11	FIB	External fault input (Low active)	14	FG	FG signal output (12 pulses)
12	CCW	Direction switch (H:CCW)	13	HB	Hall bias output

● Functional descriptions

1) Commutation logic

When the hall cycle is about 5Hz or less (e.g. when the motor starts up), the commutation mode is 120° rectangle drive with an upper and lower switching (no lead angle). The controller monitors the hall cycle, and switches to 150° commutation drive when the hall cycle reaches or exceeds about 5Hz over four consecutive cycles. Refer to the timing chart, figure 7 and 8.

Table 1 120° commutation (Six-state) truth table

HU	HV	HW	UH	VH	WH	UL	VL	WL
H	L	H	L	PWM	L	H	$\overline{\text{PWM}}$	L
H	L	L	L	L	PWM	H	L	$\overline{\text{PWM}}$
H	H	L	L	L	PWM	L	H	$\overline{\text{PWM}}$
L	H	L	PWM	L	L	$\overline{\text{PWM}}$	H	L
L	H	H	PWM	L	L	$\overline{\text{PWM}}$	L	H
L	L	H	L	PWM	L	L	$\overline{\text{PWM}}$	H

2) Duty control

The switching duty can be controlled by forcing the DC voltage to the VSP pin, from V_{SPMIN} to V_{SPMAX}. When the VSP voltage is higher than V_{SPTST}, the controller forces PC pin voltage to the ground (Testing mode, the maximum duty and no lead angle). The VSP pin is pulled down internally by a 200kΩ resistor. Therefore, note the impedance when setting the VSP voltage with the resistance voltage divider.

3) Carrier frequency setting

The carrier frequency setting can be freely adjusted by connecting an external resistor between the RT pin and ground. The RT pin is biased to a constant voltage, which determines the charge current to the internal capacitor. Carrier frequencies can be set within a range from about 16kHz to 50kHz. Refer to the formula to the right.

$$F_{OSC}\ [\text{kHz}] = \frac{400}{R_T\ [\text{k}\Omega]}$$

4) FG signal output

The FG signal is output from the FG pin, and it is generated from the three hall signals (exclusive NOR, 12 pulses).

5) Direction of motor rotation setting

The direction of rotation may be switched with the CCW pin. When CCW pin is “H” or open, the motor rotates for CCW direction. When the real direction is different from the setting, the commutation mode is 120° rectangle drive (no lead angle). It is recommended to pull up to VREG voltage when malfunctioning because of the noise.

CCW	Direction
H	CCW
L	CW

6) Hall signal comparator

The hall comparator provides voltage hysteresis to prevent noise malfunctions. The bias current to the hall elements should be set to the input voltage amplitude from the element, at a value higher than the minimum input voltage, $V_{HALLMIN}$. We recommend connecting a ceramic capacitor from 100pF to 0.01µF, between the differential input pins of the hall comparator. Note that the bias to hall elements must be set within the common mode input voltage range V_{HALLCM}.

7) Hall bias switch

When the VSP voltage is higher than V_{SPHB}, the controller outputs VREG voltage to HB pin by an internal switch. A power saving is enabled at the motor rotation stop, by using HB output for the Hall elements bias current. In addition, since the HB output is supplied from the VREG power supply, take into consideration as load connected to the VREG pin, and be aware of the I_{OMAX} value.

8) Output duty pulse width limiter

PWM switching duty pulse width limitation is provided to ensure proper external level shifter and power transistor switching. Because of the pulse width limitation, the controller will not output a pulse of less than T_{MIN} (0.8µs minimum), nor can it output a duty pulse of D_{MAX} or more, because the controller does not keep the external power transistors full on. Also, since the upper and lower external power transistors cannot be turned on simultaneously, the controller is shut off for the period T_{DT} (1.6µs minimum) at the upper and lower part of each phase output (for example, UH and UL). Therefore, the switching maximum duty at the motor starts up is 90 percent (nominal).

9) Phase control setting

The driving signal phase can be advanced to the hall signal - (Phase control). The lead angle is set by forcing the DC voltage to the PC pin. The input voltage is converted digitally with the 6-bit A/D converter, in which internal VREG voltage is assumed to be full-scale, and the converted data is processed by logic circuit. The lead angle can be set from 0° to +30° at 1° intervals, and updated fourth hall cycle of phase W falling edge.
For the phase control function to operate is only 150° commutation mode. However, the controller forces PC pin voltage to ground (no lead angle) when the testing mode.
The VSP offset voltage (Figure 29) is buffered to PCT pin, to connect an external resistor between PCT pin and ground. The internal bias current is determined by PCT voltage and the resistor value - V_{PCT} / R_{PCT} -, and mix to PC pin. As a result, the lead angle setting is followed with the duty control voltage, and the performance of the motor can be improved.
Please select the R_{PCT} value from 50kΩ to 200kΩ in the range on the basis of 100kΩ, because the PCT pin current capability is a 100µA or less.

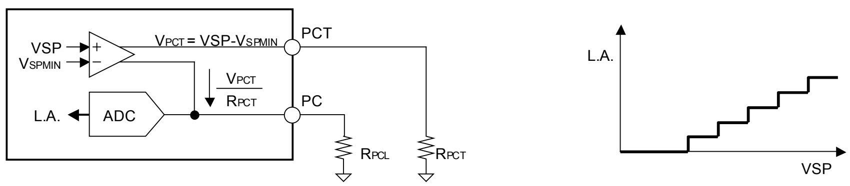


Fig. 4 Phase control setting example 1

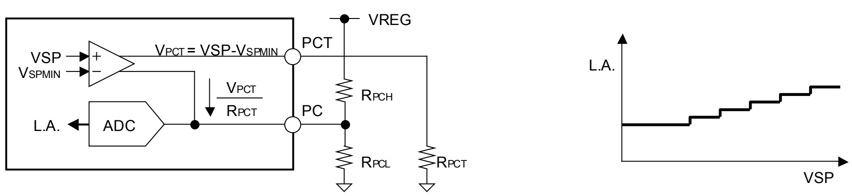


Fig. 5 Phase control setting example 2

10) Overcurrent protection (OCP) circuit

The over current protection circuit can be activated by connecting a low value resistor for current detection between the external output stage ground and the controller IC ground. When the RCL pin voltage reaches or surpasses the threshold value, the controller forces all the upper switching arm imports low (UH, VH, WH = L, L, L), thus initiating the overcurrent protection operation. When the RCL pin voltage swings below the ground, it is recommended to insert a resistor - 1.5kΩ or more - between RCL pin and current detection resistor because of the malfunction prevention. Since this protection circuit is not a latch type, it returns to normal operation - synchronizing with the carrier frequency - once the RCL pin voltage falls below the threshold voltage. A filter is built into the overcurrent detection circuit to prevent malfunctions, so that the protection function does not activate when a short pulse of less than T_{RCL} is input.

11) External fault signal input pin (FIB pin, low active)

The FIB pin can force all controller driver outputs low at any time. The FIB pin is pulled up to VREG internally by a 100kΩ resistor, therefore, an open drain output can be connected directly. It is recommended to pull up to VREG voltage when this function is not used and malfunctioning because of the noise.

12) Thermal shutdown (TSD) circuit

The TSD circuit operates when the junction temperature of the controller exceeds the preset temperature (175°C nominal). At this time, the controller forces all driver outputs low. Since thermal hysteresis is provided in the TSD circuit, the chip returns to normal operation when the junction temperature falls below the preset temperature (150°C nominal). The TSD circuit is designed only to shut the IC off to prevent thermal runaway. It is not designed to protect the IC or guarantee its operation in the presence of extreme heat. Do not continue to use the IC after the TSD circuit is activated, and do not use the IC in an environment where activation of the circuit is assumed.

13) Under voltage lock out (UVLO) circuit

To secure the lowest power supply voltage necessary to operate the controller, and to prevent under voltage malfunctions, a UVLO circuit is built into this controller. When the power supply voltage falls to V_{UVL} or below, the controller forces all driver outputs low. When the voltage rises to V_{UVH} or above, the UVLO circuit ends the lockout operation and returns the chip to normal operation.

The voltage monitor circuit is built into for the VREG pin voltage (4.0V nominal) and HB pin voltage (3.5V nominal). Therefore, the UVLO circuit does not release operation when either voltage rising is delayed behind the VCC voltage rising even if VCC voltage becomes V_{UVH} or more.

14) Hall signal wrong input detection

Hall element abnormalities may cause incorrect inputs that vary from the normal logic. When all hall input signals go high or low, the hall signal wrong input detection circuit forces all driver outputs low. And when the controller detects the abnormal hall signals continuously four times or more a motor rotation, the controller forces all driver outputs low and latches the state. It is released that if the duty control voltage VSP is forced ground level once.

15) Motor lock protect

When the controller detects the motor locking during the fixed time (4sec. nominal, each edge of the hall signal doesn't input either), the controller forces all driver outputs low in the under in fixed time (20sec. nominal), and self-returns to the normal operation. This circuit is enabled the voltage force to VSP over the duty minimum voltage V_{SPMIN}, and note that the motor cannot starts up when the controller doesn’t detect the motor rotation by the minimum duty control.

16) Internal voltage regulator

The internal voltage regulator VREG is output for the bias of the hall element, the phase control setting. However, when using the VREG function, be aware of the I_{OMAX} value. If a capacitor is connected to the ground in order to stabilize output, a 1μF or lower capacitor should be used. In this case, be sure to confirm that there is no oscillation in the output.

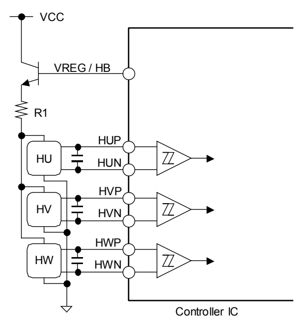


Fig. 6 VREG output pin application example

● **Timing charts (CW)**

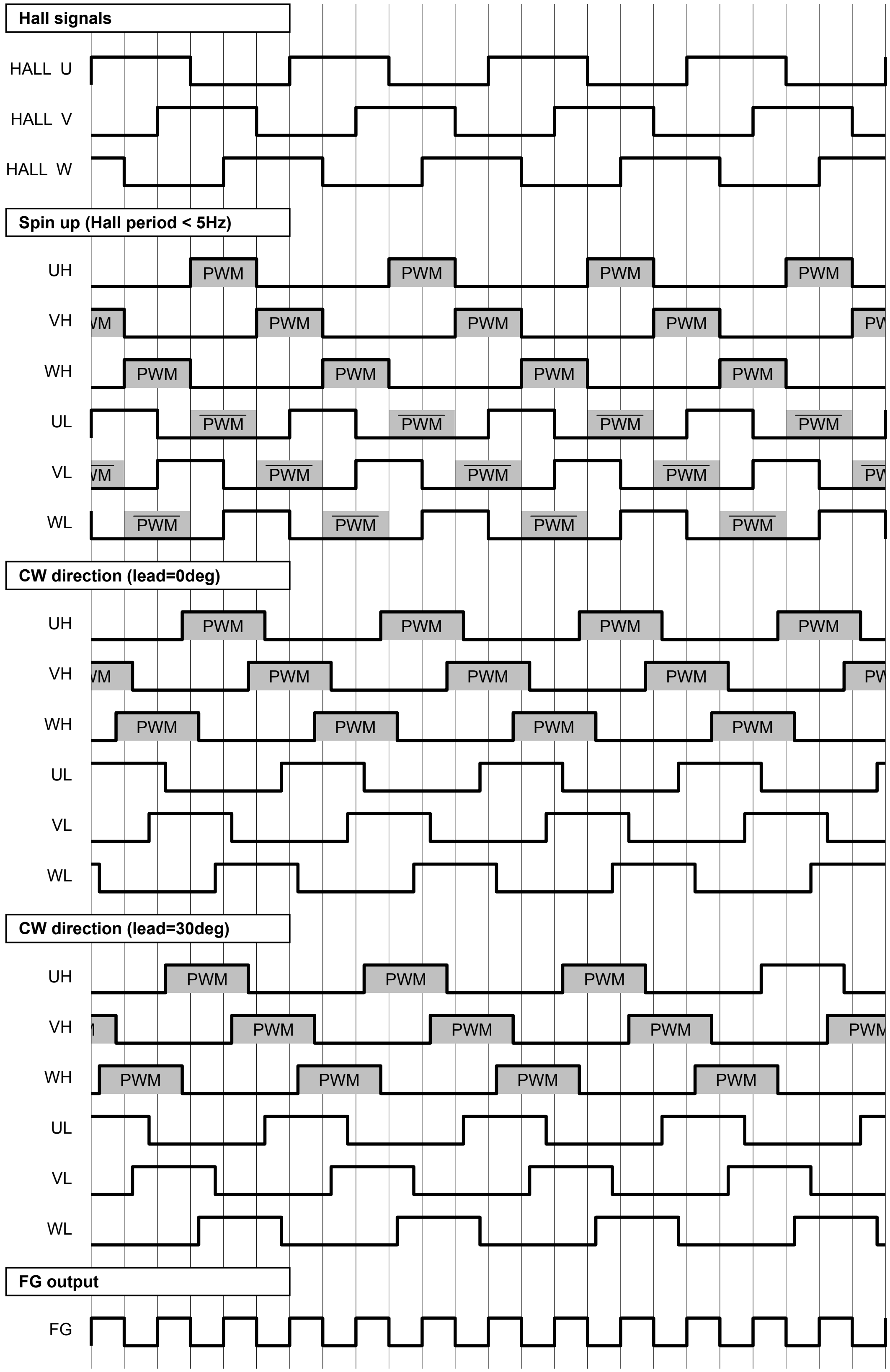


Fig. 7 BD62013FS (Clockwise) timing charts

● **Timing charts (CCW)**

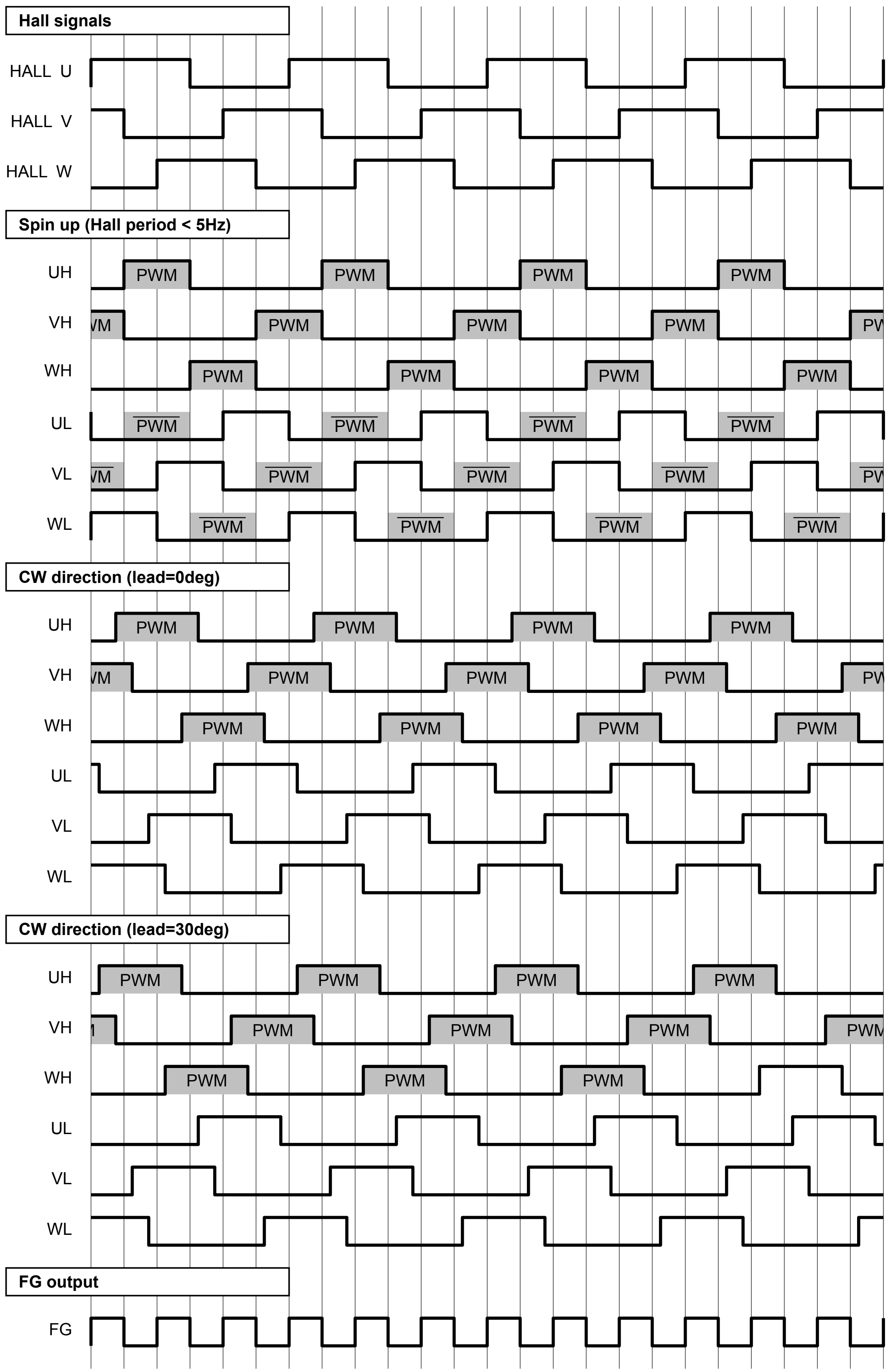


Fig. 8 BD62013FS (Counter clockwise) timing charts

● Controller outputs and operation mode summary

<table>
<tr><td rowspan="2">Conditions</td><td>Detected direction</td><td colspan="2">Forward (CW:U~V~W, CCW:U~W~V)</td><td colspan="2">Reverse (CW:U~W~V, CCW:U~V~W)</td></tr>
<tr><td>Hall sensor period</td><td>< 5Hz</td><td>5Hz <</td><td>< 5Hz</td><td>5Hz <</td></tr>
<tr><td rowspan="3">Normal operation</td><td>V_{SPHB} < VSP < V_{SPMIN}
(Duty off)</td><td colspan="4">Upper and lower arm off</td></tr>
<tr><td>V_{SPMIN} < VSP < V_{SPMAX}
(Control range)</td><td rowspan="2">120°
Upper and lower switching</td><td>150°
Upper switching</td><td rowspan="2">120°
Upper and lower switching</td><td rowspan="2">120°
Upper switching</td></tr>
<tr><td>V_{SPTST} < VSP
(Testing mode)</td><td>150°
Upper switching
(No lead angle)</td></tr>
<tr><td rowspan="6">Protect operation</td><td>Overcurrent</td><td colspan="2">Upper arm off</td><td colspan="2">Upper and lower arm off</td></tr>
<tr><td>UVLO</td><td colspan="4" rowspan="4">Upper and lower arm off</td></tr>
<tr><td>TSD</td></tr>
<tr><td>Motor lock</td></tr>
<tr><td>External input</td></tr>
<tr><td>Hall sensor abnormally</td><td colspan="4">Upper and lower arm off and latch</td></tr>
</table>

* The controller monitors both edge of three hall sensors for detecting period.
* For the phase control function to operate is only 150° commutation mode. However, the controller forces no lead angle when the testing mode.

● Absolute maximum ratings (Ta=25°C, All voltages are with respect to ground)

Parameter	Symbol	Ratings BD62013FS	Unit
Supply voltage	V_{CC}	20*1	V
Duty control voltage	V_{SP}	-0.3 to 20	V
All others	$V_{I/O}$	-0.3 to 5.5	V
Driver outputs	$I_{OMAX(OUT)}$	±15*1	mA
Monitor output	$I_{OMAX(FG)}$	±5*1	mA
VREG outputs	$I_{OMAX(VREG)}$	-40*1	mA
Operating temperature	T_{OPR}	-40 to 110	°C
Storage temperature	T_{STG}	-55 to 150	°C
Power dissipation	Pd	1.00*2	W
Junction temperature	T_{jmax}	150	°C

*1 Do not, however, exceed Pd or ASO.
*2 Mounted on a 70mm x 70mm x 1.6mm FR4 glass-epoxy board with less than 3% copper foil. Derated at 8mW/°C above 25°C.

● Operating conditions (Ta=25°C)

Parameter	Symbol	BD62013FS	Unit
Supply voltage	V_{CC}	10 to 18	V

● **Electrical characteristics** (Unless otherwise specified, Ta=25°C and VCC=15V)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Power supply						
Supply current	I_{CC}	1.3	2.5	5.0	mA	
VREG voltage	V_{REG}	4.5	5.0	5.5	V	I_O=-30mA
Driver outputs						
Output high voltage	V_{OH}	V_{REG}-0.60	V_{REG}-0.20	V_{REG}	V	I_O=-5mA
Output low voltage	V_{OL}	0	0.14	0.60	V	I_O=5mA
Dead time	T_{DT}	1.6	2.0	2.4	μs	
Minimum pulse width	T_{MIN}	0.8	1.0	1.2	μs	
Hall comparators						
Input bias current	I_{HALL}	-2.0	-0.1	2.0	μA	V_{IN}=0V
Common mode input	V_{HALLCM}	0	-	V_{REG}-1.5	V	
Minimum input level	$V_{HALLMIN}$	50	-	-	mV_{p-p}	
Hysteresis voltage P	$V_{HALLHY+}$	5	13	23	mV	
Hysteresis voltage N	$V_{HALLHY-}$	-23	-13	-5	mV	
Duty control						
Input bias current	I_{SP}	15	25	35	μA	V_{IN}=5V
Duty minimum voltage	V_{SPMIN}	1.7	2.1	2.5	V	
Duty maximum voltage	V_{SPMAX}	5.0	5.4	5.8	V	
Testing operation range	V_{SPTST}	13	-	18	V	
Minimum output duty	D_{MIN}	1.2	1.8	2.4	%	F_{OSC}=18kHz
Maximum output duty	D_{MAX}	92	95	98	%	F_{OSC}=18kHz
HB enable voltage	V_{SPHB}	0.5	1.0	1.5	V	
Mode switch and the external input - CCW and FIB						
Input bias current	I_{IN}	-70	-50	-30	μA	V_{IN}=0V
Input high voltage	V_{INH}	3	-	VREG	V	
Input low voltage	V_{INL}	0	-	1	V	
Hysteresis voltage	V_{INHY}	0.2	0.5	0.8	V	
Monitor output - FG						
Output high voltage	V_{MONH}	V_{REG}-0.40	V_{REG}-0.08	V_{REG}	V	I_O=-2mA
Output low voltage	V_{MONL}	0	0.06	0.40	V	I_O=2mA
Overcurrent protection						
Input bias current	I_{RCL}	-30	-20	-10	μA	V_{IN}=0V
Threshold voltage	V_{RCL}	0.48	0.50	0.52	V	
Noise masking time	T_{RCL}	0.8	1.0	1.2	μs	
Phase control						
Minimum lead angle	P_{MIN}	-	0	1	deg	V_{PC}=0V
Maximum lead angle	P_{MAX}	29	30	-	deg	V_{PC}=1/2·V_{REG}
VSP controlled lead angle	P_{VSP}	23	26	29	deg	V_{SP}=4V,R_{PCT}/R_{PC}=100kΩ/96.97kΩ
OSC						
Carrier frequency	F_{OSC}	16	18	20	kHz	R_T=22kΩ
UVLO						
Release voltage	V_{UVH}	8.5	9.0	9.5	V	
Lockout voltage	V_{UVL}	7.5	8.0	8.5	V	
Hysteresis voltage	V_{UVHY}	0.5	1.0	1.5	V	

● **Typical performance curves (Reference data)**

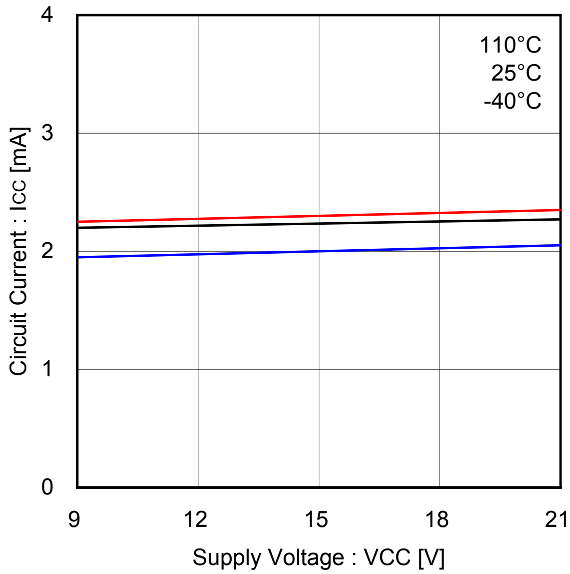


Fig.9 Circuit current

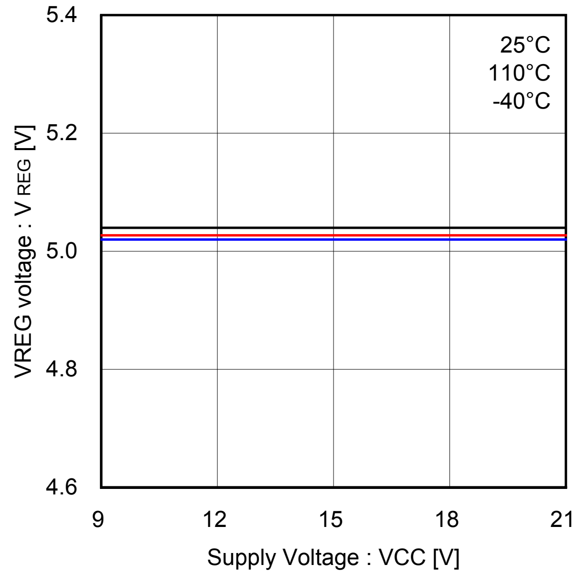


Fig.10 VREG vs VCC

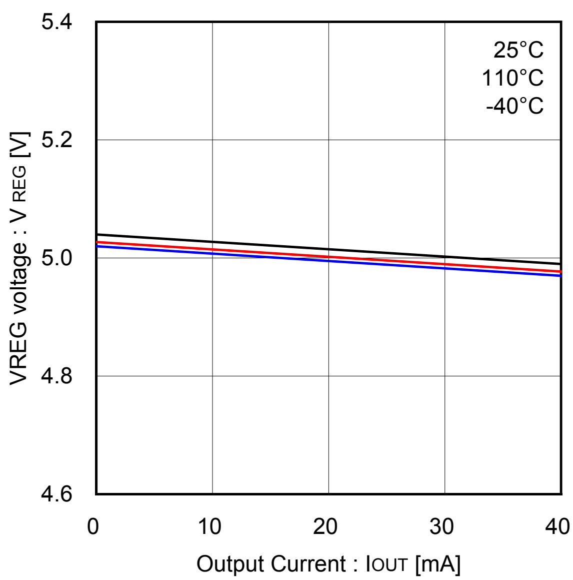


Fig.11 VREG drive capability

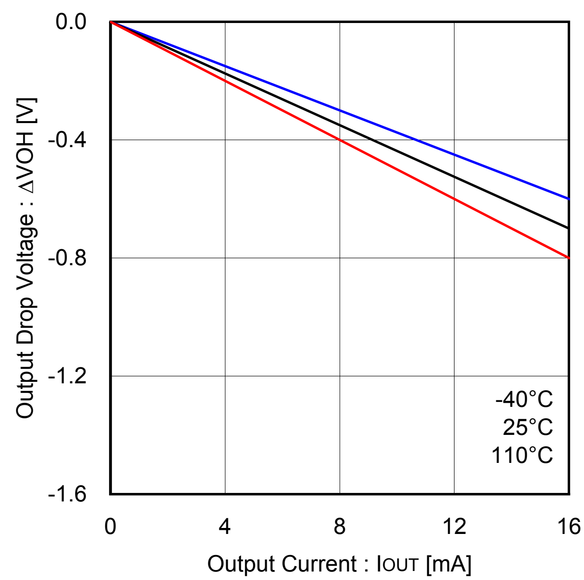


Fig.12 High side output voltage (XH, XL)

● **Typical performance curves (Reference data) - Continued**

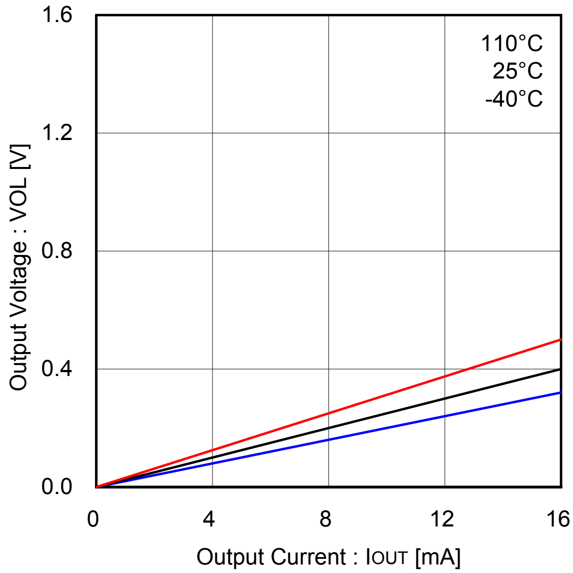


Fig.13 Low side output voltage (XH, XL)

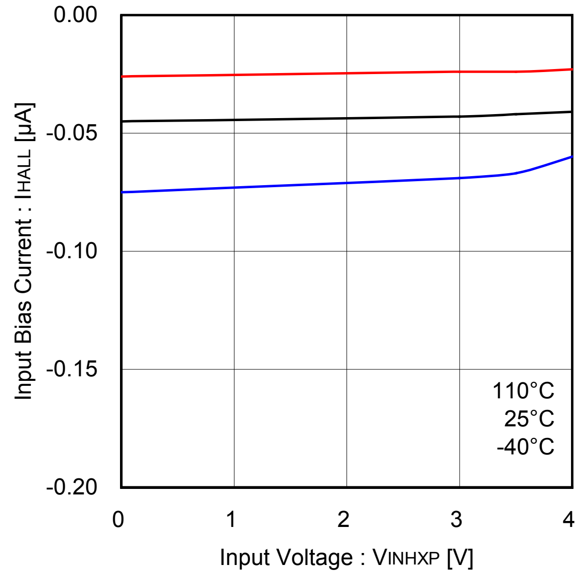


Fig.14 Hall comparator input bias current (HXP, HXN)

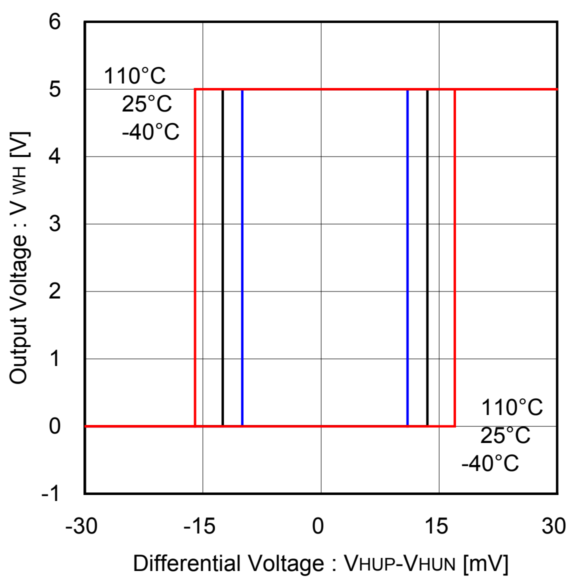


Fig.15 Hall comparator hysteresis voltage

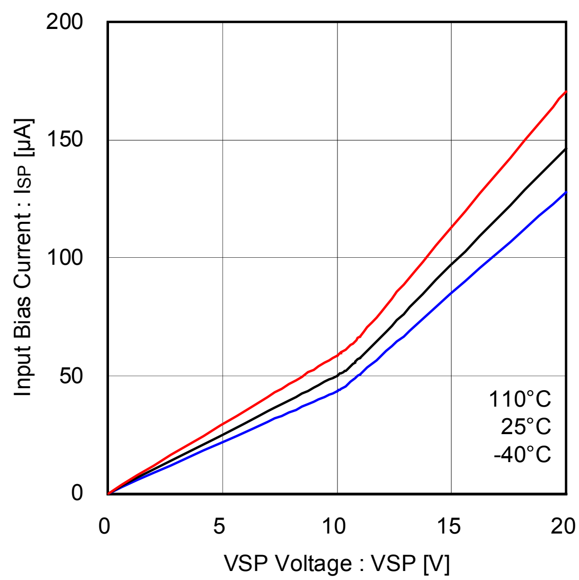


Fig.16 VSP input bias current

● **Typical performance curves (Reference data) - Continued**

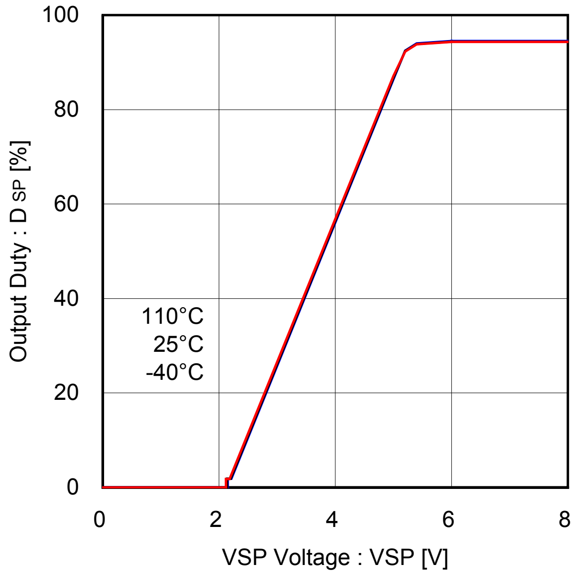


Fig.17 Output duty – VSP voltage

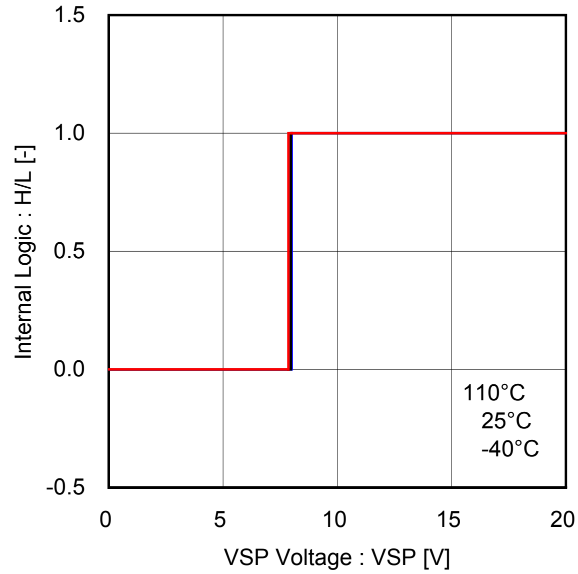


Fig.18 Testing mode threshold voltage

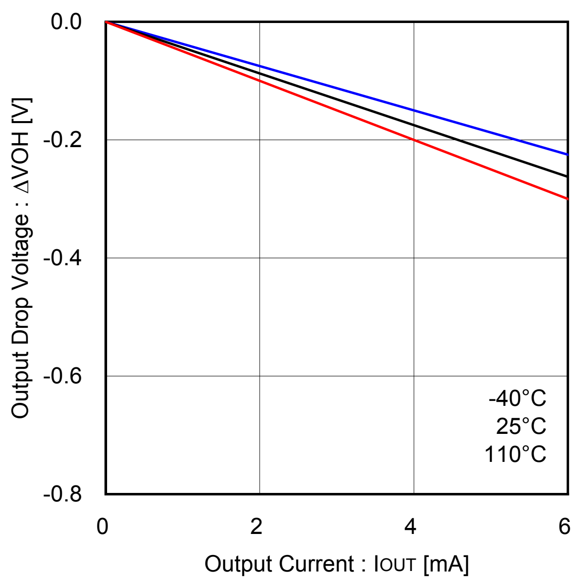


Fig.19 High side output voltage (FG)

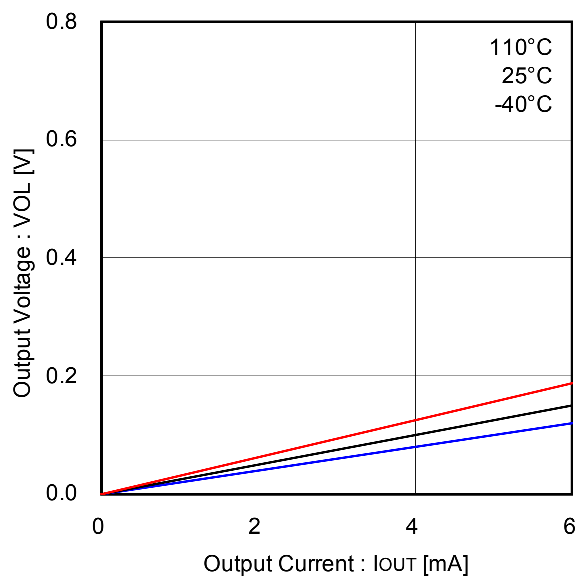


Fig.20 Low side output voltage (FG)

● **Typical performance curves (Reference data) - Continued**

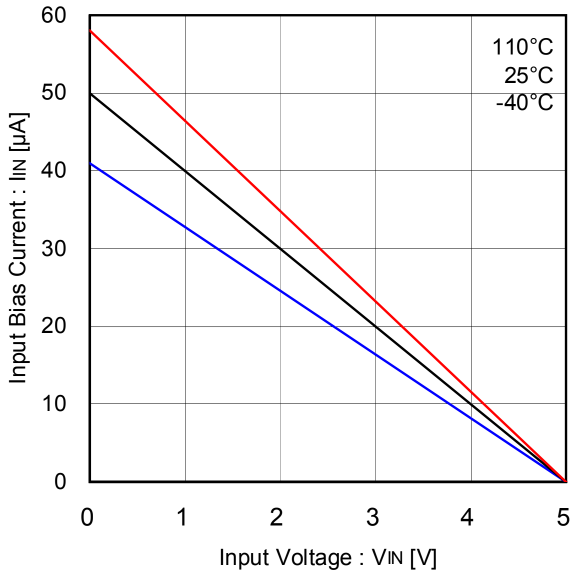


Fig.21 Input bias current
(CCW, FIB)

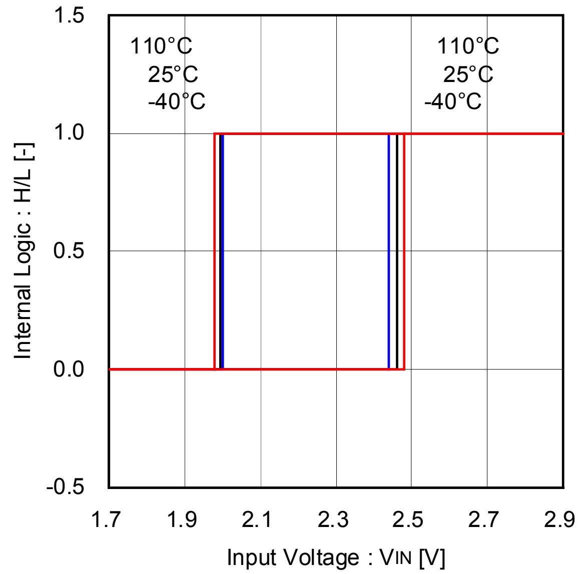


Fig.22 Input threshold voltage
(CCW, FIB)

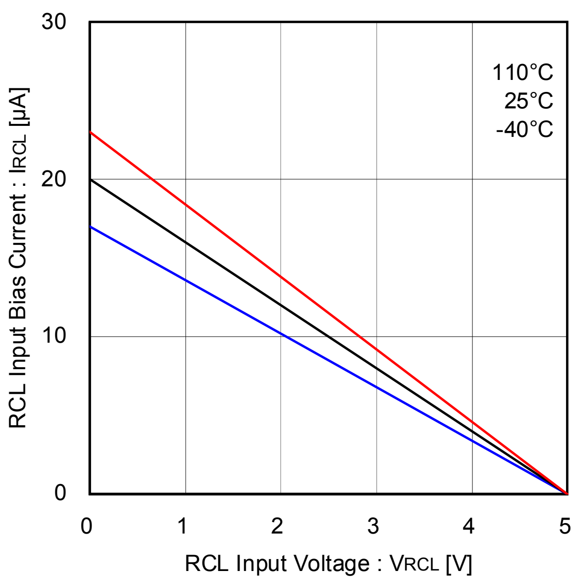


Fig.23 RCL input bias current

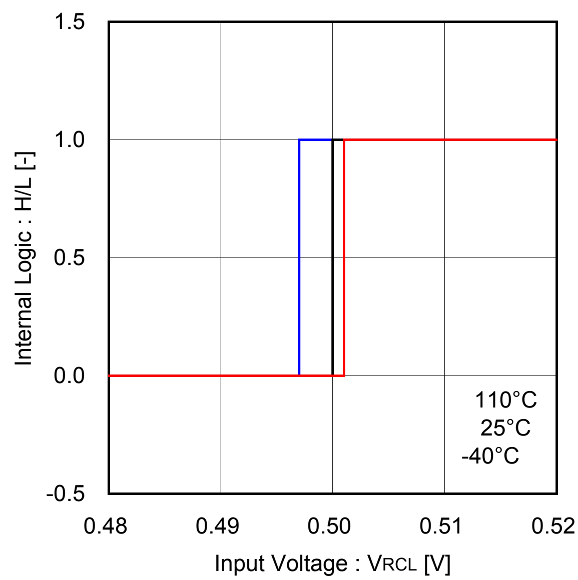


Fig.24 RCL input threshold voltage

● **Typical performance curves (Reference data) - Continued**

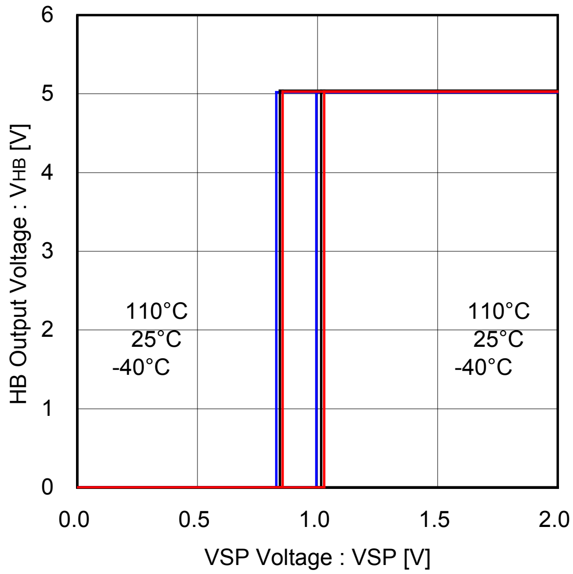


Fig.25 HB enable voltage

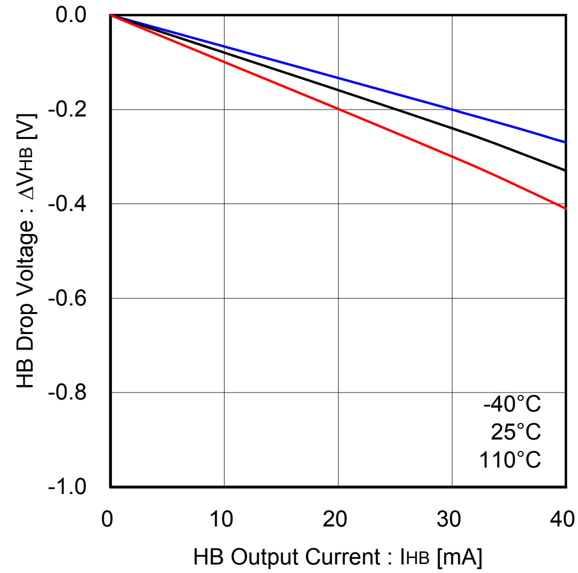


Fig.26 HB output drive capability

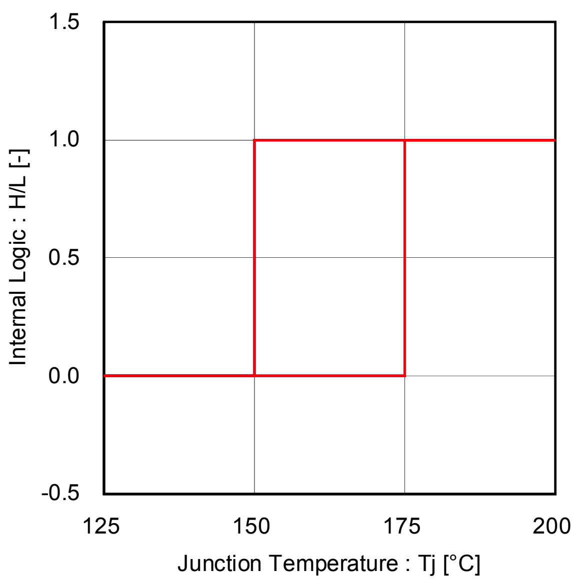


Fig.27 Thermal shut down

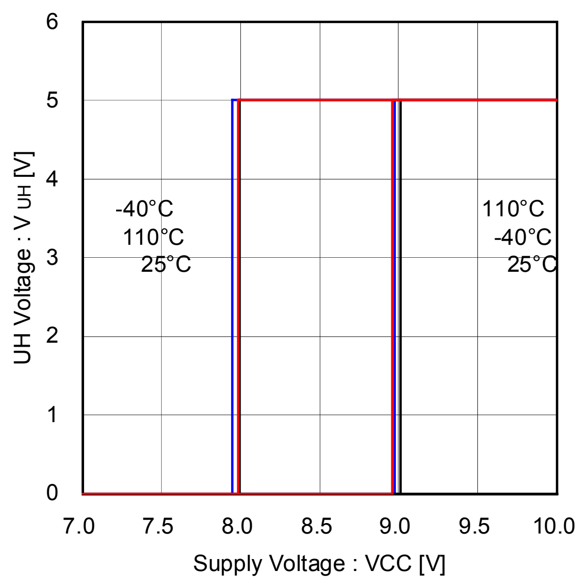


Fig.28 Under voltage lock out (VCC)

● **Typical performance curves (Reference data) - Continued**

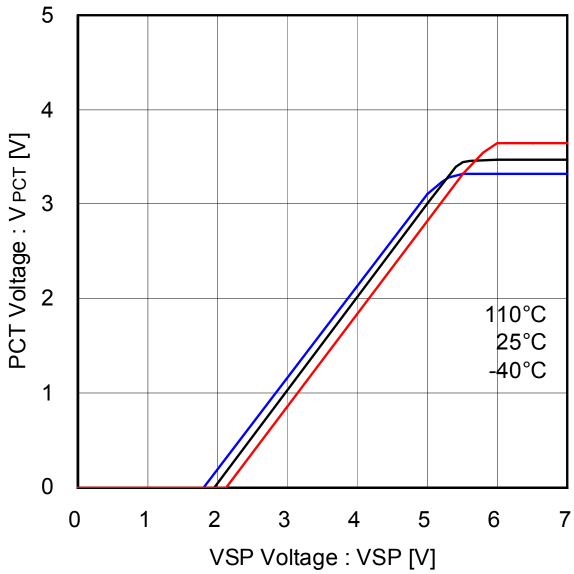


Fig.29 VSP-PCT offset voltage

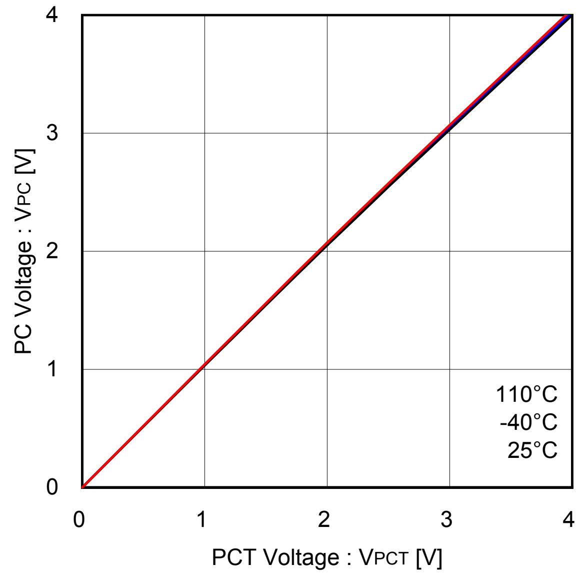


Fig.30 PCT-PC linearity
(RPCT=RPC=100kΩ)

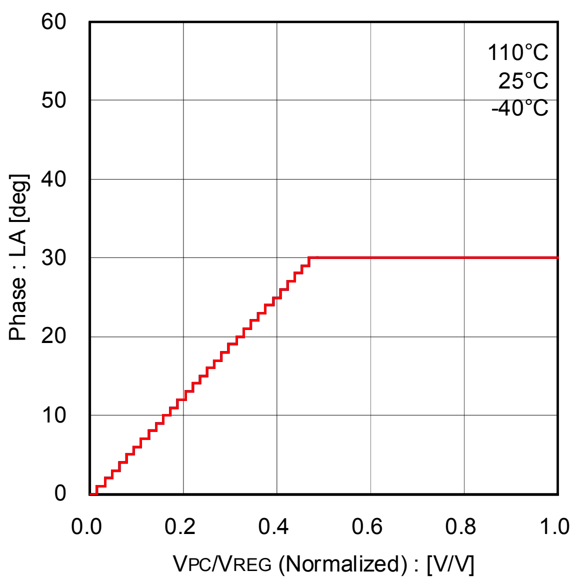


Fig.31 PC voltage normalized - Lead angle

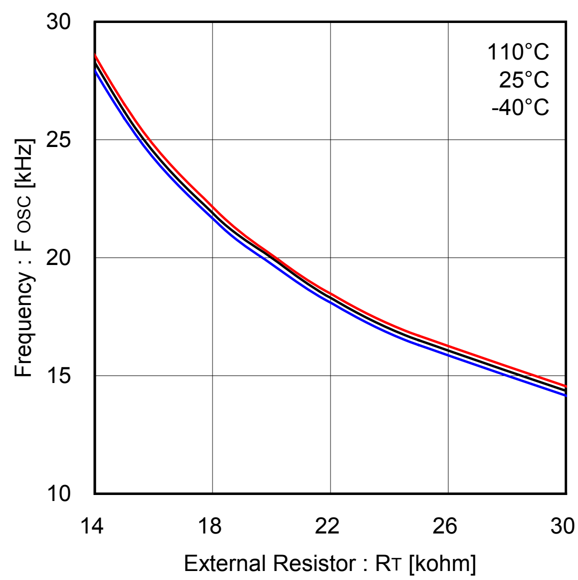


Fig.32 Carrier frequency - RT

● **Application circuit example**

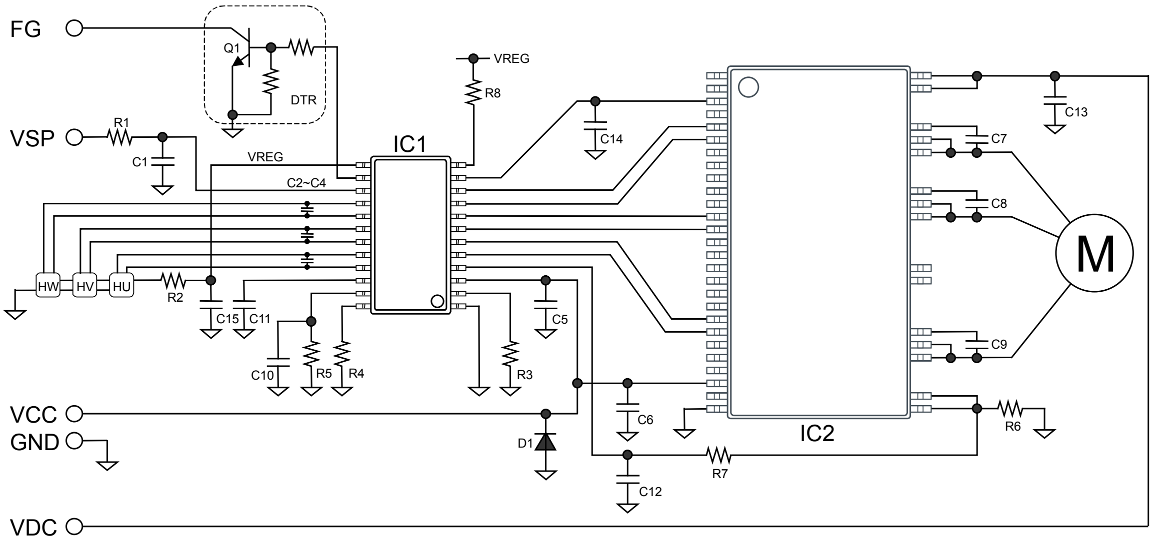


Fig.33 Application circuit example (150° commutation driver)

Parts list

Parts	Value	Manufacturer	Type	Parts	Value	Ratings	Type
IC1	-	ROHM	BD62013FS	C1	0.1µF	50V	Ceramic
IC2	-	ROHM	BM6201FS	C2~4	2200pF	50V	Ceramic
R1	1kΩ	ROHM	MCR18EZPF1001	C5	10 µF	50V	Ceramic
R2	150Ω	ROHM	MCR18EZPJ151	C6	10 µF	50V	Ceramic
R3	22kΩ	ROHM	MCR18EZPF2202	C7~9	1µF	50V	Ceramic
R4	100kΩ	ROHM	MCR18EZPF1003	C10	0.1µF	50V	Ceramic
R5	51kΩ	ROHM	MCR18EZPF5102	C11	1µF	50V	Ceramic
R6	0.5Ω	ROHM	MCR50JZHFL1R50 x 3	C12	100pF	50V	Ceramic
R7	10kΩ	ROHM	MCR18EZPF1002	C13	0.1µF	630V	Ceramic
R8	0Ω	ROHM	MCR18EZPJ000	C14	0.1µF	50V	Ceramic
Q1	-	ROHM	DTC124EUA	C15	1µF	50V	Ceramic
D1	-	ROHM	KDZ20B	HX	-	-	Hall elements

● Interfaces

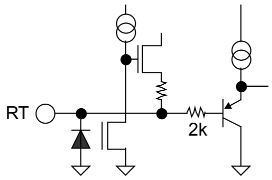


Fig.34 RT

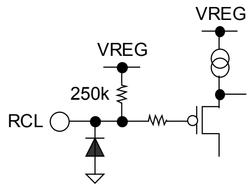


Fig.35 RCL

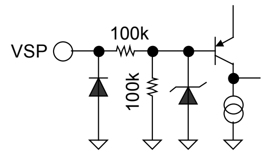


Fig.36 VSP

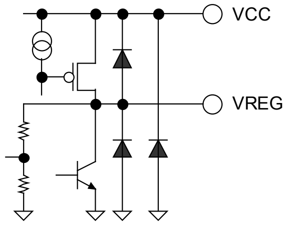


Fig.37 VREG, VCC

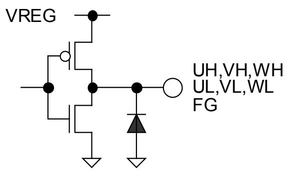


Fig.38 XH, XL, FG

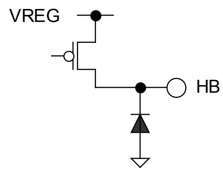


Fig.39 HB

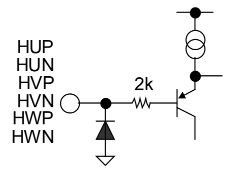


Fig.40 HXP, HXN

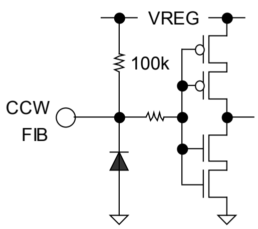


Fig.41 CCW, FIB

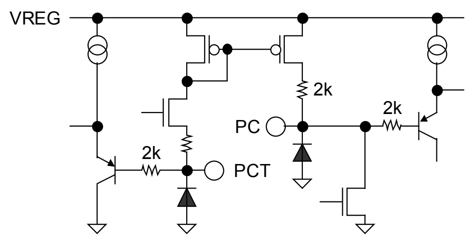


Fig.42 PC, PCT

● Notes for use

1) Absolute maximum ratings
Devices may be destroyed when supply voltage or operating temperature exceeds the absolute maximum rating. Because the cause of this damage cannot be identified as, for example, a short circuit or an open circuit, it is important to consider circuit protection measures - such as adding fuses - if any value in excess of absolute maximum ratings is to be implemented.

2) Electrical potential at GND
Keep the GND terminal potential to the minimum potential under any operating condition. In addition, check to determine whether there is any terminal that provides voltage below GND, including the voltage during transient phenomena. However, note that even if the voltage does not fall below GND in any other operating condition, it can still swing below GND potential when the motor generates back electromotive force at the RCL terminal. The chip layout in this product is designed to avoid this sort of electrical potential problem, but pulling excessive current may still result in malfunctions. Therefore, it is necessary to observe operation closely to conclusively confirm that there is no problem in actual operation. If there are a small signal GND and a high current GND, it is recommended to separate the patterns for the high current GND and the small signal GND and provide a proper grounding to the reference point of the set not to affect the voltage at the small signal GND with the change in voltage due to resistance component of pattern wiring and high current. Also for GND wiring pattern of the component externally connected, pay special attention not to cause undesirable change to it.

3) Driver outputs
The high voltage semiconductor generally driven by this product is connected to the next stage via the controller. If any special mode in excess of absolute maximum ratings is to be implemented with this product or its application circuits, it is important to take physical safety measures, such as providing voltage clamping diodes or fuses.

4) Thermal design
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

5) Inter-pin shorts and mounting errors
Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together. Also, connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply lines, such as establishing an external diode between the power supply and the IC power supply pin.

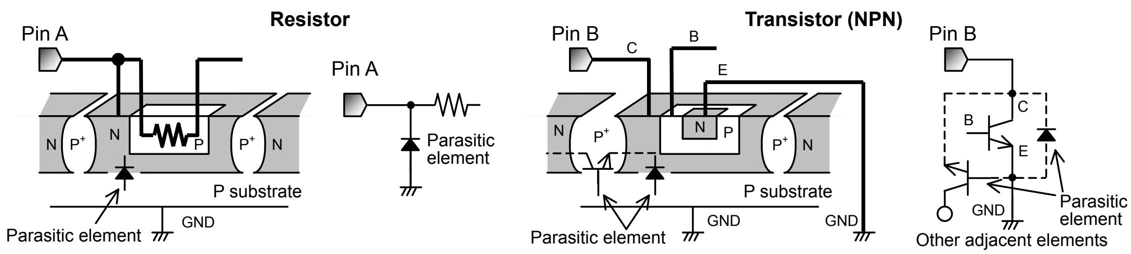
6) Operation in strong electromagnetic fields
Using this product in strong electromagnetic fields may cause IC malfunctions. Use extreme caution with electromagnetic fields.

7) Testing on application boards
When testing the IC on an application board, connecting a capacitor to a low impedance pin subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

8) Regarding the input pin of the IC
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements, in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, as well as operating malfunctions and physical damage. Therefore, do not use methods by which parasitic diodes operate, such as applying a voltage lower than the GND (P substrate) voltage to an input pin.



Appendix: Example of monolithic IC structure

Status of this document
The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document formal version takes priority.

● Ordering information

B	D	6	2	0	1	3	F	S	-	E	2

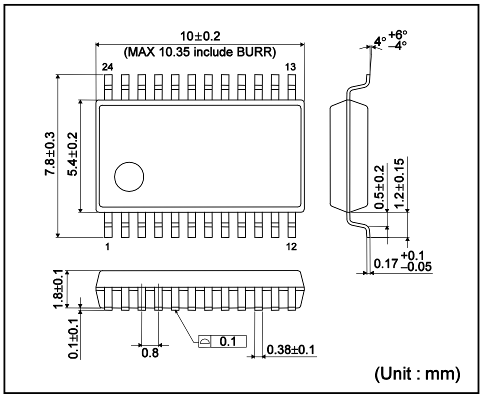
ROHM Part Number

Package
FS : SSOP-A24

Packaging specification
E2 : Embossed taping

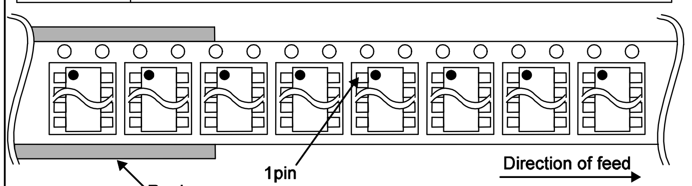
● Physical dimension, tape and reel information

SSOP-A24



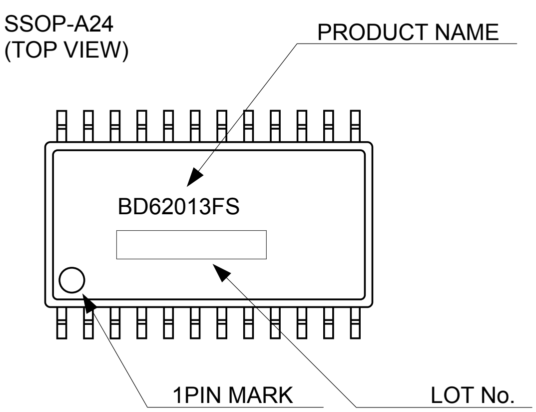
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

● Marking diagram



● **Revision history**

Date	Revision	Changes
01.JUN.2012	001	New release

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4) The Products are not subject to radiation-proof design.

5) Please verify and confirm characteristics of the final or mounted products in using the Products.

6) In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse) is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7) De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8) Confirm that operation temperature is within the specified range described in the product specification.

9) ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

●Precaution for Mounting / Circuit board design

1) When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2) In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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1) If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

●Precaution for Storage / Transportation

1) Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2) Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3) Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4) Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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