R2J20701NP

Peak Current Mode Synchronous Buck Controller with Power MOS FETs

REJ03G1459-0400
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Description

This all-in-one SiP for POL (point-of-load) applications is a multi-chip module incorporating a high-side MOS FET, low-side MOS FET, and PWM controller in a single QFN package. The on and off timing of the power MOS FET is optimized by the built-in driver circuit, making this device suitable for large-current high-efficiency buck converters.

In a simple peak-current mode topology, stable operation is obtained in a closed power loop, and a fast converter is easily realized with the addition of simple components. Furthermore, the same topology can be applied to realize converters for parallel synchronized operation with current sharing, and two-phase operation.

The package also incorporates a high-side bootstrap Schottky barrier diode (SBD), eliminating the need for an external SBD for this purpose.

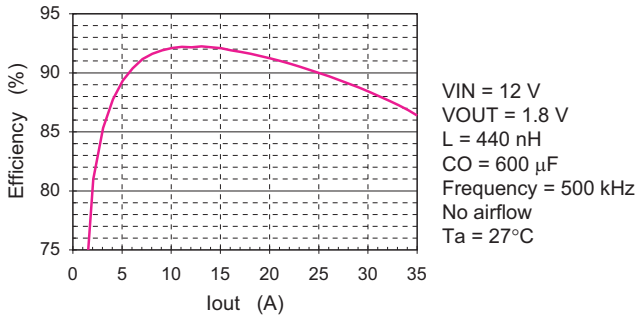
Features

- Three chips in one package for high-efficiency and space saving
- Large average output current (35 A)
- Wide input voltage range: 8 to 14 V
- 0.6 V reference voltage accurate to within 1%
- Wide programmable switching frequency: 200 kHz to 1 MHz
- Fast response by peak-current-mode topology.
- Simple current sharing (up to five modules in parallel)
- Two-phase operation in parallel operation
- Built-in SBD for boot strapping
- On/off control
- Hiccup operation under over load condition
- Tracking function
- Thin small package: 56-pin QFN (8 mm × 8 mm)
- Pb-free

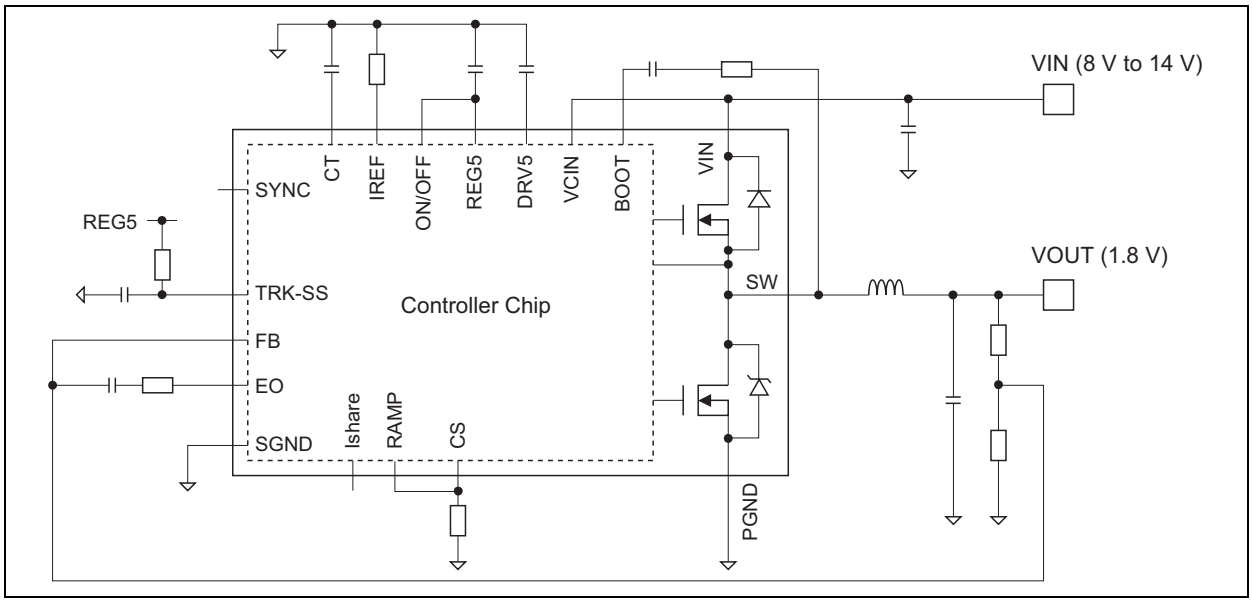
Applications

- Network equipment
- Telecommunications equipment
- Servers
- POL modules

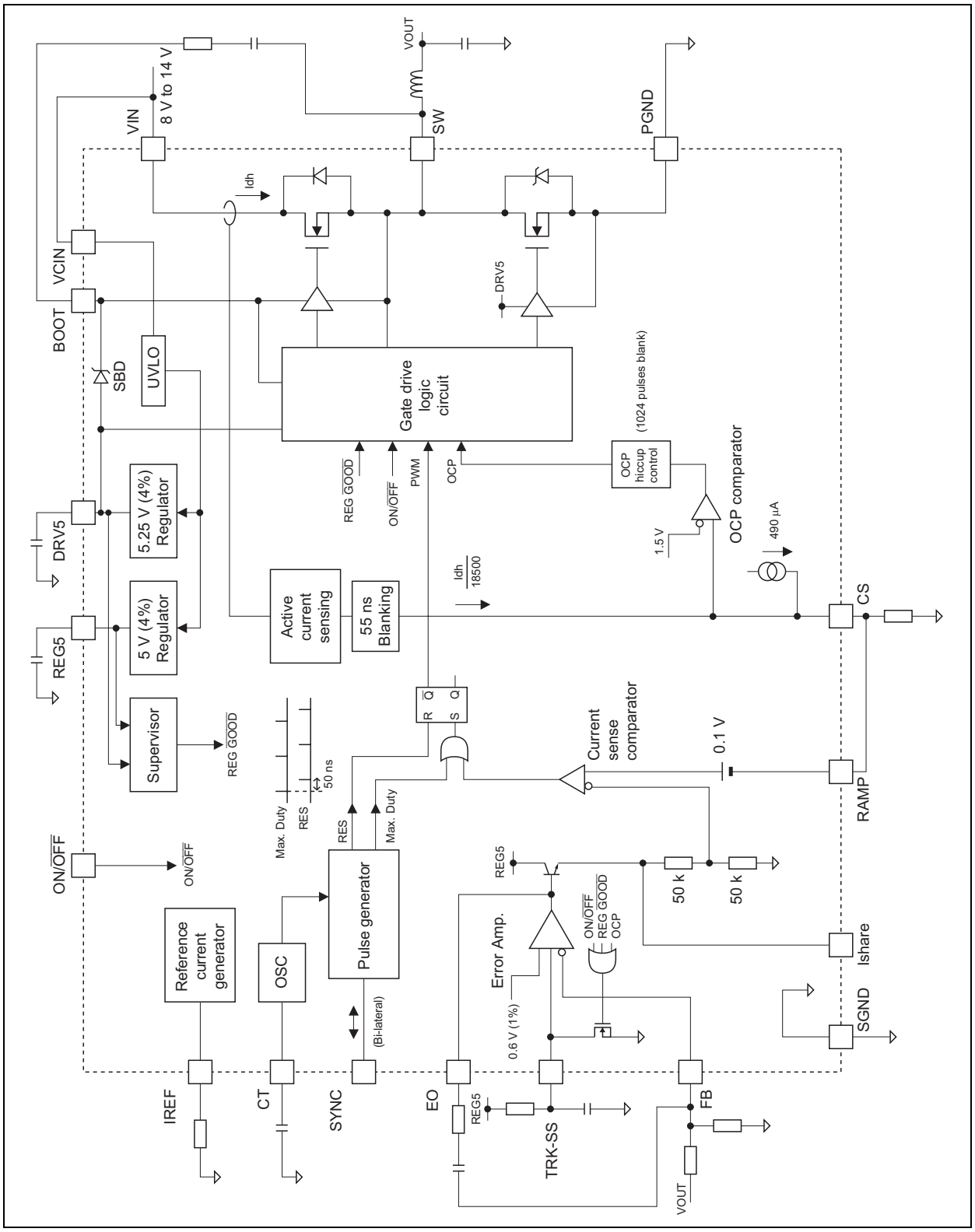
Typical Characteristic Curve



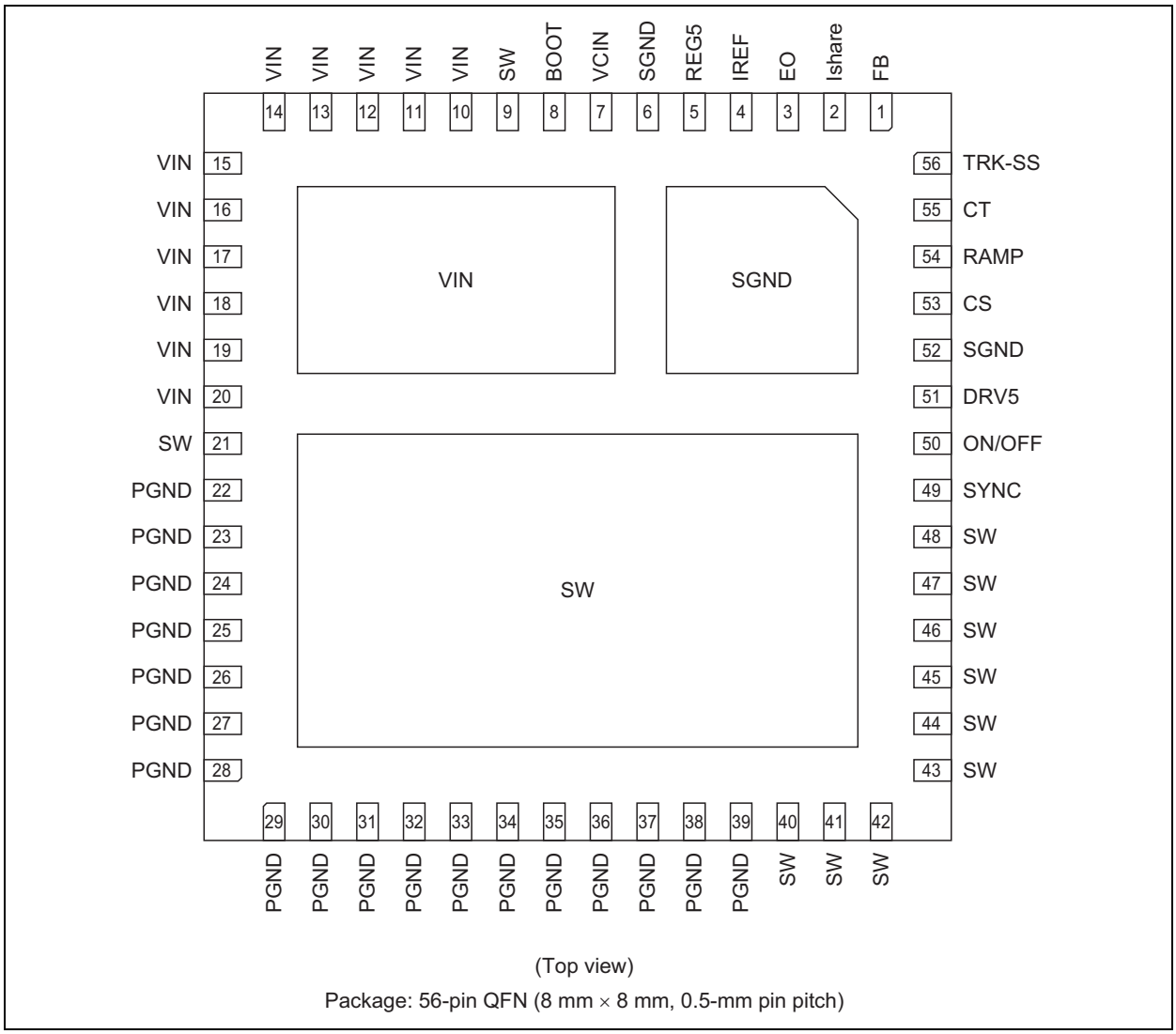
Application Circuit Example



Block Diagram



Pin Arrangement



(Top view)

Package: 56-pin QFN (8 mm × 8 mm, 0.5-mm pin pitch)

Note: All die-pads (three pads in total) should be soldered to PCB.

Pin Description

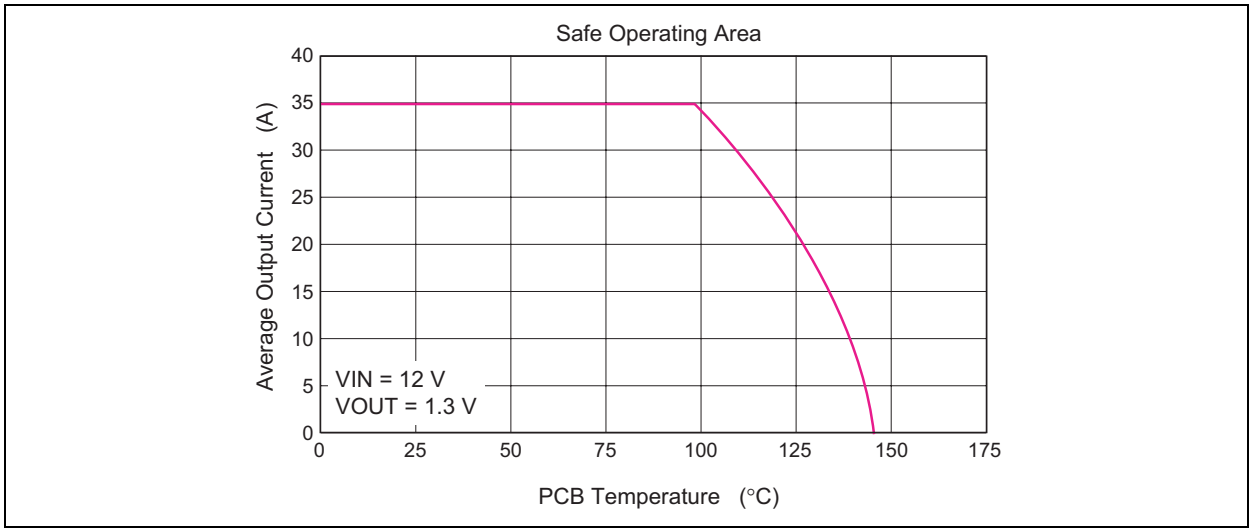
Pin Name	Pin No.	Description	Remarks
VIN	10 to 20	Input voltage for the buck converter.	
SW	9, 21, 40 to 48	Switching node. Connect a choke coil between the SW pin and dc output node of the converter.	
PGND	22 to 39	Ground of the power stage.	Should be externally connected to SGND.
SGND	6, 52	Ground of the IC chip.	Should be externally connected to PGND.
VCIN	7	Input voltage for the control circuit.	Should be externally connected to VIN.
BOOT	8	Bootstrap voltage pin. A bootstrap capacitor should be connected between the BOOT and SW pin.	To be supplied +5 V through the internal SBD.
REG5	5	+5 V logic power-supply output.	Requires decoupling from the GND plane by a capacitance 0.1 μF.
ON/OFF	50	Signal disable pin.	Disabled when ON/OFF pin is in the low state.
IREF	4	Reference current generator for the IC.	Should be connected via 27 kΩ to the SGND pin.
CT	55	Timing capacitor pin for the oscillator. This pin has a select function for operation in slave mode.	If the pin voltage is <1 V or >4 V, the IC operates in slave mode.
SYNC	49	I/O pin for synchronous operation.	
TRK-SS	56	Start-up timing control input.	
FB	1	Feedback voltage input for the closed loop.	
EO	3	Error amplifier output pin.	Requires connection to an RC circuit for loop compensation.
Ishare	2	For current-sharing bus.	Simply connect the Ishare pins of all devices to get balanced current.
RAMP	54	RAMP signal input pin for peak current mode PWM control.	
CS	53	Current output pin of active current sensing circuit.	Appropriate resistance is required between CS and the GND plane.
DRV5	51	+5.25 V generator output for driving power MOS FETs.	Requires decoupling from the GND plane by a capacitance from 0.1 μF to 1.0 μF.

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Rating	Unit	Note
Power dissipation	Pt(25)	25	W	1
	Pt(100)	8		1
Average output current	Iout	35	A	
Input voltage	Vin (dc), Vcin (dc)	–0.3 to +16	V	2
	Vin (ac), Vcin (ac)	20		2, 4
Switch node voltage	Vsw (dc)	16	V	2
	Vsw (ac)	20		2, 4
BOOT pin voltage	Vboot (dc)	22	V	2
	Vboot (ac)	25		2, 4
ON/OFF pin voltage	Von/off	–0.3 to VIN	V	2
SYNC pin voltage	Vsync	–0.3 to +5.5	V	2
Voltage on other pins	Vic	–0.3 to (REG5 + 0.3)	V	2
REG5 current	Ireg5	–10 to 0	mA	3
Ishare current	Ishare	–500 to 0	μA	3
TRK-SS dc current	Itrk	0 to 1	mA	3
IREF current	Iref	–120 to 0	μA	3
EO sink current	Ieo	0 to 2	mA	3
Operating junction temperature	Tj-opr	–40 to +150	°C	
Storage temperature	Tstg	–55 to +150	°C	

Notes: 1. Pt(25) represents a PCB temperature of 25°C, and Pt(100) represents 100°C.
2. Rated voltages are relative to voltages on the SGND and PGND pins.
3. For rated current, (+) indicates inflow to the chip and (–) indicates outflow.
4. Ratings for which “ac” is indicated are limited to within 100 ns.



Electrical Characteristics

(Ta = 25°C, VIN = VCIN = 12 V, unless otherwise specified)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Supply	VIN start threshold	VH	6.8	7.2	7.6	V	
	VIN shutdown threshold	VL	6.45	6.85	7.25	V	
	UVLO hysteresis	dUVL	—	0.35 *1	—	V	
	Input bias current	Iin	36	73	110	mA	CT = 68 pF, Duty cycle = 50%
	Input shutdown current	Isd	3.0	4.5	6.0	mA	On/off = 0 V
5-V regulator	Output voltage	Vreg	4.8	5.0	5.2	V	
	Line regulation	Vreg-line	–5	0	+5	mV	VIN = 10 to 16 V
	Load regulation	Vreg-load	–8	–3	+2	mV	Ireg = 0 to 10 mA
5.25-V regulator	Output voltage	Vdrv	5.04	5.25	5.46	V	
Remote On/off	Disable threshold	Voff	1.0	1.3	1.6	V	
	Enable threshold	Von	2.0	2.5	3.0	V	
	Input current	Ion/off	0.5	2.0	5.0	μA	Von/off = 1 V
Reference current generator	IREF pin voltage	VIref	2.6	2.7	2.8	V	Riref = 27 kΩ
Oscillator	CT oscillating frequency	Fct	—	930 *1	—	kHz	CT = 68 pF
	SW switching frequency	Fsw	418	465	512	kHz	CT = 68 pF
	CT higher trip voltage	Vhct	—	3 *1	—	V	CT = 68 pF
	CT lower trip voltage	Vlct	—	2 *1	—	V	CT = 68 pF
	CT source current	Ict-src	–170	–160	–150	μA	CT = 1.5 V
	CT sink current	Ict-snk	150	160	170	μA	CT = 3.5 V
	CT threshold for two-phase operation	Vct-two	3.6	4.0	4.4	V	
	CT threshold for synchronous operation	Vct-one	0.8	1.0	1.2	V	
SYNC and pulse generator	SYNC frequency	Fsync	418	465	512	kHz	CT = 68 pF
	SYNC high voltage	Vh-sync	4.0	5.0	—	V	Rsync = 51 kΩ to GND
	SYNC low voltage	Vl-sync	0	—	1.0	V	Rsync = 51 kΩ to REG5
	SYNC input threshold	Vsync	1.0	2.0	3.0	V	CT = 0 V or 5 V
Error amplifier	Feedback voltage	Vfb	594	600	606	mV	TRK-SS = 1 V
	Input bias current	Ifb	–0.1	0	+0.1	μA	FB = 0.6 V
	Output source current	Io-src	150	200	250	μA	EO = 4 V, FB = 0 V
	Output sink transient current	Io-snk	5.0	10.6	19.0	mA	EO = 1 V, FB = 1 V
	Voltage gain	Av	—	80 *1	—	dB	
	Band width	BW	—	15 *1	—	MHz	
	Resistance connected to the Ishare pin	Rshare	70	100	130	kΩ	EO = 0 V. Ishare = 1 V

Note: 1. These are reference values for design and have not been 100% tested in production.

(Ta = 25°C, VIN = VCIN = 12 V, unless otherwise specified)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Current sense	CS current ratio	Idh/Ics	—	18500 *1	—	—	
	Leading edge blanking time	TLD	—	55 *1	—	ns	
	CS comparator delay to output	Td-cs	—	50 *1	—	ns	
	OCP comparator threshold on CS pin	Vocp	1.43	1.5	1.57	V	
	Hiccup interval	Tocp	1.98	2.20	2.42	ms	CT = 68 pF
	RAMP offset voltage	Vramp-dc	77	92	107	mV	
	CS offset current	Ics-dc	—	490 *1	—	μA	CS = 0 V

Note: 1. These are reference values for design and have not been 100% tested in production.

Description of Operation

Peak Current Control

The control IC operates in a current-programmed control mode, in which the output of the converter is controlled by the choice of the peak current from the high-side MOS FET. The current from this MOS FET is sensed by an active current-sensing circuit (ACS), the output current of which is 1/18500 (54 ppm) of the MOS FET current. The ACS current is then converted to a certain voltage by the external resistor on the CS pin. The CS voltage is fed to the RAMP pin by an external connection, then compared with the current-control signal which is determined from the error amplifier output voltage (EO) via an NPN transistor and resistor network.

To start with, the RES pulse from the pulse generator resets a latch, then the high-side MOS FET is turned on. The latch output (Q bar) is toggled when the voltage on RAMP reaches the level of the current-control signal on EO, the high-side MOS FET is turned off, and the low-side MOS FET is turned off after a certain dead-time interval. The IC remains in this state until the arrival of the next RES pulse.

Since current information is used in the control loop, loop compensation design for the converter is simple and easy.

Maximum Duty-Cycle Limitation

If the current-sense comparator output is not toggled 50-ns prior to the arrival of the next RES pulse, an internal maximum duty pulse is generated and forces toggling of the SR latch. So, the duty cycle of the high-side MOS FET is limited by the maximum duty period.

The maximum duty period of the high-side MOS FET depends on its switching frequency.

$$\text{Maximum duty period} = 1 - 50\ \text{ns} \times \text{Fsw}$$

OCP Hiccup Operation

Once the voltage of CS exceeds 1.5 V, OCP hiccup circuit disables switching operation of the IC and MOS FETs.

Internal circuitry also pulls the TRK-SS pin down to SGND. The IC is turned off for a period of 1024 RES pulses; after this has elapsed, switching operation of the IC is restarted from the soft-start state.

UVLO and On/off Control

When VIN (=Vcin) is below the start-up voltage, that is, is in the UVLO condition, functioning of the IC is disabled. The oscillator is turned off, both high- and low-side MOS FETs are turned off, and the TRK-SS pin is pulled down.

Furthermore, if the ON/OFF pin is in the low state or left open, functioning of the IC is disabled and both MOS FETs are turned off.

Oscillator and Pulse Generator

The frequency of oscillation is set by the value of the external capacitor connected to the CT pin. This frequency is twice as high as the actual switching frequency. The frequencies are determined by the following equations:

Oscillator frequency; Fct = 160 μA / {2 × (CT(F) + 18 pF) × 1 V} (in Hz)

Switching frequency; Fsw = 0.5 × Fct (Hz)

When the chip is operating in standalone mode or as the master chip for parallel operation, it requires a capacitor on the CT pin. In this case, the SYNC pin outputs a synchronization signal with a frequency of Fsw.

In operation as a slave chip, the CT pin must be connected to SGND or REG5, after which it acts as an input pin for the synchronized operation by external clock. The internal circuit is synchronized its rising edge when CT<0.8 V, falling edge when CT>4.4 V. In two-phase operation in parallel configuration, the CT pin should be at a voltage over 4.4 V.

Item	Mode			
	Standalone	Master	Slave –0°	Slave –180°
CT pin	Has a cap.	Has a cap.	< 0.8 V	> 4.4 V
SYNC pin	Output mode	Output mode	Input mode	Input mode
Synchronizing trigger	—	—	Rising	Falling

The internal RES pulse and maximum duty-cycle-control pulses are produced from the signal at half the oscillator frequency in standalone and master operating modes. In slave mode, internal pulses are produced from the externally supplied input signal on the SYNC pin.

Current Sharing

It is easy to obtain balanced-current operation in a parallel configuration due to the application of peak current control.

To obtain current-sharing operation, simply tie the buffered error-amplifier outputs of all of the devices (Ishare pins) together.

No more than five devices can operate in parallel.

Soft Start

Both simple soft starting and tracking start-up can be realized with the setup of the TRK-SS pin provided for soft-starts. The error amplifier has three inputs, two of which are designed to give priority to low-level non-inverting inputs for the amplifier. All that is required to realize soft-start operation is to simply attach an RC charging circuit to the TRK-SS pin.

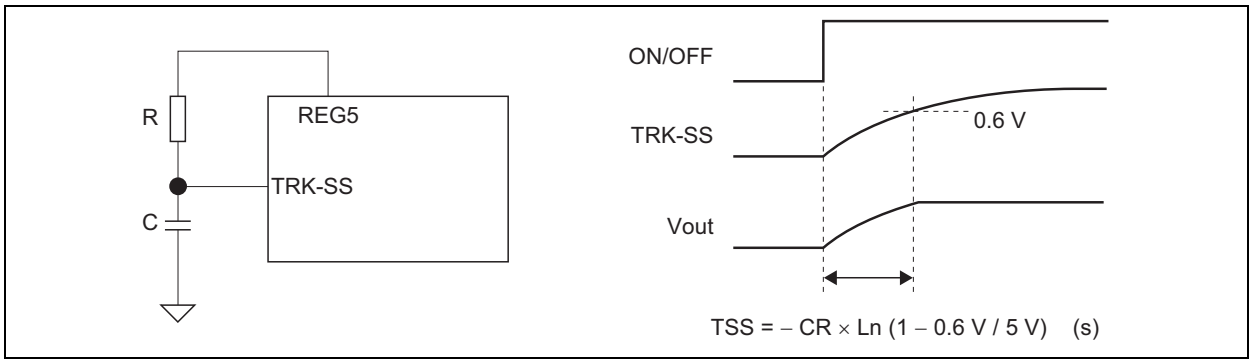
The soft-start period is determined by the following equation, with C and R as the values for the RC charging circuit attached to the TRK-SS pin.

Tss = –C · R · Ln (1 – 0.6 V / REG5) (s)

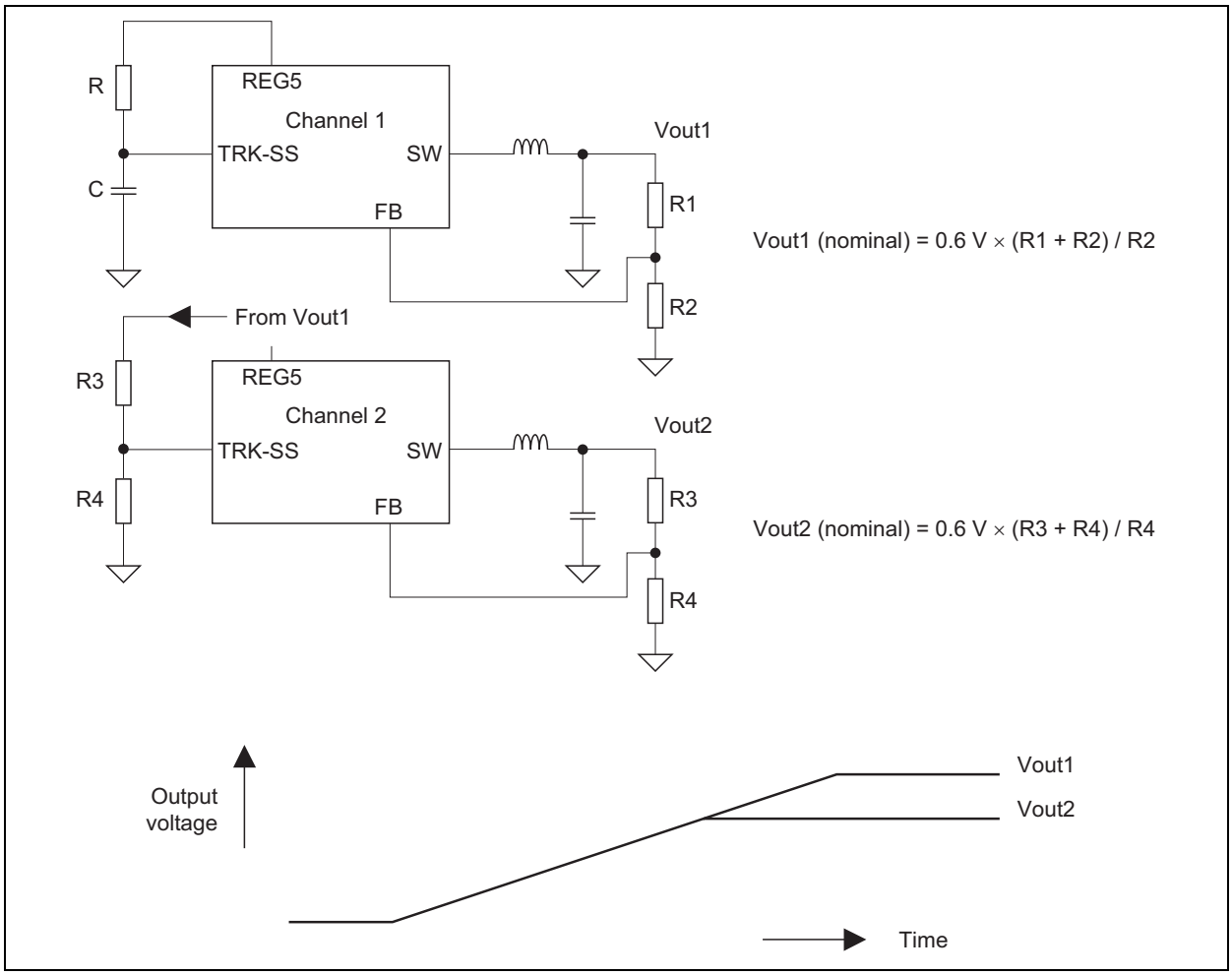
Application Example

Start-up Settings

Case 1) Standalone or master chip in parallel operation
With the RC network on the TRK-SS pin, the voltage on the pin should ramp up slowly.



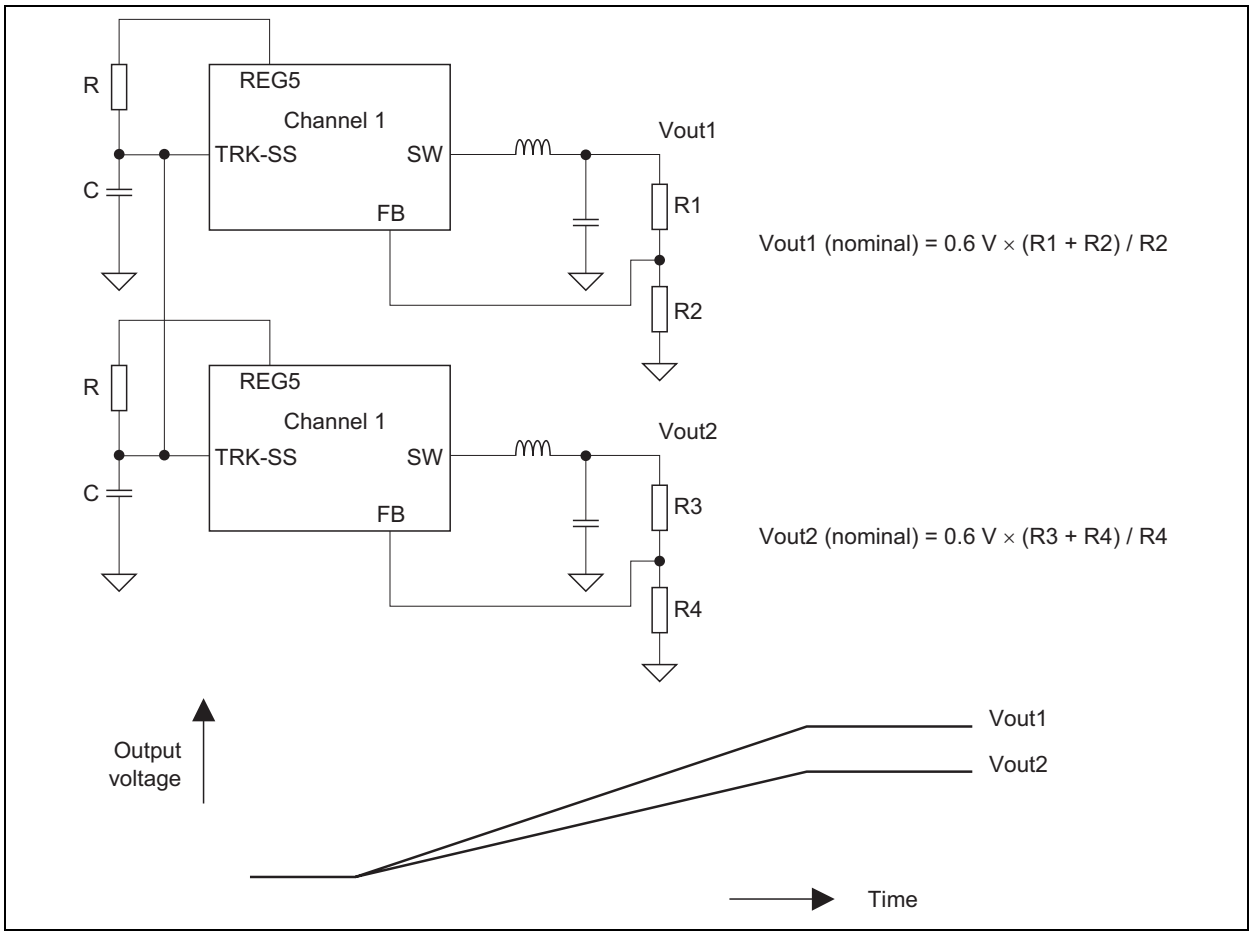
Case 2) Coincident tracking
The TRS-SS signal for channel two is the voltage from Vout1 after division by a resistor network. Vout1 must be greater than Vout2. Cross-talk is not generated between the channels.



Case 3) Retiometric tracking

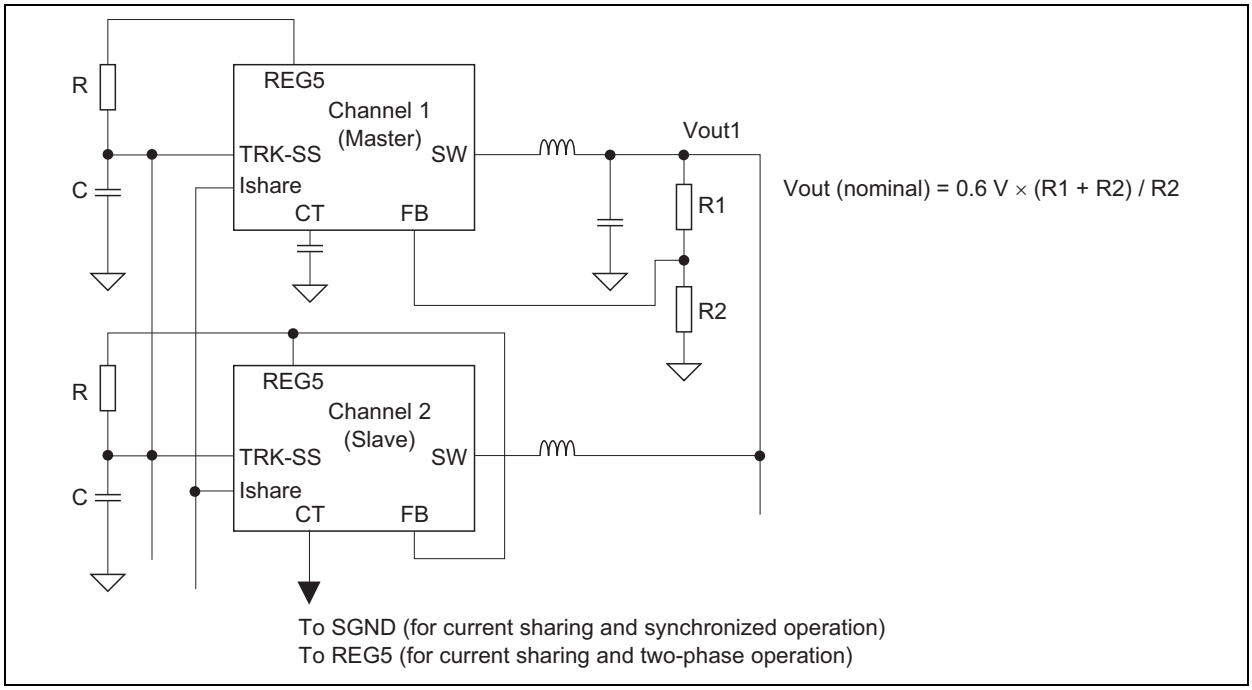
The TRS-SS of channel two is tied to TRK-SS of channel 1.

No cross talk is observed between the channels.



Case 4) Current sharing or two-phase operation

In the case of master–slave operation, the TRK-SS pin on the master device should be attached to an RC network for soft starts. TRK-SS pins of slave devices should be tied to the master's TRK-SS pin. The error amplifiers on the slave devices can be disabled by pulling up the corresponding FB pins to REG5, and the slave devices do not require loop-compensation networks.



Choice of The Resistance of CS Pin

The CS pin is a current-output pin. A current 1/18500 of that of the high-side MOS FET flows through this pin, which also has a dc current offset of 490 μA. The converter's maximum current is determined by the voltage on the CS pin, i.e. 1.5 V, and by the value of the external resistor attached to this pin. The resistance is determined as shown below.

Specification: L = 360 nH, Vin = 12 V, Vout = 1.8 V, Fsw = 500 kHz, Iout(max) = 25 A

Current through the choke coil is

$$ILpp = (Vin - Vout) \times Vout / (L \times Vin \times Fsw) = 8.5\ A\ (p\text{-}p)$$

Peak choke current is the current when Io is at its maximum, i.e.

$$Ilmax = Io(max) + 0.5 \times ILpp = 25A + 4.25A = 29.25\ A$$

Maximum CS pin output current is;

$$Icsmax = Ilmax / 18500 + Ics\text{-}dc = 29.25\ A / 18500 + 490\ \mu A = 2.071\ mA$$

The ideal resistance for attachment to the CS pin is

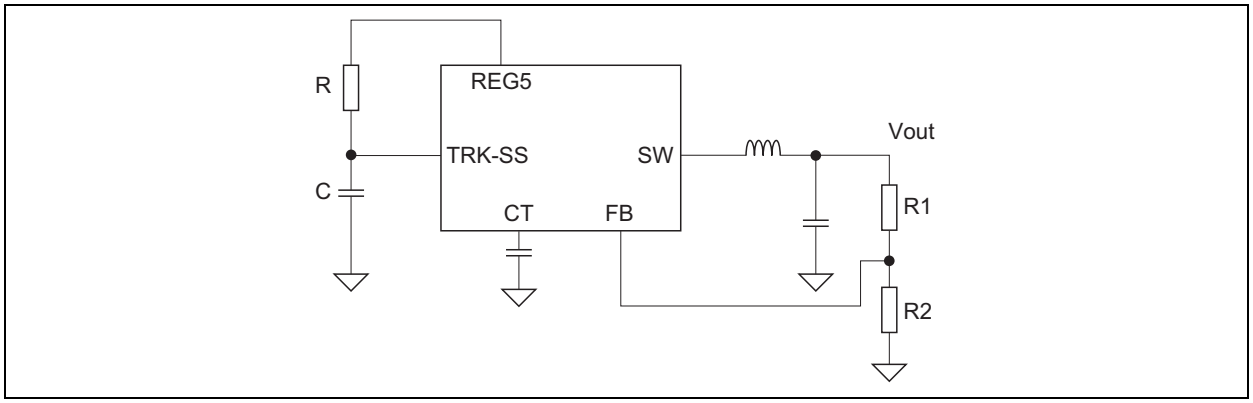
$$RCS = Vcl / Icsmax = 1.5\ V / 2.071\ mA = 724\ \Omega$$

Therefore choose 750 Ω as the value of the resistor for attachment to the CS pin.

Output Voltage Setting

The error amplifier of the device has an accurate 0.6 V reference voltage. Feedback thus leads to a voltage of about 0.6 V on the FB pin once the converter system has stabilized, so the output voltage is

$$Vout = 0.6\ V \times (R1 + R2) / R2$$



Loop Compensation

Peak-current control makes design in terms of phase margins easier than is the case with voltage control. This is because of differences between the characteristics of the PWM modulator and power stage in the two methods.

Figures 1 and 2 show the behavior of the PWM modulator and power stage in the cases of voltage control and peak current control, respectively.

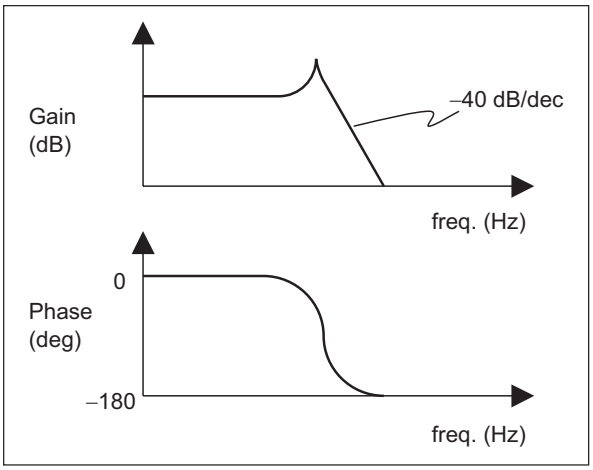


Figure 1 Bode Plot of Modulator + Power Stage (Voltage Mode)

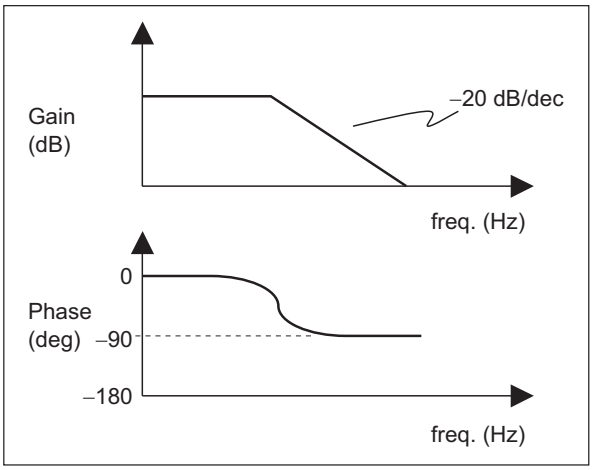


Figure 2 Bode Plot of Modulator + Power Stage (Peak Curent Mode)

Feed-forward current to the modulator in the case of peak-current control means that the system is single pole, so we see a –20 dB/decade cutoff and phase margin of 90° in the Bode plot. In voltage control, the system configures a two-pole pole system. That is why rather complicated loop compensation of the error amplifier is required, such as type-III compensation.

The design of effective compensation is thus much simpler in the case of peak-current control (refer to figure 3).

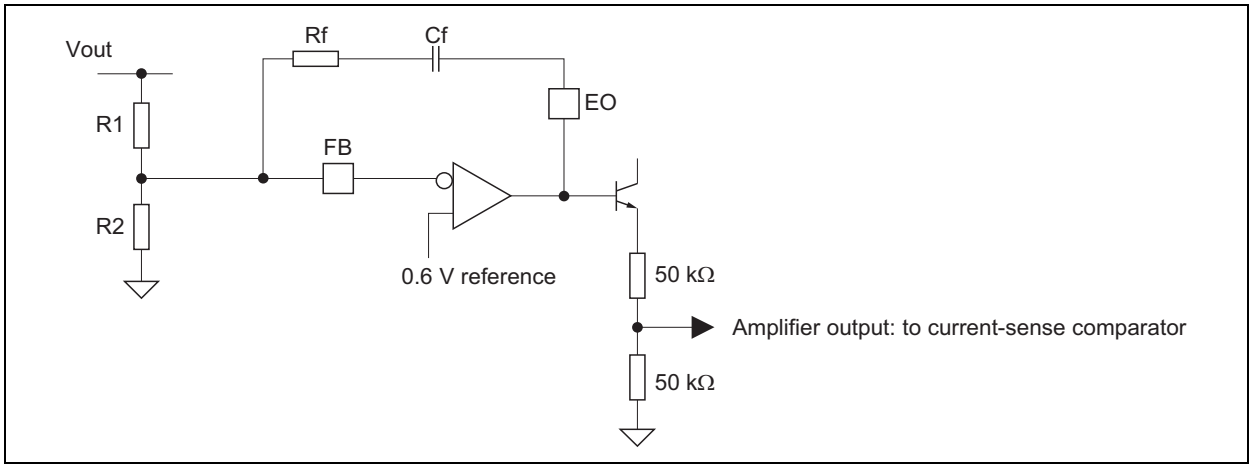


Figure 3 Error Amplifier Compensation

Design example

Specification: L = 360 nH, Co = 600 μF, Fsw = 500 kHz, Vin = 12 V, Vout = 1.8 V, R1 = 2 kΩ, R2 = 1 kΩ, RCS = 750 Ω

1. Flat-band gain of error amplifier

   The flat-band gain is; $Af = Rf / (R1 // R2) / 2 \times \{R2 / (R1 + R2)\}$

   $$\text{Hence, } Rf = 2 \times Af \times R1 \quad \ldots\ldots(1)$$

   In the Bode plot, the total gain should be less than 1 (0 dB) at the switching frequency.
   The total gain at Fsw (= Asw) depends on the flat-band gain, so Af should be expressed as follows.

   $$Af = Asw \times 2\pi \times Fsw \times Co \times RCS / Nt \quad \ldots\ldots(2)$$

   $$\text{Here, } Nt = Idh / Ics = 18500$$

   In the typical way, the value chosen for Asw is in the range from 0.1 to 0.5, since this produces a stable control loop.
   The transient response will be faster if a larger Asw is adopted ,but the system might be unstable.
   We choose 0.2 for Asw in the example below.

   $$Af = 0.2 \times 2\pi \times 500\ \text{kHz} \times 600\ \mu\text{F} \times 750\ \Omega / 18500 = 15.283$$

   $$Rf = 2 \times 15.283 \times 2\ \text{k}\Omega = 61.132\ \text{k}\Omega$$

   Therefore, we select a value of 62 kΩ for Rf.

2. Selecting the Cf value to determine the frequency of the zero

   The frequency of the zero established by Cf and Rf is about ten times the frequency of the pole for the power stage and modulator.
   We must start with the dc gain of the power stage and modulator.

   $$A0 = \frac{2 \times Nt / RCS \times L \times Vin \times Fsw}{SQRT\{Vin^2 - 8 \times L \times Vin \times Fsw \times (VCS0 \times Nt / RCS)\}} \quad \ldots\ldots(3)$$

   Here VCS0 is the peak ac voltage on the CS pin when the load current is zero, thus

   $$VCS0 = 0.5 \times RCS \times (Vin - Vout) \times Vout / (L \times Vin \times Fsw) / 18500 \quad \ldots\ldots(4)$$

   $$= 0.5 \times 750\ \Omega \times (12\ \text{V} - 1.8\ \text{V}) \times 1.8\ \text{V} / (360\ \text{nH} \times 12\ \text{V} \times 500\ \text{kHz}) / 18500$$

   $$= 0.172\ \text{V}$$

Equation (3)

$$A0 = \frac{2 \times Nt / RCS \times L \times Vin \times Fsw}{SQRT\{Vin^2 - 8 \times L \times Vin \times Fsw \times (VCS0 \times Nt / RCS)\}} \quad \ldots\ldots(3)$$

$$= \frac{2 \times 18500 / 750\ \Omega \times 360\ nH \times 12\ V \times 500\ kHz}{SQRT\{12\ V^2 - 8 \times 360\ nH \times 12\ V \times 500\ kHz \times (0.172\ V \times 18500 / 750\ \Omega)\}}$$

$$= \frac{106.56}{SQRT\{70.687\}}$$

$$= 12.674$$

The frequency of the pole established by the power stage and modulator is

$F0 = Nt / (2 \pi \times Co \times RCS \times A0)$ ……(5)

Thus,

$F0 = 18500 / (2 \pi \times 600\ \mu F \times 750\ \Omega \times 12.674) = 516\ Hz$

Therefore, the frequency of the zero established by Cf and Rf is

$Fzero = 10 \times F0 = 5.16\ kHz$

$Cf = (2 \pi \times Fzero \times Rf)^{-1} = (2 \pi \times 5.16\ kHz \times 62\ k\Omega)^{-1} = 497\ pF$

Therefore, we select the value 510 pF for Cf.

Basically, the transient response is faster when Cf is smaller, but too small a value will make the system-loop unstable.

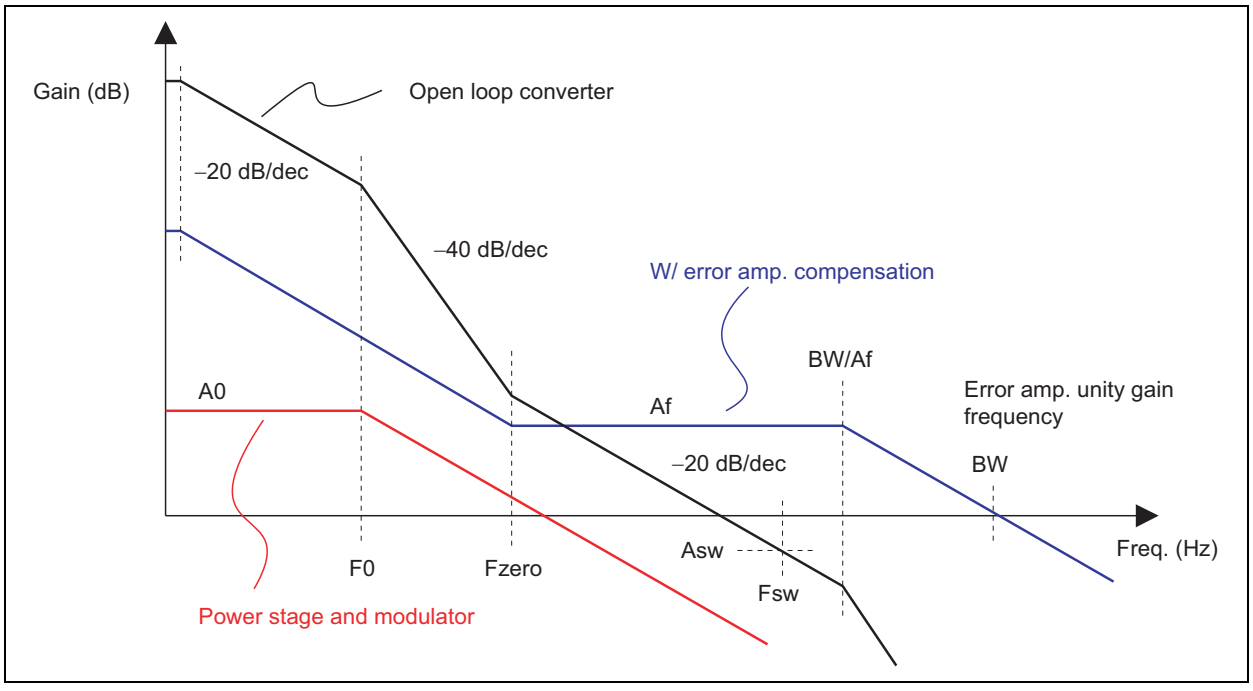


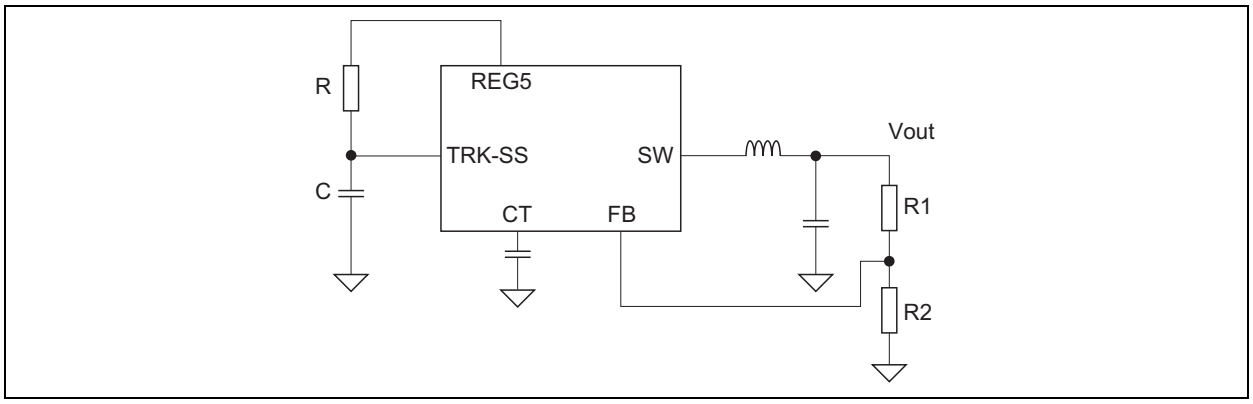
Figure 4

Study of Vout Accuracy

The nominal output voltage is calculated as

$$Vout = VFB \times (R1 + R2) / R2 \quad \ldots\ldots(6)$$

Here, the typical feedback voltage is 0.6 V.



The accuracy of Vout is strongly dependent on the variation of VFB, R1 and R2. VFB has a variation of 1% and resistance intrinsically has a certain variation. When we take the variation in resistance into account, equation (6) is extended to produce equation (7).

$$Vout = \frac{R1 \times K1 + R2 \times K2}{R2 \times K2} \times VFB$$

$$= \frac{R1 \times K1 / K2 + R2}{R2} \times VFB \quad \ldots\ldots(7)$$

Here, K1 and K2 are coefficients. Both are 1.00 in the ideal case.

By equation (6), R1 is chosen as

$$R1 = \left[\frac{Vout\ (typical)}{VFB\ (typical)} - 1 \right] \times R2 \quad \ldots\ldots(8)$$

Substituting this expression for R1 into equation (7) yields the following.

$$Vout = VFB \times \left\{ \left[\frac{Vout\ (typical)}{VFB\ (typical)} - 1 \right] \times \frac{K1}{K2} + 1 \right\} \quad \ldots\ldots(9)$$

Therefore, variation in Vout is expressed as

$$\frac{Vout}{Vout\ (typical)} = \left[\frac{VFB}{Vout\ (typical)} \times \left\{ \left[\frac{Vout\ (typical)}{VFB\ (typical)} - 1 \right] \times \frac{K1}{K2} + 1 \right\} - 1 \right] \times 100\ (\%) \quad \ldots\ldots (10)$$

The accuracy of Vout can be estimated by using equation (10).

For example, if Vout (typical) = 1.8 V, resistance variation is 1% (i.e. K1, K2 = 1.01 and 0.99), and VFB = 594 mV to 606 mV:

$$\frac{\text{Vout}}{\text{Vout (typical)}} = \left[\frac{\text{VFB}}{\text{Vout (typical)}} \times \left\{ \left[\frac{\text{Vout (typical)}}{\text{VFB (typical)}} - 1 \right] \times \frac{\text{K1}}{\text{K2}} + 1 \right\} - 1 \right] \times 100 \ (\%) \quad \ldots\ldots (10)$$

$$= \left[\frac{606 \text{ mV}}{1.8 \text{ V}} \times \left\{ \left[\frac{1.8 \text{ V}}{600 \text{ mV}} - 1 \right] \times \frac{1.01}{0.99} + 1 \right\} - 1 \right] \times 100 \ (\%)$$

$$= 2.36\%$$

or

$$= \left[\frac{594 \text{ mV}}{1.8 \text{ V}} \times \left\{ \left[\frac{1.8 \text{ V}}{600 \text{ mV}} - 1 \right] \times \frac{0.99}{1.01} + 1 \right\} - 1 \right] \times 100 \ (\%)$$

$$= -2.31\%$$

Therefore, the output accuracy will be ±2.3% under the above conditions.

Figure 5 shows the relationship between the accuracy of the resistance and the accuracy of the output voltage. The resistor value must have an accuracy of 0.5% if the variation in output voltage from the system is to be kept within two percent across the voltage range from 0.6 to 3.3 V.

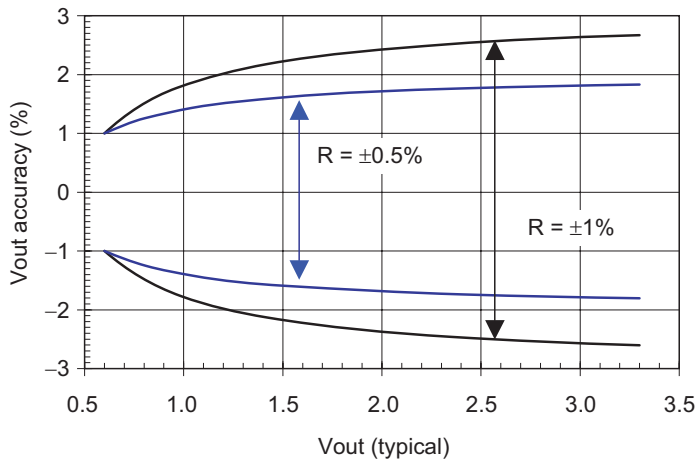
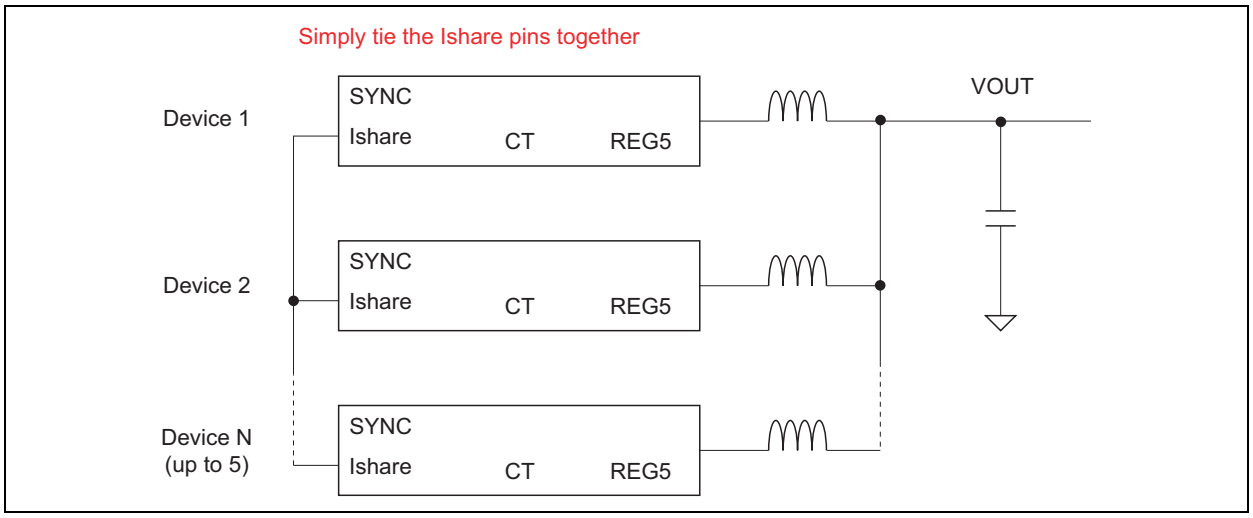
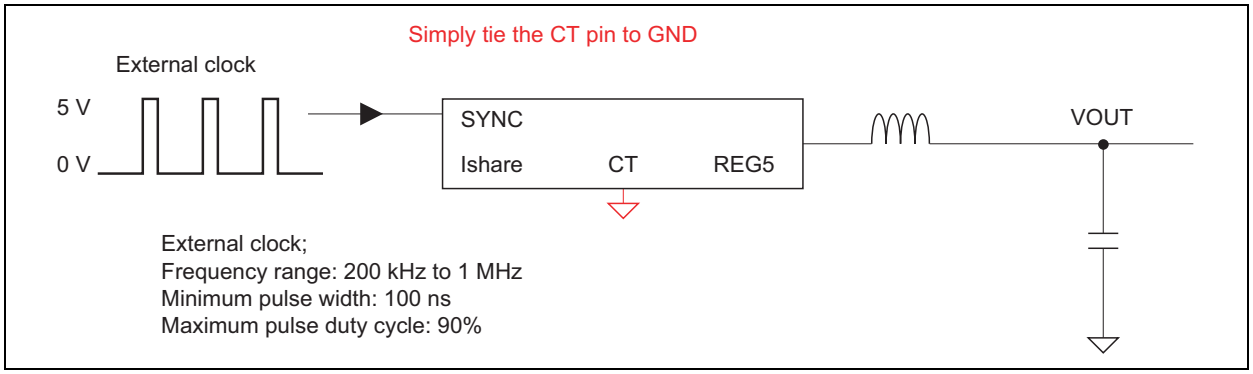


Figure 5 Vout Accuracy vs. Vout Set Voltage

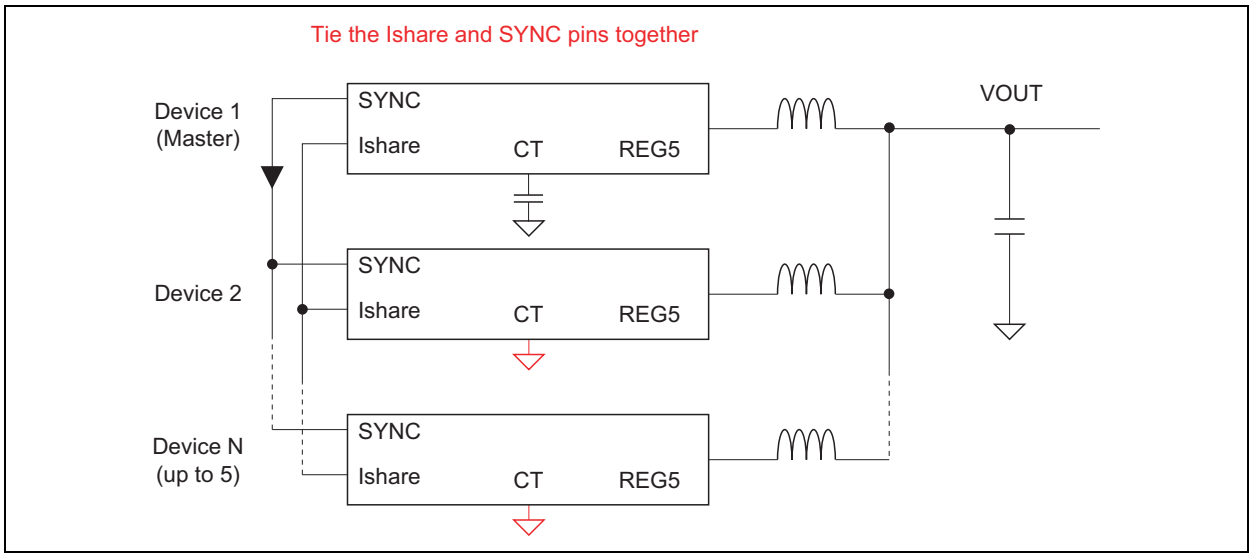
Current Sharing



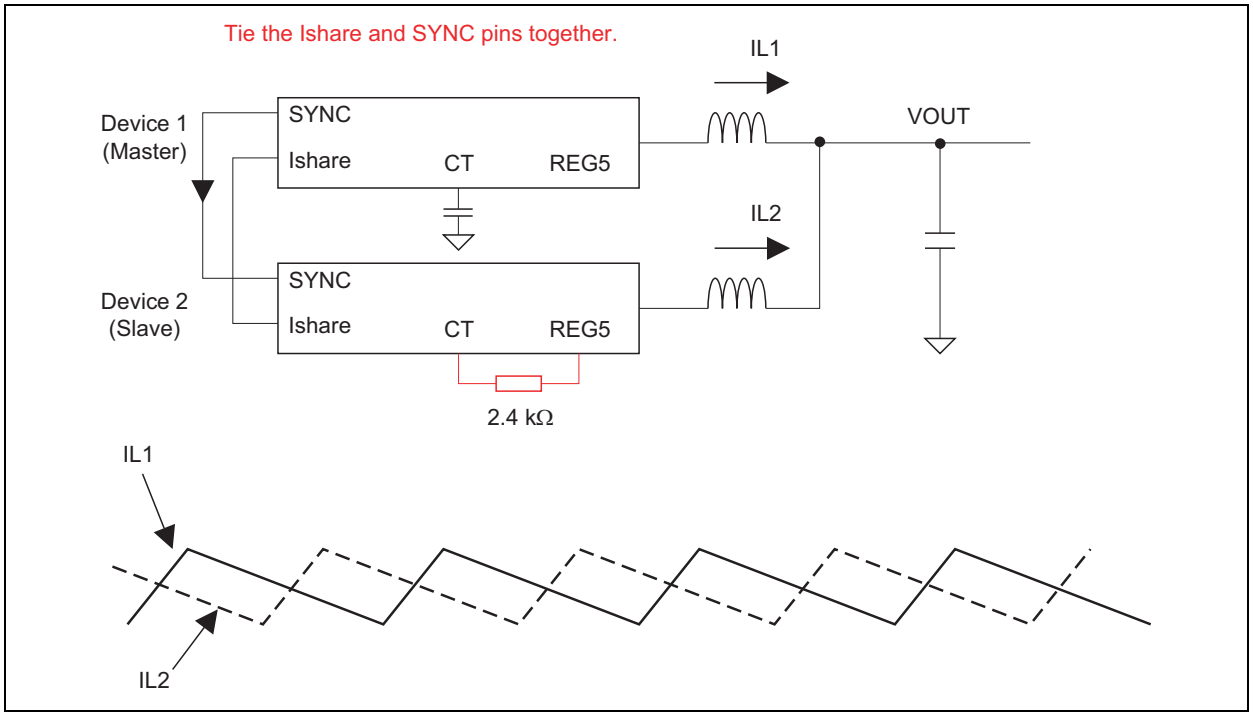
External Synchronization



Current Sharing and Synchronization

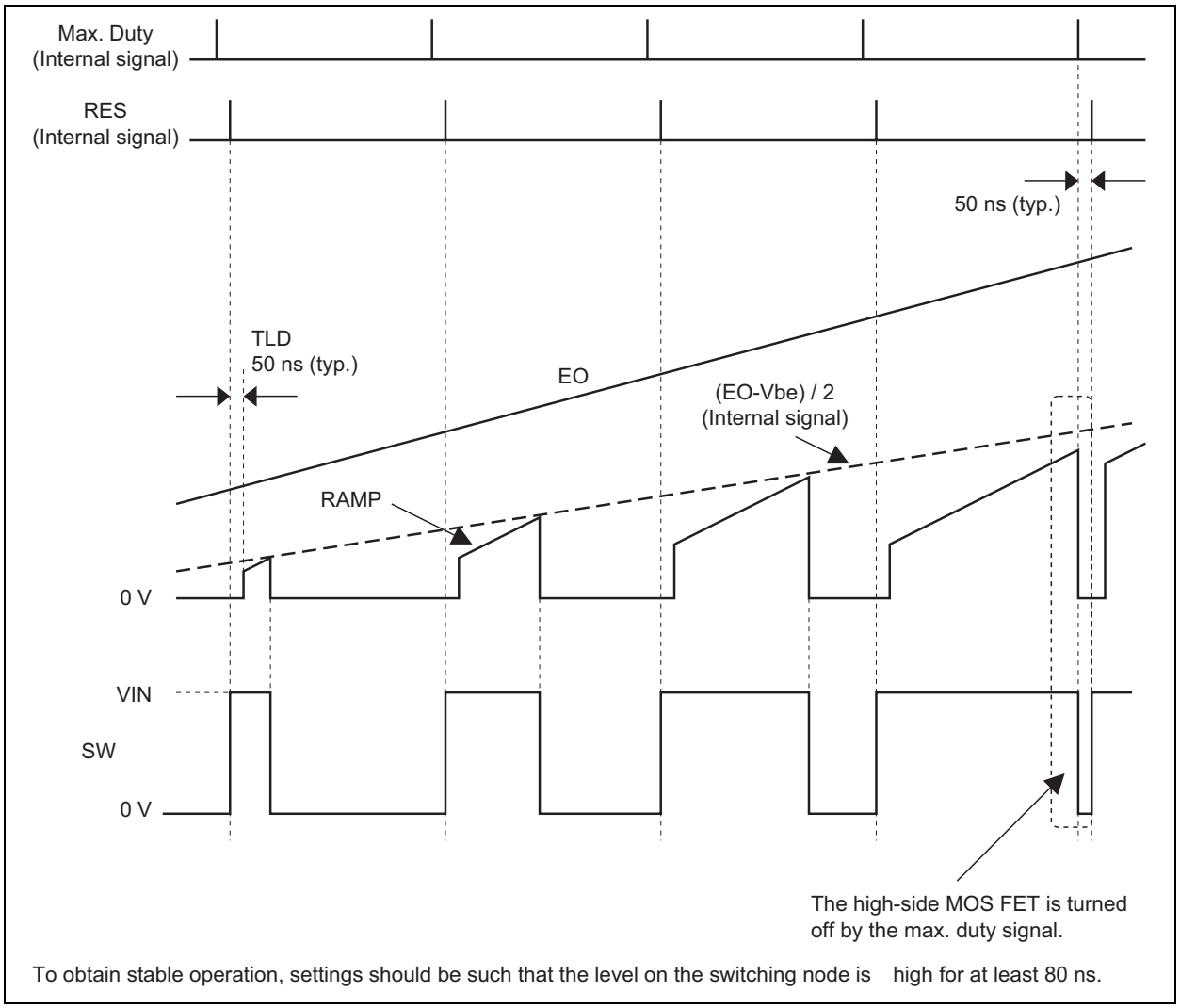


Two-Phase Operation



Timing Chart

Peak Current Control

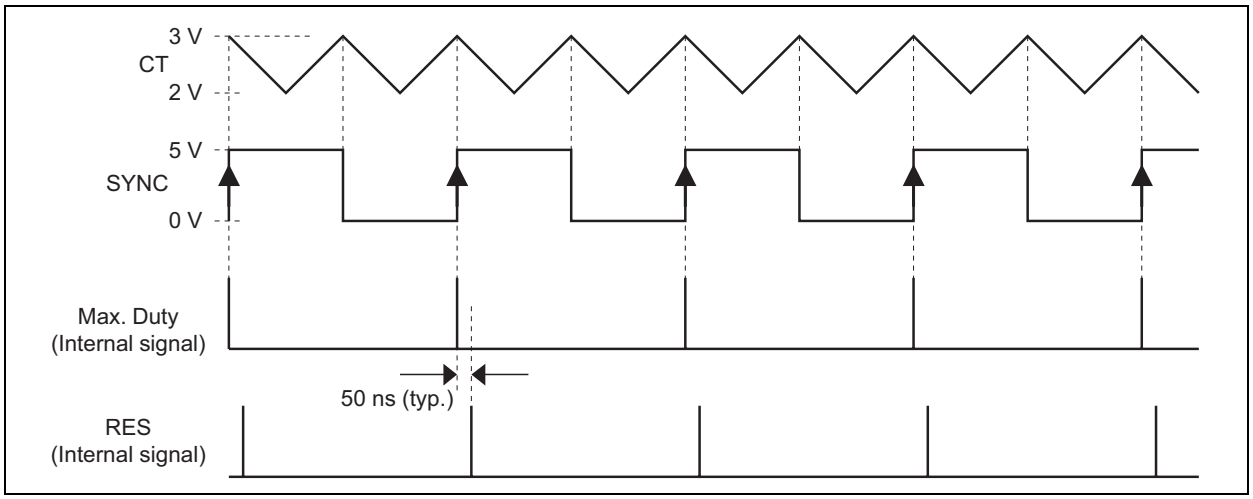


To obtain stable operation, settings should be such that the level on the switching node is high for at least 80 ns.

Note: Propagation delay is ignored.

Oscillator and Pulse Generator

1. Standalone operation or operation as the master chip in a parallel configuration with other chips.



Note: Propagation delay is ignored.

Frequency of oscillation for CT:

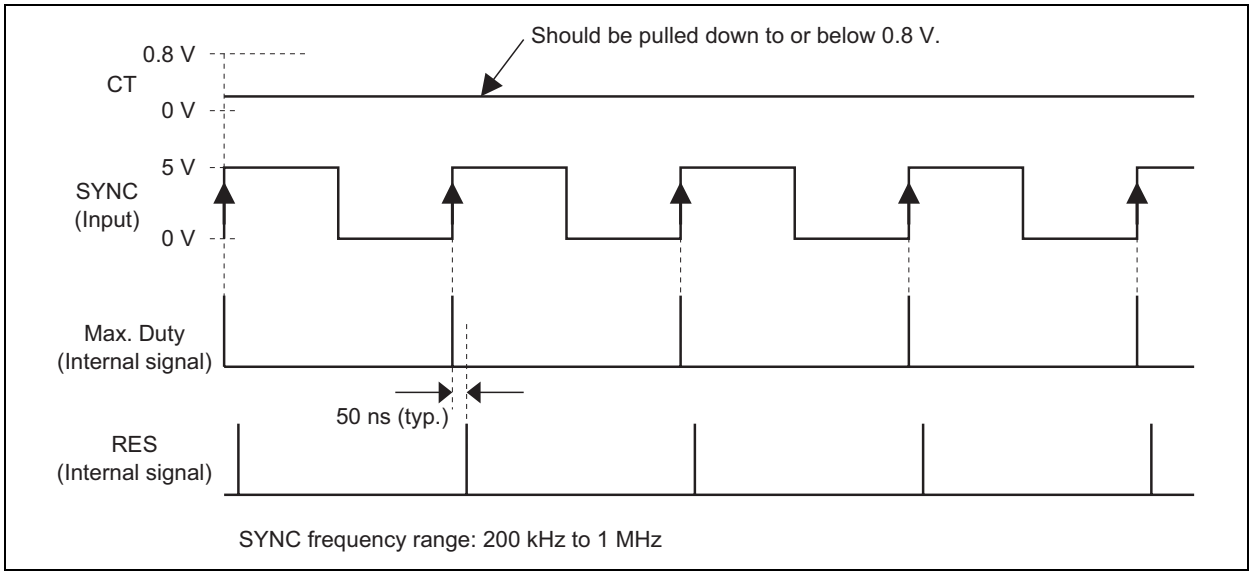
$$Fct = \frac{160\ \mu A}{2 \times (CT(F) + 18\ pF) \times 1\ V} \quad (Hz)$$

Switching frequency

$$Fsw = 0.5 \times Fct \quad (Hz)$$

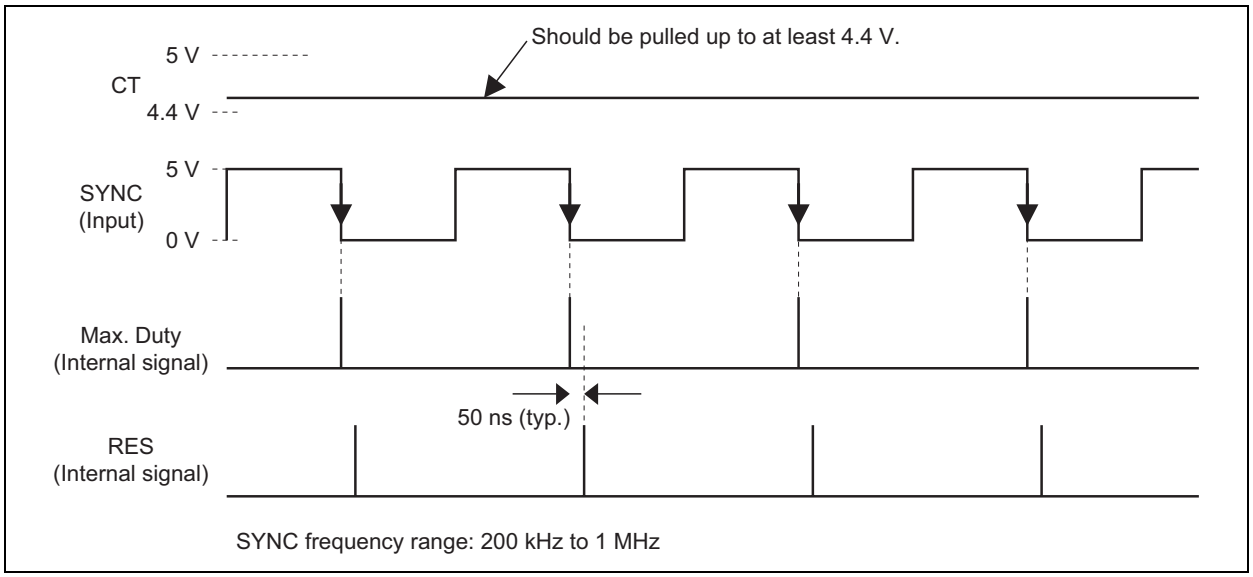
Frequency setting range (for Fsw): 200 kHz to 1 MHz (i.e. 400 kHz to 2 MHz for Fct)

2. Operation as a slave chip (simple synchronous operation)



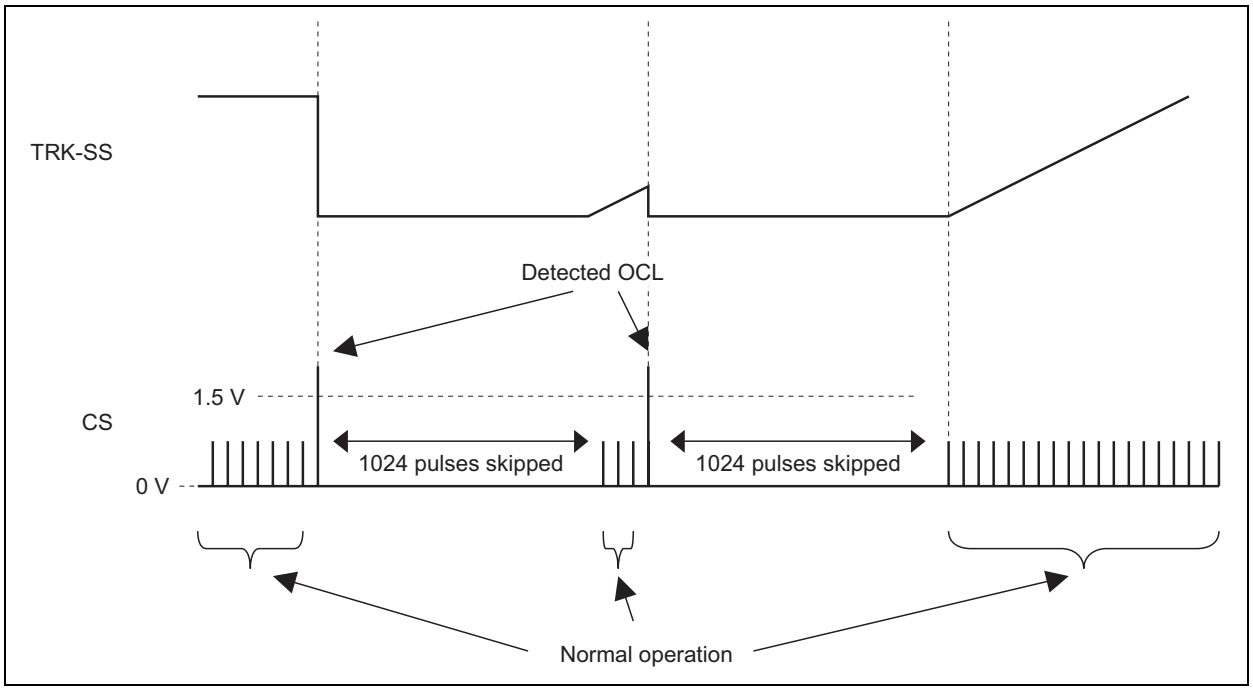
Note: Propagation delay is ignored.

3. Operation as a slave chip in a parallel configuration (two-phase operation)



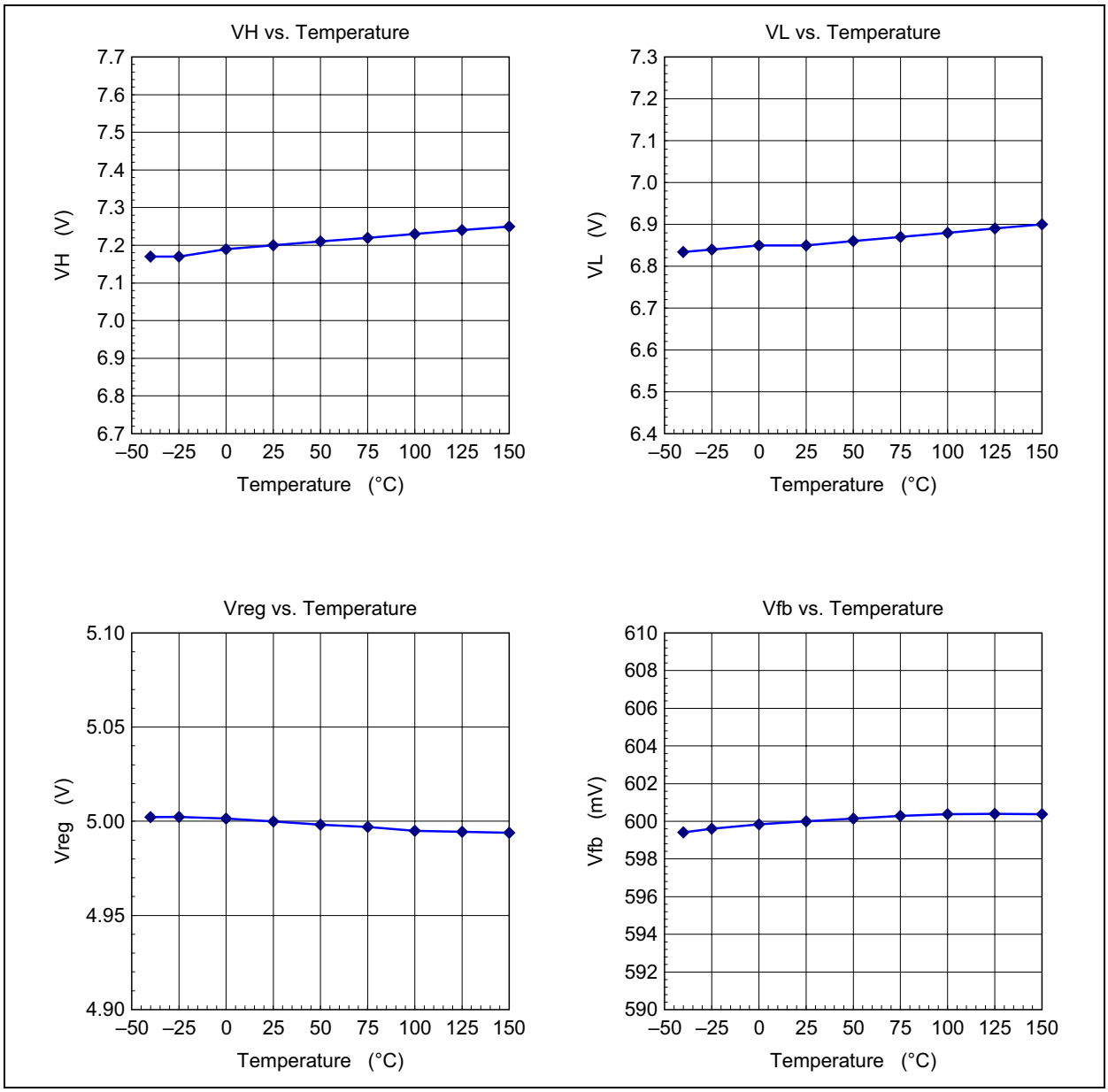
Note: Propagation delay is ignored.

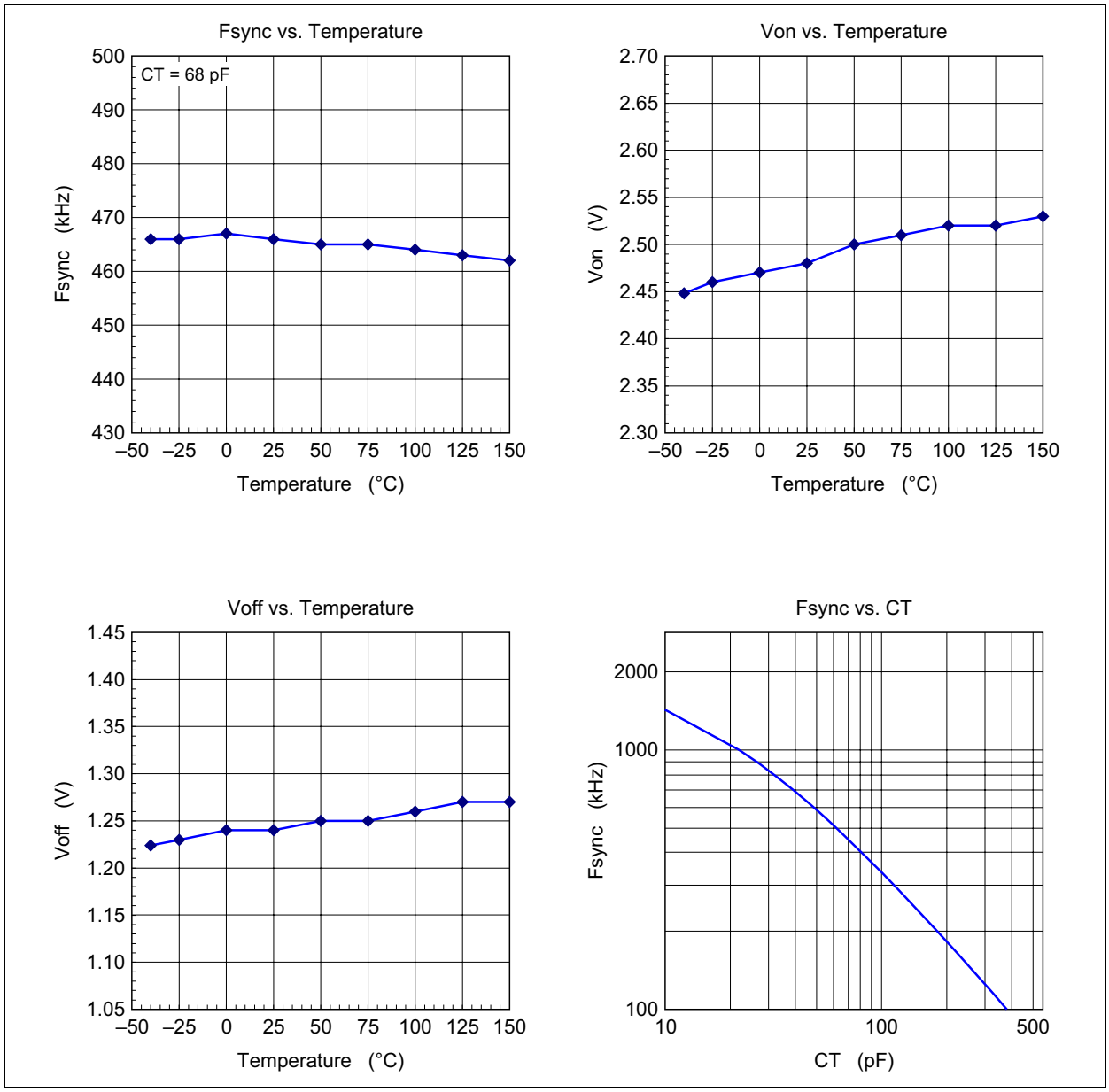
Hiccup Operation when the Over-Current Limit (OCL) is Reached



Note: Propagation delay is ignored.

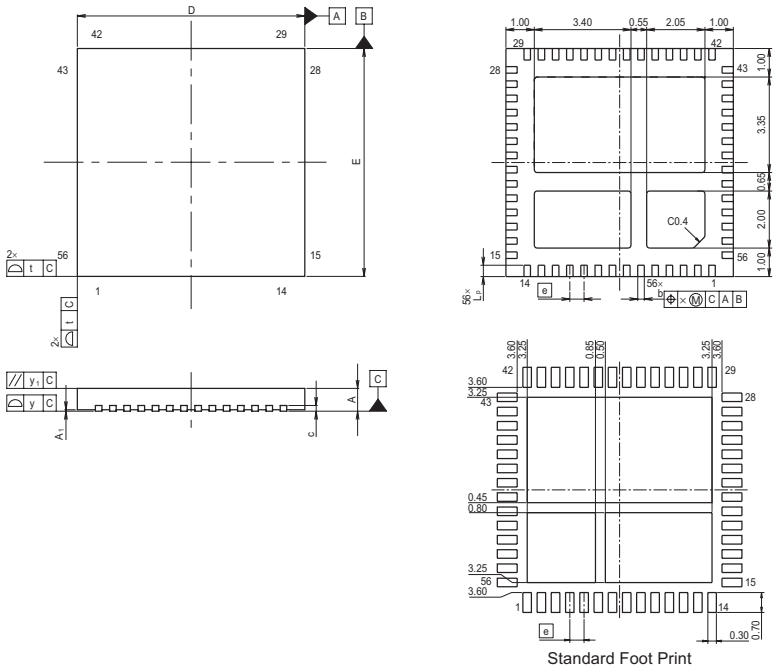
Main Characteristics





Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
—	PWQN0056KB-A	—	0.17g



Standard Foot Print

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	7.90	8.00	8.10
E	7.90	8.00	8.10
A_2	—	—	—
A	—	—	0.80
A_1	0	—	0.05
b	0.18	0.23	0.28
b_1	—	—	—
e	—	0.50	—
L_p	0.30	0.40	0.50
x	—	—	0.10
y	—	—	0.08
y_1	—	—	0.10
t	—	—	0.15
H_D	—	—	—
H_E	—	—	—
Z_D	—	—	—
Z_E	—	—	—
c	—	0.20	—
c_1	—	—	—

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Colophon .7.2