Power Management Switch ICs for PCs and Digital Consumer Products

1ch High Side Switch ICs for USB Devices and Memory Cards

BD2041AFJ,BD2051AFJ,BD6519FJ

No.11029EBT03

●Description

Single channel high side switch IC for USB port is a high side switch having over current protection used in power supply line of universal serial bus (USB).
N-channel power MOSFET of low on resistance and low supply current are realized in this IC.
And, over current detection circuit, thermal shutdown circuit, under voltage lockout and soft start circuit are built in.

●Features

1) Built-in low on resistance Nch MOS FET Switch.
   Typ = 80mΩ (BD2041AF/BD2051AFJ)
   Typ = 100mΩ (BD6519FJ)
2) Continuous current load 0.5A
3) Control input logic
   Active-Low : BD2041AFJ/ BD6519FJ
   Active-High : BD2051AFJ
4) Soft start circuit
5) Over current detection
6) Thermal shutdown
7) Under voltage lockout
8) Open drain error flag output
9) Reverse-current protection when power switch off
10) Power supply voltage range
    2.7V~5.5V (BD2041AF/BD2051AFJ)
    3.0V~5.5V (BD6519FJ)
11) Operating temperature range -40°C~85°C

●Applications

USB hub in consumer appliances, Car accessory, PC, PC peripheral equipment, and so forth

●Lineup

Parameter	BD2041AFJ	BD2051AFJ	BD6519FJ
Continuous current load (A)	0.5	0.5	0.5
Output current at short (A)	1.0	1.0	1.1
Control input logic	Low	High	Low

●Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
Supply voltage	V_{IN}	-0.3 to 6.0	V
Enable voltage	V_{EN}, $V_{/EN}$	-0.3 to 6.0	V
/OC voltage	$V_{/OC}$	-0.3 to 6.0	V
/OC current	$I_{S/OC}$	10	mA
OUT voltage	V_{OUT}	-0.3 to 6.0	V
Storage temperature	T_{STG}	-55 to 150	°C
Power dissipation	PD	560*1	mW

*1 In the case of exceeding Ta = 25°C, 4.48mW should be reduced per 1°C.
* This chip is not designed to protect itself against radioactive rays.

※ IN, EN (/EN), and /OC terminal of BD2041AFJ/BD2051AFJ correspond to VDD, CTRL, and FLAG terminal of BD6519FJ, respectively.

●Operating conditions

◎BD2041AF/BD2051AFJ

Parameter	Symbol	Limits	Unit
Operating voltage	V_{IN}	2.7 to 5.5	V
Operating temperature	T_{OPR}	-40 to 85	°C
Continuous output current	I_{LO}	0 to 500	mA

◎BD6519FJ

Parameter	Symbol	Limits	Unit
Operating voltage	V_{IN}	3.0 to 5.5	V
Operating temperature	T_{OPR}	-40 to 85	°C
Continuous output current	I_{LO}	0 to 500	mA

●Electrical characteristics

◎BD2041AFJ (Unless otherwise specified, V_{IN} = 5.0V, Ta = 25°C)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Operating Current	I_{DD}	-	90	120	μA	$V_{/EN}$ = 0V, OUT = OPEN
Standby Current	I_{STB}	-	0.01	1	μA	$V_{/EN}$ = 5V, OUT = OPEN
/EN input voltage	$V_{/EN}$	2.0	-	-	V	High input
	$V_{/EN}$	-	-	0.8	V	Low input
		-	-	0.4	V	Low input 2.7V≤ V_{IN} ≤4.5V
/EN input current	$I_{/EN}$	-1.0	0.01	1.0	μA	$V_{/EN}$ = 0V or $V_{/EN}$ = 5V
/OC output LOW voltage	$V_{/OC}$	-	-	0.5	V	$I_{/OC}$ = 5mA
/OC output leak current	$I_{L/OC}$	-	0.01	1	μA	$V_{/OC}$ = 5V
ON resistance	R_{ON}	-	80	100	mΩ	I_{OUT} = 500mA
Output current at short	I_{SC}	0.7	1.0	1.3	A	V_{IN} = 5V, V_{OUT} = 0V, C_L = 100μF (RMS)
Output rise time	T_{ON1}	-	1.2	10	ms	R_L = 10Ω , C_L = OPEN
Output turn on time	T_{ON2}	-	1.5	20	ms	
Output fall time	T_{OFF1}	-	1	20	μs	
Output turn off time	T_{OFF2}	-	3	40	μs	
UVLO threshold	V_{TUVH}	2.1	2.3	2.5	V	Increasing V_{IN}
	V_{TUVL}	2.0	2.2	2.4	V	Decreasing V_{IN}

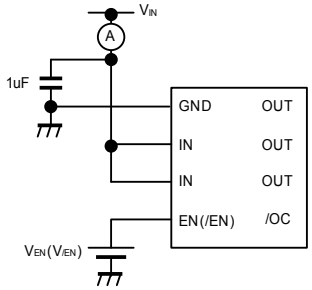
◎BD6519FJ (Unless otherwise specified, V_{DD} = 5.0V, Ta = 25°C)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Operating Current	I_{DD}	-	90	140	μA	V_{CTRL}= 0V, OUT = OPEN
Standby Current		-	0.01	2	μA	V_{CTRL}= 5V, OUT = OPEN
CTRL input voltage	V_{CTRL}	2.5	-	-	V	High input
		-	-	0.7	V	Low input
CTRL input voltage	I_{CTRL}	-1.0	0.01	1.0	μA	V_{CTRL} = 0V or V_{CTRL} = 5V
FLAG output resistance	R_{FLAG}	-	180	450	Ω	I_{FLAG} = 1mA
FLAG output leak current	I_{LFLAG}	-	0.01	1	μA	V_{FLAG} = 5V
FLAG output delay	TD_{FLAG}	-	2.5	8	ms	
ON resistance	R_{ON}	-	100	140	mΩ	V_{DD} = 5V, I_{OUT} = 500mA
		-	140	180	mΩ	V_{DD} = 3.3V, I_{OUT} = 500mA
Short circuit output current	I_{SC}	0.6	-	1.6	A	V_{DD} = 5V , V_{OUT} = 0V
Output leak current	I_{LEAK}	-	-	10	μA	V_{CTRL} = 5V
Output rise time	T_{ON1}	-	1	4	ms	R_L = 10Ω , C_L = OPEN
Output turn on delay time	T_{ON2}	-	1.3	6	ms	
Output fall time	T_{OFF1}	-	1	20	μs	
Output turn off delay time	T_{OFF2}	-	3	20	μs	
Thermal shutdown threshold	T_{TS}	-	135	-	°C	Tj increase
UVLO threshold	V_{TUVH}	2.3	2.5	2.7	V	V_{DD} increasing
	V_{TUVL}	2.1	2.3	2.5	V	V_{DD} decreasing

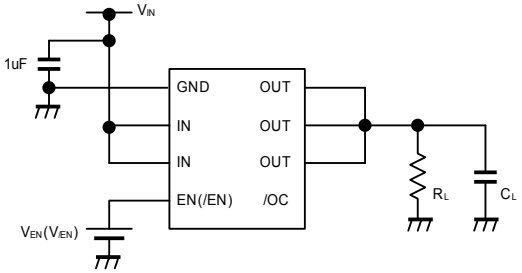
◎BD2051AFJ (Unless otherwise specified, V_{IN} = 5.0V, Ta = 25°C)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Operating Current	I_{DD}	-	90	120	μA	V_{EN} = 5V, OUT = OPEN
Standby Current	I_{STB}	-	0.01	1	μA	V_{EN} = 0V, OUT = OPEN
EN input voltage	V_{EN}	2.0	-	-	V	High input
	V_{EN}	-	-	0.8	V	Low input
		-	-	0.4	V	Low input 2.7V≤ V_{IN} ≤4.5V
EN input current	I_{EN}	-1.0	0.01	1.0	μA	V_{EN} = 0V or V_{EN} = 5V
/OC output LOW voltage	$V_{/OC}$	-	-	0.5	V	$I_{/OC}$ = 5mA
/OC output leak current	$IL_{/OC}$	-	0.01	1	μA	$V_{/OC}$ = 5V
ON resistance	R_{ON}	-	80	100	mΩ	I_{OUT} = 500mA
Output current at short	I_{SC}	0.7	1.0	1.3	A	V_{IN} = 5V, V_{OUT} = 0V, C_L = 100μF (RMS)
Output rise time	T_{ON1}	-	1.2	10	ms	R_L = 10Ω , C_L = OPEN
Output turn on time	T_{ON2}	-	1.5	20	ms	
Output fall time	T_{OFF1}	-	1	20	μs	
Output turn off time	T_{OFF2}	-	3	40	μs	
UVLO threshold	V_{TUVH}	2.1	2.3	2.5	V	Increasing V_{IN}
	V_{TUVL}	2.0	2.2	2.4	V	Decreasing V_{IN}

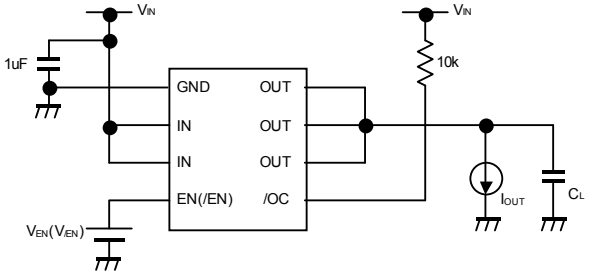
●Measurement circuit



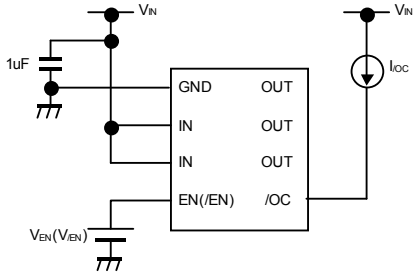
Operating current



EN, /EN input voltage, Output rise, fall time



ON resistance, Over current detection



/OC output LOW voltage

Fig.1 Measurement circuit

●Timing diagram

◎BD2041AFJ/BD6519FJ

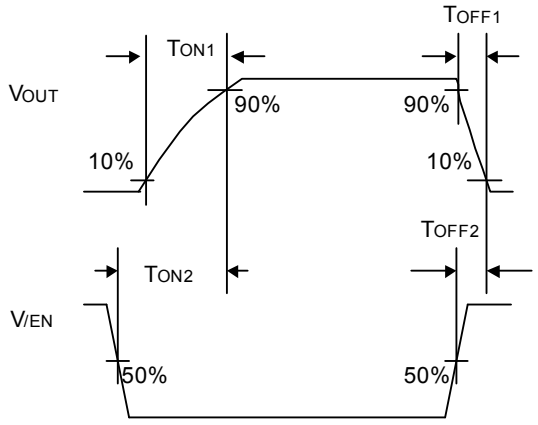


Fig.2 Timing diagram

◎BD2051AFJ

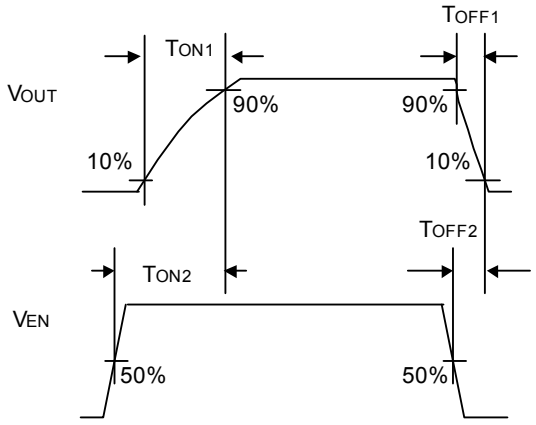


Fig.3 Timing diagram

※IN, EN (/EN), and /OC terminal of BD2041AFJ/BD2051AFJ correspond to VDD, CTRL, and FLAG terminal of BD6519FJ, respectively.

●**Reference data (BD2041AFJ/BD2051AFJ)**

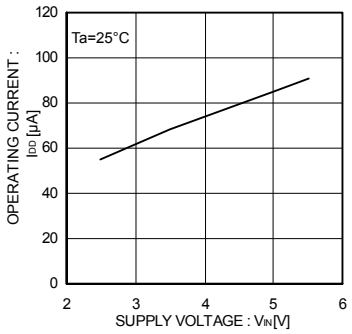


Fig.4 Operating current
EN,/EN Enable

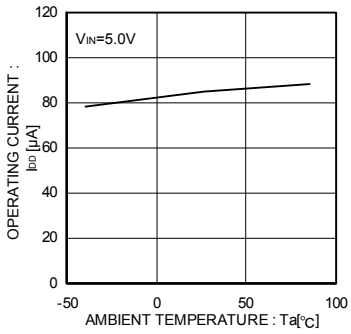


Fig.5 Operating current
EN,/EN Enable

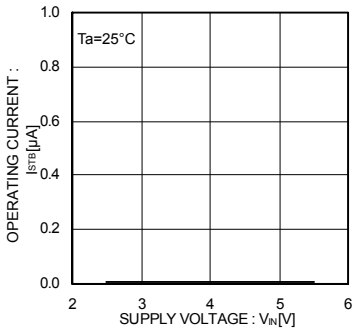


Fig.6 Operating current
EN,/EN Disable

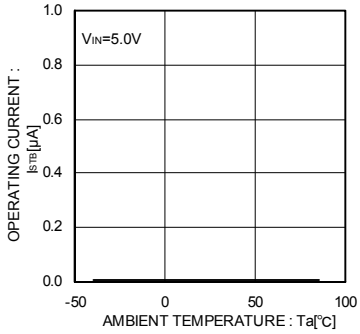


Fig.7 Operating current
EN,/EN Disable

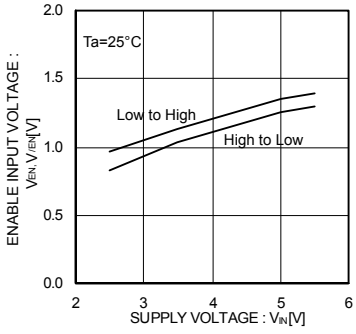


Fig.8 EN,/EN input voltage

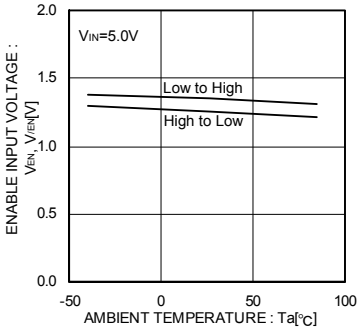


Fig.9 EN,/EN input voltage

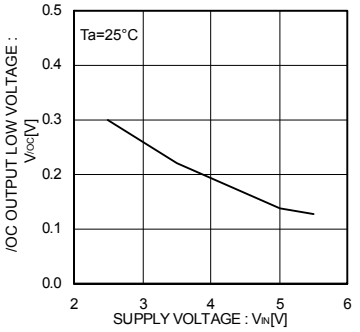


Fig.10 /OC output LOW voltage

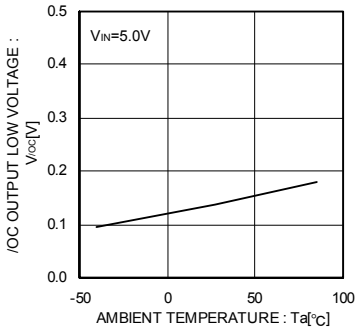


Fig.11 /OC output LOW voltage

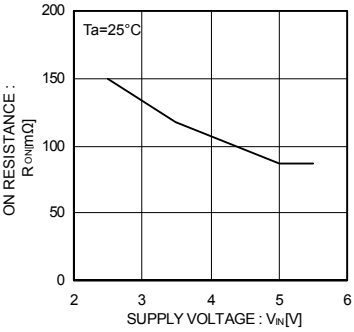


Fig.12 ON resistance

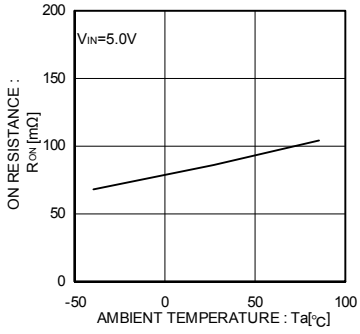


Fig.13 ON resistance

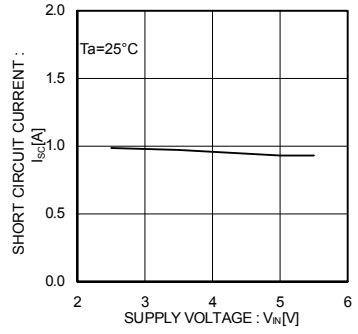


Fig.14 Output current at shortcircuit
(BD2041AFJ/51AFJ)

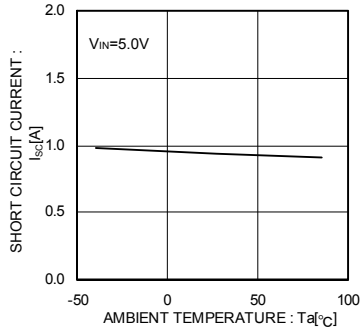


Fig.15 Output current at shortcircuit
(BD2041AFJ/51AFJ)

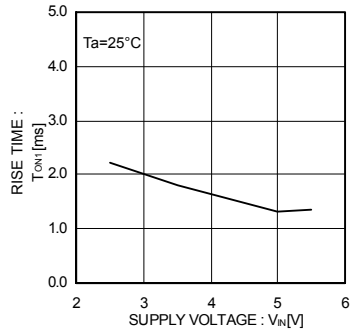


Fig.16 Output rise time

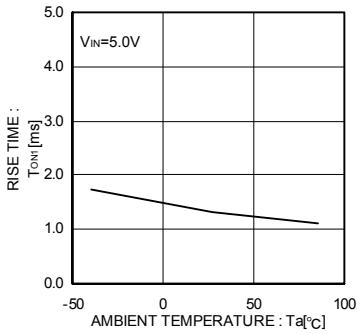


Fig.17 Output rise time

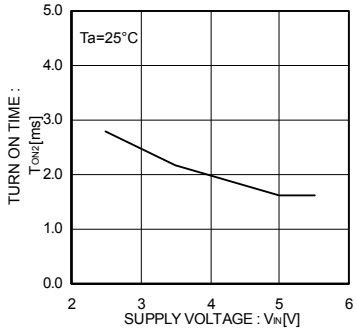


Fig.18 Output turn on time

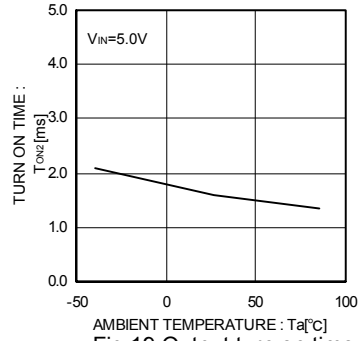


Fig.19 Output turn on time

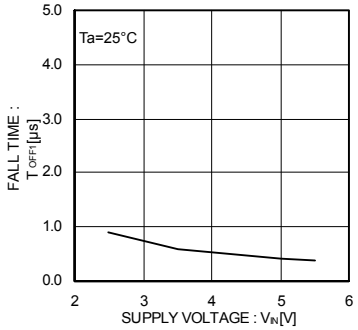


Fig.20 Output fall time

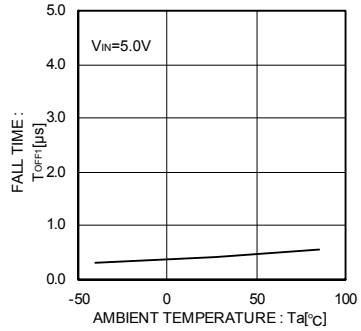


Fig.21 Output fall time

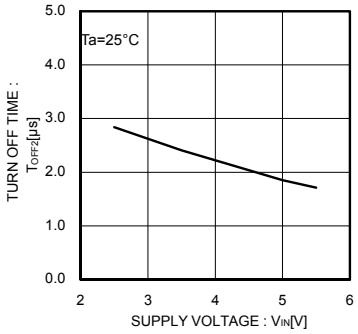


Fig.22 Output turn off time

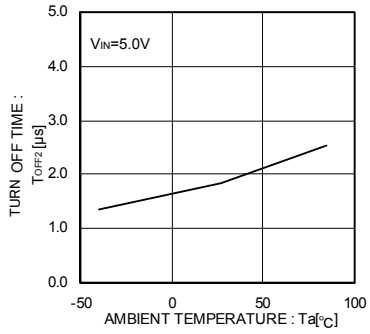


Fig.23 Output turn off time

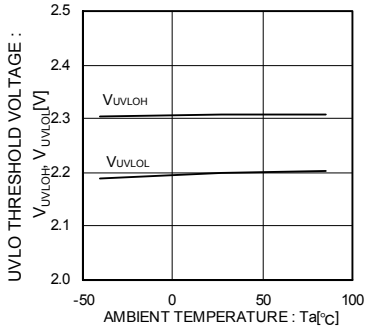


Fig.24 UVLO threshold voltage

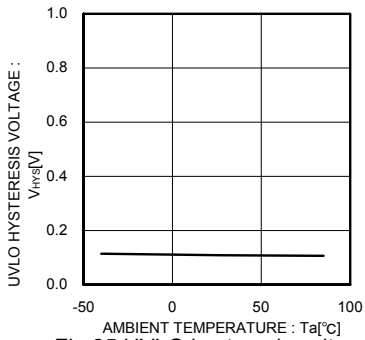


Fig.25 UVLO hysteresis voltage

●Waveform data (BD2041AFJ/BD2051AFJ)

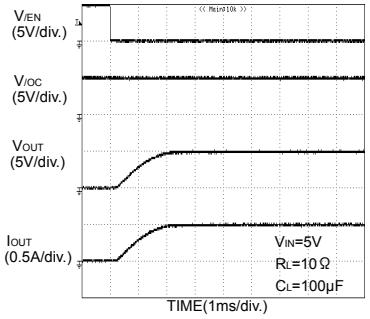


Fig.26 Output rise characteristic (BD2041AFJ)

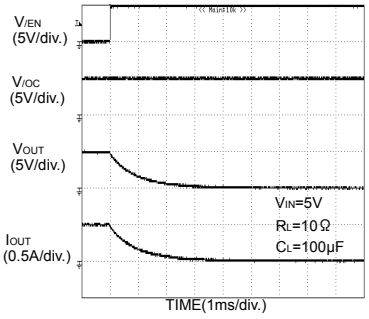


Fig.27 Output fall characteristic (BD2041AFJ)

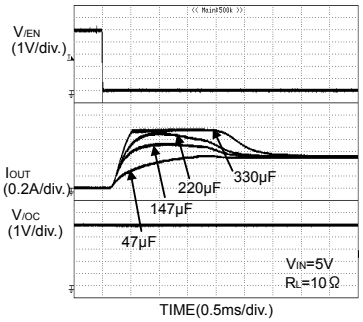


Fig.28 Inush current (BD2041AFJ)

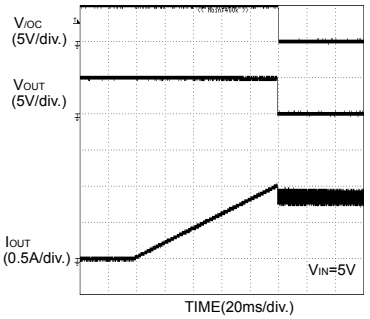


Fig.29 Over current response Ramped load (BD2041AFJ)

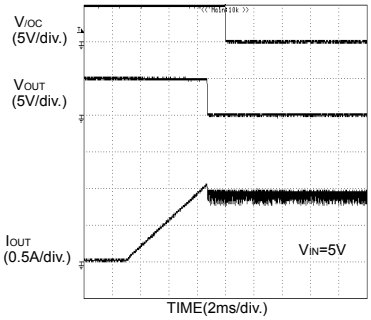


Fig.30 Over current response Ramped load (BD2041AFJ)

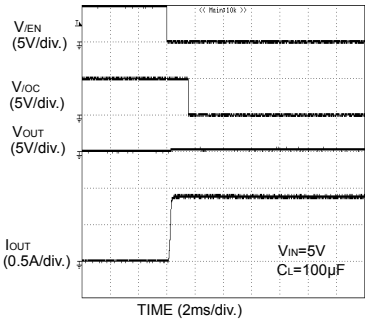


Fig.31 Over current response Enable to shortcircuit (BD2041AFJ)

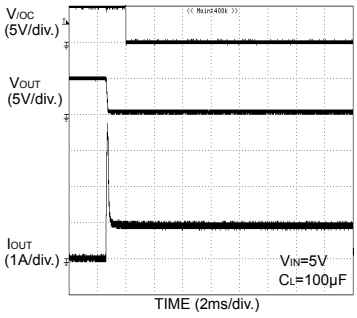


Fig.32 Over current response Output shortcircuit at Enable (BD2041AFJ)

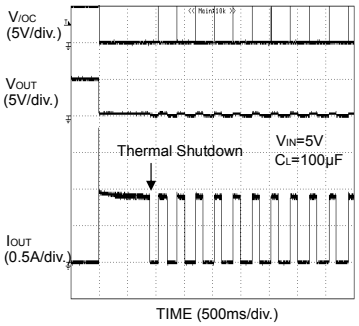


Fig.33 Over current response Output shortcircuit at Enable (BD2041AFJ)

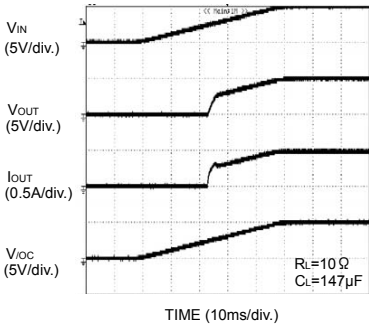


Fig.34 UVLO V_{DD} increasing (BD2041AFJ)

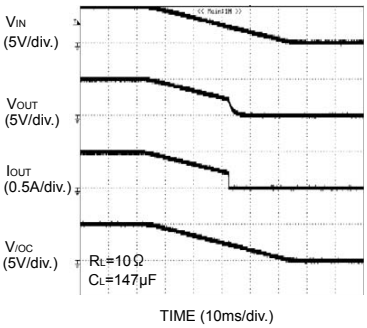


Fig.35 UVLO V_{DD} decreasing (BD2041AFJ)

Regarding the output rise/fall and over current detection characteristics of BD2051AFJ, refer to the characteristic of BD2041AFJ.

●Reference data (BD6519FJ)

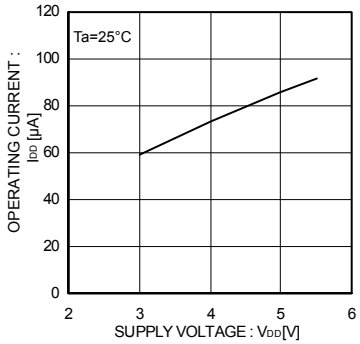


Fig.36 Operating current
CTRL Enable

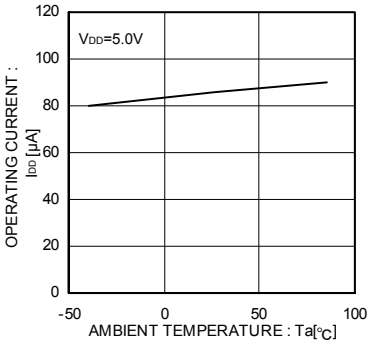


Fig.37 Operating current
CTRL Enable

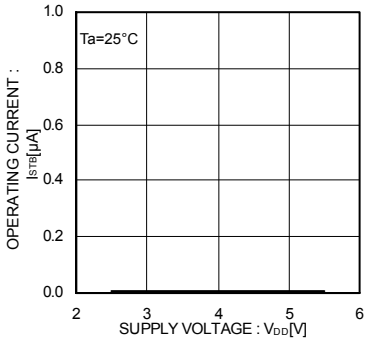


Fig.38 Operating current
CTRL Disable

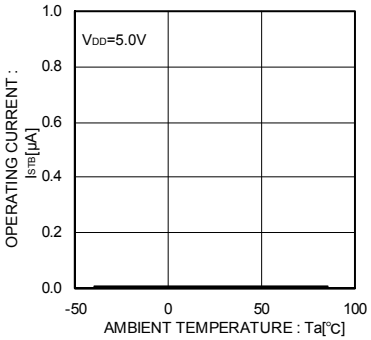


Fig.39 Operating current
CTRL Disable

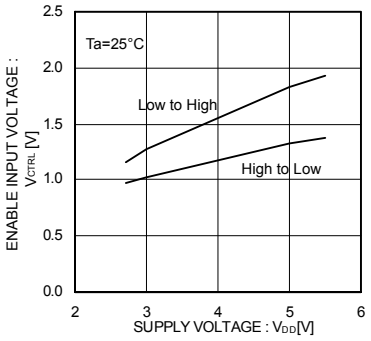


Fig.40 CTRL input voltage

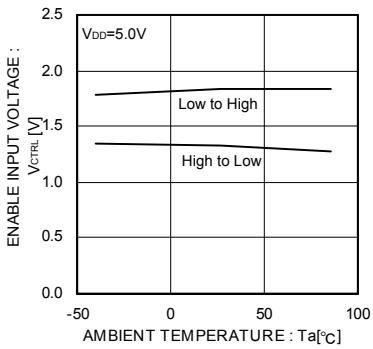


Fig.41 CTRL input voltage

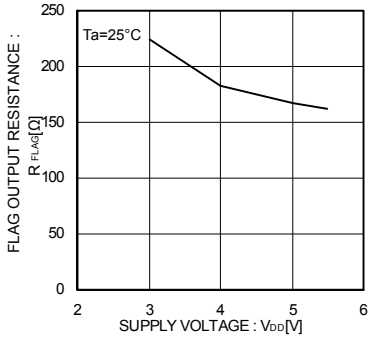


Fig.42 FLAG output resistance

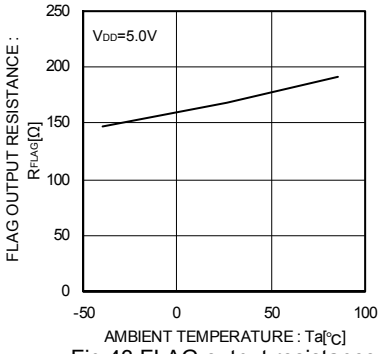


Fig.43 FLAG output resistance

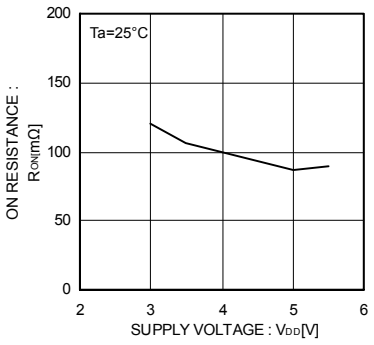


Fig.44 ON resistance

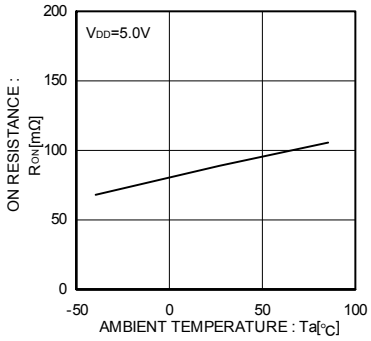


Fig.45 ON resistance

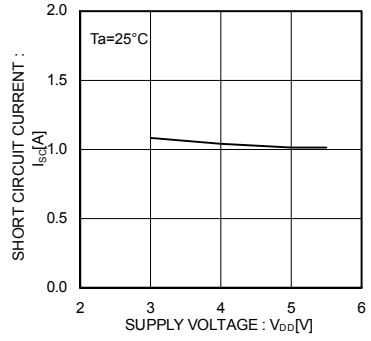


Fig.46 Output current at shortcircuit

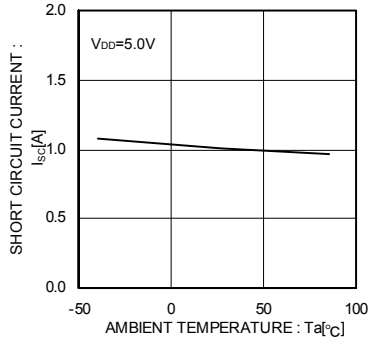


Fig.47 Output current at shortcircuit

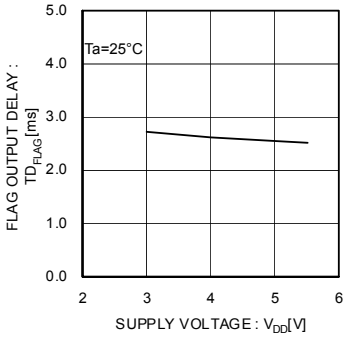


Fig.48 FLAG output delay

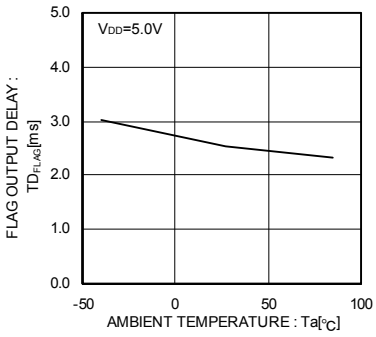


Fig.49 FLAG output delay

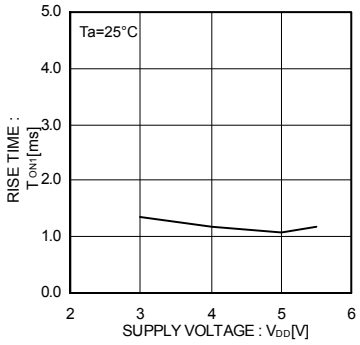


Fig.50 Output rise time

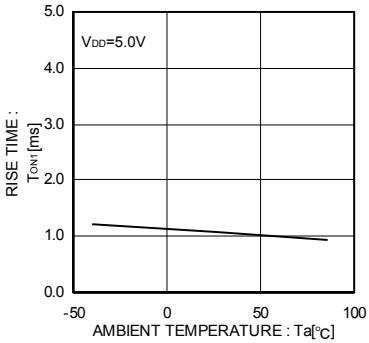


Fig.51 Output rise time

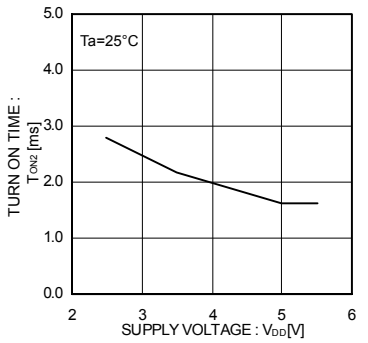


Fig.52 Output turn on delay time

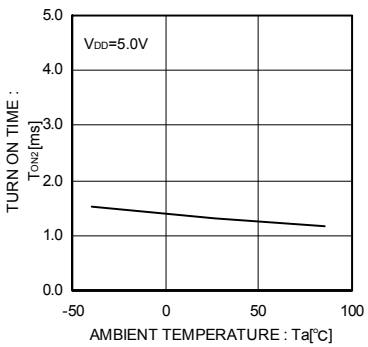


Fig.53 Output turn on delay time

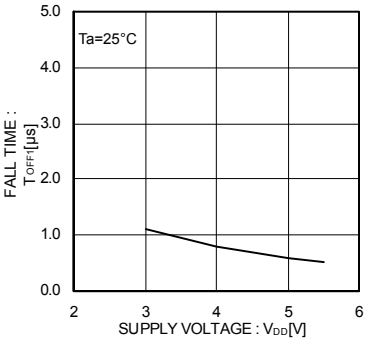


Fig.54 Output fall time

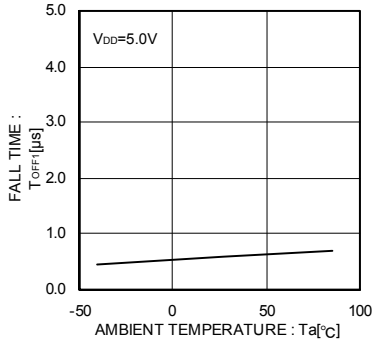


Fig.55 Output fall time

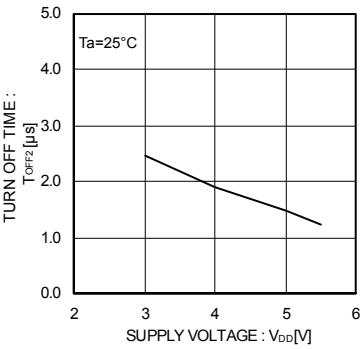


Fig.56 Output turn off delay time

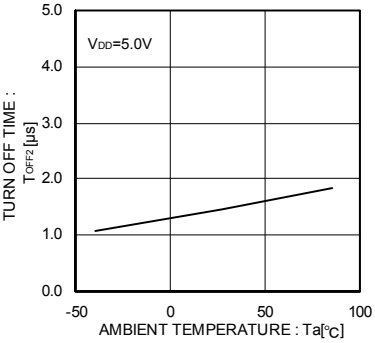


Fig.57 Output turn off delay time

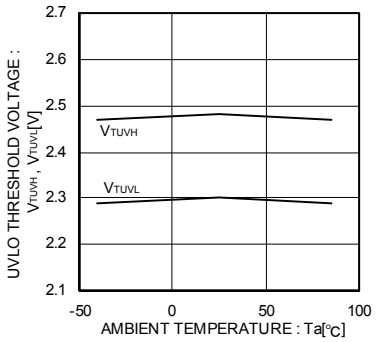


Fig.58 UVLO threshold voltage

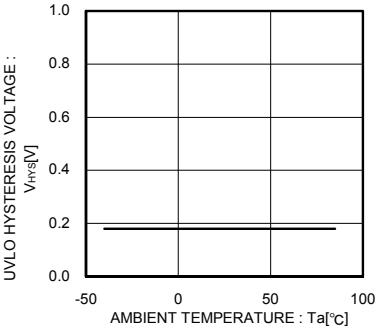


Fig.59 UVLO hysteresis voltage

●Waveform data (BD6519FJ)

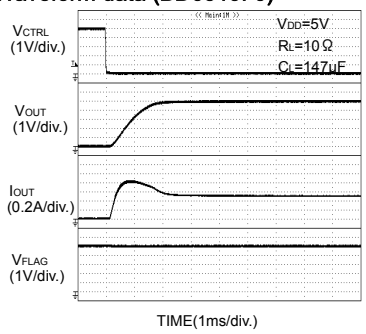


Fig.60 Output rise characteristic

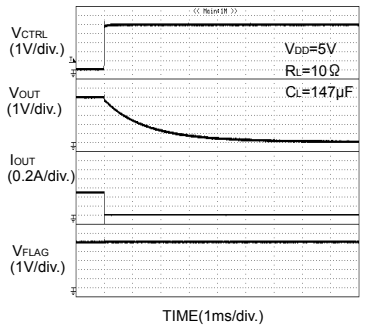


Fig.61 Output fall characteristic

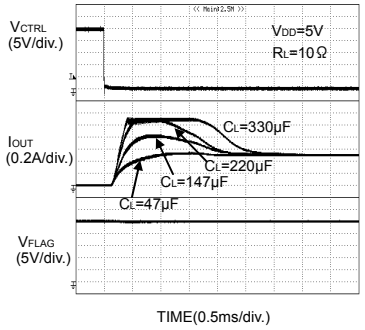


Fig.62 Inrush current characteristic

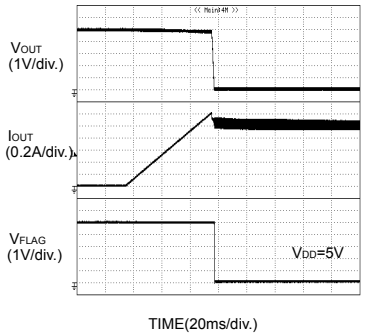


Fig.63 Over current response
Ramped load

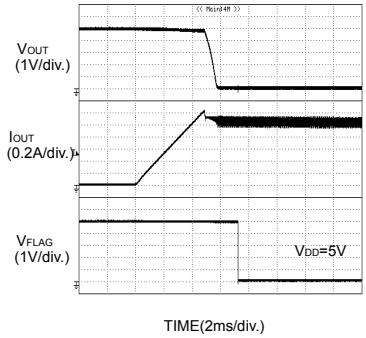


Fig.64 Over current response
Ramped load

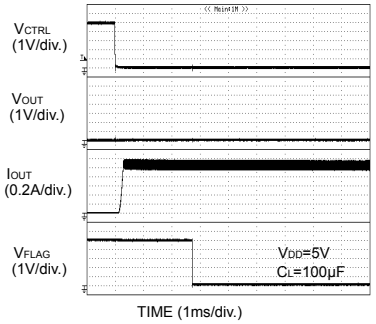


Fig.65 Over current response
Enable to shortcircuit

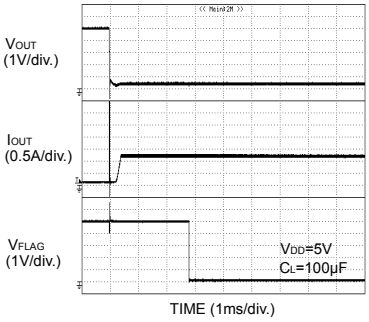


Fig.66 Over current response
Output shortcircuit at Enable

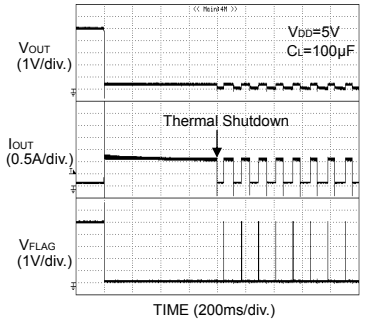


Fig.67 Over current response
Output shortcircuit at Enable

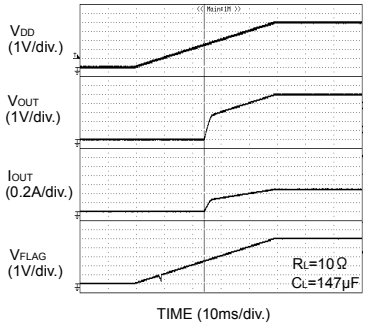


Fig.68 UVLO
V_{IN} increasing

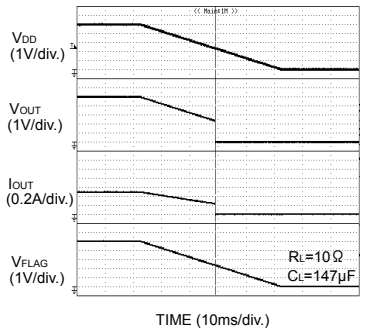


Fig.69 UVLO
V_{IN} decreasing

●Block diagram (BD2041AFJ/2051AFJ)

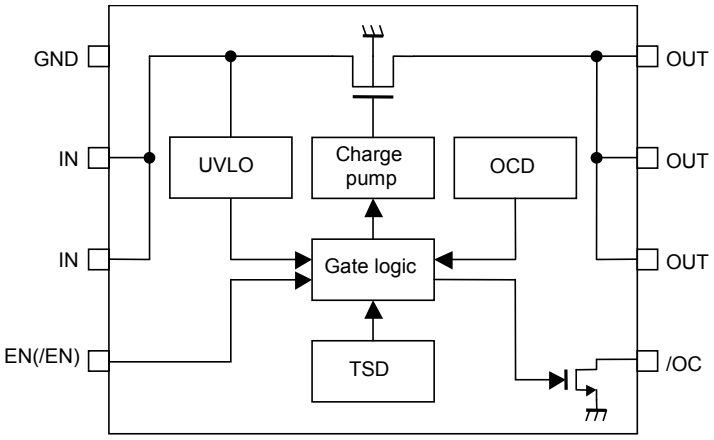


Fig.70 Block diagram

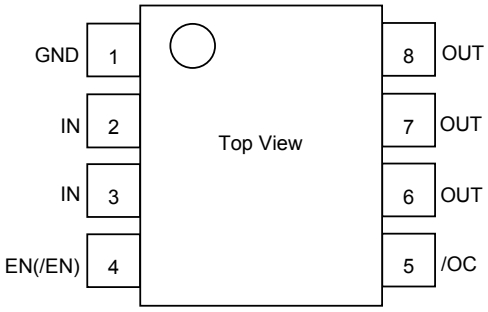
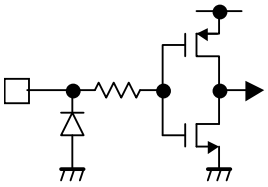
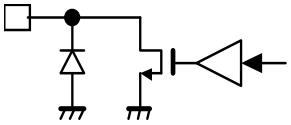
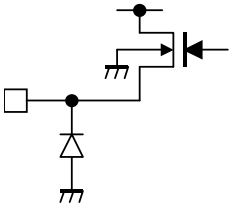


Fig.71 Pin Configuration

●Pin description (BD2041AFJ/2051AFJ)

Pin No.	Symbol	I / O	Pin function
1	GND	I	Ground.
2, 3	IN	I	Power supply input. Input terminal to the power switch and power supply input terminal of the internal circuit. At use, connect each pin outside.
4	EN (/EN)	I	Enable input. Power switch on at Low level. (BD2041AFJ) Power switch on at High level. (BD2051AFJ) High level input > 2.0V, Low level input < 0.8V.
5	/OC	O	Error flag output. Low at over current, thermal shutdown. Open drain output.
6, 7, 8	OUT	O	Power switch output. At use, connect each pin outside.

●I/O circuit (BD2041AFJ/2051AFJ)

Symbol	Pin No	Equivalent circuit
EN(/EN)	4	
/OC	5	
OUT	6,7,8	

●Block diagram (BD6519FJ)

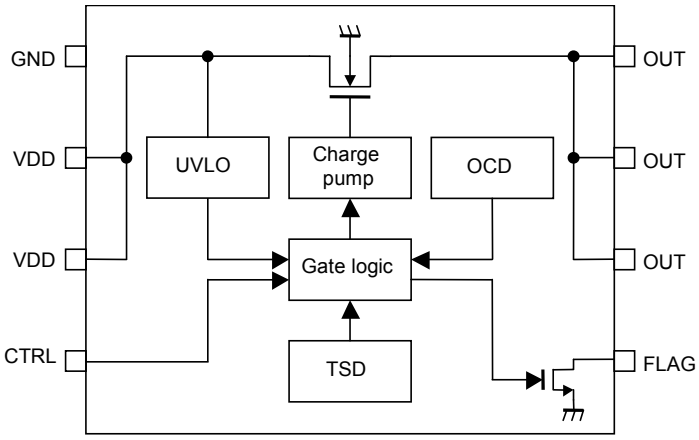


Fig.72 Block diagram

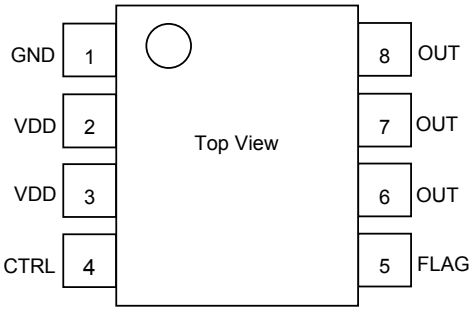
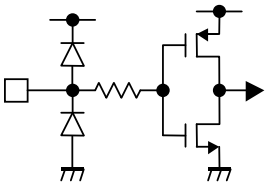
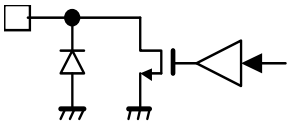
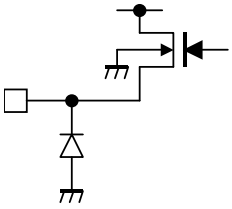


Fig.73 Pin Configuration

●Pin description (BD6519FJ)

Pin No.	Symbol	I / O	Pin function
1	GND	I	Ground.
2, 3	VDD	I	Power supply input. Input terminal to the power switch and power supply input terminal of the internal circuit. At use, connect each pin outside.
4	CTRL	I	Enable input. Power switch on at Low level. (BD6519FJ) High level input > 2.5V, Low level input < 0.7V.
5	FLAG	O	Error flag output. Low at over current, thermal shutdown. Open drain output.
6, 7, 8	OUT	O	Power switch output. At use, connect each pin outside.

●I/O circuit (BD6519FJ)

Symbol	Pin No	Equivalent circuit
CTRL	4	
FLAG	5	
OUT	6,7,8	

●Functional description (BD2041AFJ/2051AFJ)

1. Switch operation

IN terminal and OUT terminal are connected to the drain and the source of switch MOSFET respectively. And the IN terminal is used also as power source input to internal control circuit.

When the switch is turned on from EN/EN control input, IN terminal and OUT terminal are connected by a 80mΩ switch. In on status, the switch is bidirectional. Therefore, when the potential of OUT terminal is higher than that of IN terminal, current flows from OUT terminal to IN terminal.

Since a parasitic diode between the drain and the source of switch MOSFET is canceled, in the off status, it is possible to prevent current from flowing reversely from OUT to IN.

2. Thermal shutdown circuit (TSD)

If over current would continue, the temperature of the IC would increase drastically. If the junction temperature were beyond 140°C (typ.) in the condition of over current detection, thermal shutdown circuit operates and makes power switch turn off and outputs error flag (/OC). Then, when the junction temperature decreases lower than 120°C (typ.), power switch is turned on and error flag (/OC) is cancelled. Unless the fact of the increasing chips temperature is removed or the output of power switch is turned off, this operation repeats.
The thermal shutdown circuit operates when the switch is on (EN,/EN signal is active).

3. Over current detection (OCD)

The over current detection circuit limits current (I_{SC}) and outputs error flag (/OC) when current flowing in each switch MOSFET exceeds a specified value. There are three types of response against over current. The over current detection circuit works when the switch is on (EN,/EN signal is active).

3-1. When the switch is turned on while the output is in shortcircuit status

When the switch is turned on while the output is in shortcircuit status or so, the switch gets in current limit status soon.

3-2. When the output shortcircuits while the switch is on

When the output shortcircuits or large capacity is connected while the switch is on, very large current flows until the over current limit circuit reacts. When the current detection, limit circuit works, current limitation is carried out.

3-3. When the output current increases gradually

When the output current increases gradually, current limitation does not work until the output current exceeds the over current detection value. When it exceeds the detection value, current limitation is carried out.

4. Under voltage lockout (UVLO)

UVLO circuit prevents the switch from turning on until the V_{IN} exceeds 2.3V(Typ.). If the V_{IN} drops below 2.2V(Typ.) while the switch turns on, then UVLO shuts off the power switch. UVLO has hysteresis of a 100mV(Typ).
Under voltage lockout circuit works when the switch is on (EN,/EN signal is active).

5. Error flag (/OC) output

Error flag output is N-MOS open drain output. At detection of over current, thermal shutdown, low level is output.

Over current detection has delay filter. This delay filter prevents instantaneous current detection such as inrush current at switch on, hot plug from being informed to outside.

●Functional description (BD6519FJ)

1. Switch operation

VDD terminal and OUT terminal are connected to the drain and the source of switch MOSFET respectively. And the VDD terminal is used also as power source input to internal control circuit.

When the switch is turned on from CTRL control input, VDD terminal and OUT terminal are connected by a 100mΩ switch. In on status, the switch is bidirectional. Therefore, when the potential of OUT terminal is higher than that of VDD terminal, current flows from OUT terminal to VDD terminal.

Since a parasitic diode between the drain and the source of switch MOSFET is canceled, in the off status, it is possible to prevent current from flowing reversely from OUT to VDD.

2. Thermal shutdown circuit (TSD)

If over current would continue, the temperature of the IC would increase drastically. If the junction temperature were beyond 135°C (typ.) in the condition of over current detection, thermal shutdown circuit operates and makes power switch turn off and outputs error flag (FALG). Then, when the junction temperature decreases lower than 125°C (typ.), power switch is turned on and error flag (FLAG) is cancelled. Unless the fact of the increasing chips temperature is removed or the output of power switch is turned off, this operation repeats.
The thermal shutdown circuit operates when the switch is on (CTRL signal is active).

3. Over current detection (OCD)

The over current detection circuit limits current (I_{SC}) and outputs error flag (FLAG) when current flowing in each switch MOSFET exceeds a specified value. There are three types of response against over current. The over current detection circuit works when the switch is on (CTRL signal is active).

3-1. When the switch is turned on while the output is in shortcircuit status
When the switch is turned on while the output is in shortcircuit status or so, the switch gets in current limit status soon.

3-2. When the output shortcircuits while the switch is on
When the output shortcircuits or large capacity is connected while the switch is on, very large current flows until the over current limit circuit reacts. When the current detection, limit circuit works, current limitation is carried out.

3-3. When the output current increases gradually
When the output current increases gradually, current limitation does not work until the output current exceeds the over current detection value. When it exceeds the detection value, current limitation is carried out.

4. Under voltage lockout (UVLO)

UVLO circuit prevents the switch from turning on until the VDD exceeds 2.5V(Typ.). If the VDD drops below 2.3V(Typ.) while the switch turns on, then UVLO shuts off the power switch. UVLO has hysteresis of a 200mV(Typ).
Under voltage lockout circuit works when the switch is on (CTRL signal is active).

5. Error flag (FLAG) output

Error flag output (FLAG) is N-MOS open drain output. At detection of over current, thermal shutdown, low level is output.

Over current detection has delay filter on 2.5ms(Typ.). This delay filter prevents instantaneous current detection such as inrush current at switch on, hot plug from being informed to outside.

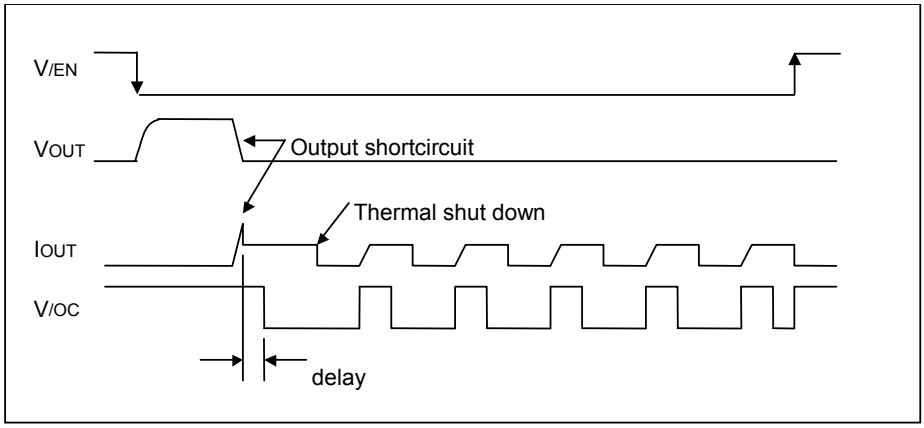


Fig.74 Over current detection, thermal shutdown timing
(BD2041AFJ/BD6519FJ)

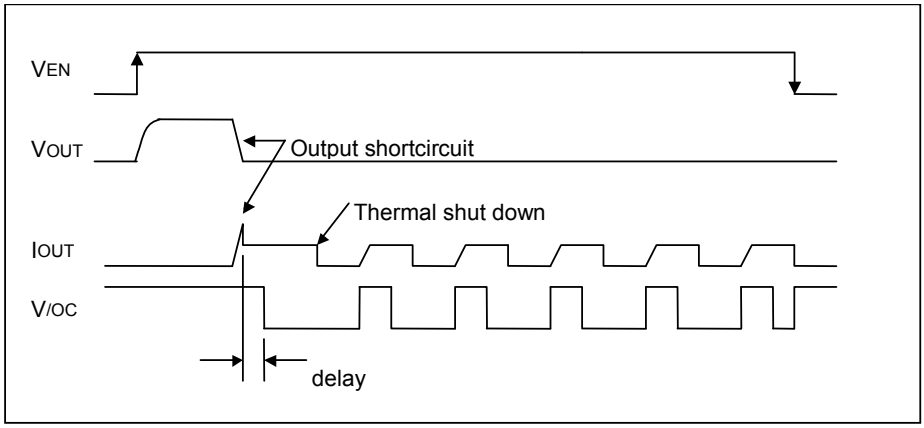


Fig.75 Over current detection, thermal shutdown timing
(BD2051AFJ)

※ IN, EN (/EN), and /OC terminal of BD2041AFJ/BD2051AFJ correspond to VDD, CTRL, and FLAG terminal of BD6519FJ, respectively.

●Typical application circuit

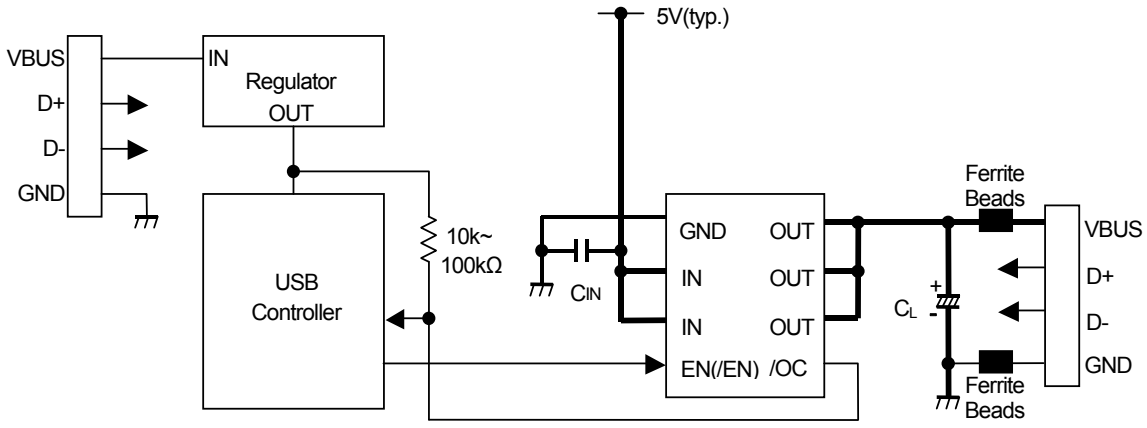


Fig.76 Typical application circuit (BD2041AFJ/51AFJ)

●Application information

When excessive current flows owing to output shortcircuit or so, ringing occurs by inductance of power source line to IC, and may cause bad influences upon IC actions. In order to avoid this case, connect a bypath capacitor by IN terminal and GND terminal of IC. 1μF or higher is recommended.

Pull up /OC output by resistance 10kΩ ~ 100kΩ.

Set up value which satisfies the application as C_L and Ferrite Beads.

This system connection diagram doesn't guarantee operating as the application.

The external circuit constant and so on is changed and it uses, in which there are adequate margins by taking into account external parts or dispersion of IC including not only static characteristics but also transient characteristics.

※ IN, EN (/EN), and /OC terminal of BD2041AFJ/BD2051AFJ correspond to VDD, CTRL, and FLAG terminal of BD6519FJ, respectively.

●Power dissipation character

(SOP-J8)

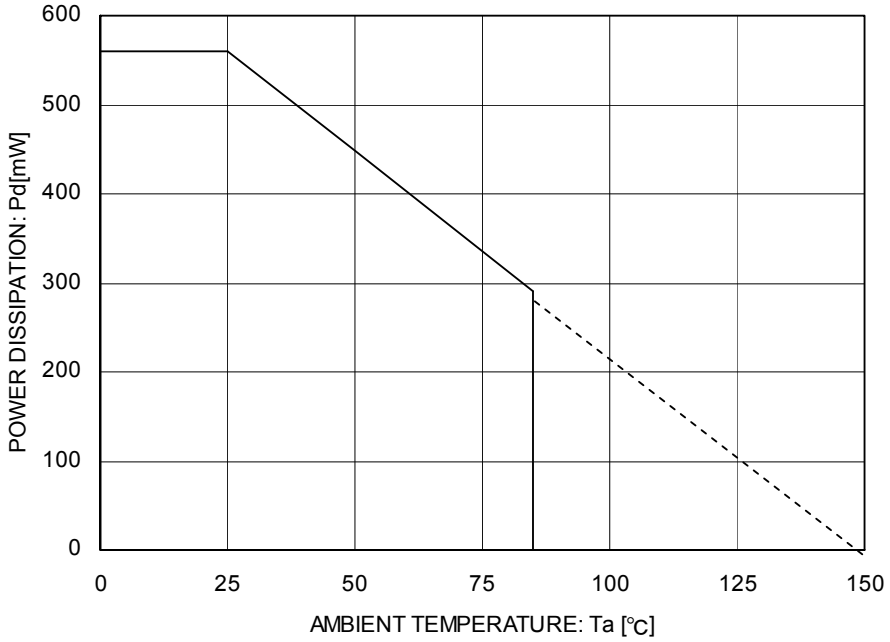


Fig.77 Power dissipation curve (Pd-Ta Curve)

●Notes for use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected.
The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.

Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(12) Thermal shutdown circuit (TSD)

When junction temperatures become detected temperatures or higher, the thermal shutdown circuit operates and turns a switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

(13) Thermal design

Perform thermal design in which there are adequate margins by taking into account the power dissipation (Pd) in actual states of use.

●Ordering part number

B	D	6	5	1	9	F	J	-	E	2

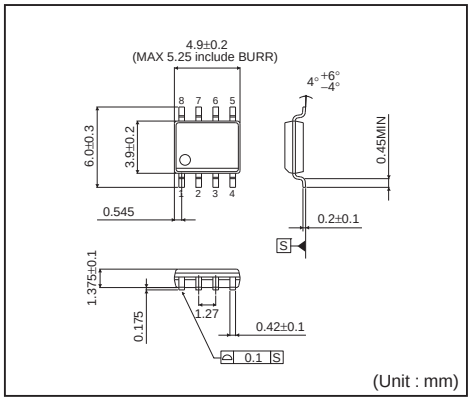
Part No.

Part No.
2041A
2051A
6519

Package
FJ: SOP-J8

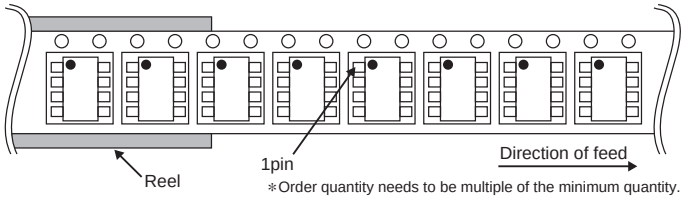
Packaging and forming specification
E2: Embossed tape and reel
(SOP-J8)

SOP-J8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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