

**High and Low Side Driver**

**Features**

- Floating channel designed for bootstrap operation
- Fully operational to +600V
- Tolerant to negative transient voltage
- dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V, 5V and 15V input logic compatible
- Matched propagation delay for both channels
- Logic and power ground +/-5V offset
- Lower di/dt gate driver for better noise immunity
- Outputs in phase with inputs

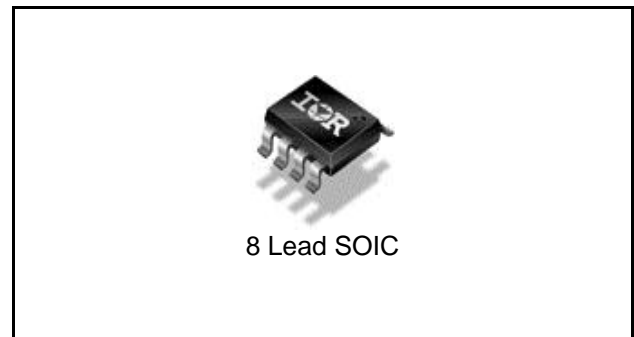
**Product Summary**

$V_{OFFSET}$	600V max.
$I_{O+/-}$	200 mA / 350 mA
$V_{OUT}$	10 – 20V
Ton/off (typ.)	220 & 200 ns

**Description**

The IR25604 is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 V.

**Package Options**

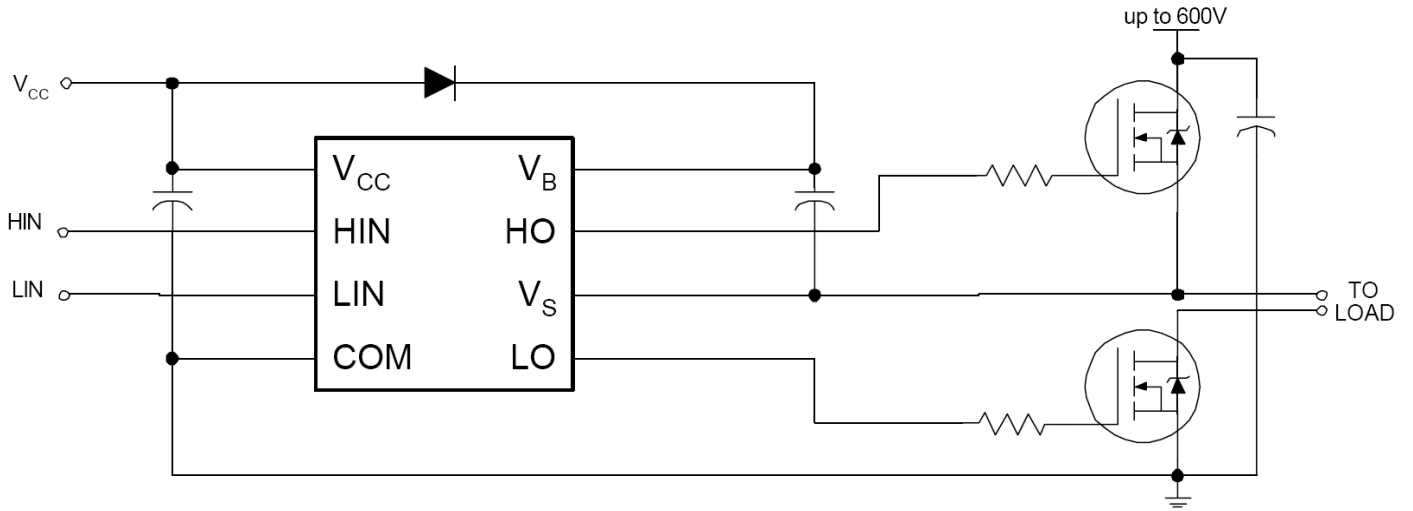


**Ordering Information**

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IR25604SPBF	SO8N	Tube	95	IR25604SPBF
IR25604SPBF	SO8N	Tape and Reel	2500	IR25604STRPBF

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**Typical Connection Diagram**



### Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
$V_B$	High side floating absolute voltage	-0.3	625	V
$V_S$	High side floating supply offset voltage	$V_B - 25$	$V_B + 0.3$	
$V_{HO}$	High side floating output voltage	$V_S - 0.3$	$V_B + 0.3$	
$V_{CC}$	Low side and logic fixed supply voltage	-0.3	25	
$V_{LO}$	Low side output voltage	-0.3	$V_{CC} + 0.3$	
$V_{IN}$	Logic input voltage	-0.3	$V_{CC} + 0.3$	
$dV_S/dt$	Allowable offset supply voltage transient	—	50	V/ns
$P_D$	Package power dissipation @ $T_A \leq +25^\circ\text{C}$	—	0.625	W
$R_{thJA}$	Thermal resistance, junction to ambient	—	200	$^\circ\text{C}/\text{W}$
$T_J$	Junction temperature	—	150	$^\circ\text{C}$
$T_S$	Storage temperature	-55	150	
$T_L$	Lead temperature (soldering, 10 seconds)	—	300	

### Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. The  $V_S$  offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
$V_B$	High side floating supply absolute voltage	$V_S + 10$	$V_S + 20$	V
$V_S$	High side floating supply offset voltage	†	600	
$V_{HO}$	High side floating output voltage	$V_S$	$V_B$	
$V_{CC}$	Low side and logic fixed supply voltage	10	20	
$V_{LO}$	Low side output voltage	0	$V_{CC}$	
$V_{IN}$	Logic input voltage	0	$V_{CC}$	
$T_A$	Ambient temperature	-40	125	$^\circ\text{C}$

† Logic operational for  $V_S$  of -5 to +600V. Logic state held for  $V_S$  of -5V to -VBS. (Please refer to Design Tip DT97-3 for more details).

## Dynamic Electrical Characteristics

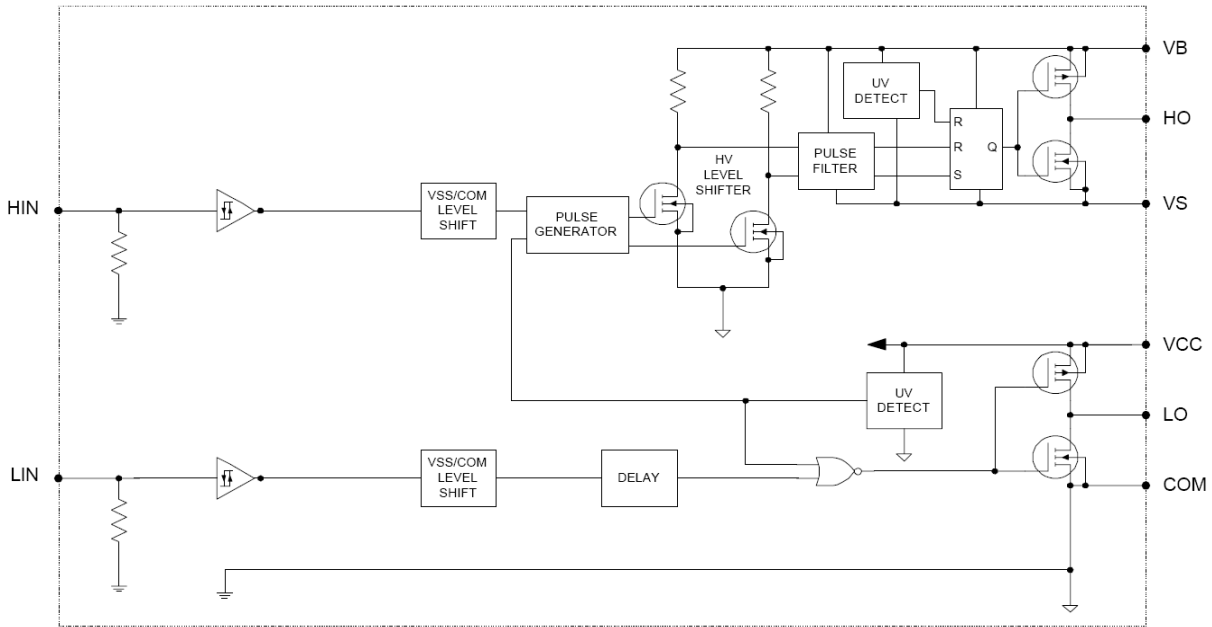
$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15V,  $C_L$  = 1000 pF and  $T_A$  = 25°C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$t_{on}$	Turn-on propagation delay	—	220	300	ns	$V_S = 0V$
$t_{off}$	Turn-off propagation delay	—	200	280		$V_S = 0V$ or 600V
$t_r$	Turn-on rise time	—	150	220		$V_S = 0V$
$t_f$	Turn-off fall time	—	50	80		$V_S = 0V$
MT	Delay matching, HS & LS turn-on/off	—	0	30		

## Static Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15V and  $T_A$  = 25°C unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$  and  $I_{IN}$  parameters are referenced to COM. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

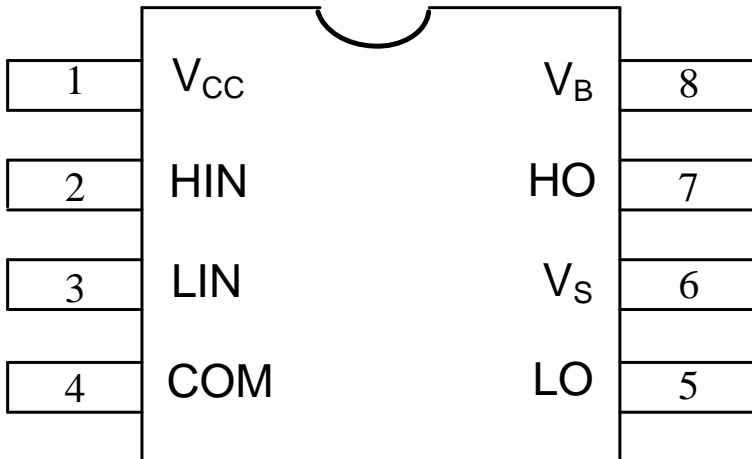
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$V_{IH}$	Logic "1" input voltage	2.9	—	—	V	$V_{CC} = 10V$ to 20V
$V_{IL}$	Logic "0" input voltage	—	—	0.8		$V_{CC} = 10V$ to 20V
$V_{OH}$	High level output voltage, $V_{BIAS} - V_O$	—	0.8	1.4		$I_O = 20$ mA
$V_{OL}$	Low level output voltage, $V_O$	—	0.3	0.6		$I_O = 20$ mA
$I_{LK}$	Offset supply leakage current	—	—	50	$\mu A$	$V_B = V_S = 600V$
$I_{QBS}$	Quiescent $V_{BS}$ supply current	20	75	130		$V_{IN} = 0V$ or 5V
$I_{QCC}$	Quiescent $V_{CC}$ supply current	60	120	180		$V_{IN} = 0V$ or 5V
$I_{IN+}$	Logic "1" input bias current	—	5	20		$V_{IN} = 5V$
$I_{IN-}$	Logic "0" input bias current	—	—	2		$V_{IN} = 0V$
$V_{CCUV+}$ $V_{BSUV+}$	$V_{CC}$ and $V_{BS}$ supply undervoltage positive going threshold	8	8.9	9.8	V	
$V_{CCUV-}$ $V_{BSUV-}$	$V_{CC}$ and $V_{BS}$ supply undervoltage negative going threshold	7.4	8.2	9		
$V_{CCUVH}$ $V_{BSUVH}$	Hysteresis	0.3	0.7	---		
$I_{O+}$	Output high short circuit pulsed current	120	200	—	mA	$V_O = 0V$ $PW \leq 10 \mu s$
$I_{O-}$	Output low short circuit pulsed current	250	350	—		$V_O = 15V$ $PW \leq 10 \mu s$

**Functional Block Diagram**


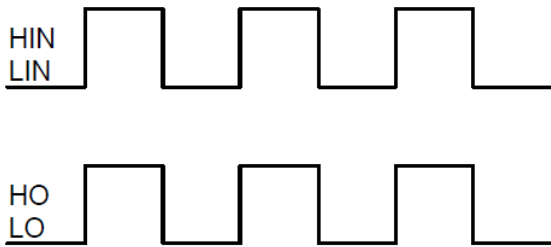
**Lead Definitions**

Symbol	Description
HIN	Logic input for high side gate driver outputs (HO), in phase
LIN	Logic input for high side gate driver outputs (LO), in phase
V <sub>B</sub>	High side floating supply
HO	High side gate drive output
V <sub>S</sub>	High side floating supply return
V <sub>CC</sub>	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

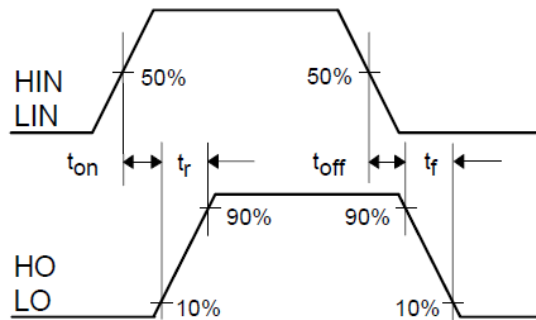
**Lead Assignments**



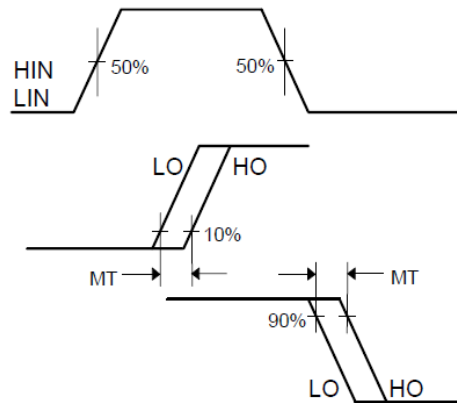
**Advance Information**



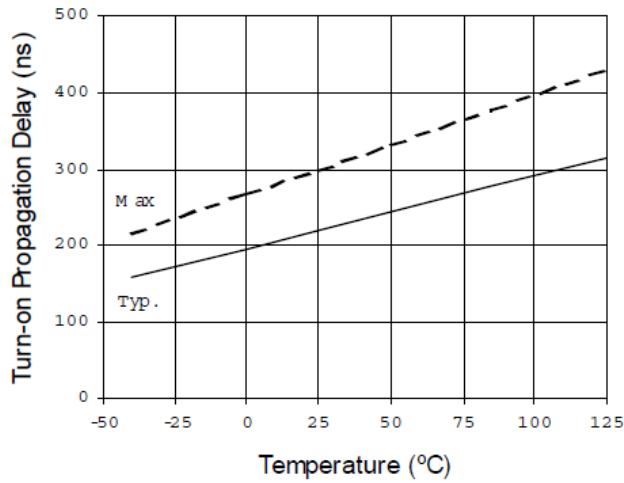
**Figure 1. Input/Output Timing Diagram**



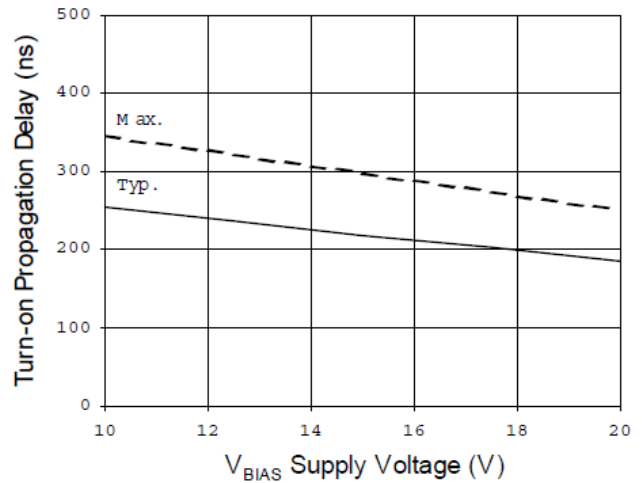
**Figure 2. Switching Time Waveform Definitions**



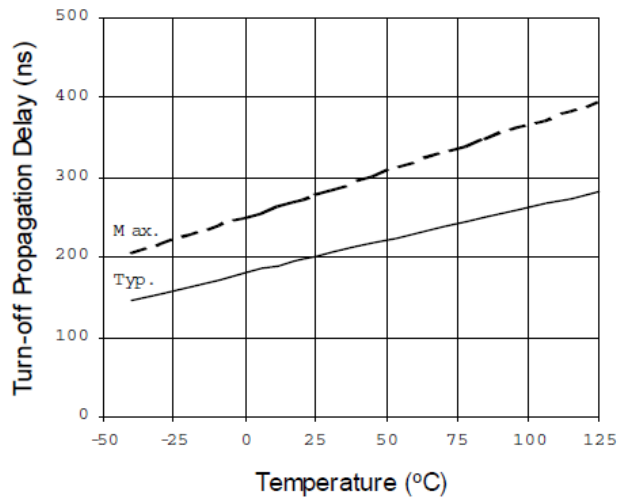
**Figure 3. Delay Matching Waveform Definitions**



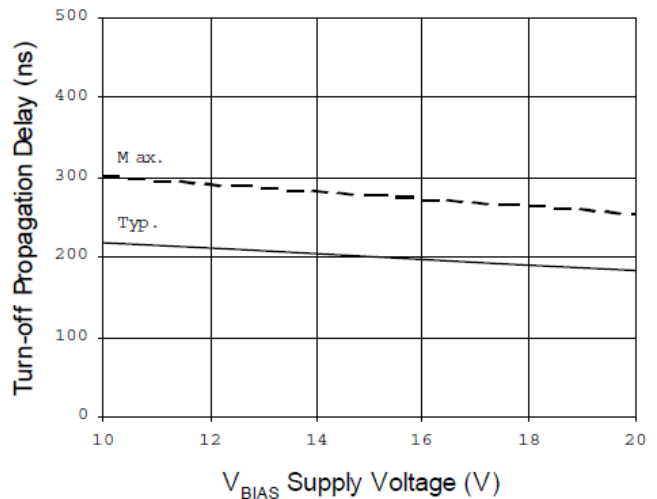
**Figure 4A. Turn-on Propagation Delay vs. Temperature**



**Figure 4B. Turn-on Propagation Delay vs. Supply Voltage**

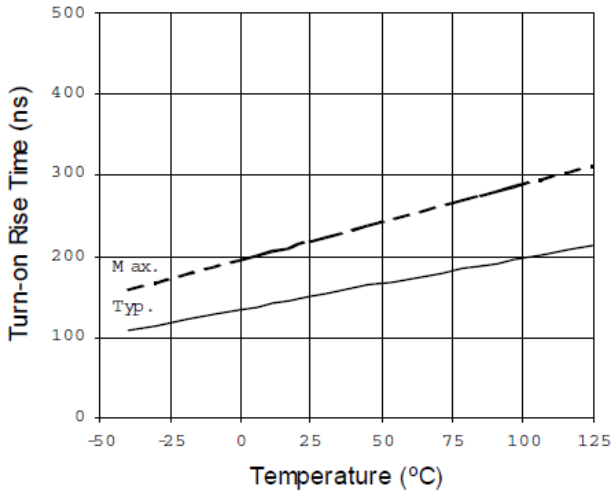


**Figure 5A. Turn-off Propagation Delay vs. Temperature**

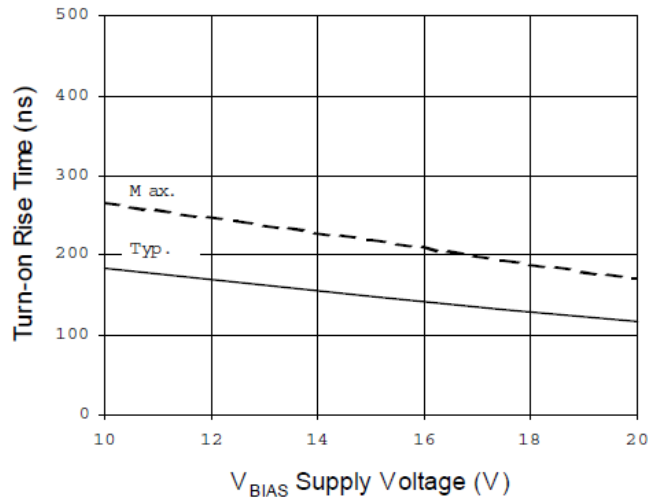


**Figure 5B. Turn-off Propagation Delay vs. Supply Voltage**

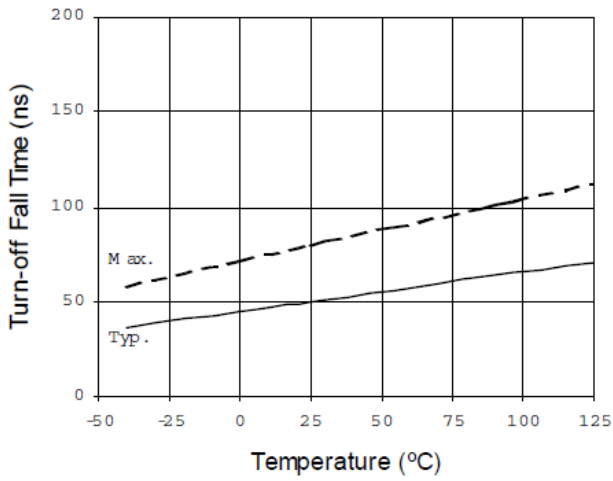




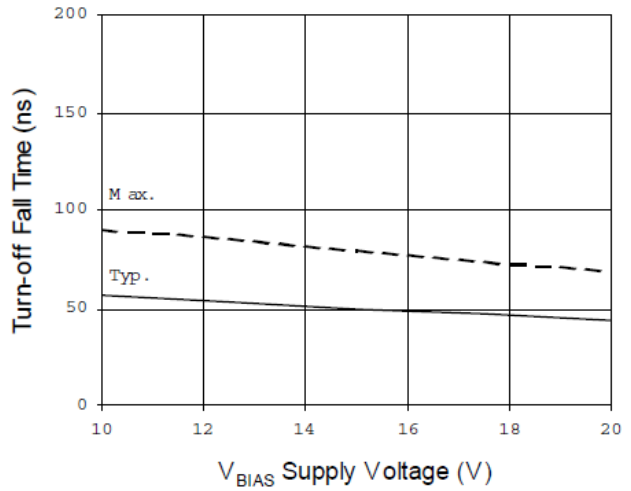
**Figure 6A. Turn-on Rise Time vs. Temperature**



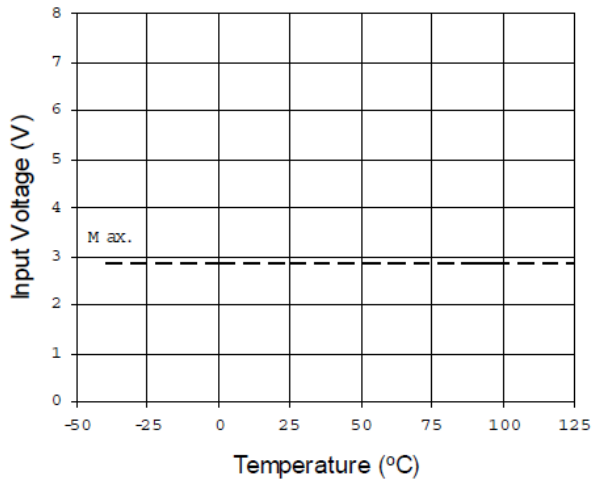
**Figure 6B. Turn-on Rise Time vs. Supply Voltage**



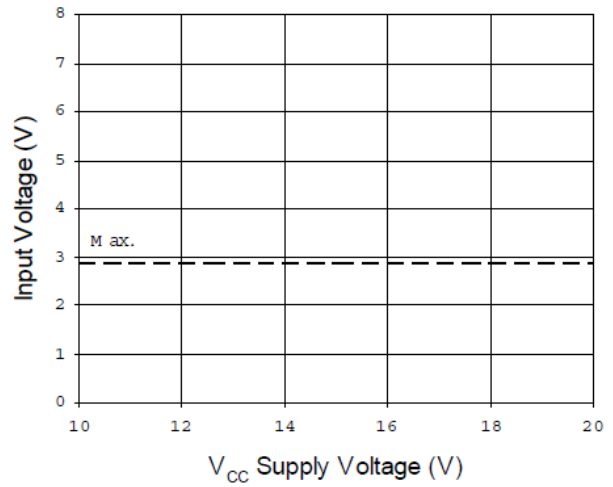
**Figure 7A. Turn-off Fall Time vs. Temperature**



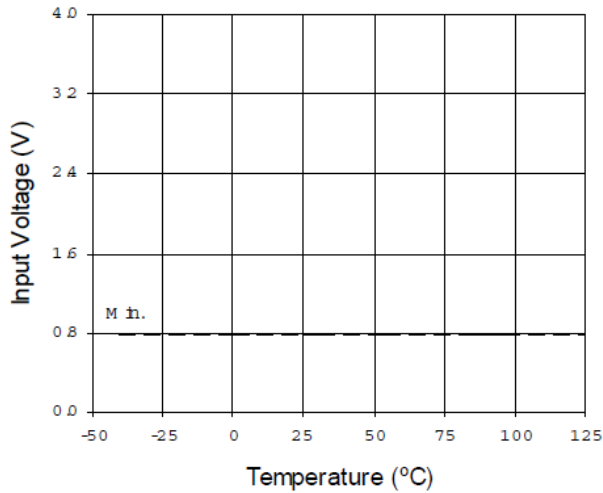
**Figure 7B. Turn-off Fall Time vs. Supply Voltage**



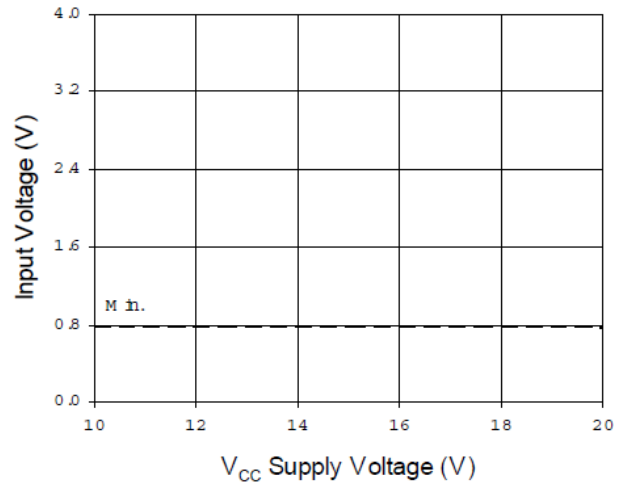
**Figure 8A. Logic "1" Input Voltage vs. Temperature**



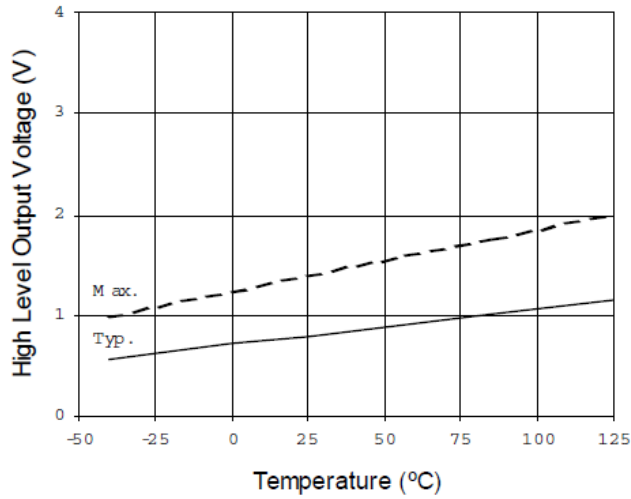
**Figure 8B. Logic "1" Input Voltage vs. Supply Voltage**



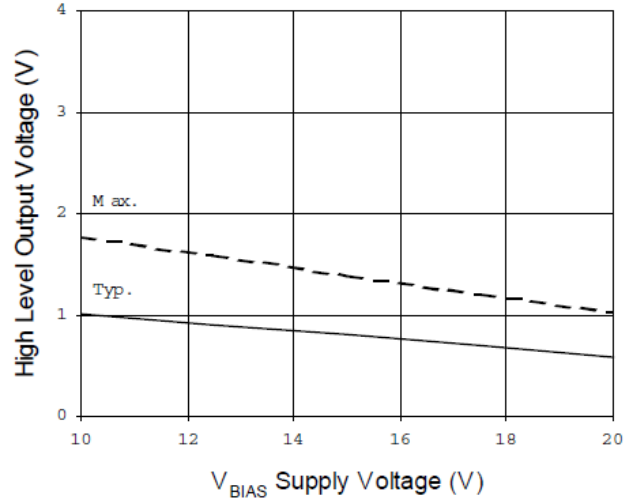
**Figure 9A. Logic "0" Input Voltage vs. Temperature**



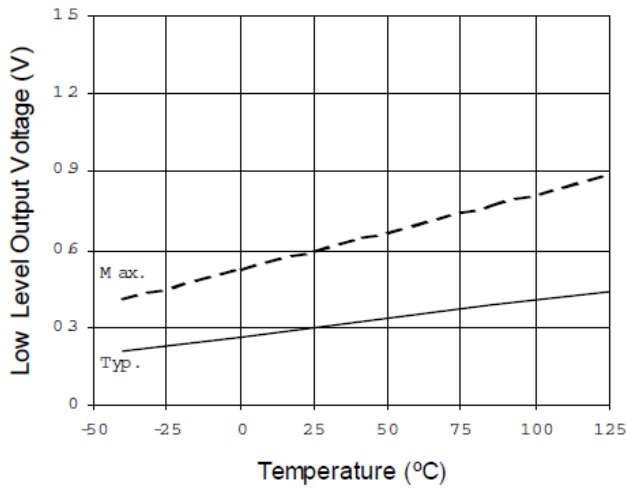
**Figure 9B. Logic "0" Input Voltage vs. Supply Voltage**



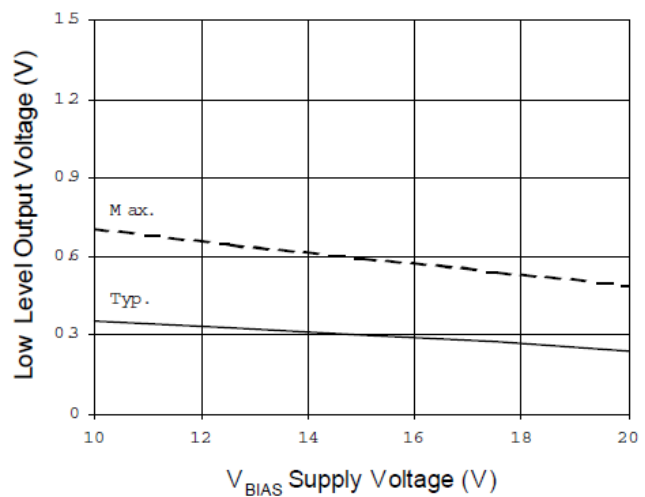
**Figure 10A. High Level Output Voltage vs. Temperature**



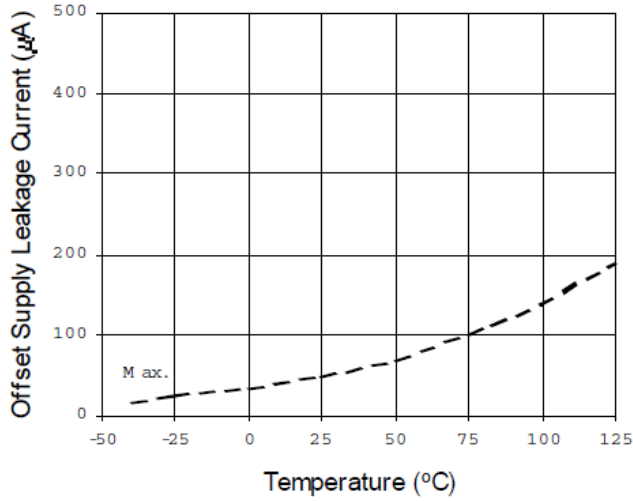
**Figure 10B. High Level Output Voltage vs. Supply Voltage**



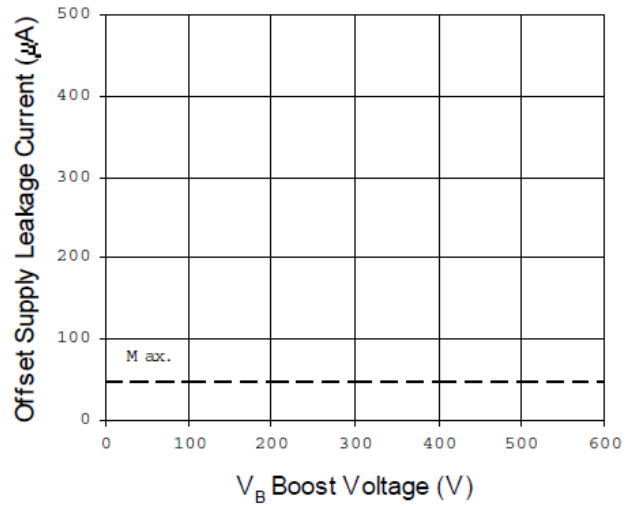
**Figure 11A. Low Level Output Voltage vs. Temperature**



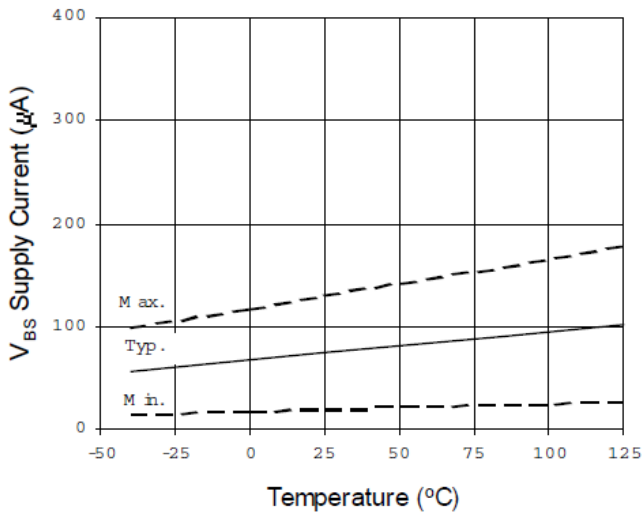
**Figure 11B. Low Level Output Voltage vs. Supply Voltage**



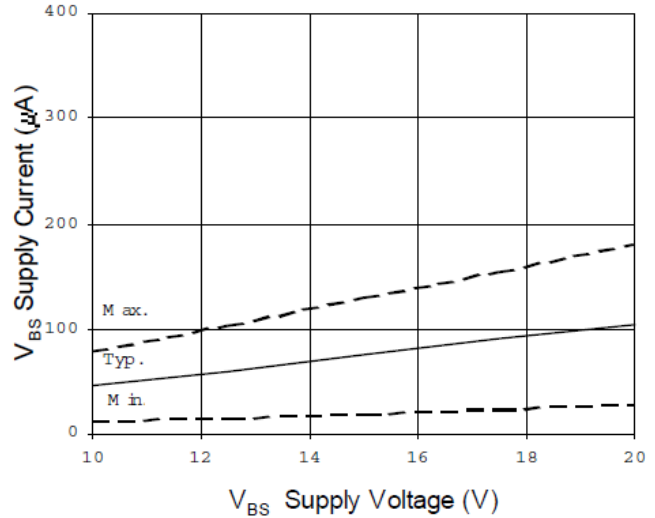
**Figure 12A. Offset Supply Leakage Current vs. Temperature**



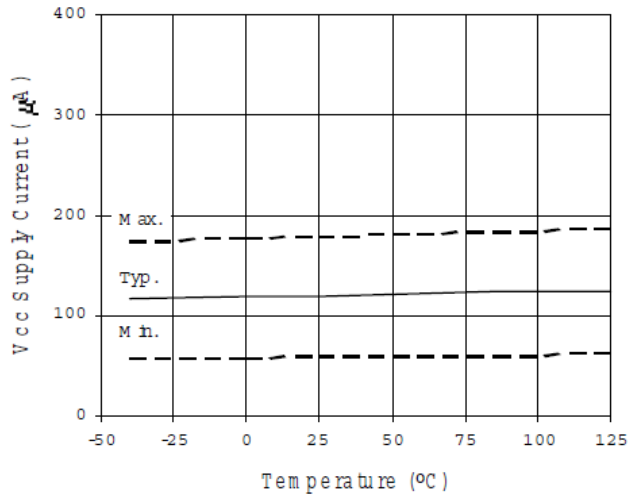
**Figure 12B. Offset Supply Leakage Current vs. Supply Voltage**



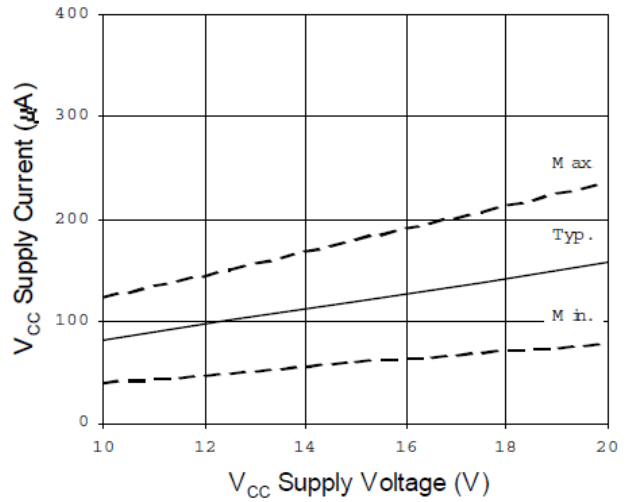
**Figure 13A. V<sub>BS</sub> Supply Current vs. Temperature**



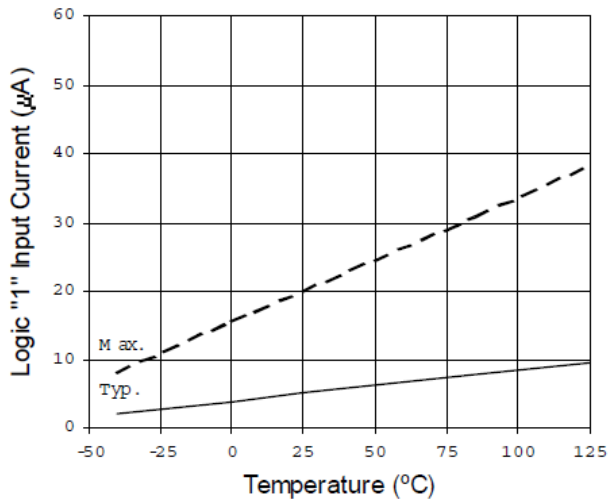
**Figure 13B. V<sub>BS</sub> Supply Current vs. Supply Voltage**



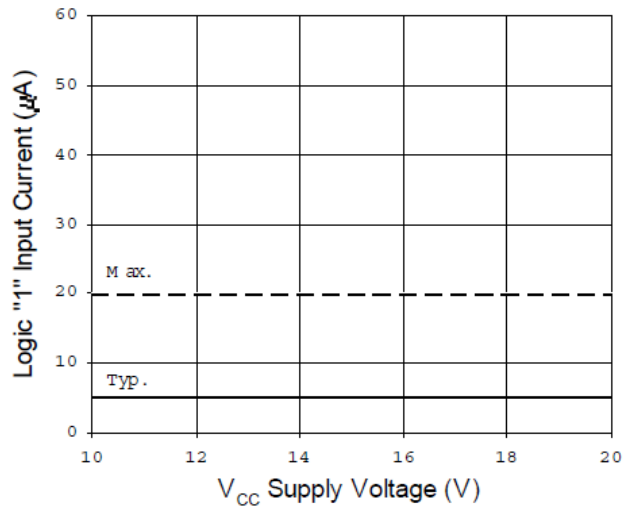
**Figure 14A. Quiescent V<sub>CC</sub> Supply Current vs. Temperature**



**Figure 14B. Quiescent V<sub>CC</sub> Supply Current vs. V<sub>CC</sub> Supply Voltage**

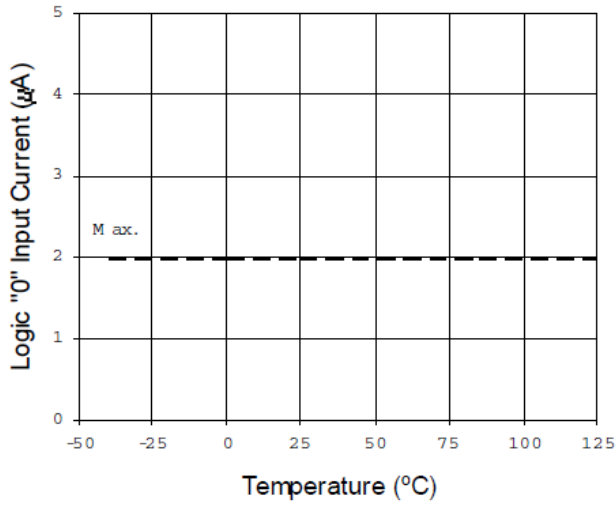


**Figure 15A. Logic "1" Input Current vs. Temperature**

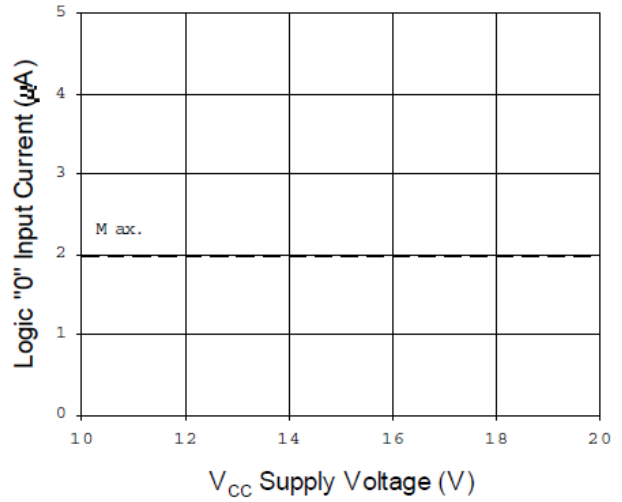


**Figure 15B. Logic "1" Bias Current vs. Supply Voltage**

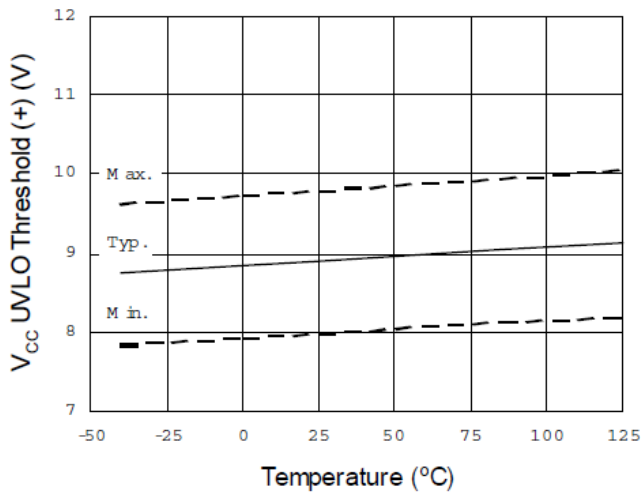
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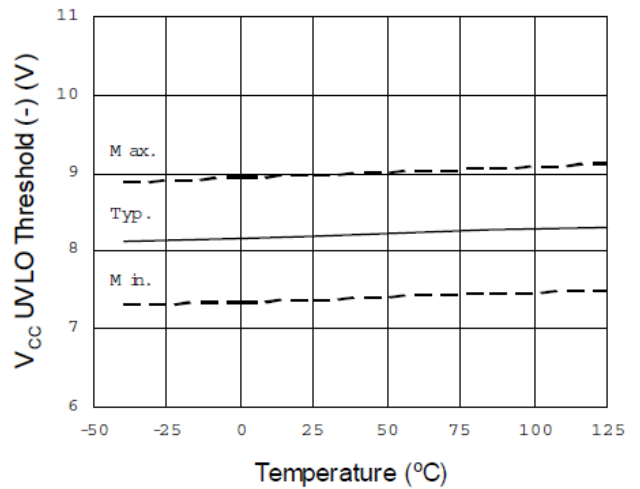
**Figure 16A. Logic "0" Input Current vs. Temperature**



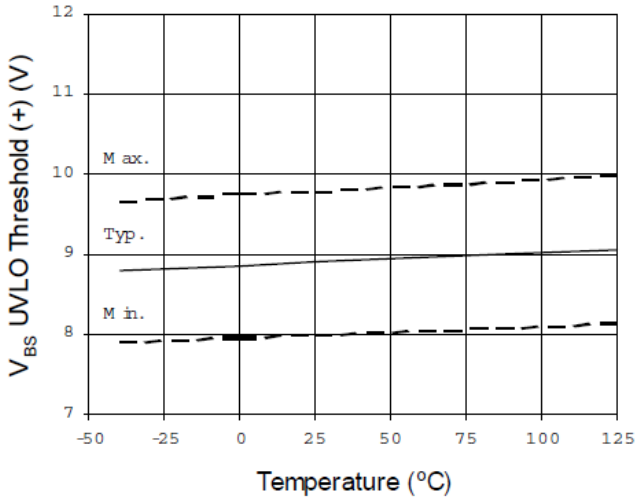
**Figure 16B. Logic "0" Input Current vs. Supply Voltage**



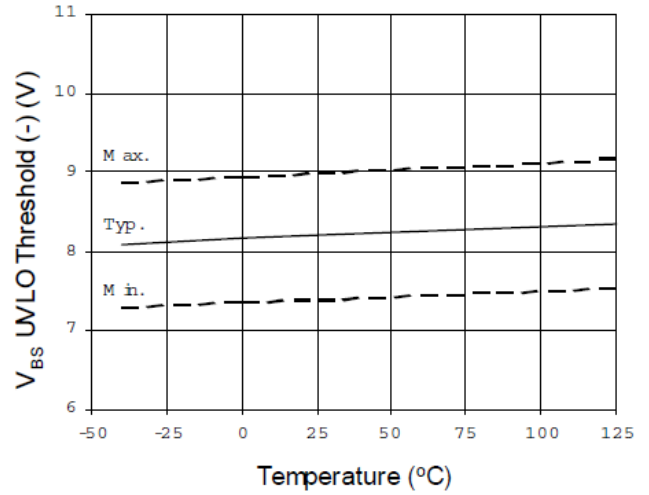
**Figure 17. V<sub>CC</sub> Undervoltage Threshold (+) vs. Temperature**



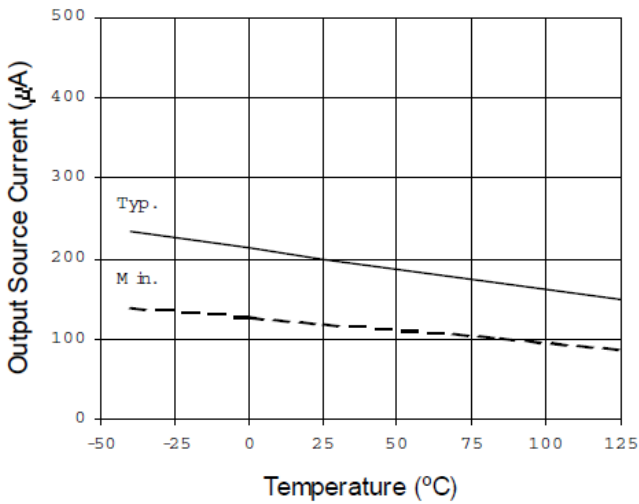
**Figure 18. V<sub>CC</sub> Undervoltage Threshold (-) vs. Temperature**



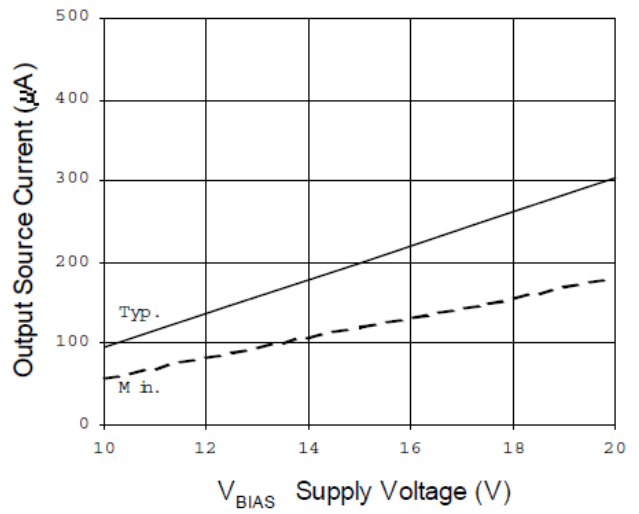
**Figure 19.  $V_{BS}$  Undervoltage Threshold (+) vs. Temperature**



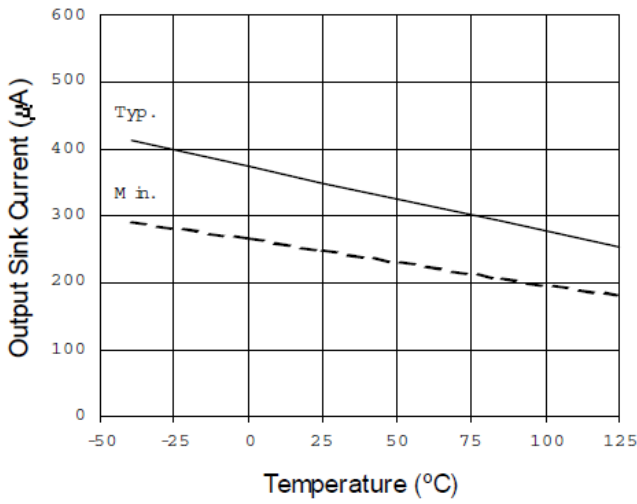
**Figure 20.  $V_{BS}$  Undervoltage Threshold (-) vs. Temperature**



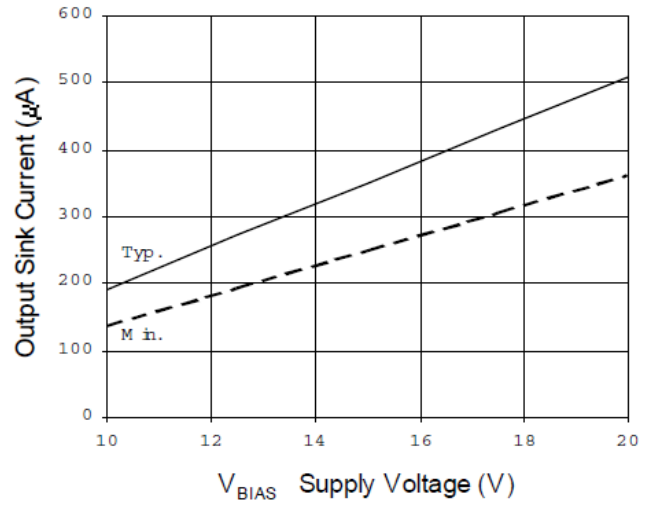
**Figure 21A. Output Source Current vs. Temperature**



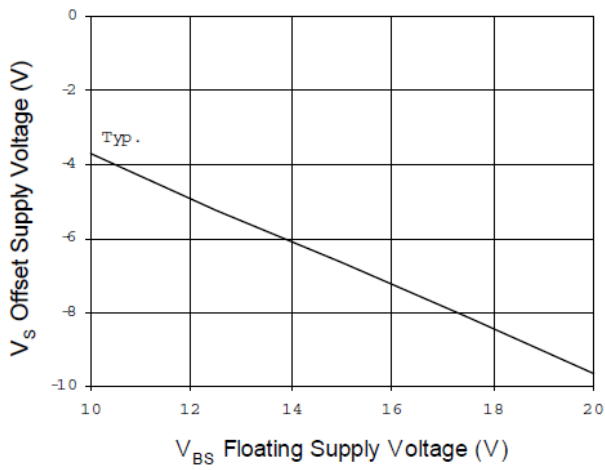
**Figure 21B. Output Source Current vs. Supply Voltage**



**Figure 22A. Output Sink Current vs. Temperature**



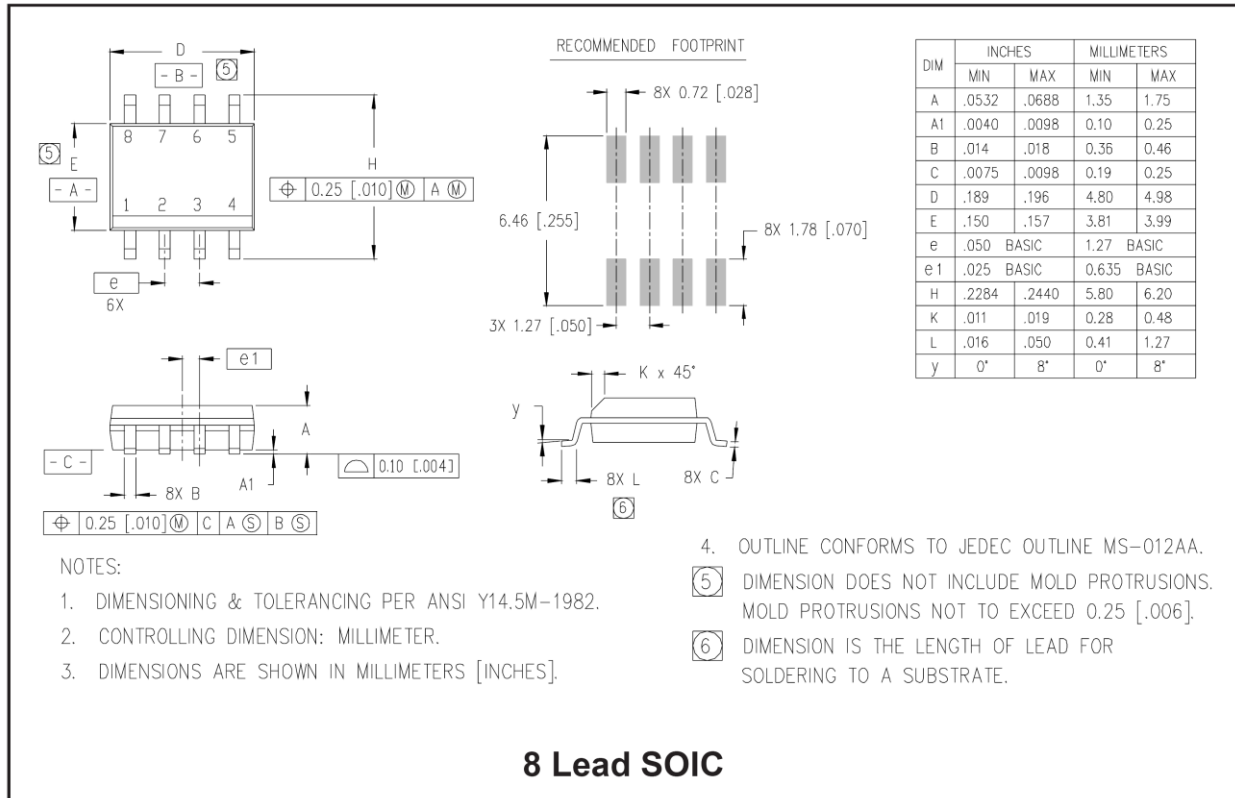
**Figure 22B. Output Sink Current vs. Supply Voltage**



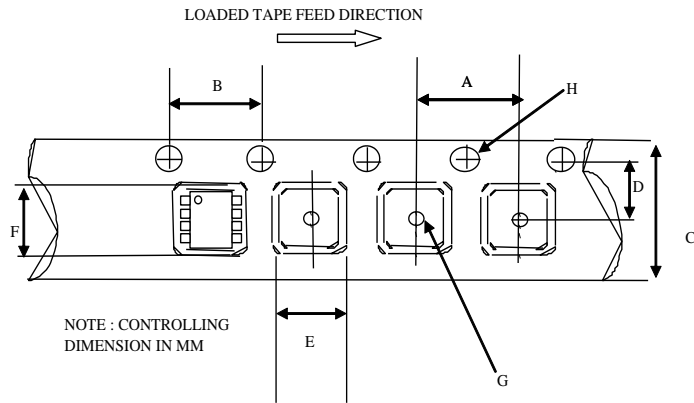
**Figure 23. Maximum V<sub>S</sub> Negative Offset vs. Supply Voltage**

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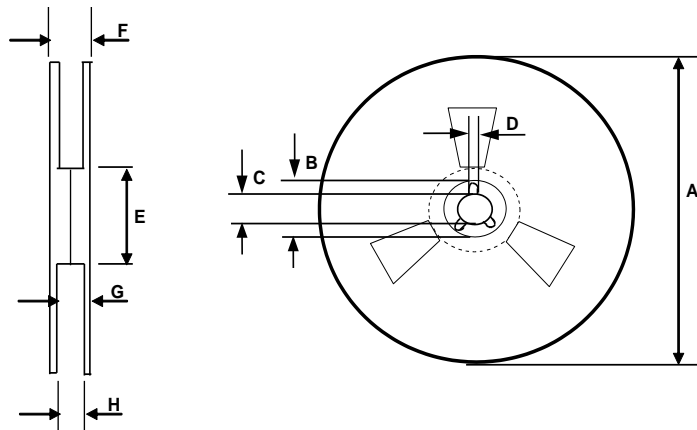
**Package Details**


## Tape and Reel Details



CARRIER TAPE DIMENSION FOR 8SOICN

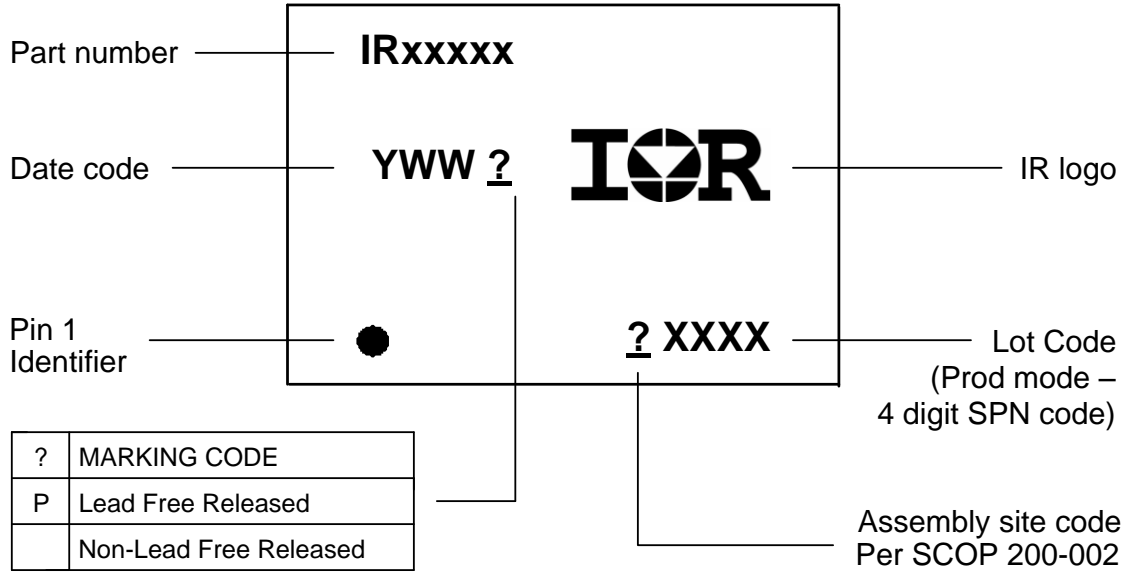
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

**Part Marking Information**



**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>	Industrial <sup>††</sup> (per JEDEC JESD 47E)
	Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.
<b>Moisture Sensitivity Level</b>	MSL2 <sup>†††</sup> (per IPC/JEDEC J-STD-020C)
<b>RoHS Compliant</b>	Yes

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

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