UBA2028

600 V dimmable power IC for compact fluorescent lamps

Rev. 01 — 9 October 2009 **Product data sheet**

1. General description

The UBA2028 is a high voltage power IC that drives and controls electronically ballasted Compact Fluorescent Lamps (CFLs). The IC includes a Metal-Oxide-Semiconductor Transistor (MOST) half bridge power circuit, a dimming function, a high voltage level shift circuit, an oscillator function, a lamp voltage monitor, a current control function, a timer function and protections.

2. Features

- Two internal 600 V, 3 Ω max MOST half bridge powers.
- For steady state currents up to 280 mA.
- For ignition currents up to 1.5 A.
- Adjustable preheat time.
- Adjustable preheat current.
- Current controlled operating.
- Single ignition attempt.
- Adaptive non-overlap time control.
- Integrated high voltage level shift function.
- Power-down function.
- Protection against lamp failures or lamp removal.
- Capacitive mode protection.

3. Applications

- 5 W to 25 W dimmable CFLs, provided that the maximum junction temperature is not exceeded.

founded by Philips

4. Quick reference data

Table 1. Quick reference data

V_{DD} = 13 V; $V_{FS} - V_{SH}$ = 13 V; T_{amb} = 25 °C; all voltages are referenced to GND; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Start-up state						
$V_{DD(startup)}$	start-up supply voltage	for oscillator	12.4	13.0	13.6	V
$V_{DD(stop)}$	stop supply voltage	for oscillator	8.6	9.1	9.6	V
I_{DD}	supply current	oscillator start-up; $V_{DD} < V_{DD(startup)}$	-	170	200	µA
High-voltage supply						
V_{hs}	high-side supply voltage	I_{HV} < 30 µA; t < 1 s	-	-	600	V
Reference voltage						
V_{ref}	reference voltage	I_{leak} = 10 µA	2.86	2.95	3.04	V
Voltage controlled oscillator						
f_{max}	maximum frequency	for bridge; C_{CF} = 100 pF	90	100	110	kHz
f_{min}	minimum frequency	for bridge; C_{CF} = 100 pF	38.9	40.5	42.1	kHz
Half bridge power transistors						
R_{on}	on-state resistance	half bridge power	-	-	3	Ω
I_D	drain current	pulsed; t_p limited by $T_{j(max)}$; $T < T_{j(max)}$	-	-	1.5	A
Preheat current sensor						
V_{ph}	preheat voltage		0.57	0.60	0.63	V
Lamp voltage sensor						
$V_{lamp(fail)}$	lamp fail voltage		0.77	0.81	0.85	V
$V_{lamp(max)}$	maximum lamp voltage		1.44	1.49	1.54	V
Average current sensor						
V_{offset}	offset voltage	V_{CS} = 0 V to 2.5 V	–2	0	+2	mV
g_m	transconductance	f = 1 kHz	1900	3800	5700	µA/mV
Preheat timer						
t_{ph}	preheat time	C_{CT} = 330 nF; R_{IREF} = 33 kΩ	1.6	1.8	2.0	s
V_{OL}	LOW-level output voltage		-	1.4	-	V
V_{OH}	HIGH-level output voltage		-	3.6	-	V

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
UBA2028T	SO20L	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

6. Block diagram

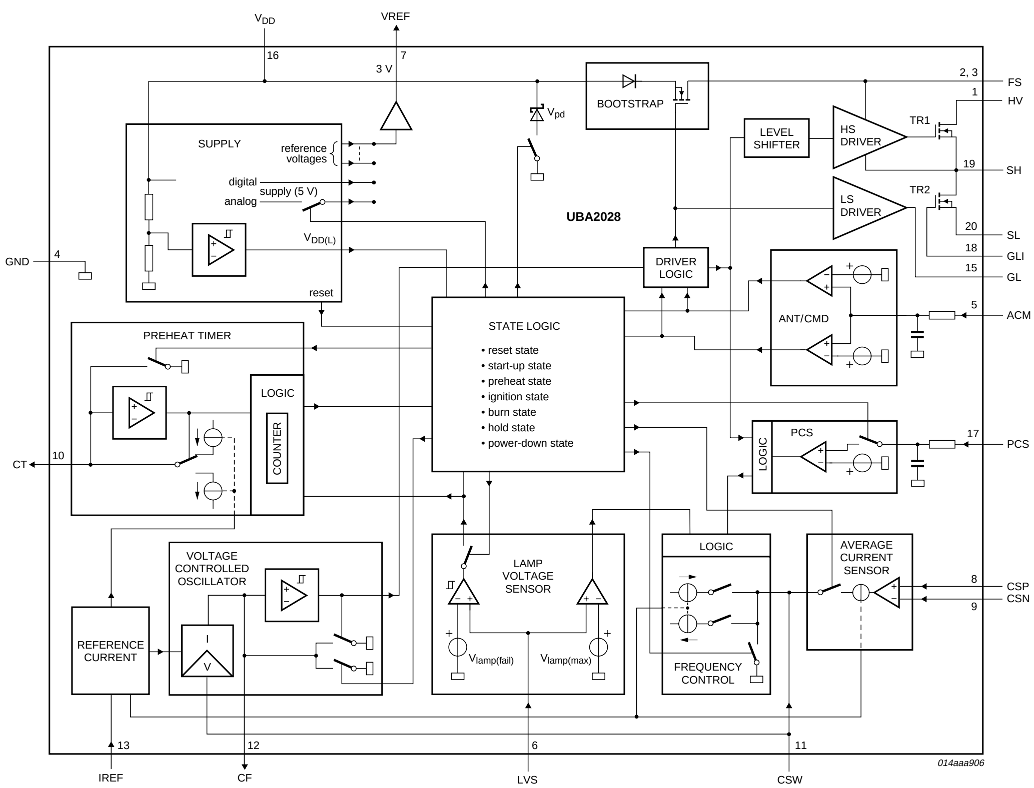


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

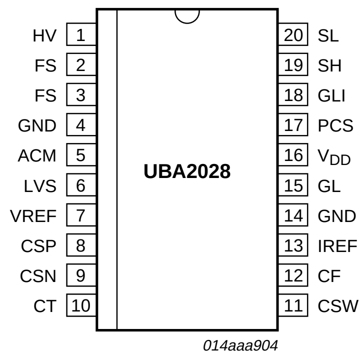


Fig 2. Pin diagram

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
HV	1	high voltage input
FS	2	floating supply voltage; supply for high-side switch
FS	3	floating supply voltage; supply for high-side switch
GND	4	ground
ACM	5	capacitive mode input
LVS	6	lamp voltage sensor input
VREF	7	reference voltage output
CSP	8	positive input for the average current sensor
CSN	9	negative input for the average current sensor
CT	10	preheat timer output
CSW	11	input of voltage controlled oscillator
CF	12	voltage controlled oscillator output
IREF	13	internal reference current input
GND	14	ground
GL	15	gate output for the low-side switch, must be wired to pin 18
V_{DD}	16	low-voltage supply
PCS	17	preheat current sensor input
GLI	18	gate input for the low-side switch, must be wired to pin 15.
SH	19	source for the high-side switch
SL	20	source low side switch, connected to PGND via a resistor[7]

8. Functional description

8.1 Start-up state

Initial start-up can be achieved by charging the low-voltage supply capacitor at pin 16 (see Figure 8 Figure 9) via an external start-up resistor. Start-up of the circuit is achieved under the condition that both half-bridge transistors TR1 and TR2 are non-conductive. The circuit will be reset in the start-up state. If the low-voltage supply (V_{DD}) reaches the value of $V_{DD(startup)}$ the circuit will start oscillating. A DC reset circuit is incorporated in the High-Side (HS) driver. Below the lockout voltage at the FS pin the output voltage (TR1 gate voltage – V_{SH}) is zero. The voltages at pins CF and CT are zero during the start-up state.

8.2 Oscillation

The internal oscillator is a Voltage Controlled Oscillator (VCO) circuit which generates a sawtooth waveform between the $V_{o(osc)max}$ level and 0 V. The frequency of the sawtooth is determined by capacitor C_{CF}, resistor R_{IREF}, and the voltage at pin CSW. The minimum and maximum switching frequencies are determined by R_{IREF} and C_{CF}; their ratio is internally fixed. The sawtooth frequency is twice the half-bridge frequency. The UBA2028 brings the transistors TR1 and TR2 into conduction alternately with a duty cycle of approximately 50 %. An overview of the oscillator signal and driver signals is illustrated in Figure 7. The oscillator starts oscillating at f_{max}. During the first switching cycle the Low-Side (LS) transistor (TR2) is switched on. The first conducting time is made extra long to enable the bootstrap capacitor to charge.

8.3 Adaptive non-overlap

The non-overlap time is realized with an adaptive non-overlap timing circuit (ANT). By using an adaptive non-overlap circuit, the application can determine the duration of the non-overlap time and make it optimum for each frequency; see Figure 7. The non-overlap time is determined by the slope of the half-bridge voltage, and is detected by the signal across resistor R15 see Figure 8 (R6 in Figure 9) which is connected directly to pin ACM. The minimum non-overlap time is internally fixed. The maximum non-overlap time is internally fixed at approximately 25 % of the bridge period time. An internal filter of 30 ns is included at the ACM pin to increase the noise immunity.

8.4 Timing circuit

A timing circuit is included to determine the preheat time and the ignition time. The circuit consists of a clock generator and a counter.

The preheat time is defined by C_{CT} and R_{IREF} connected to pins 10 and 13, and consists of 7 pulses at C_{CT}; the maximum ignition time is 1 pulse at C_{CT}. The timing circuit starts operating after the start-up state, as soon as the low supply voltage (V_{DD}) has reached $V_{DD(startup)}$ or when a critical value of the lamp voltage ($V_{lamp(fail)}$) is exceeded. When the timer is not operating C_{CT} is discharged to 0 V at 1 mA.

8.5 Preheat state

After starting at f_{max}, the frequency decreases until the momentary value of the voltage across sense resistor R21 (see Figure 8) or R5 (Figure 9) reaches the internally fixed preheat voltage level (pin PCS). Detection of the pre-heat voltage occurs during the end of the ‘on-time’ of the low side switch TR2 when the internal pre-heat fixed voltage reference level is exceeded. Once detection has occurred the output current of the Preheat Current Sensor (PCS) circuit discharges the capacitor C_{CSW}, thus raising the frequency. The internal pre-heat control is reset during each “on-time’ of the high side switch TR1, thus C_{CSW} is charged, and the frequency decreases. It remains in this condition when no detection occurs. The preheat time begins at the moment that the circuit starts oscillating. During the preheat time the Average Current Sensor (ACS) circuit is disabled. An internal filter of 30 ns is included at pin PCS to increase the noise immunity.

8.6 Ignition state

After the preheat time the ignition state is entered and the frequency will sweep down due to charging of the capacitor at pin CSW with an internally fixed current; see Figure 4. During this continuous decrease in frequency, the circuit approaches the resonant frequency of the load. This will cause a high voltage across the load, which normally ignites the lamp. The ignition voltage of a lamp is designed above the $V_{lamp(fail)}$ level. If the lamp voltage exceeds the $V_{lamp(fail)}$ level the ignition timer is started.

8.7 Burn state

If the lamp voltage does not exceed the $V_{lamp(max)}$ level the voltage at pin CSW will continue to increase until the clamp level at pin CSW is reached; see Figure 4. As a consequence the frequency will decrease until the minimum frequency is reached.

When the frequency reaches its minimum level it is assumed that the lamp has ignited and the circuit will enter the burn state. The Average Current Sensor (ACS) circuit will be enabled. As soon as the averaged voltage across sense resistor R21 (see Figure 8) or R5 (Figure 9), measured at pin CSN, reaches the reference level at pin CSP, the average current sensor circuit will take over the control of the lamp current. The average current through R21 or R5 is transferred to a voltage at the voltage controlled oscillator and regulates the frequency and, as a result, the lamp current.

8.8 Lamp failure mode

8.8.1 During ignition state

If the lamp does not ignite, the voltage level increases. When the lamp voltage exceeds the $V_{lamp(max)}$ level, the voltage will be regulated at the $V_{lamp(max)}$ level; see Figure 5. When the $V_{lamp(fail)}$ level is crossed the ignition timer has already started. If the voltage at pin LVS is above the $V_{lamp(fail)}$ level at the end of the ignition time the circuit stops oscillating and is forced into the Power-down mode. The circuit will be reset only when the supply voltage is powered down.

8.8.2 During burn state

If the lamp fails during normal operation, the voltage across the lamp will increase and the lamp voltage will exceed the $V_{lamp(fail)}$ level; see Figure 6. At that moment the ignition timer is started. If the lamp voltage increases further it will reach the $V_{lamp(max)}$ level. This forces the circuit to re-enter the ignition state and results in an attempt to re-ignite the lamp. If during restart the lamp still fails, the voltage remains high until the end of the ignition time. At the end of the ignition time the circuit stops oscillating and the circuit will enter the Power-down mode.

8.9 Power-down mode

The Power-down mode will be entered if, at the end of the ignition time, the voltage at pin LVS is above $V_{lamp(fail)}$. In the Power-down mode the oscillator will be stopped and both TR1 and TR2 will be non-conductive. The V_{DD} supply is internally clamped. The circuit is released from the Power-down mode by lowering the low-voltage supply below $V_{DD(rst)}$.

8.10 Capacitive mode protection

The signal across R15 see Figure 8 (R6 in Figure 9) also gives information about the switching behavior of the half bridge. If, after the preheat state, the voltage across the ACM resistor (R15 or R6) does not exceed the $V_{det(capm)}$ level during the non-overlap time, the Capacitive Mode Detection circuit (CMD) assumes that the circuit is in the capacitive mode of operation. As a consequence the frequency will directly be increased to f_{max}. The frequency behavior is de coupled from the voltage at pin CSW until C_{CSW} has been discharged to zero.

8.11 Charge coupling

Due to parasitic capacitive coupling to the high voltage circuitry all pins are burdened with a repetitive charge injection. Given the typical application the pins IREF and CF are sensitive to this charge injection. For charge coupling of approximately 8 pC, a safe functional operation of the IC is guaranteed, independent of the current level.

Charge coupling at current levels below 50 µA will not interfere with the accuracy of the V_{CS}, $V_{i(PCS)}$ and $V_{i(ACM)}$ levels.

Charge coupling at current levels below 20 µA will not interfere with the accuracy of any parameter.

8.12 Design equations

The following design equations are used to calculate the desired preheat time, the maximum ignition time, and the minimum and the maximum switching frequency.

$$t_{ph} = 1.8 \times \frac{C_{CT}}{330 \times 10^{-9}} \times \frac{R_{IREF}}{33 \times 10^{3}} \quad (1)$$

$$t_{ign} = 0.26 \times \frac{C_{CT}}{330 \times 10^{-9}} \times \frac{R_{IREF}}{33 \times 10^{3}} \quad (2)$$

$$f_{min} = 40.5 \times 10^{3} \times \frac{100 \times 10^{-12}}{C_{CF}} \times \frac{33 \times 10^{3}}{R_{IREF}} \quad (3)$$

$$f_{max} = 2.5 \times f_{min} \quad (4)$$

Start of ignition is defined as the moment at which the measured lamp voltage crosses the $V_{lamp(fail)}$ level; see Section 8.8.

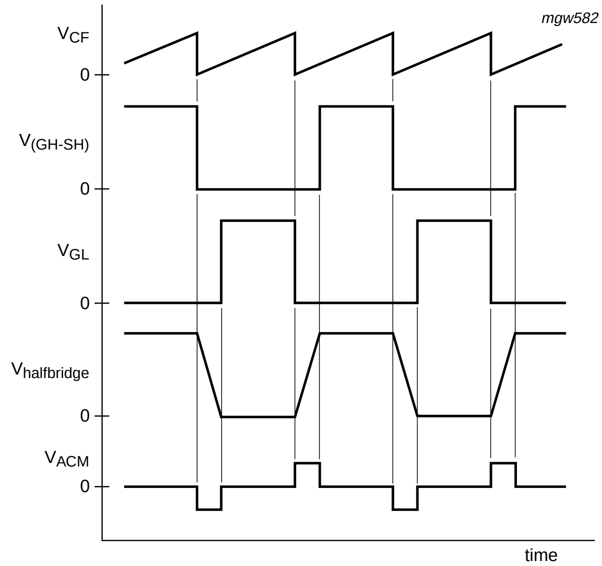


Fig 3. Oscillator and drive signals

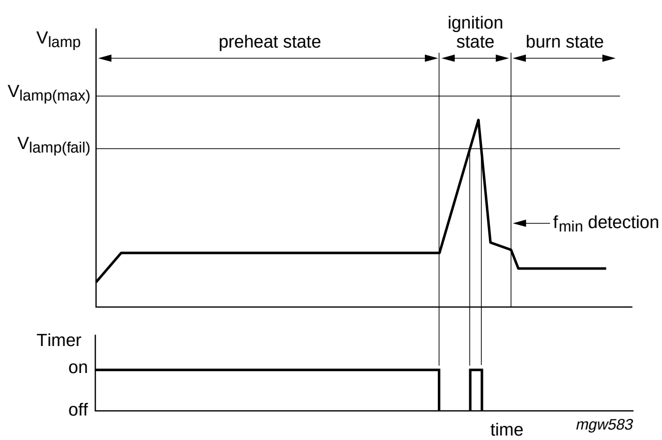


Fig 4. Normal ignition behavior

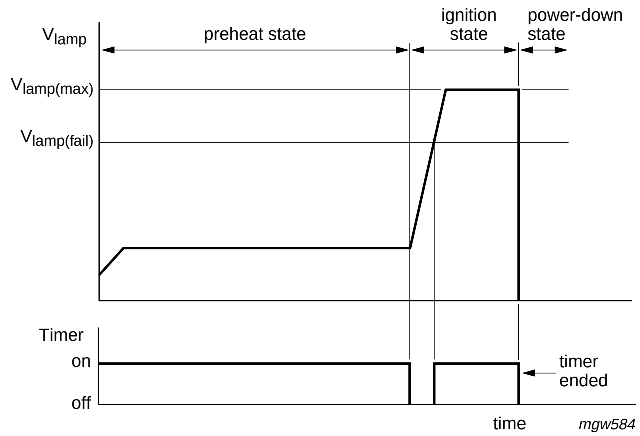


Fig 5. Failure mode during ignition

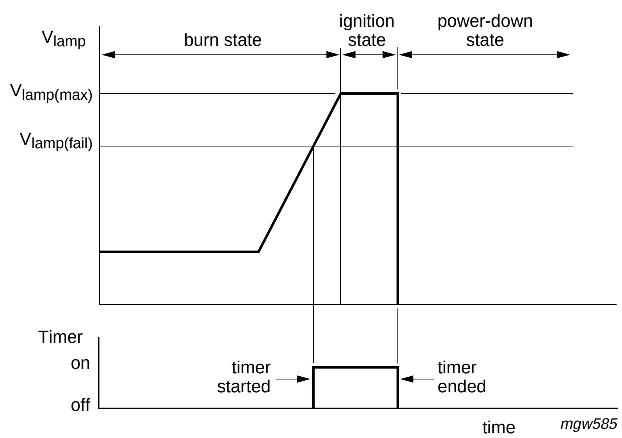


Fig 6. Failure mode during burn

8.13 Layout considerations

The connection of PGND and GND is shown in Figure 7

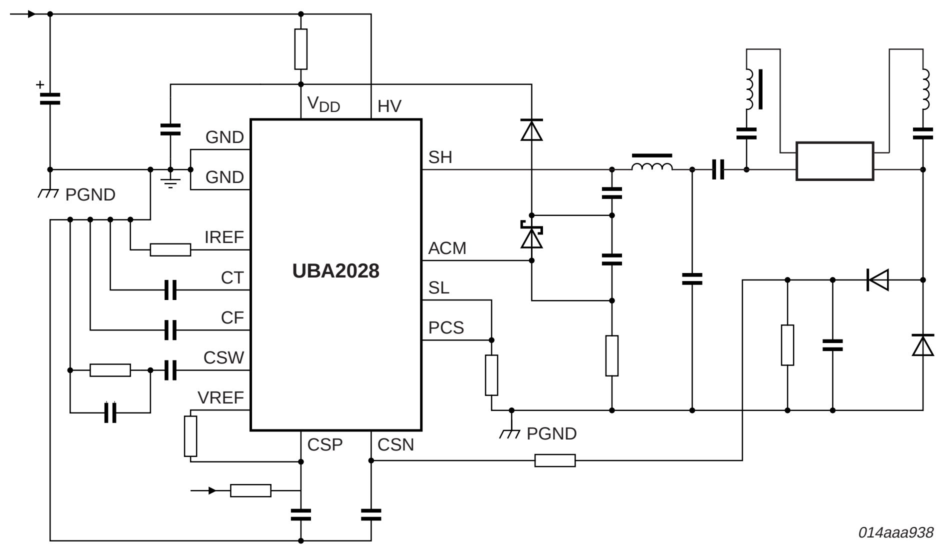


Fig 7. PGND and GND connection

9. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages referenced to GND.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{HV}	voltage on pin HV	operating; during 1 s		-	600	V
		operating		-	510	V
I_D	drain current	TR1 pulsed; t_p limited by $T_{j(max)}$; $T < T_{j(max)}$		-	1.5	A
		TR2 pulsed; t_p limited by $T_{j(max)}$; $T < T_{j(max)}$		-	1.5	A
V_{VDD}	voltage on pin V_{DD}			-	14	V
V_{FS}	voltage on pin FS	with respect to SH		0	14	V
$V_{i(ACM)}$	input voltage on pin ACM			–5	+5	V
$V_{i(PCS)}$	input voltage on pin PCS			–5	+5	V
$V_{i(LVS)}$	input voltage on pin LVS			0	5	V
$V_{i(CSP)}$	input voltage on pin CSP			0	5	V
$V_{i(CSN)}$	input voltage on pin CSN			–0.3	+5	V
$V_{i(CSW)}$	input voltage on pin CSW			0	5	V
SR	slew rate	pin SH; repetitive		–4	+4	V/ns
T_{amb}	ambient temperature			–25	+80	°C
T_j	junction temperature			–25	+150	°C
T_{stg}	storage temperature			–55	+150	°C
V_{ESD}	electrostatic discharge voltage	pin HV	[1]	-	1500	V
		pins FS, SH	[1]	-	1000	V
		pin GL	[1]	-	< 500	V
		pin GL	[2]	-	150	V

[1] In accordance with the human body model, i.e. equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[2] In accordance with the machine model, i.e. equivalent to discharging a 200 pF capacitor through a 0.75 μH coil and a 10 Ω resistor.

10. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	SO20L; in free air	75	K/W

11. Characteristics

Table 6. Characteristics
V_{DD} = 13 V; $V_{FS} - V_{SH}$ = 13 V; T_{amb} = 25 °C; all voltages referenced to GND; see application circuits of [8] [9] unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Start-up state: pin V_{DD}							
V_{DD}	supply voltage	for defined driver output; TR1 = off; TR2 = off		-	-	6	V
$V_{DD(rst)}$	reset supply voltage	TR1 = off; TR2 = off		4.5	5.5	7.0	V
$V_{DD(startup)}$	start-up supply voltage	for oscillator		12.4	13.0	13.6	V
$V_{DD(stop)}$	stop supply voltage	for oscillator		8.6	9.1	9.6	V
$V_{DD(hys)}$	hysteresis of supply voltage	for start-stop		3.5	3.9	4.4	V
$V_{clamp(VDD)}$	clamp voltage on pin VDD	Power-down mode		10	11	12	V
I_{DD}	supply current	oscillator start-up; $V_{DD} < V_{DD(startup)}$		-	170	200	µA
$I_{DD(pd)}$	power-down supply current	V_{DD} = 9 V		-	170	200	µA
High voltage supply: pins HV, SH and FS							
V_{hs}	high-side supply voltage	I_{HV} < 30 µA; t < 1 s		-	-	600	V
I_{leak}	leakage current	600 V at high-voltage pins		-	-	30	µA
Reference voltage: pin VREF							
V_{ref}	reference voltage	I_{leak} = 10 µA		2.86	2.95	3.04	V
$\Delta V_{ref}/V_{ref}$	relative reference voltage variation	I_{leak} = 10 µA; T_{amb} = 25 °C to 150 °C		-	–0.64	-	%
I_{source}	source current			1	-	-	mA
I_{sink}	sink current			1	-	-	mA
Z_o	output impedance	I_{leak} = 1 mA source		-	3.0	-	Ω
Current supply: pin IREF							
V_I	input voltage			-	2.5	-	V
I_I	input current	reference range		65	-	95	µA
Voltage controlled oscillator							
Output: pin CSW							
V_O	output voltage	for control		2.7	3.0	3.3	V
V_{clamp}	clamp voltage	burn state		2.8	3.1	3.4	V
Voltage controlled oscillator output: pin CF							
f_{max}	maximum frequency	for bridge; C_{CF} = 100 pF		90	100	110	kHz
f_{min}	minimum frequency	for bridge; C_{CF} = 100 pF		38.9	40.5	42.1	kHz
$\Delta f/f$	relative frequency variation	T_{amb} = –20 °C to +80 °C		-	1.3	-	%
t_{start}	start time	first output oscillator stroke		-	50	-	µs
$t_{no(min)}$	minimum non-overlap time	TR1 to TR2 gate voltages		0.68	0.90	1.13	µs
		TR2 to TR1 gate voltages		0.75	1.00	1.25	µs
$t_{no(max)}$	maximum non-overlap time	f_{bridge} = 40 kHz	[1]	-	7.5	-	µs
$V_{O(osc)max}$	maximum oscillator output voltage	$f = f_{min}$		-	2.5	-	V

Table 6. Characteristics *…continued*

V_{DD} = 13 V; $V_{FS} - V_{SH}$ = 13 V; T_{amb} = 25 °C; all voltages referenced to GND; see application circuits of [8] [9] unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{o(startup)}$	start-up output current	for oscillator; V_{CF} = 1.5 V	3.8	4.5	5.2	µA
I_{osc}	oscillator current	V_{CF} = 1.5 V	21	-	54	µA
Output driver						
Low-side driver output: pin GL						
V_{OH}	HIGH-level output voltage	I_o = 10 mA	12.5	-	-	V
V_{OL}	LOW-level output voltage	I_o = 10 mA	-	-	0.5	V
$I_{O(source)}$	output source current	V_{GL} = 0 V	135	180	235	mA
$I_{sink(o)}$	output sink current	V_{GL} = 13 V	265	330	415	mA
R_{on}	on-state resistance	I_o = 10 mA	32	39	45	Ω
R_{off}	off-state resistance	I_o = 10 mA	16	21	26	Ω
Output stage						
Power transistors						
R_{on}	on-state resistance	TR1 high side power	-	-	3	Ω
		TR2 low side power	-	-	3	Ω
$R_{on(150)}/R_{on(25)}$	on-state resistance ratio (150 °C to 25 °C)		-	2.7	-	-
Floating supply voltage: pin FS						
V_{FS}	voltage on pin FS	for lockout	2.8	3.5	4.2	V
I_{FS}	current on pin FS	DC level at TR1 gate voltage – V_{SH} = 13 V	-	35	-	µA
Bootstrap diode						
$V_{Fd(bs)}$	bootstrap diode forward voltage	I = 5 mA	1.3	1.7	2.1	V
Preheat current sensor						
Input: pin PCS						
I_I	input current	$V_{i(PCS)}$ = 0.6 V	-	-	1	µA
V_{ph}	preheat voltage		0.57	0.60	0.63	V
Output: pin CSW						
$I_{source(o)}$	output source current	$V_{i(CSW)}$ = 2.0 V	9.0	10	11	µA
$I_{sink(o)}$	output sink current	$V_{i(CSW)}$ = 2.0 V	-	10	-	µA
Adaptive non-overlap and capacitive mode detection; pin ACM						
I_I	input current	$V_{i(ACM)}$ = 0.6 V	-	-	1	µA
$V_{det(capm)}$	capacitive mode detection voltage	positive	80	100	120	mV
		negative	–68	–85	–102	mV
Input: pin LVS						
I_I	input current	$V_{i(LVS)}$ = 0.81 V	-	-	1	µA
$V_{lamp(fail)}$	lamp fail voltage		0.77	0.81	0.85	V
$V_{lamp(fail)hys}$	lamp fail voltage hysteresis		119	144	169	mV
$V_{lamp(max)}$	maximum lamp voltage		1.44	1.49	1.54	V
Output: pin CSW						
$I_{sink(o)}$	output sink current	$V_{i(CSW)}$ = 2.0 V	27	30	33	µA

Table 6. Characteristics *…continued*

V_{DD} = 13 V; $V_{FS} - V_{SH}$ = 13 V; T_{amb} = 25 °C; all voltages referenced to GND; see application circuits of [8] [9] unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{source(o)}$	output source current	$V_{i(CSW)}$ = 2.0 V	9.0	10	11	µA
Average current sensor						
Input: pins CSP and CSN						
I_I	input current	V_{CS} = 0 V	-	-	1	µA
V_{offset}	offset voltage	$V_{i(CSP)} = V_{i(CSN)}$ = 0 V to 2.5 V	–2	0	+2	mV
g_m	transconductance	f = 1 kHz	1900	3800	5700	µA/mV
Output: pin CSW						
I_o	output current	source and sink; $V_{i(CSW)}$ = 2 V	85	95	105	µA
Preheat timer; pin CT						
t_{ph}	preheat time	C_{CT} = 330 nF; R_{IREF} = 33 kΩ	1.6	1.8	2.0	s
t_{ign}	ignition time	C_{CT} = 330 nF; R_{IREF} = 33 kΩ	-	0.32	-	s
I_o	output current	$V_{o(CT)}$ = 2.5 V	5.5	5.9	6.3	µA
V_{OL}	LOW-level output voltage		-	1.4	-	V
V_{OH}	HIGH-level output voltage		-	3.6	-	V
V_{hys}	hysteresis voltage	for output	2.05	2.20	2.35	V

[1] The maximum non-overlap time is determined by the level of the CF signal. If this signal exceeds a level of 1.25 V, the non-overlap will end, resulting in a maximum non-overlap time of 7.5 µs at a bridge frequency of 40 kHz.

12. Application information

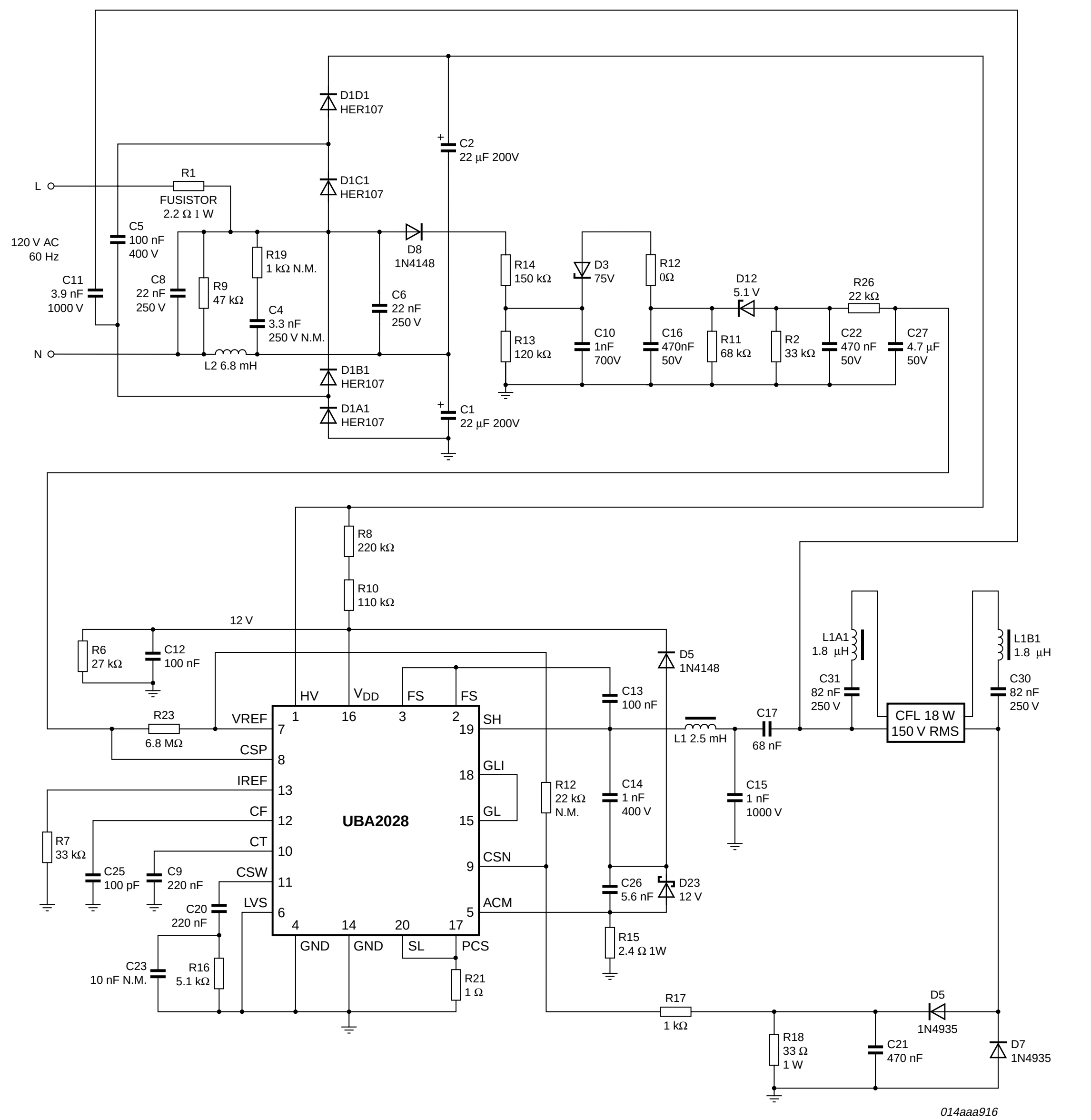


Fig 8. Application circuit 120 V

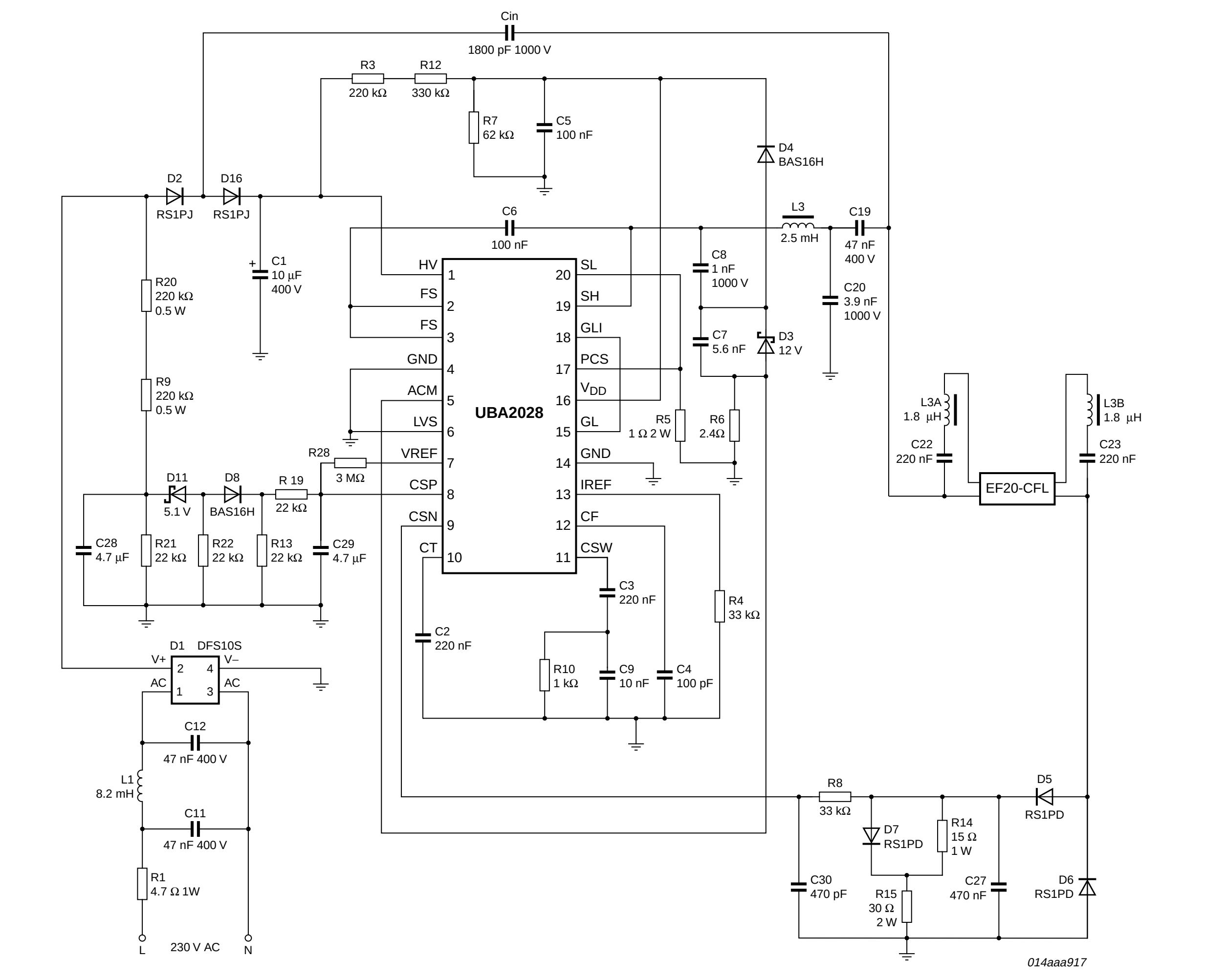


Fig 9. Application circuit 230 V

13. Test information

13.1 Quality information

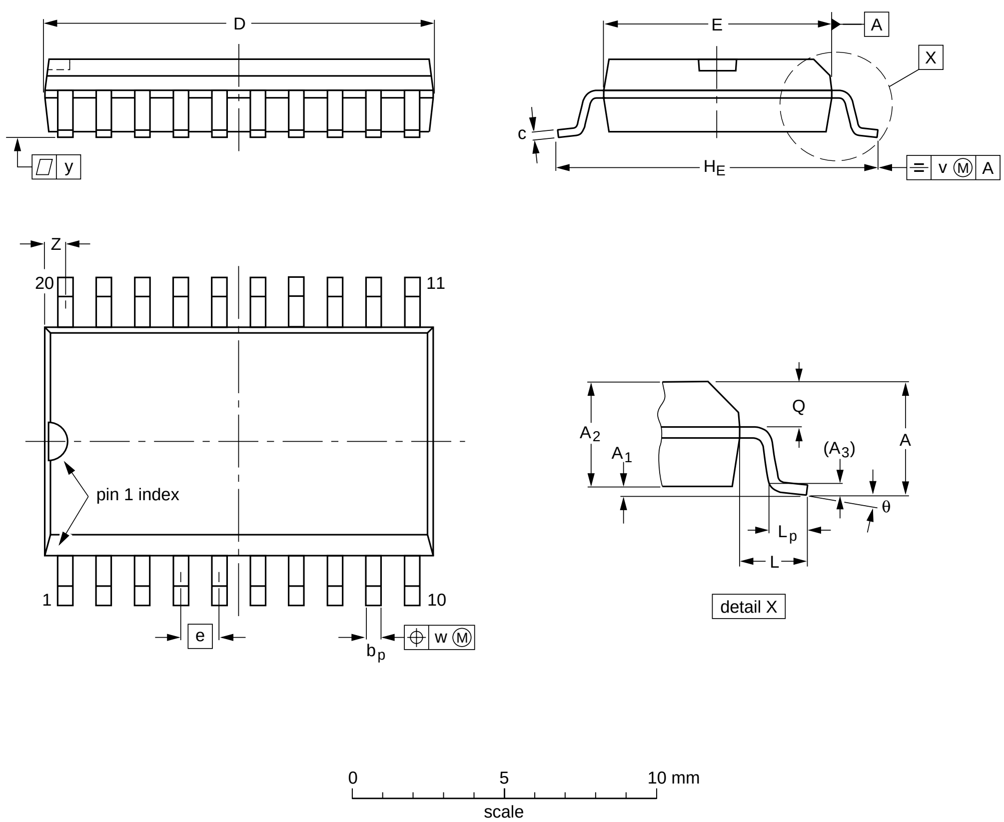
13.1.1 Safety: Electric, Magnetic and ElectroMagnetic Fields (EMF)

- NXP Semiconductors manufactures and sells many products, which, like any electronic apparatus, in general may have the ability to emit and receive electromagnetic signals.
- One of NXP Semiconductors' leading business principles is to take health and safety measures for our products, to comply with all applicable legal requirements and to stay well within the EMF standards applicable at the time of printing this document for each individual product.
- NXP Semiconductors aims, at all times, to supply safe products and services.

- The consensus of scientific opinion is that EMF exposure below the limits prescribed by safety standards and recommendations, applicable at the time of printing this document, poses no risk to human health.
- NXP Semiconductors plays an active role in the development of international EMF and safety standards, enabling NXP Semiconductors to anticipate further developments in standardization for early integration in its products.
- Additional information can be obtained from:
  - Institute of Electrical and Electronic Engineers (www.ieee.org)
  - Office of Communications (www.ofcom.org.uk)
  - EU pages on EMF and Public Health (ec.europa.eu/health/index_en.htm).

14. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT163-1 (SO20)

15. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
UBA2028_1	20091009	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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Date of release: 9 October 2009

Document identifier: UBA2028_1