Power Supply IC Series for TFT-LCD Panels

12V Input Multi-channel System Power Supply IC

BD8160AEFV

No.09035EBT01

●Description

The BD8160AEFV is a system power supply for the TFT-LCD panels used for liquid crystal TVs.
Incorporates two high-power FETs with low on resistance for large currents that employ high-power packages, thus driving large current loads while suppressing the generation of heat. A charge pump controller is incorporated as well, thus greatly reducing the number of application components.

●Features

1) Step-up and step-down DC/DC converter
2) Incorporates 2.6 A N-channel FET.
3) Incorporates positive/negative charge pumps.
4) Input voltage limit: 8 V to 18 V
5) Feedback voltage: 1.162 V ± 1%
6) Switching frequency: 500 kHz / 750kHz
7) Protection circuit: Under voltage lockout protection circuit
   Thermal shutdown circuit
   Overcurrent protection circuit
   Short Circuit Protection
   Overvoltage protection circuit for VS voltage (Boost DC/DC output)
8) HTSSOP-B28 Package

●Applications

Power supply for the TFT-LCD panels used for LCD TVs

●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage	SUP,VIN	20	V
Power Dissipation	Pd	4700*	mW
Operating Temperature Range	Topr	-40～+85	℃
Storage Temperature Range	Tstg	-55～+150	℃
Junction Temperature	Tjmax	150	℃
SW Voltage	V_{SW}	21	V
SWB Voltage	V_{SWB}	19	V
EN1,EN2 Voltage	V_{EN1},V_{EN2}	19	V

* Derating in done 37.6mW/℃ for operating above Ta≧25℃(On 4-layer 70.0mm×70.0mm×1.6mm board)

●Recommendable Operation Range (Ta=25℃)

Parameter	Symbol	Limits			Unit
		Min	Typ	Max	
Supply Voltage	SUP,VIN	8	12	18	V
Vs Voltage	Vs	VIN+2	15	18	V
Switch current for SW	I_{SW}	—	—	2.6**	A
Switch current for SWB	I_{SWB}	—	—	2.0**	A
EN1,EN2,FREQ Voltage	V_{EN1},V_{EN2},V_{FREQ}	—	—	18	V

** Pd, ASO should not be exceeded

●**Electrical characteristics (unless otherwise specified VIN=12V and Ta=25°C)**

1. DC/DC converter controller block

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Soft start – SS						
SS source current	I_{SO}	6	10	14	μA	V_{SS}=0.5V
Error amplifier block – FB and FBB						
FB and FBB input bias current	I_{FB12}	-	0.1	2	μA	
Feedback voltage for boost converter	V_{FB}	1.150	1.162	1.174	V	Voltage follower
Feedback voltage for buck converter	V_{FBB}	1.188	1.213	1.238	V	
SW block – SW						
On resistance N-channel	R_{ONN}	-	0.2	0.3	Ω	I_O=0.8A
Leak current N-channel	I_{LEAKN1}	-	0	10	μA	V_{SW} =18V
Switch current limit for SW	I_{SW}	2.6	-	-	A	
Maximum duty cycle	M_{DUTY}	75	90	97	%	FB= 0V
SW block – SWB						
On resistance N-channel	R_{ONH}	-	0.2	0.3	Ω	I_O=0.8A
Leak current N-channel	I_{LEAKN2}	-	0	10	μA	V_{INB}=18V , V_{SWB} =0V
Switch current limit for SWB	I_{SWB}	2.0	-	-	A	
Protections						
Over Voltage Protection for SW	V_{SWOVP}	18.5	19	19.5	V	

2. Charge pump driver block

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Error amplifier block – FBP and FBN						
FBP, FBN input bias current	I_{FBP}, I_{FBN}	-	0.1	1	μA	
Feedback voltage for VGH	V_{FBP}	1.188	1.213	1.238	V	
Feedback voltage for VGL	V_{FBN}	0.18	0.2	0.22	V	
Delay start block						
DLY1, DLY2 source current	I_{DLY1}, I_{DLY2}	2	5	9	μA	V_{DLY}=0.5V
DRP, DRN block						
On resistance N-channel	R_{ONN}	-	5	-	Ω	I_O=20mA
On resistance P-channel	R_{ONP}	-	3	-	Ω	I_O=20mA

●**Electrical characteristics (unless otherwise specified VIN=12V and Ta=25°C)**

3. General

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Supply current						
Average supply current	I_{CC}	-	5	8	mA	
Oscillator						
Oscillation frequency1	F_{OSC1}	600	750	900	kHz	FREQ = High
Oscillation frequency2	F_{OSC2}	400	500	600	kHz	FREQ = low
Protections						
Under voltage lockout threthold1	V_{UVLO1}	6.9	7.4	7.9	V	VIN rising
Under voltage lockout threthold2	V_{UVLO2}	6.5	7.0	7.5	V	VIN falling
Thermal Shutdown	T_{TSD}	-	175	-	℃	*1
Short Circuit Protection Time 1	T_{SCP1}	153	219	285	ms	FREQ = High
Short Circuit Protection Time 2	T_{SCP2}	230	328	426	ms	FREQ = Low
FB threshold1 for SCP	V_{FBSCP1}	0.985	1.065	1.145	V	FB rising
FB threshold2 for SCP	V_{FBSCP2}	-	0.969	-	V	FB falling
FBB threshold1 for SCP	$V_{FBBSCP1}$	-	1.055	-	V	FBB rising
FBB threshold2 for SCP	$V_{FBBSCP2}$	-	0.874	-	V	FBB falling
FBP threshold1 for SCP	$V_{FBPSCP1}$	-	0.967	-	V	FBP rising
FBP threshold2 for SCP	$V_{FBPSCP2}$	-	0.859	-	V	FBP falling
FBN threshold1 for SCP	$V_{FBNSCP1}$	-	0.406	-	V	FBN falling
FBN threshold2 for SCP	$V_{FBNSCP2}$	-	0.505	-	V	FBN rising
Reference Voltage						
Reference Voltage	V_{REF}	1.188	1.213	1.238	V	
Gate Drive						
Gate drive threshold	V_{GD}	0.985	1.065	1.145	V	
GD output low voltage	V_{OL}	-	0.7	1.4	V	I=1mA
GD output leakage current	I_{LK}	-	0	10	μA	
Logic signals EN1, EN2, FREQ						
High level input voltage	V_{IH}	2.0	-	-	V	
Low level input voltage	V_{IL}	-	-	0.8	V	

* This product is not designed for protection against radioactive rays.

●**Reference Data (Unless otherwise specified, Ta = 25°C)**

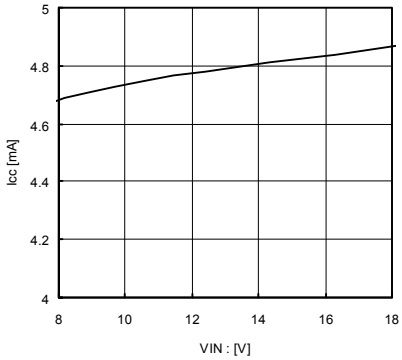


Fig.1 SUPPLY CURRENT

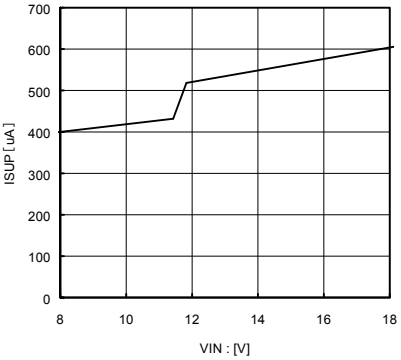


Fig.2 SUPPLY CURRENT

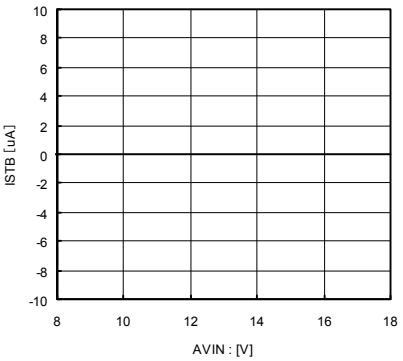


Fig.3 STANDBY CURRENT

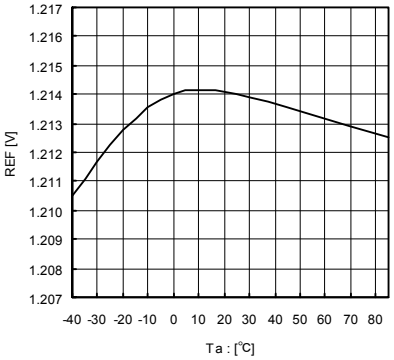


Fig.4 REF VOLTAGE

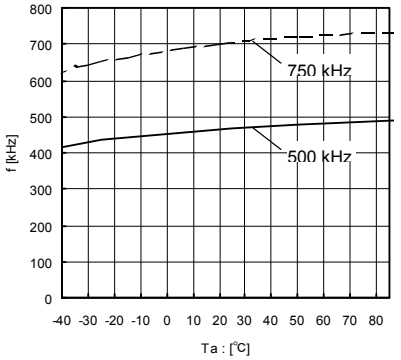


Fig.5 SWITCHING FREQUENCY

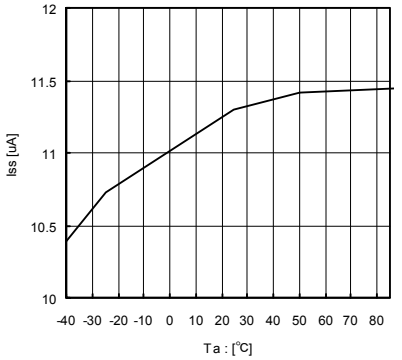


Fig.6 SS SOURCE CURRENT

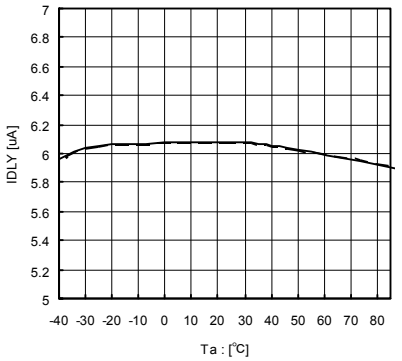


Fig.7 DLY1,2 SOURCE CURRENT

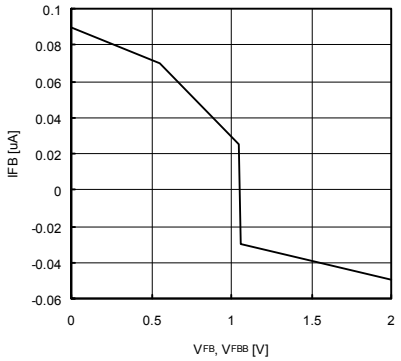


Fig.8 INPUT BIAS CURRENT

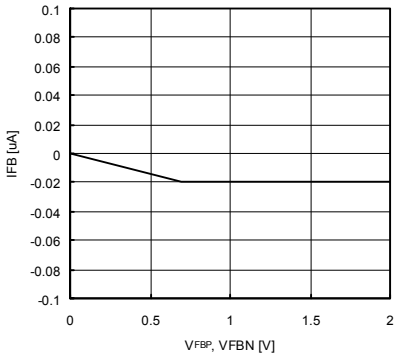


Fig.9 INPUT BIAS CURRENT

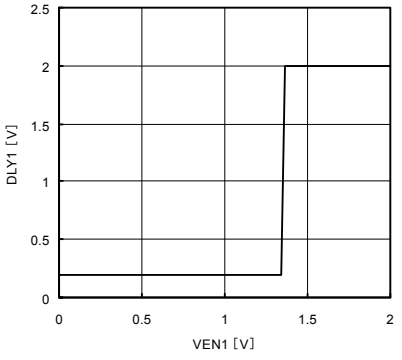


Fig.10 EN1 THRESHOLD VOLTAGE

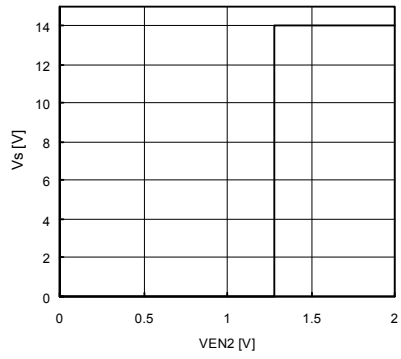


Fig.11 EN2 THRESHOLD VOLTAGE

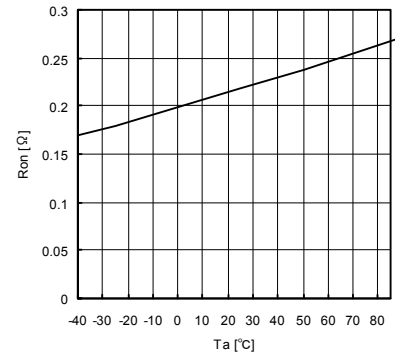


Fig.12 SW ON RESISTANCE

●**Reference Data (Unless otherwise specified, Ta = 25°C)**

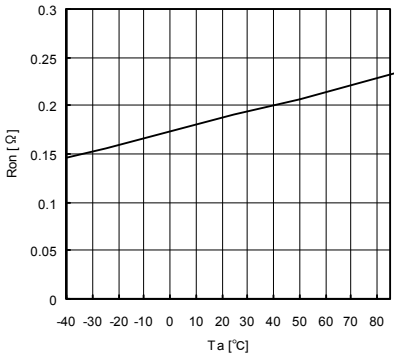


Fig.13 SWB ON RESISTANCE

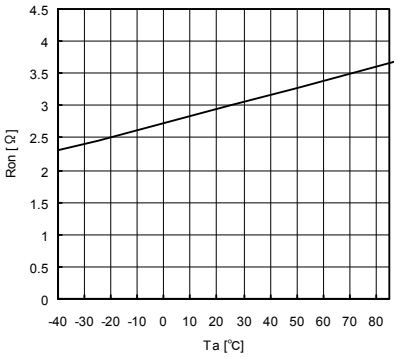


Fig.14 DRP ON RESISTANCE

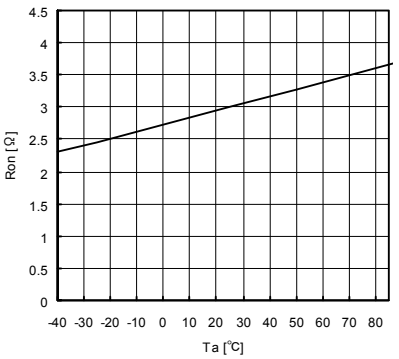


Fig.15 DRN ON RESISTANCE

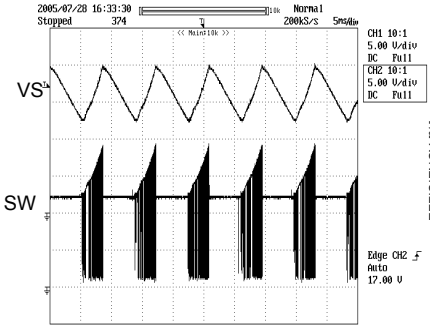


Fig.16 OVP WAVEFORM

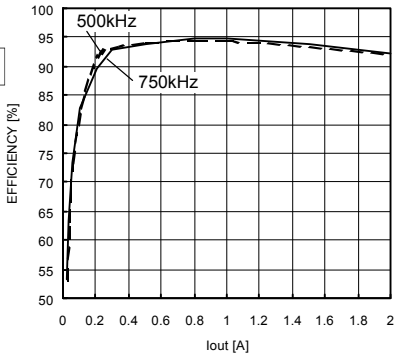


Fig.17 STEP UP EFFICIENCY

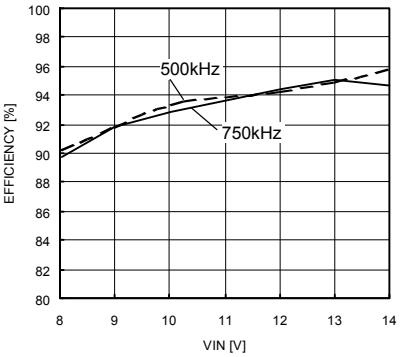


Fig.18 STEP UP EFFICIENCY

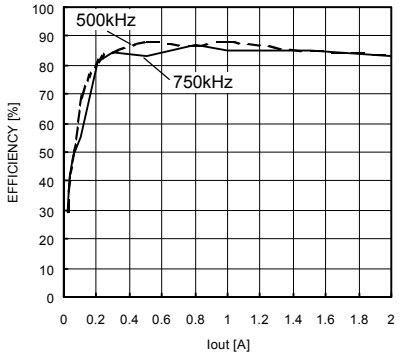


Fig.19 STEP DOWN EFFICIENCY

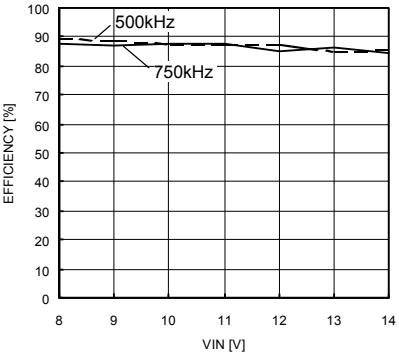


Fig.20 STEP DOWN EFFICIENCY

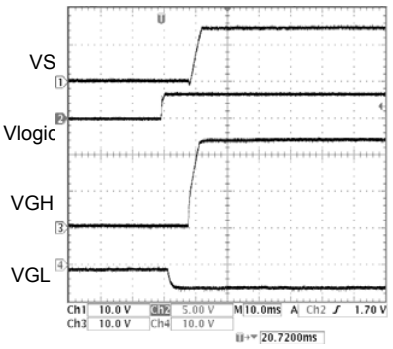


Fig.21 START UP WAVEFORM

●Block Diagram

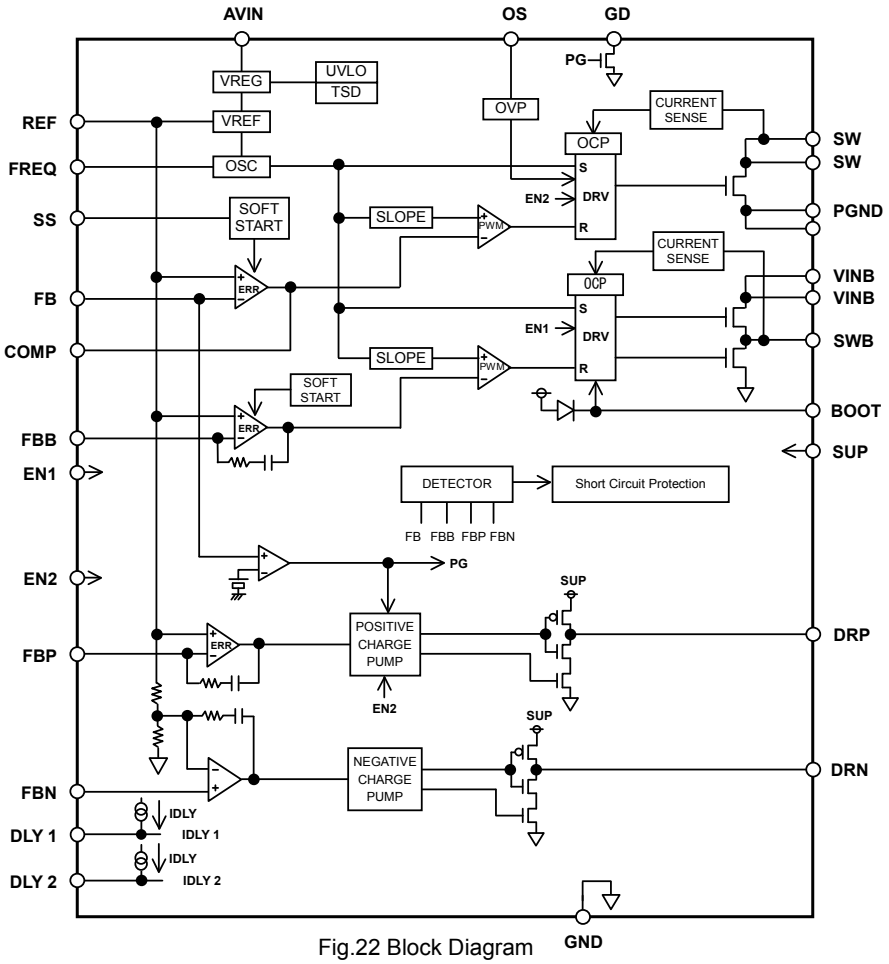


Fig.22 Block Diagram

●Typical Application

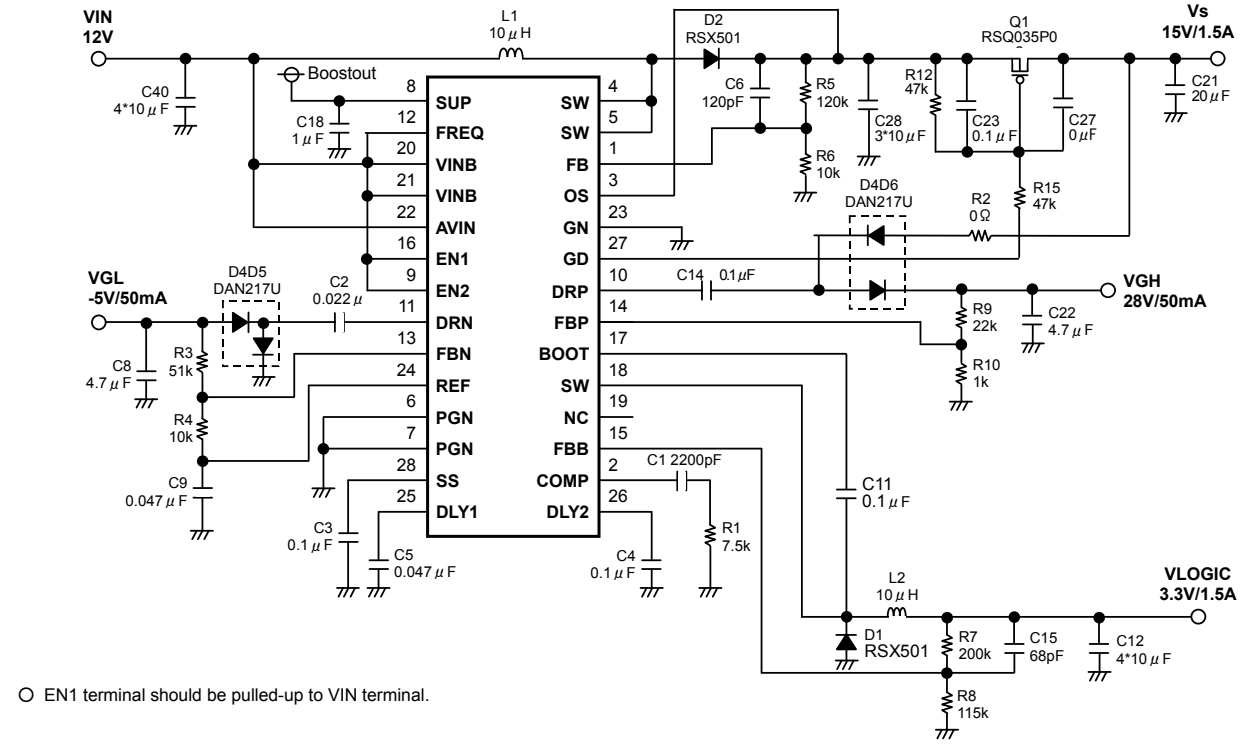


Fig.23 Typical Application

●**Pin Assignment Diagram**

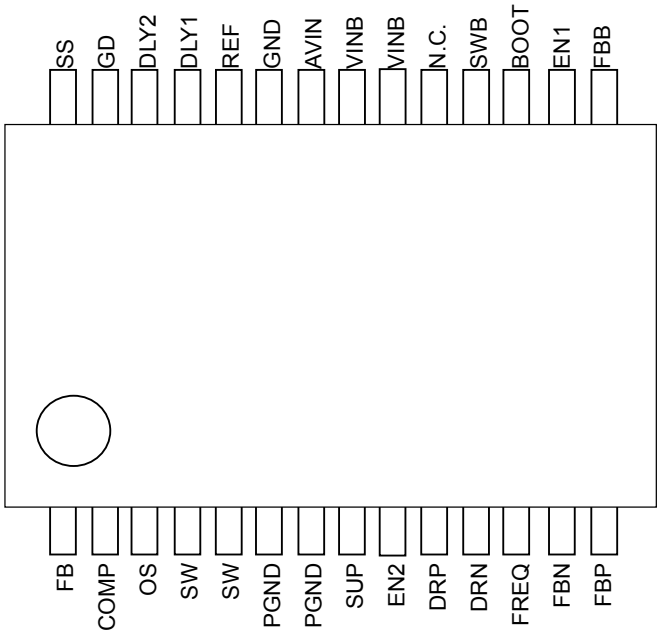


Fig. 24 Pin Assignment Diagram

●**Pin Assignment and Pin Function**

Pin No.	Pin name	Function	Pin No.	Pin name	Function
1	FB	Feedback input 1 for VS	15	FBB	Feedback input for Vlogic
2	COMP	Error amp output	16	EN1	Enable pin for Vlogic and VGL
3	OS	Output sense pin	17	BOOT	Capacitance connection pin for booting
4	SW	Switching pin for VS	18	SWB	Switching pin for Vlogic
5	SW	Switching pin for VS	19	N.C.	Non-connect pin
6	PGND	Ground pin	20	VINB	Power supply input pin
7	PGND	Ground pin	21	VINB	Power supply input pin
8	SUP	Power supply input pin	22	AVIN	Power supply input pin
9	EN2	Enable pin for VS and VGH	23	GND	Analog Ground pin
10	DRP	Switching pin for VGH	24	REF	Internal reference output pin
11	DRN	Switching pin for VGL	25	DLY1	Delay start capacitance connection pin for VGL
12	FREQ	Frequency	26	DLY2	Delay start capacitance connection pin for VS
13	FBN	Feedback input 1 for VGL	27	GD	Gate drive pin for load switch
14	FBP	Feedback input 1 for VGH	28	SS	Soft start capacitance connection pin for VS

●Block Operation

- VREG
  A block to generate constant-voltage for DC/DC boosting.

- VREF
  A block that generates internal reference voltage of 2.9 V (Typ.).

- TSD/UVLO
  TSD (Thermal shutdown)/UVLO (Under Voltage Lockout) protection block. The TSD circuit shuts down IC at 175°C (Typ.) The UVLO circuit shuts down the IC when the Vcc is 7 V (Typ.) or below.

- Error amp block (ERR)
  This is the circuit to compare the reference voltage and the feedback voltage of output voltage. The COMP pin voltage resulting from this comparison determines the switching duty. At the time of startup, since the soft start is operated by the SS pin voltage, the COMP pin voltage is limited to the SS pin voltage.

- Oscillator block (OSC)
  This block generates the oscillating frequency.

- SLOPE block
  This block generates the triangular waveform from the clock created by OSC. Generated triangular waveform is sent to the PWM comparator.

- PWM block
  The COMP pin voltage output by the error amp is compared to the SLOPE block's triangular waveform to determine the switching duty. Since the switching duty is limited by the maximum duty ratio which is determined internally, it does not become 100%.

- DRV block
  A DC/DC driver block. A signal from the PWM is input to drive the power FETs.

- CURRENT SENSE
  Current flowing to the power FET is detected by voltage at the CURRENT SENSE and the overcurrent protection operates at 2.0/2.6A (min.). When the overcurrent protection operates, switching is turned OFF and the SS pin capacitance is discharged.

- DELAY START
  A start delay circuit for positive/negative charge pump and Boost converter.

- Soft start circuit
  Since the output voltage rises gradually while restricting the current at the time of startup, it is possible to prevent the output voltage overshoot or the rush current.

•Positive charge pump
A controller circuit for the positive-side charge pump. The switching amplitude is controlled so that the feedback voltage FBP will be set to 1.213 V (Typ.).
The start delay time can be set in the DLY2 pin at the time of startup. When the DLY2 voltage reaches 0.65 V (Typ.), switching waves will be output from the DRP pins.

- Negative charge pump
  A controller circuit for the negative-side charge pump. The switching amplitude is controlled so that the feedback voltage FBN will be set to 0.2 V (Typ.).
  The start delay time can be set in the DLY1 pin at the time of startup. When the DLY2 voltage reaches 0.65 V (Typ.), switching waves will be output from the DRN pins.

- Over Voltage protection of the Boost Converter
  The boost converter has an overvoltage protection to protect the internal power MOS FET (SW) in case the feed back (FB) pin is floating or shorted to GND. Vs voltage is monitored with comparator over the OS pin. When the voltage of OS pin reached 19V (typ.), the Boost Converter stops its switching until the OS pin voltage falls below the comparator threshold.

●Start-up Sequence

The DC/DC converter of this IC incorporates a soft start function, and the charge pump incorporates a delay function, for which independent time settings are possible through external capacitors.

As the capacitance, 0.01 μF to 0.1 μF is recommended. If the capacitance is set lower than 0.01 μF, the overshooting may occur on the output voltage. If the capacitance is set larger than 0.1 μF, the excessive back current flow may occur in the internal parasitic elements when the power is turned OFF and it may damage IC. When the capacitor more than 0.1 μF is used, be sure to insert a diode to VIN in series, or a bypass diode between the SS and VIN pins.

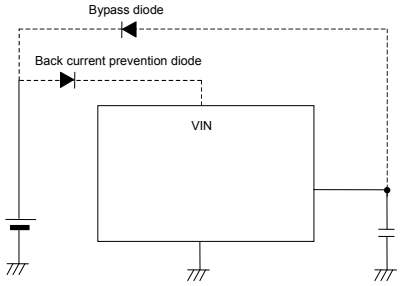


Fig.25 Example of Bypass Diode Use

When there is the activation relation (sequences) with other power supplies, be sure to use the high-precision product (such as X5R). Soft start time may vary according to the input voltage, output loads, coils, voltage, and output capacitance. Be sure to verify the operation using the actual product.

A delay of the charge pump starts from a point where V_{LOGIC} reaches 85% of its nominal value (Typ.).

Soft start time of DC/DC converter block: tss
Tss = (Css × 0.6V) / 10 μA [s]
Where, Css is an external capacitor.

Delay time of charge pump block: t DELAY
t DELAY = (Css ×0.65) / 5μA [s]
Where, Css is an external capacitor.

Startup example

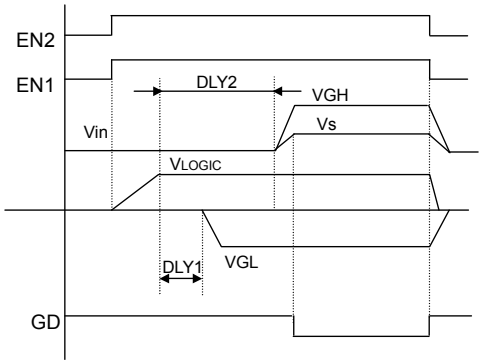


Fig. 26 Output Timing Sequence with EN2 always high (EN2=VIN)

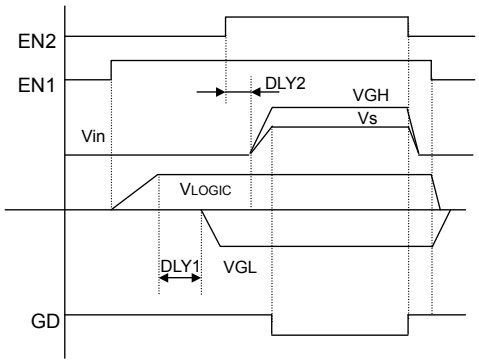


Fig. 27 Output Timing Sequence(with using EN1 and EN2)

●Short Circuit Protection

BD8160AEFV has a short circuit protection feature to prevent the large current flowing when the output is shorted to GND. This function is monitoring V_S, V_{LOGIC}, VGH and VGL voltage and starts the timer when at least one of the outputs is not operating properly (when the output voltage was lower than expected) After TBD ms (Typ) of this abnormal state, BD8160AEFV will shutdown the all outputs and latch the state.

The timer operation will be done even when BD8160AEFV starts up. Therefore, please adjust the capacitor for SS, DLY1 and DLY2 (Softstart and Delaystart) so that the all output voltage reach the expected value within the Short Circuit Protection Time (TBD ms Typ)

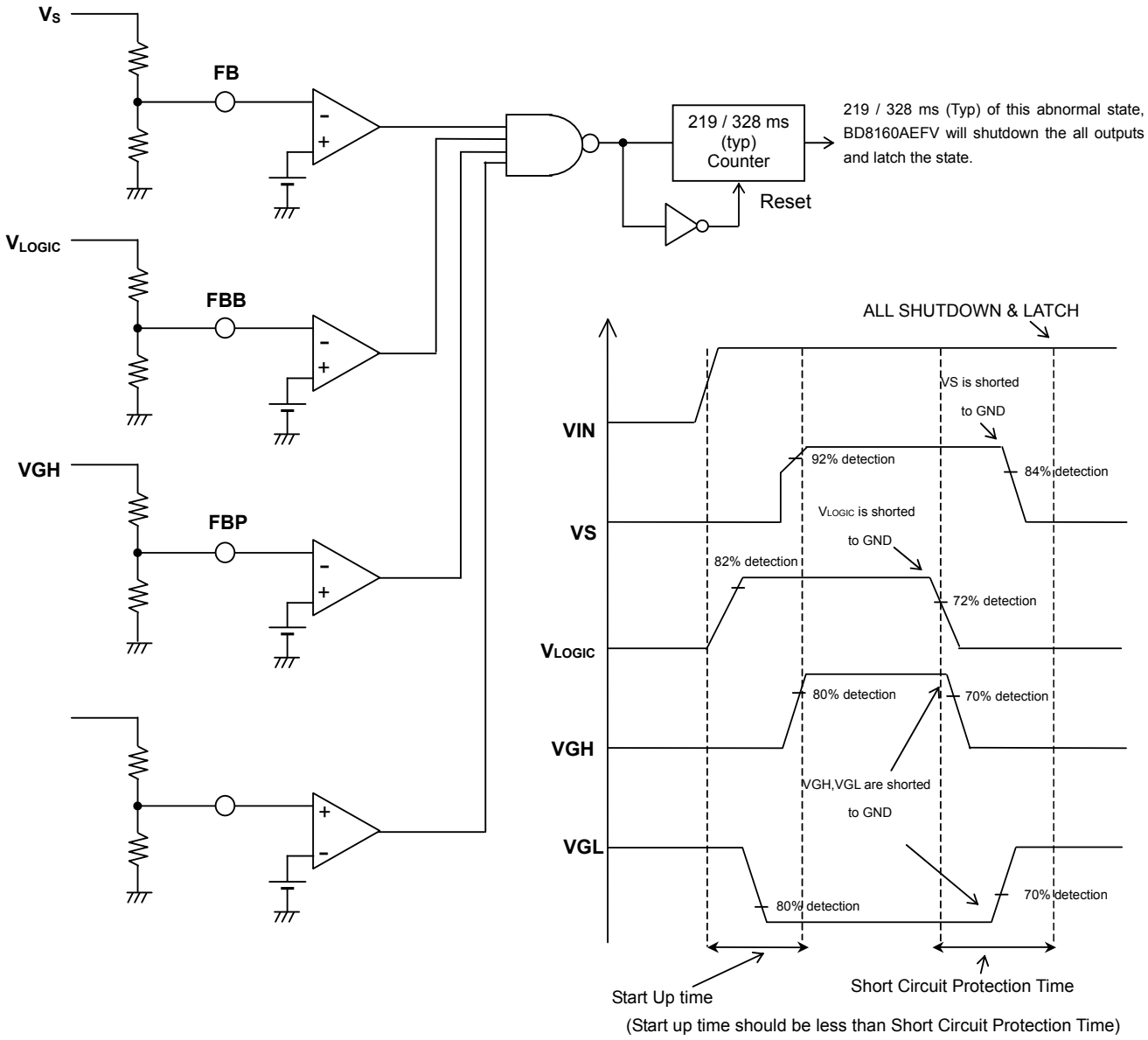


Fig. 28

●Selecting Application Components

(1) Output LC constant (Boost Converter)

The inductance L to use for output is decided by the rated current ILR and input current maximum value IOMAX of the inductance.

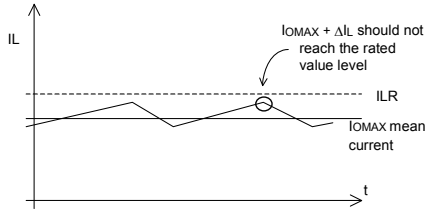


Fig. 29

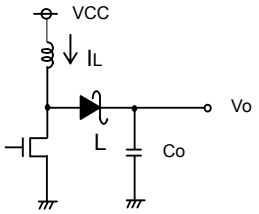


Fig. 30

Adjust so that IOMAX + ΔIL does not reach the rated current value ILR. At this time, ΔIL can be obtained by the following equation.

$$\Delta I_L = \frac{1}{L} \times Vcc \times \frac{Vo-Vcc}{Vo} \times \frac{1}{f} \quad [A]$$

Set with sufficient margin because the inductance L value may have the dispersion of ± 30%.

For the capacitor C to use for the output, select the capacitor which has the larger value in the ripple voltage VPP permissible value and the drop voltage permissible value at the time of sudden load change.

Output ripple voltage is decided by the following equation.

$$\Delta V_{PP} = I_{LMAX} \times R_{ESR} + \frac{1}{f_{Co}} \times \frac{Vcc}{Vo} \times \left(I_{LMAX} - \frac{\Delta I_L}{2} \right) \quad [V]$$

Perform setting so that the voltage is within the permissible ripple voltage range.

For the drop voltage VDR during sudden load change, please perform the rough calculation by the following equation.

$$V_{DR} = \frac{\Delta I}{Co} \times 10\ \mu s \quad [V]$$

However, 10 µs is the rough calculation value of the DC/DC response speed.

Make Co settings so that these two values will be within the limit values.

(2) Output LC constant (Buck Converter)

The inductance L to use for output is decided by the rated current ILR and input current maximum value IOMAX of the inductance.

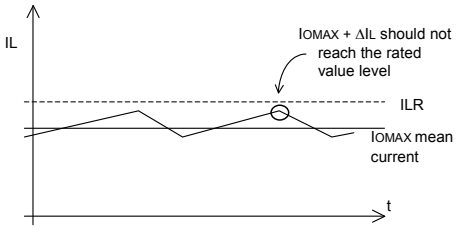


Fig. 31

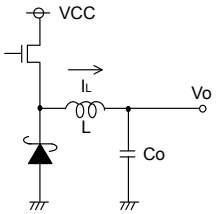


Fig. 32

Adjust so that IOMAX + ΔIL does not reach the rated current value ILR. At this time, ΔIL can be obtained by the following equation.

$$\Delta I_L = \frac{1}{L} \times (Vcc - Vo) \times \frac{Vo}{Vcc} \times \frac{1}{f} \quad [A]$$

Set with sufficient margin because the inductance L value may have the dispersion of ± 30%.

For the capacitor C to use for the output, select the capacitor which has the larger value in the ripple voltage VPP permissible value and the drop voltage permissible value at the time of sudden load change.

Output ripple voltage is decided by the following equation.

$$\Delta V_{PP} = \Delta I_L \times R_{ESR} + \frac{\Delta I_L}{2Co} \times \frac{Vo}{Vcc} \times \frac{1}{f} \quad [V]$$

Perform setting so that the voltage is within the permissible ripple voltage range.

For the drop voltage VDR during sudden load change, please perform the rough calculation by the following equation.

$$V_{DR} = \frac{\Delta I}{Co} \times 10\ \mu s \quad [V]$$

However, 10 µs is the rough calculation value of the DC/DC response speed.

Make Co settings so that these two values will be within the limit values.

(3) Phase compensation

Phase Setting Method

The following conditions are required in order to ensure the stability of the negative feedback circuit.

- Phase lag should be 150° or lower during gain 1 (0 dB) (phase margin of 30° or higher).

Because DC/DC converter applications are sampled using the switching frequency, the overall GBW should be set to 1/10 the switching frequency or lower. The target application characteristics can be summarized as follows:

- Phase lag should be 150° or lower during gain 1 (0 dB) (phase margin of 30° or higher).
- The GBW at that time (i.e., the frequency of a 0-dB gain) is 1/10 of the switching frequency or below.

In other words, because the response is determined by the GBW limitation, it is necessary to use higher switching frequencies to raise response.

One way to maintain stability through phase compensation involves canceling the secondary phase lag (-180°) caused by LC resonance with a secondary phase advance (by inserting 2 phase advances).
The GBW (i.e., the frequency with the gain set to 1) is determined by the phase compensation capacitance connected to the error amp. Increase the capacitance if a GBW reduction is required.

(a) Standard integrator (low-pass filter)

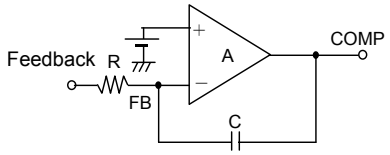


Fig. 33

(b) Open loop characteristics of integrator

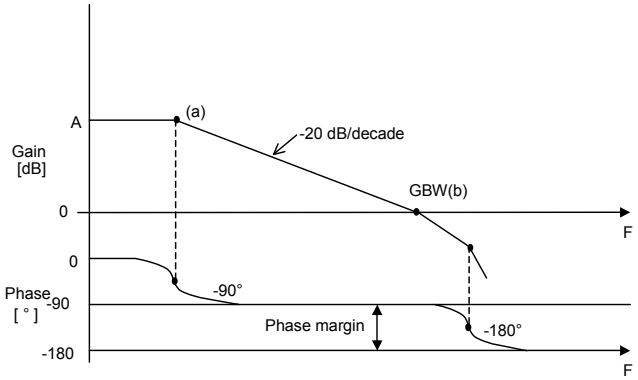
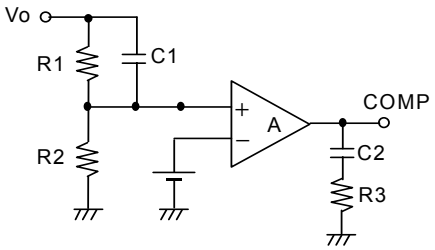


Fig. 34

Point (a) $fa = \frac{1}{2\pi RCA}$ [Hz]

Point (b) $fb = GBW = \frac{1}{2\pi RC}$ [Hz]

The error amp performs phase compensation of types (a) and (b), making it act as a low-pass filter.
For DC/DC converter applications, R refers to feedback resistors connected in parallel.
From the LC resonance of output, the number of phase advances to be inserted is two.



LC resonant frequency $fp = \frac{1}{2\pi\sqrt{LC}}$ [Hz]

Phase advance $fz1 = \frac{1}{2\pi C_1 R_1}$ [Hz]

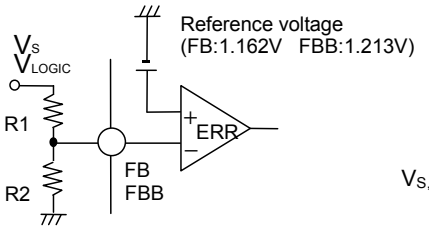
Phase advance $fz2 = \frac{1}{2\pi C_2 R_3}$ [Hz]

Fig. 35

Set a phase advancing frequency close to the LC resonant frequency for the purpose of canceling the LC resonance.

(4) Design of Feedback Resistance constant

Set the feedback resistance as shown below.



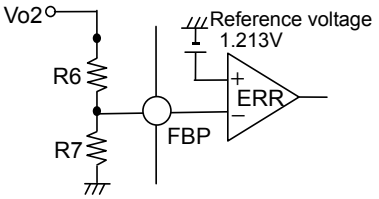
$$V_{S,}\,V_{LOGIC} = \frac{R1 + R2}{R2} \times \text{Reference Voltage} \quad [V]$$

Fig. 36

(5) Positive-side Charge Pump Settings

The IC incorporates a charge pump controller, thus making it possible to generate stable gate voltage.

The output voltage is determined by the following equation. As the setting range, 10kΩ to 330kΩ is recommended. If the resistor is set lower than 10kΩ, it causes reduction of power efficiency. If it is set more than 330kΩ, the offset voltage becomes larger by the input bias current of 0.1μA (Typ.) in the internal error amp.



$$Vo2 = \frac{R6 + R7}{R7} \times \text{Reference Voltage} \quad [V]$$

Fig. 37

By connecting capacitance to the DLY2 pin, the rising delay time can be set for the positive-side charge pump output. The delay time is determined by the following equation.

- Delay time of charge pump block t_{DELAY}

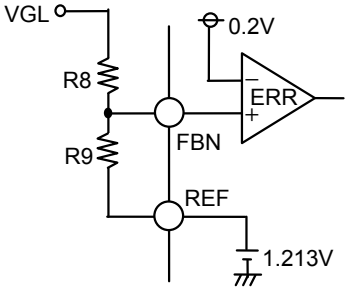
$t_{DELAY} = (C_{DLS} \times 0.65) / 5\ \mu A\ [s]$

Where, C_{DLS} is an external capacitor.

(6) Negative-side Charge Pump Settings

BD8160AEFV incorporates a charge pump controller for negative voltage, thus making it possible to generate stable gate voltage.

The output voltage is determined by the following equation. As the setting range, 10kΩ to 330kΩ is recommended. If the resistor is set lower than 10kΩ, it causes reduction of power efficiency. If it is set more than 330kΩ, the offset voltage becomes larger by the input bias current of 0.1μA (Typ.) in the internal error amp.



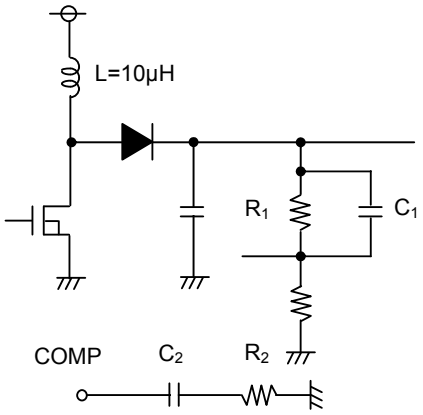
$$VGL = -\frac{R8}{R9} \times 1.013 + 0.2\ V \quad [V]$$

Fig.38

Like the positive-side charge pump, the rise delay time can be set by connecting capacitance to the DLY1 pin.

●Selecting the Feedforward Capacitor (Boost Converter)

Across the upper resistor R_1, a bypass capacitor is needed to have a stable converter loop.
C_1 will set a zero in the loop together with R_1.



$$C_1 = \frac{1}{2\times\pi\times fz_1\times R_1}$$

(Fz_1=11kHz @L=10μH)

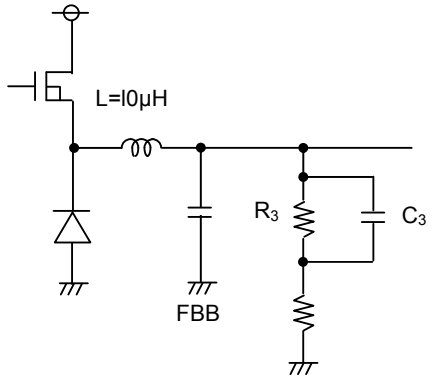
Fig.39

The regulator loop can be compensated by adjusting the exfernal components connected to the COMP pin.
C_2,R_2 are decided by the following formula.

$$Fz_1\text{=11kHZ} = \frac{1}{2\times\pi\times C_2\times R_2}$$

●Selecting the Feedforward Capacitor (Buck converter)

The feedforward capacitor across the upper feedback resistor divider sets a zero in the control loop.



$$C_3 = \frac{1}{2\times\pi\times fz_2\times R_3}$$

(Fz_2=12kHz @L=10μH)

Fig.40

●**I/O Equivalent Circuit Diagram**

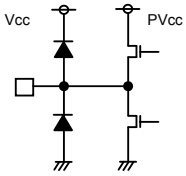
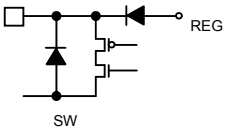
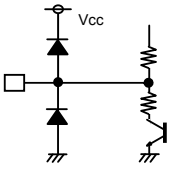
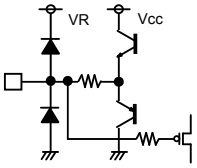
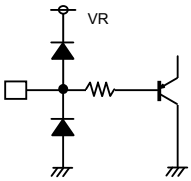
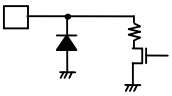
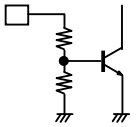
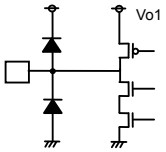
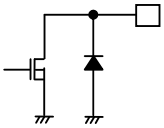
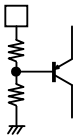
18.SWB	17.BOOT	25.DLY1 26.DLY2 28.SS
		
2.COMP 24.REF	1.FB 13.FBN 14.FBP 15.FBB	27.GD
		
9.EN2 12.FREQ 16.EN1	10.DRP 11.DRN	4.SW 5.SW
		
3.OS		
		

Fig.41

●Notes for use

1) Absolute maximum ratings
Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) GND potential
Ensure a minimum GND pin potential in all operating conditions.

3) Setting of heat
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4) Pin short and mistake fitting
Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pins caused by the presence of a foreign object may result in damage to the IC.

5) Actions in strong magnetic field
Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

6) Testing on application boards
When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.

7) Ground wiring patterns
When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring patterns of any external components.

8) Regarding input pin of the IC
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements. For example, when the resistors and transistors are connected to the pins as shown in Fig.42, a parasitic diode or a transistor operates by inverting the pin voltage and GND voltage. The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements such as by the application of voltages lower than the GND (P substrate) voltage to input and output pins.

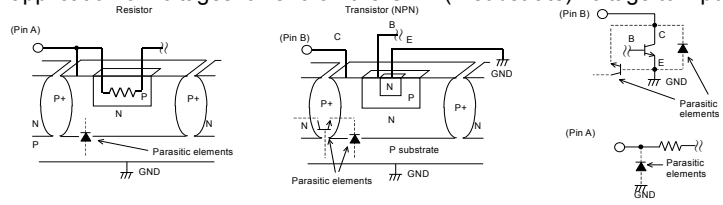


Fig. 42 Example of a Simple Monolithic IC Architecture

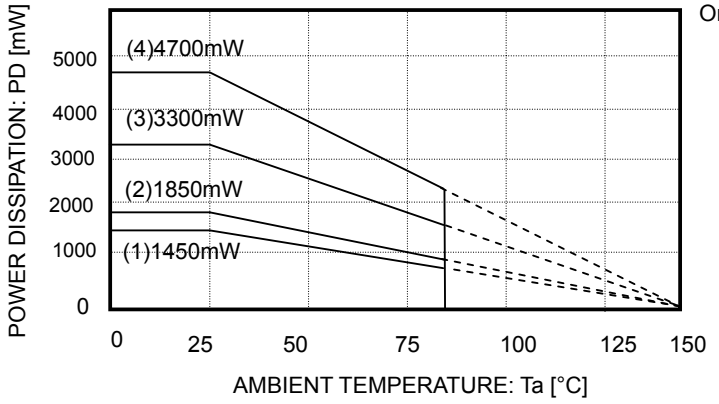
9) Overcurrent protection circuits
An overcurrent protection circuit designed according to the output current is incorporated for the prevention of IC damage that may result in the event of load shorting. This protection circuit is effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits. At the time of thermal designing, keep in mind that the current capacity has negative characteristics to temperatures.

10) Thermal shutdown circuit (TSD)
This IC incorporates a built-in TSD circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the attendant rise in the chip's junction temperature Tj will trigger the TSD circuit to turn off all output power elements. Operation of the TSD circuit presumes that the IC's absolute maximum ratings have been exceeded. Application designs should never make use of the TSD circuit.

11) Testing on application boards
At the time of inspection of the installation boards, when the capacitor is connected to the pin with low impedance, be sure to discharge electricity per process because it may load stresses to the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC.

12) EN1 terminal
EN1 terminal should be pulled up to VIN terminal.

●**Power Dissipation**



On 70 × 70 × 1.6 mm glass epoxy PCB
(1) 1-layer board (Backside copper foil area 0 mm × 0 mm)
(2) 2-layer board (Backside copper foil area 15 mm × 15 mm)
(3) 2-layer board (Backside copper foil area 70 mm × 70 mm)
(4) 4-layer board (Backside copper foil area 70 mm × 70 mm)

Fig. 43

●Ordering part number

B	D	8	1	6	0	A	E	F	V	-	E	2

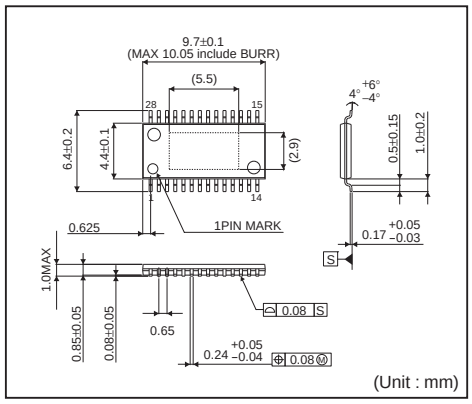
Part No. (BD)

Part No. (8160A)

Package
EFV : HTSSOP-B28

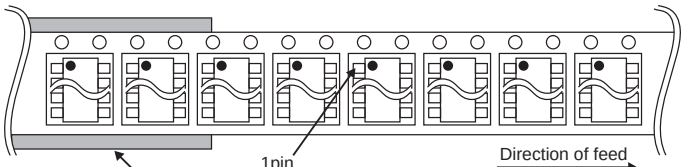
Packaging and forming specification
E2: Embossed tape and reel

HTSSOP-B28



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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