NCP348

Positive Overvoltage Protection Controller with Internal Low R_{ON} NMOS FET and Status FLAG

The NCP348 is able to disconnect the systems from its output pin in case wrong input operating conditions are detected. The system is positive overvoltage protected up to +28 V.

Due to this device using internal NMOS, no external device is necessary, reducing the system cost and the PCB area of the application board.

The NCP348 is able to instantaneously disconnect the output from the input, due to integrated Low R_{ON} Power NMOS (65 mΩ), if the input voltage exceeds the overvoltage threshold (6.4 V) or undervoltage threshold, of 3.25 V (UVLO).

At powerup ($\overline{EN}$ pin = low level), the V_{out} turns on 50 ms after the V_{in} exceeds the undervoltage threshold.

The NCP348 provides a negative going flag ($\overline{FLAG}$) output, which alerts the system that a fault has occurred.

In addition, the device has ESD−protected input (15 kV Air) when bypassed with a 1.0 µF or larger capacitor.

Features

- Overvoltage Protection up to 28 V
- On−Chip Low $R_{DS(on)}$ NMOS Transistor: 65 mΩ
- Internal Charge Pump
- Overvoltage Lockout (OVLO)
- Undervoltage Lockout (UVLO)
- Internal 50 ms Startup Delay
- Alert $\overline{FLAG}$ Output
- Shutdown $\overline{EN}$ Input
- Compliance to IEC61000−4−2 (Level 4)
  8.0 kV (Contact)
  15 kV (Air)
- ESD Ratings: Machine Model = B
  Human Body Model = 3
- 10 Lead WDFN 2.5x2 mm Package
- This is a Pb−Free Device

Applications

- Cell Phones
- Camera Phones
- Digital Still Cameras
- Personal Digital Applications
- MP3 Players

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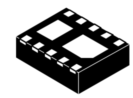
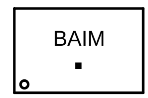
http://onsemi.com



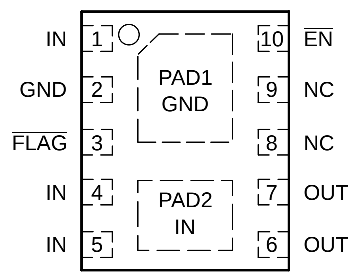
WDFN10
MT SUFFIX
CASE 516AA

MARKING DIAGRAM



BAI = Specific Device Code
M = Date Code
▪ = Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping
NCP348MTTBG	WDFN−10 (Pb−Free)	3000 / Tape & Reel
NCP348MTTXG	WDFN−10 (Pb−Free)	10000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

November, 2006 − Rev. 2

Publication Order Number:
NCP348/D

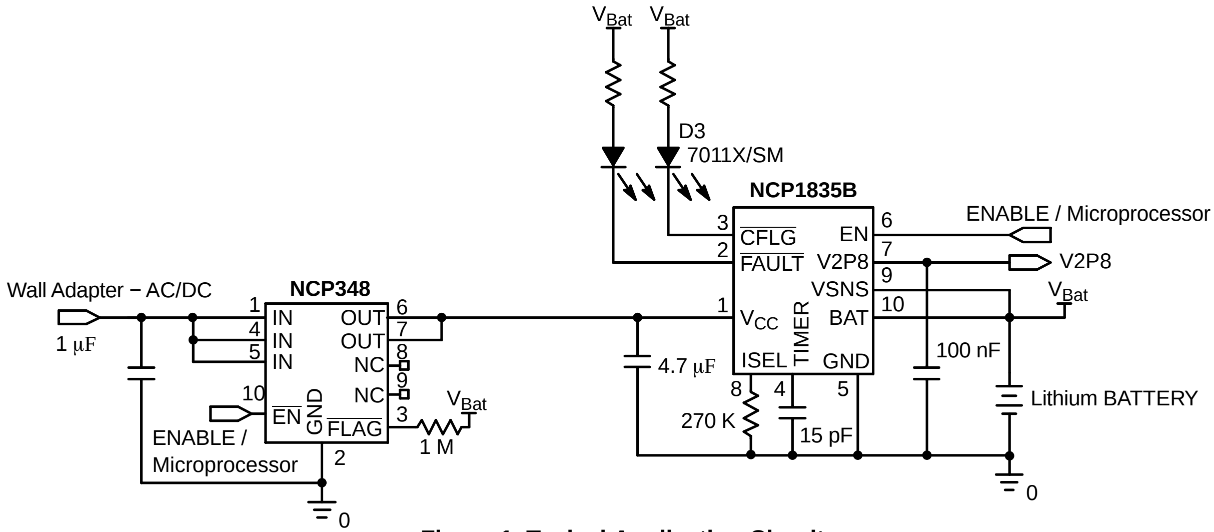


Figure 1. Typical Application Circuit

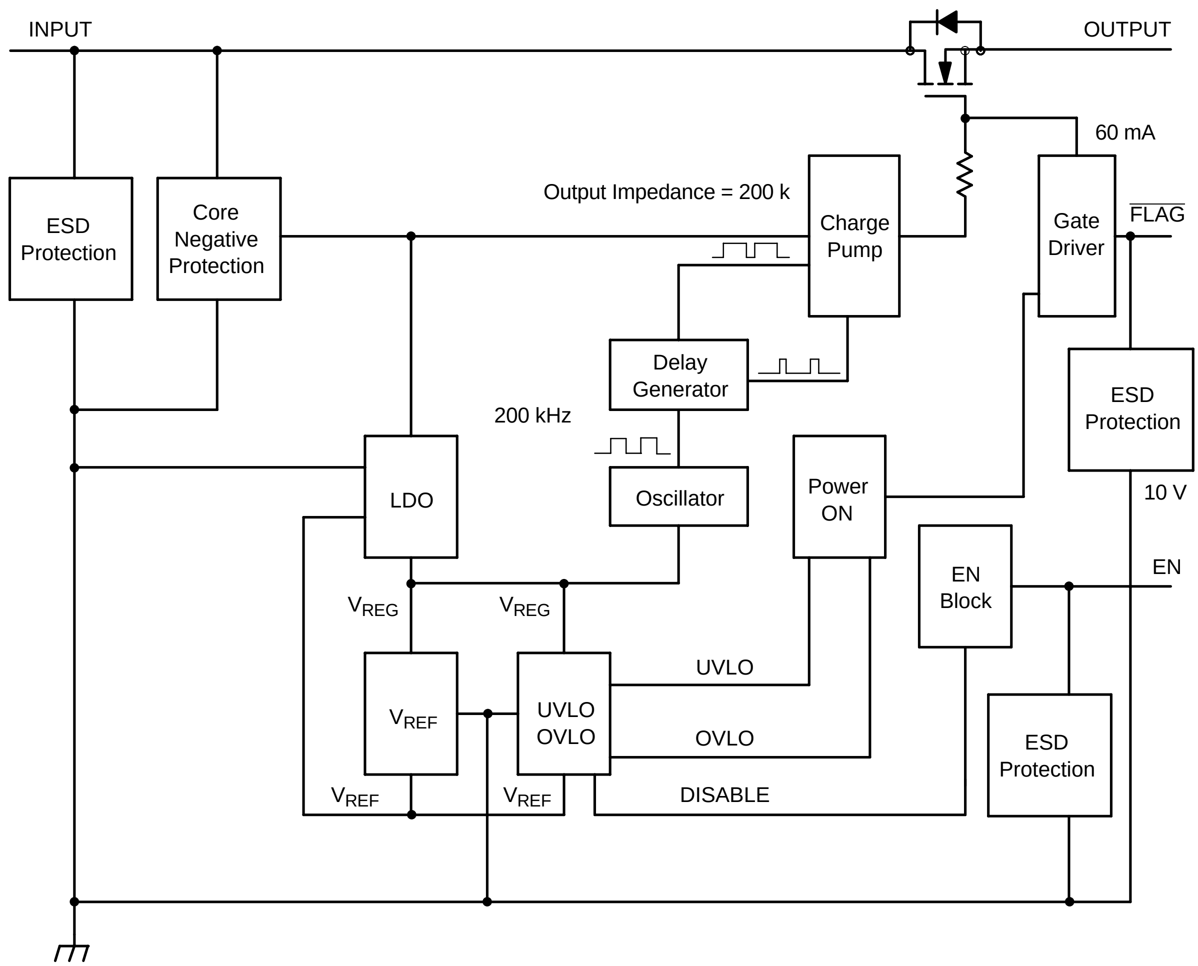


Figure 2. Functional Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Function	Description
1 4 5	IN	POWER	Input Voltage Pin. This pin is connected to the power supply. The device system core is supplied by this input. A 1 μF low ESR ceramic capacitor, or larger, must be connected between this pin and GND. The three IN pins must be hardwired to common supply.
2	GND	POWER	Ground
3	$\overline{FLAG}$	OUTPUT	Fault Indication Pin. This pin allows an external system to detect a fault on IN pin. The $\overline{FLAG}$ pin goes low when input voltage exceeds OVLO threshold or drop below UVLO threshold. Since the $\overline{FLAG}$ pin is open drain functionality, an external pull up resistor to V_{CC} must be added.
6 7	OUT	OUTPUT	Output Voltage Pin. This pin follows IN pin when “no fault” is detected. The output is disconnected from the V_{in} power supply when the input voltage is under the UVLO threshold or above OVLO threshold. The two OUT pins must be hardwired to common supply.
8	NC	OPEN	No Connect
9	NC	OPEN	No Connect
10	$\overline{EN}$	INPUT	Enable Pin. The device enters in shutdown mode when this pin is tied to a high level. In this case the output is disconnected from the input. To allow normal functionality, the $\overline{EN}$ pin shall be connected to GND to a pull down or to a I/O pin. This pin does not have an impact on the fault detection.
PAD1			PAD1, under the device. See PCB recommendations page 10. Can be shorted to GND.
PAD2			The PAD2 is electrically connected to the internal NMOS drain and connected to Pins 4 and 5. See PCB recommendations page 10.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Minimum Voltage (IN to GND)	$Vmin_{in}$	−0.3	V
Minimum Voltage (All others to GND)	Vmin	−0.3	V
Maximum Voltage (IN to GND)	$Vmax_{in}$	30	V
Maximum Voltage (All others to GND)	Vmax	7.0	V
Maximum Current (UVLO<V_{IN}<OVLO)	Imax	2.0	A
Thermal Resistance, Junction−to−Air (Note 1)	$R_{\theta JA}$	280	°C/W
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Operating Temperature	T_J	150	°C
ESD Withstand Voltage (IEC 61000−4−2) (input only) when bypassed with 1.0 μF capacitor Human Body Model (HBM), Model = 2 (Note 2) Machine Model (MM) Model = B (Note 3)	Vesd	15 Air, 8.0 Contact 2000 200	kV V V
Moisture Sensitivity	MSL	Level 1	−

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The $R_{\theta JA}$ is highly dependent on the PCB heat sink area (connected to pad 2). As example $R_{\theta JA}$ is 268 °C/W with 30 mm^2 (copper 35 μm) and 189 °C/W with 400 mm^2.
2. Human Body Model, 100 pF discharged through a 1.5 kΩ resistor following specification JESD22/A114.
3. Machine Model, 200 pF discharged through all pins following specification JESD22/A115.

ELECTRICAL CHARACTERISTICS (Min/Max limits values (−40°C < T_A < +85°C) and V_{in} = +5.0 V. Typical values are T_A = +25°C, unless otherwise noted.)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{in}	−	1.2	−	28	V
Undervoltage Lockout Threshold (Note 4)	UVLO	−	3.00	3.25	3.5	V
Undervoltage Lockout Hysteresis	$UVLO_{hyst}$	−	20	50	100	mV
Overvoltage Lockout Threshold (Note 4)	OVLO	V_{in} rises up OVLO threshold	6.00	6.4	6.8	V
Overvoltage Lockout Hysteresis	$OVLO_{hyst}$	−	50	100	150	mV
V_{in} versus V_{out} Resistance	$R_{DS(on)}$	V_{in} = 5.0 V, $\overline{EN}$ = GND, Load connected to V_{out}	−	65	120	mΩ
Disable Quiescent Current	Idd_{dis}	V_{in} = 5.0 V, $\overline{EN}$ = 1.2 V, Load connected to V_{out}	−	6.0	20	μA
Supply Quiescent Current	Idd	No load. $\overline{EN}$ = 5.0 V	−	90	150	μA
		No load. $\overline{EN}$ = Gnd	−	170	250	μA
UVLO Supply Current	Idd_{uvlo}	V_{IN} = 2.9 V	−	70	100	μA
$\overline{FLAG}$ Output Low Voltage	Vol_{flag}	1.2 V < V_{IN} < UVLO Sink 50 μA on/$\overline{FLAG}$ pin	−	20	400	mV
		V_{IN} > OVLO Sink 1.0 mA on $\overline{FLAG}$ pin	−	−	400	mV
$\overline{FLAG}$ Leakage Current	$\overline{FLAG}_{leak}$	$\overline{FLAG}$ level = 5.0 V	−	1.0	−	nA
$\overline{EN}$ Voltage High	Vih	−	1.2	−	−	V
$\overline{EN}$ Voltage Low	Vol	−	−	−	0.4	V
$\overline{EN}$ Leakage Current	$\overline{EN}_{leak}$	$\overline{EN}$ = 5.0 V or GND	−	1.0	−	nA
TIMINGS						
Startup Delay	ton	From V_{in} > UVLO to V_{out} = 0.3 V (See Figures 3 & 7)	30	55	70	ms
$\overline{FLAG}$ Going Up Delay	tstart	From V_{out} = 0.3 V to FLAG = 1.2 V (See Figures 3 & 9)	30	50	70	ms
Output Turn Off Time	toff	From V_{in} > OVLO to V_{out} < = 0.3 V (See Figures 4 & 8) V_{in} increasing from 5.0 V to 8.0 V at 3.0 V/μs Rload connected on V_{out}	−	1.5	5.0	μs
Alert Delay	tstop	From V_{in} > OVLO to $\overline{FLAG}$ < = 0.4 V (See Figures 4 & 10) V_{in} increasing from 5.0 V to 8.0 V at 3.0 V/μs Rload connected on V_{out}	−	1.0	−	μs
Disable Time	tdis	From $\overline{EN}$ > = 1.2 V to V_{out} < 0.3 V Rload = 5.0 Ω (See Figures 5 & 12)	−	1.0	5.0	μs

NOTE: Electrical parameters are guaranteed by correlation across the full range of temperature.

4. Additional UVLO and OVLO thresholds ranging from UVLO and from OVLO can be manufactured. Contact your ON Semiconductor representative for availability.

TIMING DIAGRAMS

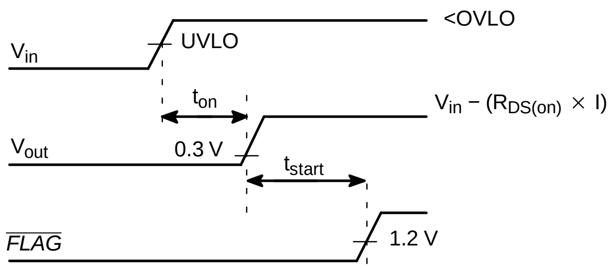


Figure 3. Startup

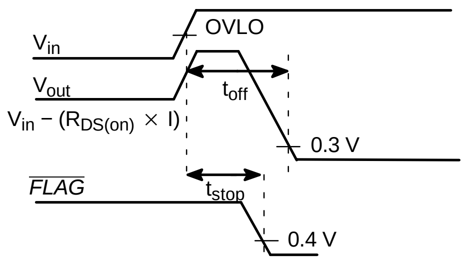


Figure 4. Shutdown on Overvoltage Detection

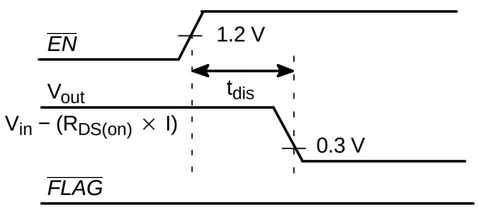


Figure 5. Disable on $\overline{EN}$ = 1

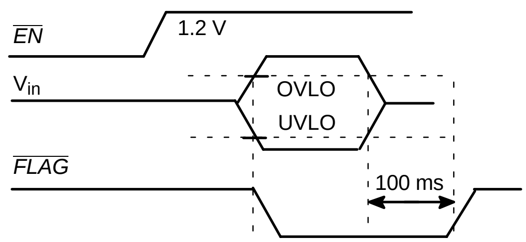


Figure 6. $\overline{FLAG}$ Response with $\overline{EN}$ = 1

TYPICAL OPERATING CHARACTERISTICS

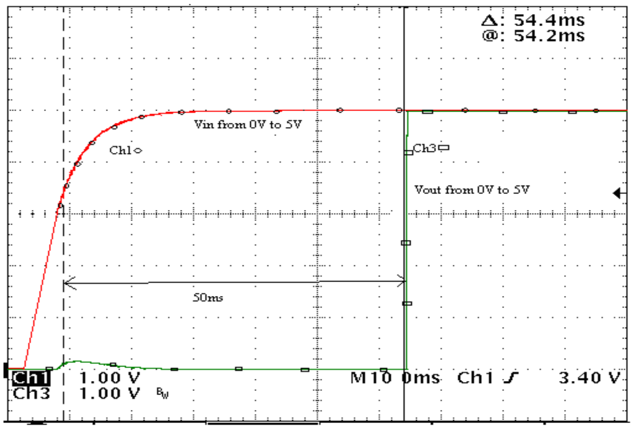


Figure 7. Startup
V_{in} = Ch1, V_{out} = Ch3

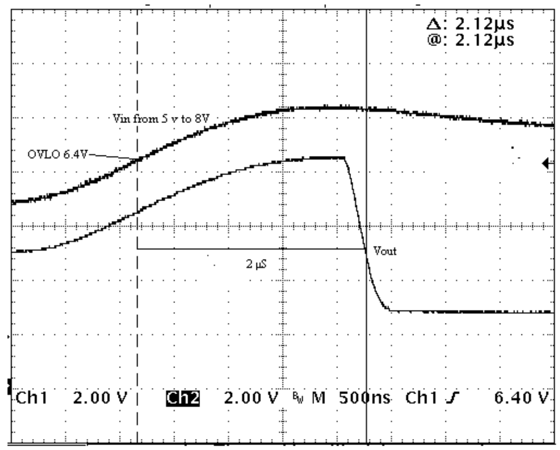


Figure 8. Output Turn Off Time
V_{in} = Ch1, V_{out} = Ch2

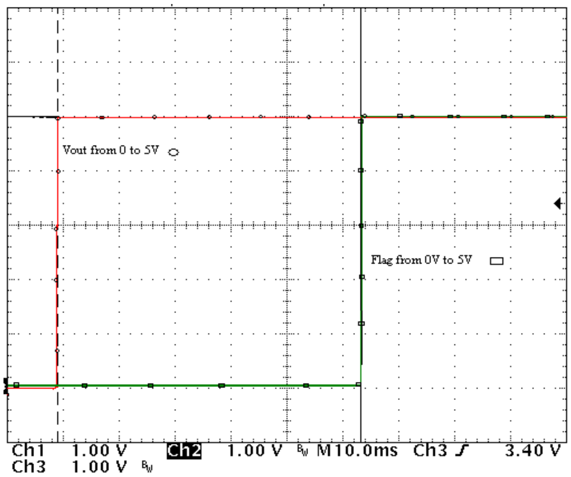


Figure 9. FLAG Going Up Delay
V_{out} = Ch3, FLAG = Ch2

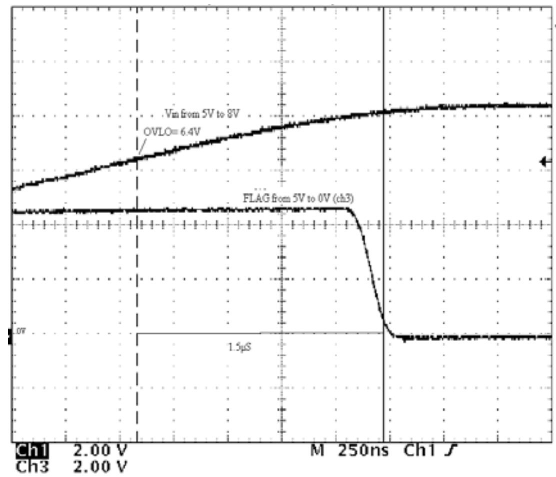


Figure 10. Alert Delay
V_{out} = Ch1, FLAG = Ch3

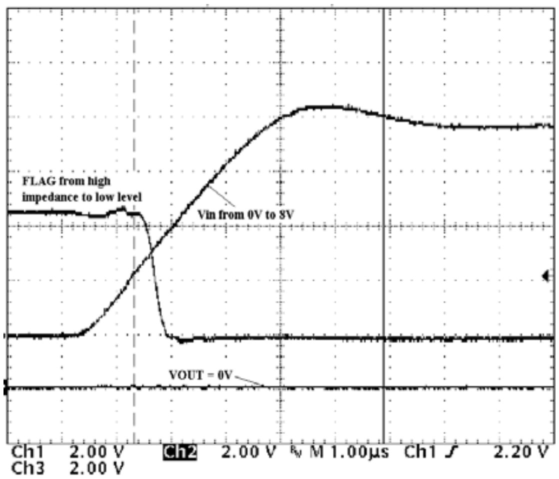


Figure 11. Initial Overvoltage Delay
V_{in} = Ch1, V_{out} = Ch2, FLAG = Ch3

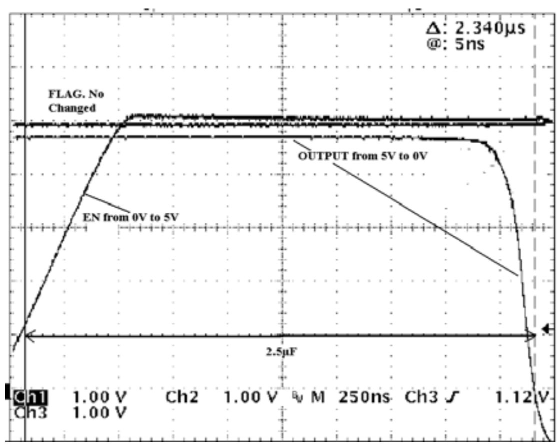


Figure 12. Disable Time
EN = Ch1, V_{out} = Ch2, FLAG = Ch3

TYPICAL OPERATING CHARACTERISTICS

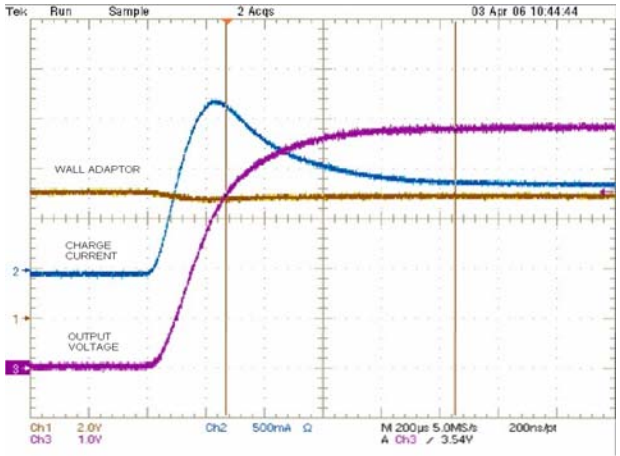


Figure 13. Inrush Current with C_{out} = 100 μF, I charge = 1 A, Output Wall Adaptor Inductance 1 μH

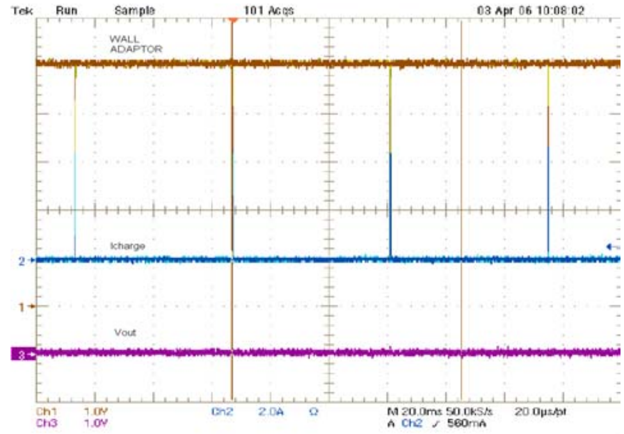


Figure 14. Output Short Circuit

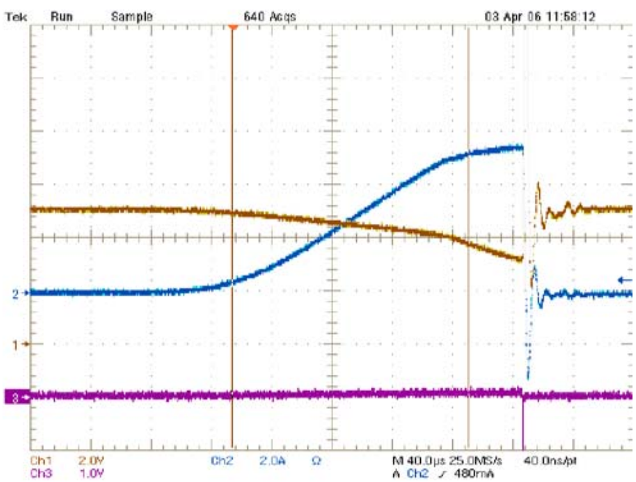


Figure 15. Output Short Circuit (Zoom Fig. 14)

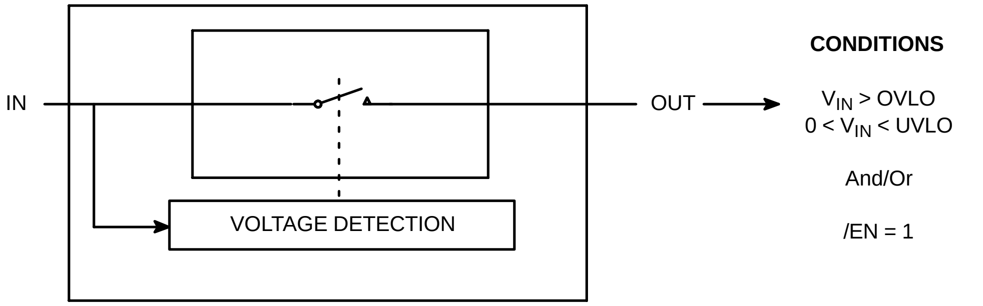


Figure 16. Simplified Diagram

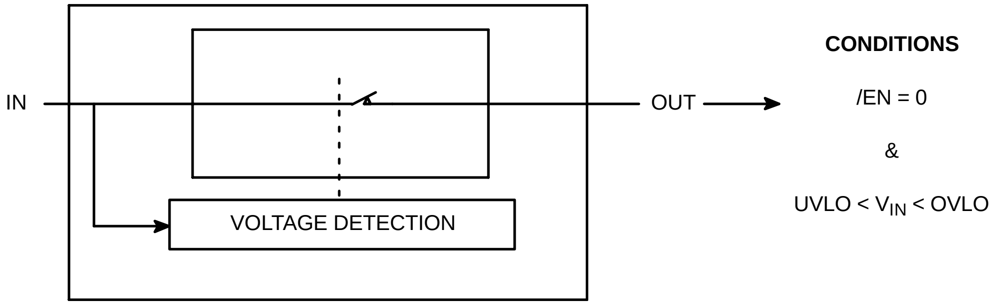


Figure 17. Simplified Diagram

Operation

The NCP348 provides overvoltage protection for positive voltage, up to 28 V. A Low $R_{DS(on)}$ NMOS FET protects the systems (i.e.: charger) connected on the Vout pin, against positive overvoltage. At powerup, with $\overline{EN}$ pin = low, the output is rising up 50 ms after the input overtaking undervoltage UVLO (Figure 3). The NCP348 provides a $\overline{FLAG}$ output, which alerts the system that a fault has occurred. A 50 ms additional delay, regarding available output (Figure 3) is added between output signal rising up and to $\overline{FLAG}$ signal rising up. $\overline{FLAG}$ pin is an open drain output.

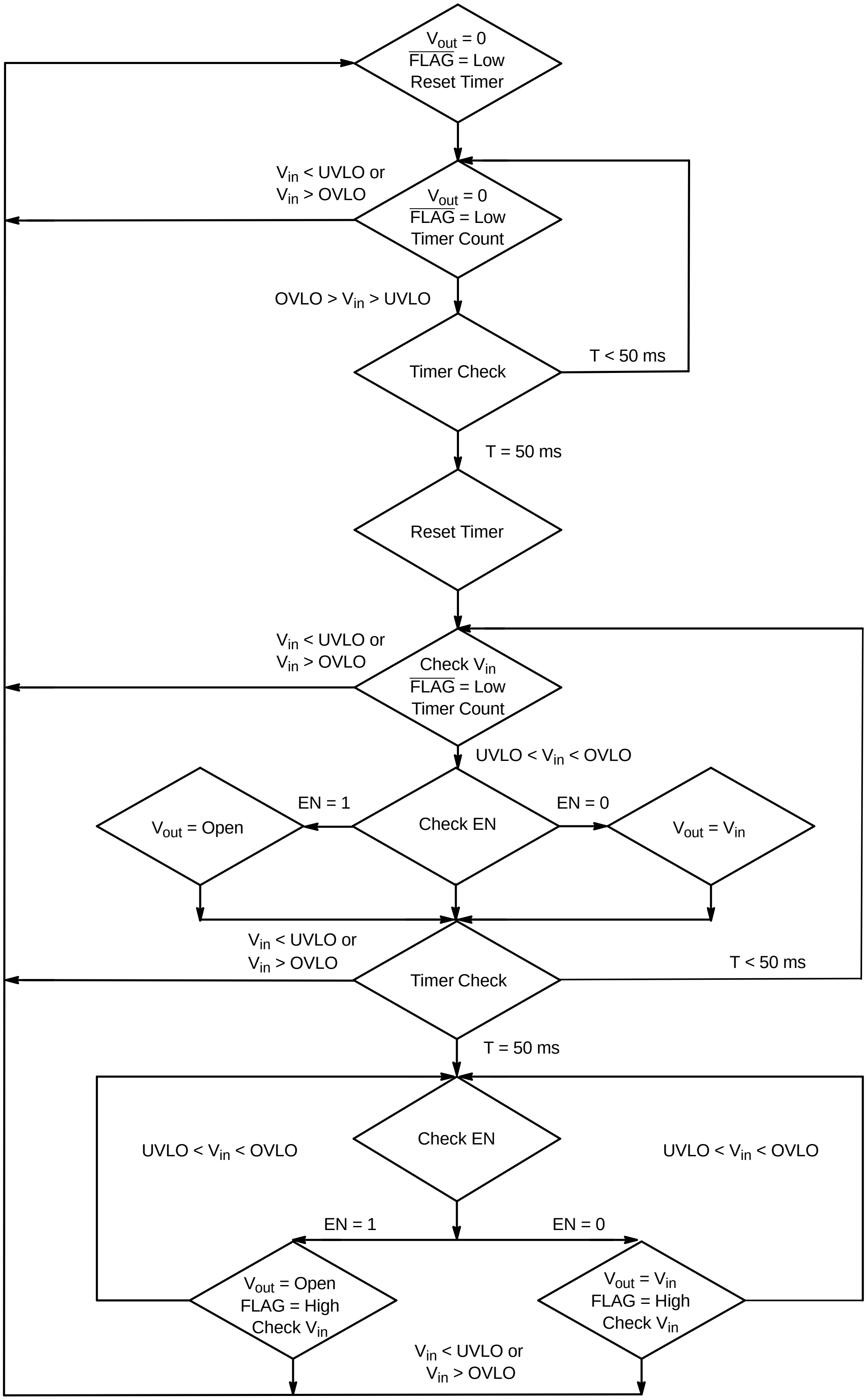


Figure 18. State Machine

Undervoltage Lockout (UVLO)

To ensure proper operation under any conditions, the device has a built−in undervoltage lockout (UVLO) circuit. During V_{in} positive going slope, the output remains disconnected from input until V_{in} voltage is below 3.25 V, plus hysteresis, nominal. The $\overline{FLAG}$ output is tied to low as long as V_{in} does not reach UVLO threshold. This circuit has a 50 mV hysteresis to provide noise immunity to transient condition. Additional UVLO thresholds ranging from UVLO can be manufactured. Contact your ON Semiconductor representative for availability.

Overvoltage Lockout (OVLO)

To protect connected systems on V_{out} pin from overvoltage, the device has a built−in overvoltage lockout (OVLO) circuit. During overvoltage condition, the output remains disabled as long as the input voltage exceeds 6.4 V typical. Additional OVLO thresholds ranging from OVLO can be manufactured. Contact your ON Semiconductor representative for availability.

$\overline{FLAG}$ output is tied to low until V_{in} is higher than OVLO. This circuit has a 100 mV hysteresis to provide noise immunity to transient conditions.

$\overline{FLAG}$ Output

The NCP348 provides a $\overline{FLAG}$ output, which alerts external systems that a fault has occurred.

This pin is tied to low as soon the OVLO threshold is exceeded or when the V_{in} level is below the UVLO threshold. When V_{in} level recovers normal condition, $\overline{FLAG}$ is held high, keeping in mind that an additional 50 ms delay has been added between available output and $\overline{FLAG}$ = high. The pin is an open drain output, thus a pull up resistor (typically 1 MΩ, minimum 10 kΩ) must be added to V_{bat}. Minimum V_{bat} supply must be 2.5 V. The $\overline{FLAG}$ level will always reflects V_{in} status, even if the device is turned off ($\overline{EN}$ = 1).

$\overline{EN}$ Input

To enable normal operation, the $\overline{EN}$ pin shall be forced to low or connected to ground. A high level on the pin, disconnects OUT pin from IN pin. $\overline{EN}$ does not overdrive an OVLO or UVLO fault.

Internal NMOS FET

The NCP348 includes an internal Low $R_{DS(on)}$ NMOS FET to protect the systems, connected on OUT pin, from positive overvoltage. Regarding electrical characteristics, the $R_{DS(on)}$, during normal operation, will create low losses on V_{out} pin.

As example: R_{load} = 8.0 Ω, V_{in} = 5.0 V
Typical $R_{DS(on)}$ = 65 mΩ, I_{out} = 618 mA

V_{out} = 8 x 0.618 = 4.95 V

NMOS losses = $R_{DS(on)}$ x $Iout^2$ = 0.065 x 0.618^2 = 25 mW

ESD Tests

The NCP348 input pin fully supports the IEC61000−4−2. 1.0 μF (minimum) must be connected between V_{in} and GND, close to the device.

That means, in Air condition, V_{in} has a ±15 kV ESD protected input. In Contact condition, V_{in} has ±8.0 kV ESD protected input.

Please refer to Figure 19 to see the IEC 61000−4−2 electrostatic discharge waveform.

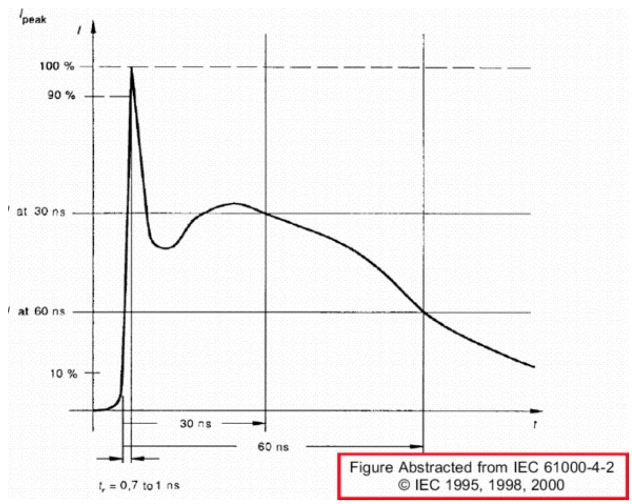


Figure 19. Electrostatic Discharge Waveform

PCB Recommendations

The NCP348 integrates a 2 amperes rated NMOS FET, and the PCB rules must be respected to properly evacuate the heat out of the silicon. The PAD1 is internally isolated from the active silicon and should preferably be connected to ground. The PAD2 of the NCP348 package is connected to the internal NMOS drain and can be used to increase the heat transfer if necessary from an applications standpoint.

Depending upon the power dissipated in the application, one can either use the PCB tracks connected to Pins 4 and 5 to evacuate heat, or make profit of the PAD2 area to add extra copper surface to reduce the junction temperature (See Figure 20). Of course, in any case, this pad shall be not connected to any other potential. Figure 20 shows copper area according to $R_{θJA}$ and allows the design of the heat transfer plane connected to PAD2.

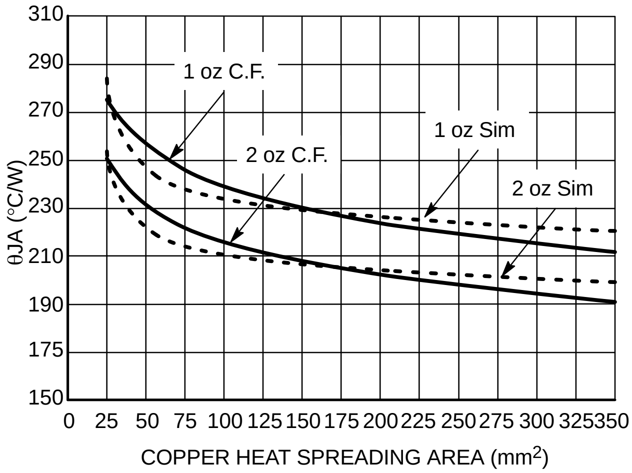


Figure 20.

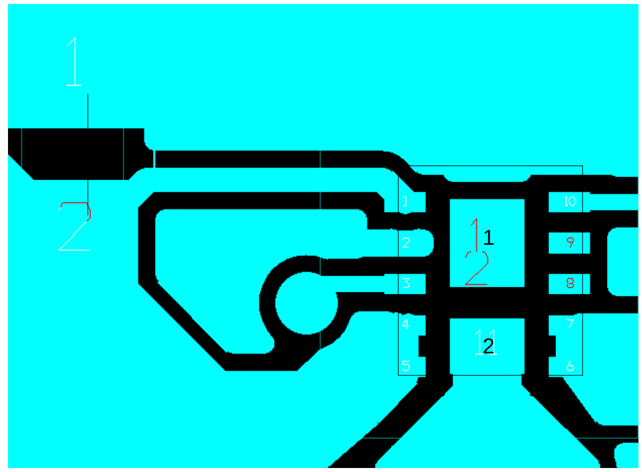


Figure 21. Demo Board Layout

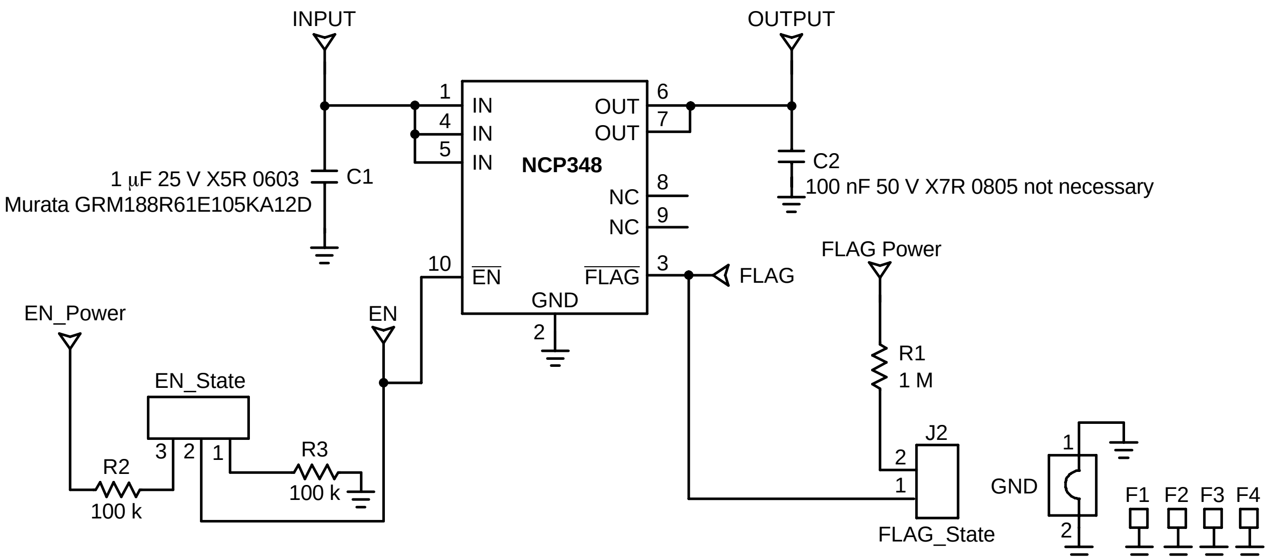
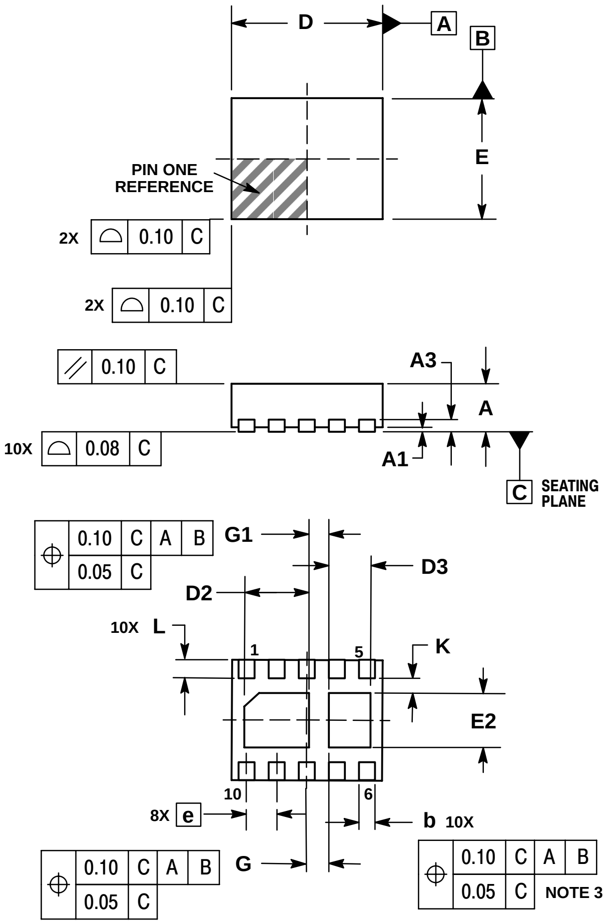


Figure 22. Demo Board Schematic

PACKAGE DIMENSIONS

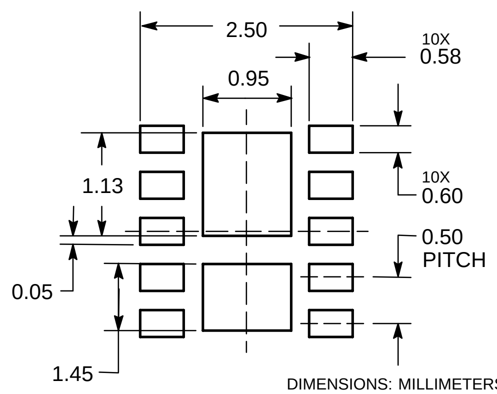
WDFN10, 2.5x2, 0.5P
CASE 516AA−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	---	0.05
A3	0.20 REF		
b	0.20	0.25	0.30
D	2.50 BSC		
D2	0.97	1.08	1.18
D3	0.57	0.68	0.78
e	0.50 BSC		
E	2.00 BSC		
E2	0.80	0.90	1.00
G	3.75 BSC		
G1	3.50 BSC		
K	0.20	---	---
L	0.20	0.30	0.40

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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