



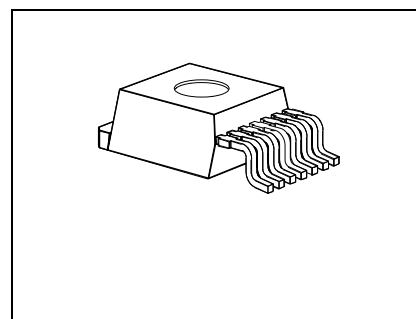
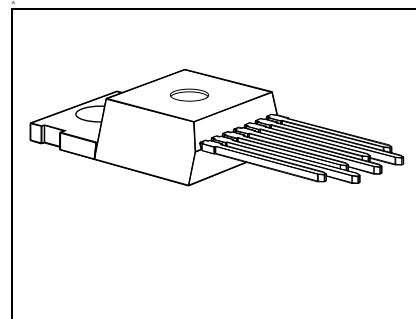
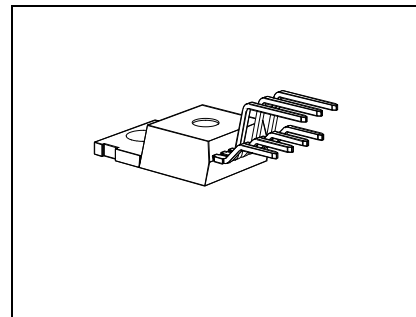
Features

- Output voltage tolerance $\leq \pm 2\%$
- Low-drop voltage
- Integrated overtemperature protection
- Reverse polarity protection
- Input voltage up to 42 V
- Overvoltage protection up to 65 V (≤ 400 ms)
- Short-circuit proof
- Suitable for use in automotive electronics
- Wide temperature range
- Adjustable reset and watchdog time
- Green Product (RoHS compliant)
- AEC Qualified

Functional Description

The TLE 4271-2 is functional and electrical identical to TLE 4271.

The device is a 5-V low drop fixed voltage regulator. The maximum input voltage is 42 V (65 V, ≤ 400 ms). Up to an input voltage of 26 V and for an output current up to 550 mA it regulates the output voltage within a 2% accuracy. The short circuit protection limits the output current of more than 650 mA. The IC can be switched off via the inhibit input. An integrated watchdog monitors the connected controller. The device incorporates overvoltage protection and temperature protection that disables the circuit at overtemperature.



| Type | Package |
|--------------|---------------|
| TLE 4271-2 | PG-TO220-7-11 |
| TLE 4271-2 S | PG-TO220-7-12 |
| TLE 4271-2 G | PG-TO263-7-1 |

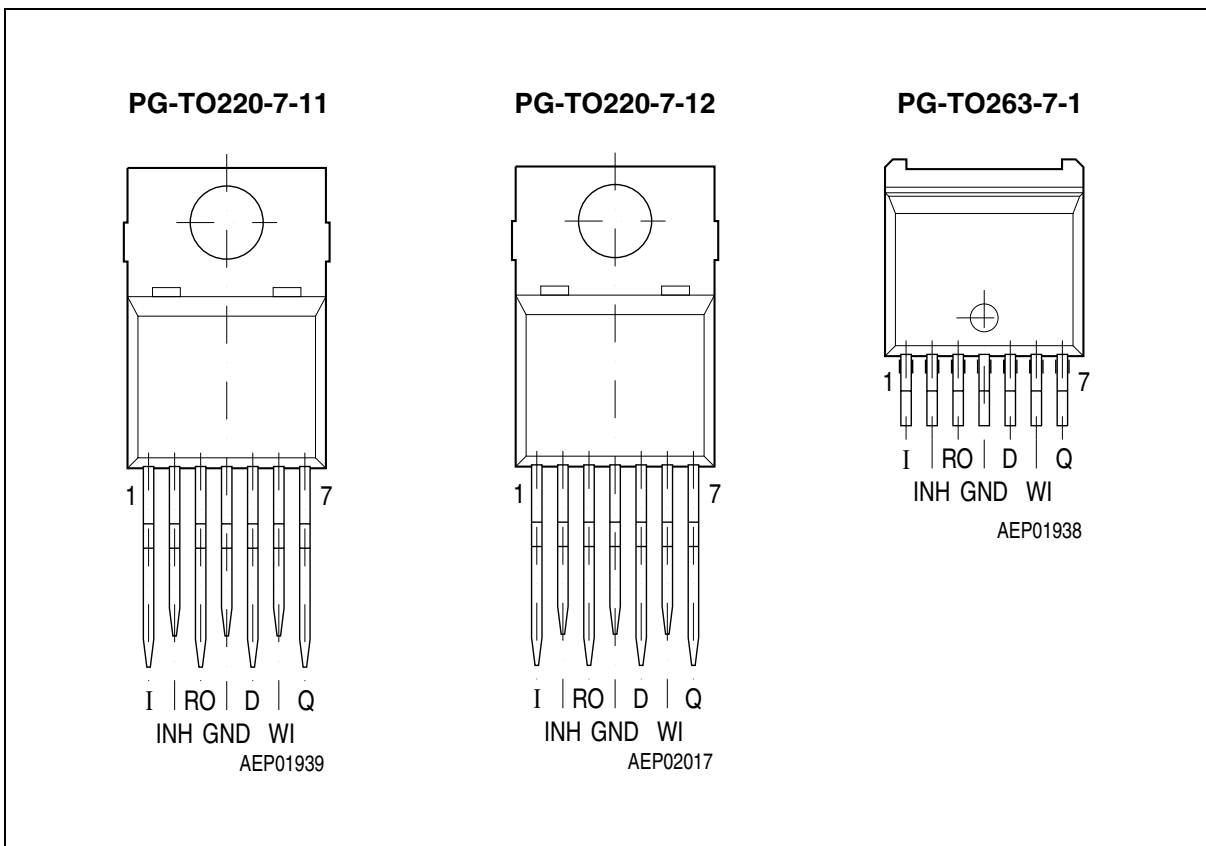


Figure 1 Pin Configuration (top view)

Table 1 Pin Definitions and Functions

| Pin | Symbol | Function |
|-----|--------|---|
| 1 | I | Input ; block to ground directly on the IC with ceramic capacitor. |
| 2 | INH | Inhibit |
| 3 | RO | Reset Output ; the open collector output is connected to the 5 V output via an integrated resistor of 30 kΩ. |
| 4 | GND | Ground |
| 5 | D | Reset Delay ; connect a capacitor to ground for delay time adjustment. |
| 6 | WI | Watchdog Input |
| 7 | Q | 5-V Output ; block to ground with 22 μF capacitor, ESR < 3 Ω. |

Circuit Description

The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and drives the base of a series transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element.

The reset output RO is in high-state if the voltage on the delay capacitor C_D is greater or equal V_{UD} . The delay capacitor C_D is charged with the current I_D for output voltages greater than the reset threshold V_{RT} . If the output voltage gets lower than V_{RT} ('reset condition') a fast discharge of the delay capacitor C_D sets in and as soon as V_D gets lower than V_{LD} the reset output RO is set to low-level.

The time for the delay capacitor charge from V_{UD} to V_{LD} is the reset delay time t_D .

When the voltage on the delay capacitor has reached V_{UD} and reset was set to high, the watchdog circuit is enabled and discharges C_D with the constant current I_{DWD} . If there is no rising edge observed at the watchdog input, C_D will be discharge down to V_{LDW} , then reset output RO will be set to low and C_D will be charged again with the current I_{DWC} until V_D reaches V_{UD} and reset will be set high again.

If the watchdog pulse (rising edge at watchdog input WI) occurs during the discharge period C_D is charged again and the reset output stays high. After V_D has reached V_{UD} , the periodical behavior starts again.

Internal protection circuits protect the IC against:

- Overload
- Overvoltage
- Overtemperature
- Reverse polarity

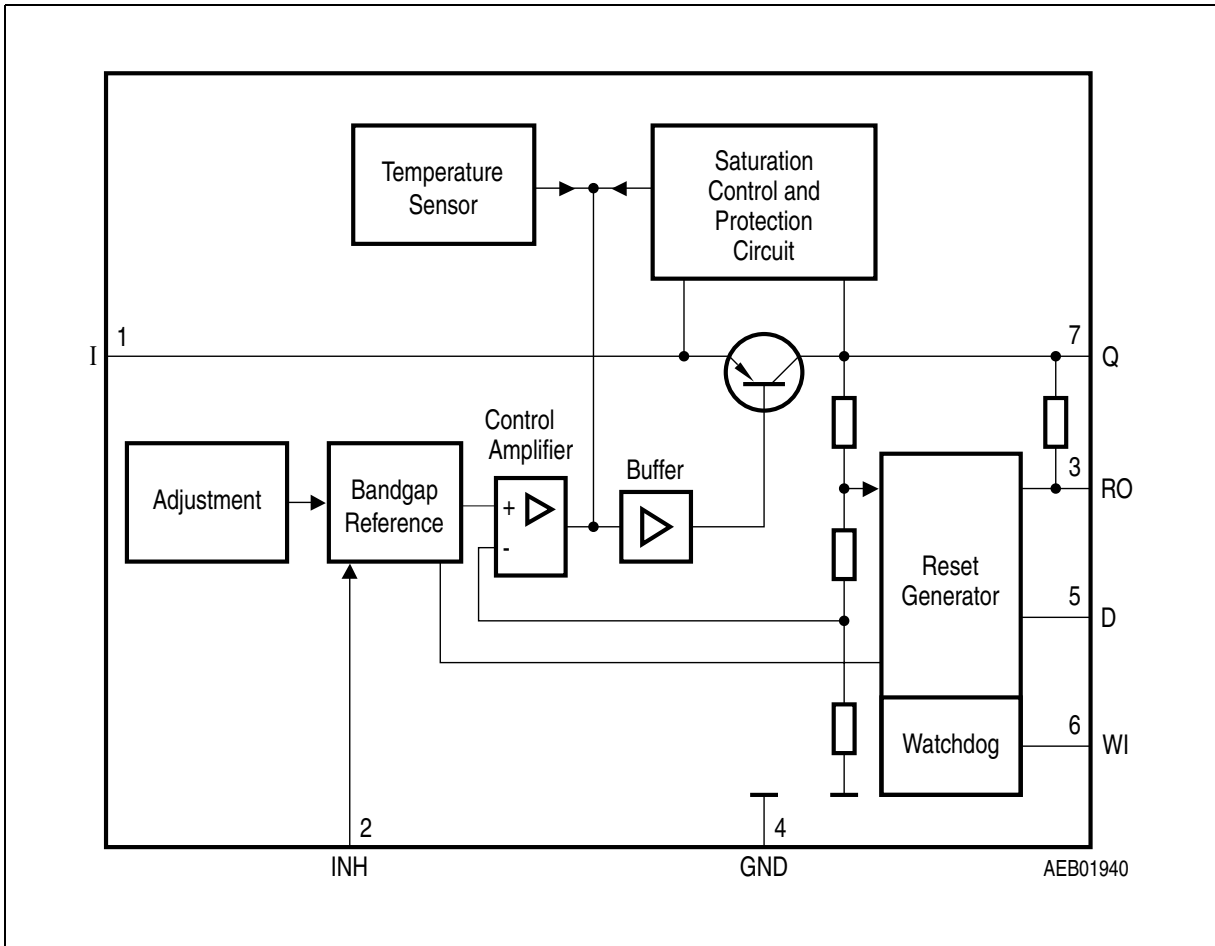


Figure 2 Block Diagram

Table 2 Absolute Maximum Ratings
 $T_j = -40$ to 150 °C

| Parameter | Symbol | Limit Values | | Unit | Notes |
|----------------------|-----------|--------------|------|------|--------------------|
| | | Min. | Max. | | |
| Input | | | | | |
| Voltage | V_I | -42 | 42 | V | – |
| Voltage | V_I | – | 65 | V | $t \leq 400$ ms |
| Current | I_I | – | – | mA | internally limited |
| Inhibit | | | | | |
| Voltage | V_{INH} | -42 | 42 | V | – |
| Voltage | V_{INH} | – | 65 | V | $t \leq 400$ ms |
| Current | I_{INH} | – | – | mA | internally limited |
| Reset Output | | | | | |
| Voltage | V_{RO} | -0.3 | 42 | V | – |
| Current | I_{RO} | – | – | mA | internally limited |
| Reset Delay | | | | | |
| Voltage | V_D | -0.3 | 7 | V | – |
| Current | I_D | -5 | 5 | mA | – |
| Watchdog | | | | | |
| Voltage | V_W | -0.3 | 7 | V | – |
| Current | I_W | -5 | 5 | mA | – |
| Output | | | | | |
| Voltage | V_Q | -1.0 | 16 | V | – |
| Current | I_Q | -5 | – | mA | internally limited |
| Ground | | | | | |
| Current | I_{GND} | -0.5 | – | A | – |
| Temperatures | | | | | |
| Junction temperature | T_j | – | 150 | °C | – |
| Storage temperature | T_{stg} | -50 | 150 | °C | – |

Table 3 Operating Range

| Parameter | Symbol | Limit Values | | Unit | Notes |
|---------------------------|------------|--------------|------|------|--------------|
| | | Min. | Max. | | |
| Input voltage | V_I | 6 | 40 | V | – |
| Junction temperature | T_j | -40 | 150 | °C | – |
| Thermal Resistance | | | | | |
| Junction ambient | R_{thja} | – | 65 | K/W | – |
| | | – | 70 | K/W | PG-TO263-7-1 |
| Junction case | R_{thjc} | – | 3 | K/W | – |
| | Z_{thjc} | – | 2 | K/W | $t < 1$ ms |

Table 4 Characteristics
 $V_I = 13.5 \text{ V}; -40 \text{ }^\circ\text{C} \leq T_j \leq 125 \text{ }^\circ\text{C}; V_{\text{INH}} > V_{\text{U,INH}}$ (unless otherwise specified)

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|--|-------------------|--------------|------|------|---------------|--|
| | | Min. | Typ. | Max. | | |
| Output voltage | V_Q | 4.90 | 5.00 | 5.10 | V | $5 \text{ mA} \leq I_Q \leq 550 \text{ mA};$ $6 \text{ V} \leq V_I \leq 26 \text{ V}$ |
| Output voltage | V_Q | 4.90 | 5.00 | 5.10 | V | $26 \text{ V} \leq V_I \leq 36 \text{ V};$ $I_Q \leq 300 \text{ mA}$ |
| Output current limiting | $I_{Q\text{max}}$ | 650 | 800 | – | mA | $V_Q = 0 \text{ V}$ |
| Current consumption $I_q = I_I$ | I_q | – | – | 6 | μA | $V_{\text{INH}} = 0 \text{ V}; I_Q = 0 \text{ mA}$ |
| Current consumption $I_q = I_I$ | I_q | – | 800 | – | μA | $V_{\text{INH}} = 5 \text{ V}; I_Q = 0 \text{ mA}$ |
| Current consumption $I_q = I_I - I_Q$ | I_q | – | 1 | 1.5 | mA | $I_Q = 5 \text{ mA}$ |
| Current consumption $I_q = I_I - I_Q$ | I_q | – | 55 | 75 | mA | $I_Q = 550 \text{ mA}$ |
| Current consumption $I_q = I_I - I_Q$ | I_q | – | 70 | 90 | mA | $I_Q = 550 \text{ mA}; V_I = 5 \text{ V}$ |
| Drop voltage | V_{dr} | – | 350 | 700 | mV | $I_Q = 550 \text{ mA}^1)$ |
| Load regulation | ΔV_Q | – | 25 | 50 | mV | $I_Q = 5 \text{ to } 550 \text{ mA};$ $V_I = 6 \text{ V}$ |
| Supply voltage regulation | ΔV_Q | – | 12 | 25 | mV | $V_I = 6 \text{ to } 26 \text{ V}$ $I_Q = 5 \text{ mA}$ |
| Power supply Ripple rejection | $PSRR$ | – | 54 | – | dB | $f_r = 100 \text{ Hz};$ $V_r = 0.5 \text{ Vpp}$ |

Table 4 Characteristics (cont'd)
 $V_I = 13.5 \text{ V}; -40 \text{ }^\circ\text{C} \leq T_j \leq 125 \text{ }^\circ\text{C}; V_{\text{INH}} > V_{\text{U,INH}}$ (unless otherwise specified)

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|------------------------------------|---------------------|--------------|------|------|---------------|---|
| | | Min. | Typ. | Max. | | |
| Reset Generator | | | | | | |
| Switching threshold | V_{RT} | 4.5 | 4.65 | 4.8 | V | – |
| Reset high voltage | V_{ROH} | 4.5 | – | – | V | – |
| Saturation voltage | $V_{\text{RO,SAT}}$ | – | 60 | – | mV | $R_{\text{intern}} = 30 \text{ k}\Omega;$ $1.0 \text{ V} \leq V_{\text{Q}} \leq 4.5 \text{ V}$ |
| Saturation voltage | $V_{\text{RO,SAT}}$ | – | 200 | 400 | mV | $I_{\text{R}} = 3 \text{ mA}^{(2)};$ $V_{\text{Q}} = 4.4 \text{ V}$ |
| Reset pull-up | R | 18 | 30 | 46 | k Ω | internally connected to Q |
| Lower reset timing threshold | V_{LD} | 0.2 | 0.45 | 0.8 | V | $V_{\text{Q}} < V_{\text{RT}}$ |
| Charge current | I_{D} | 8 | 14 | 25 | μA | $V_{\text{D}} = 1.0 \text{ V}$ |
| Upper timing threshold | V_{UD} | 1.4 | 1.8 | 2.3 | V | – |
| Delay time | t_{D} | 8 | 13 | 18 | ms | $C_{\text{D}} = 100 \text{ nF}$ |
| Reset reaction time | t_{RR} | – | – | 3 | μs | $C_{\text{D}} = 100 \text{ nF}$ |
| Overvoltage Protection | | | | | | |
| Turn-off voltage | $V_{\text{I,ov}}$ | 40 | 44 | 46 | V | – |
| Inhibit | | | | | | |
| Turn-on voltage | $V_{\text{U,INH}}$ | 1.0 | 2.0 | 3.5 | V | $V_{\text{Q}} = \text{high} (> 4.5 \text{ V})$ |
| Turn-off voltage | $V_{\text{L,INH}}$ | 0.8 | 1.3 | 3.3 | V | $V_{\text{Q}} = \text{low} (< 0.8 \text{ V})$ |
| Inhibit current | I_{INH} | 8 | 12 | 25 | μA | $V_{\text{INH}} = 5 \text{ V}$ |
| Watchdog | | | | | | |
| Upper watchdog switching threshold | V_{UDW} | 1.4 | 1.8 | 2.3 | V | – |
| Lower watchdog switching threshold | V_{LDW} | 0.2 | 0.45 | 0.8 | V | – |
| Discharge current | I_{DWD} | 1.5 | 2.7 | 3.5 | μA | $V_{\text{D}} = 1 \text{ V}$ |
| Charge current | I_{DWC} | 8 | 14 | 25 | μA | $V_{\text{D}} = 1 \text{ V}$ |
| Watchdog period | $t_{\text{WD,P}}$ | 40 | 55 | 80 | ms | $C_{\text{D}} = 100 \text{ nF}$ |

Table 4 Characteristics (cont'd)
 $V_I = 13.5 \text{ V}; -40 \text{ }^\circ\text{C} \leq T_j \leq 125 \text{ }^\circ\text{C}; V_{\text{INH}} > V_{\text{U,INH}}$ (unless otherwise specified)

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|--------------------------|--------------------|--------------|------|------|------------------|---------------------------------------|
| | | Min. | Typ. | Max. | | |
| Watchdog trigger time | $t_{\text{WI,tr}}$ | 30 | 45 | 66 | ms | $C_D = 100 \text{ nF}$ see diagram |
| Watchdog pulse slew rate | V_{WI} | 5 | – | – | V/ μs | from 20% to 80% V_Q |

- 1) Drop voltage = $V_I - V_Q$ (measured when the output voltage has dropped 100 mV from the nominal value obtained at 13.5 V input)
- 2) Test condition not applicable during delay time for power-on reset.

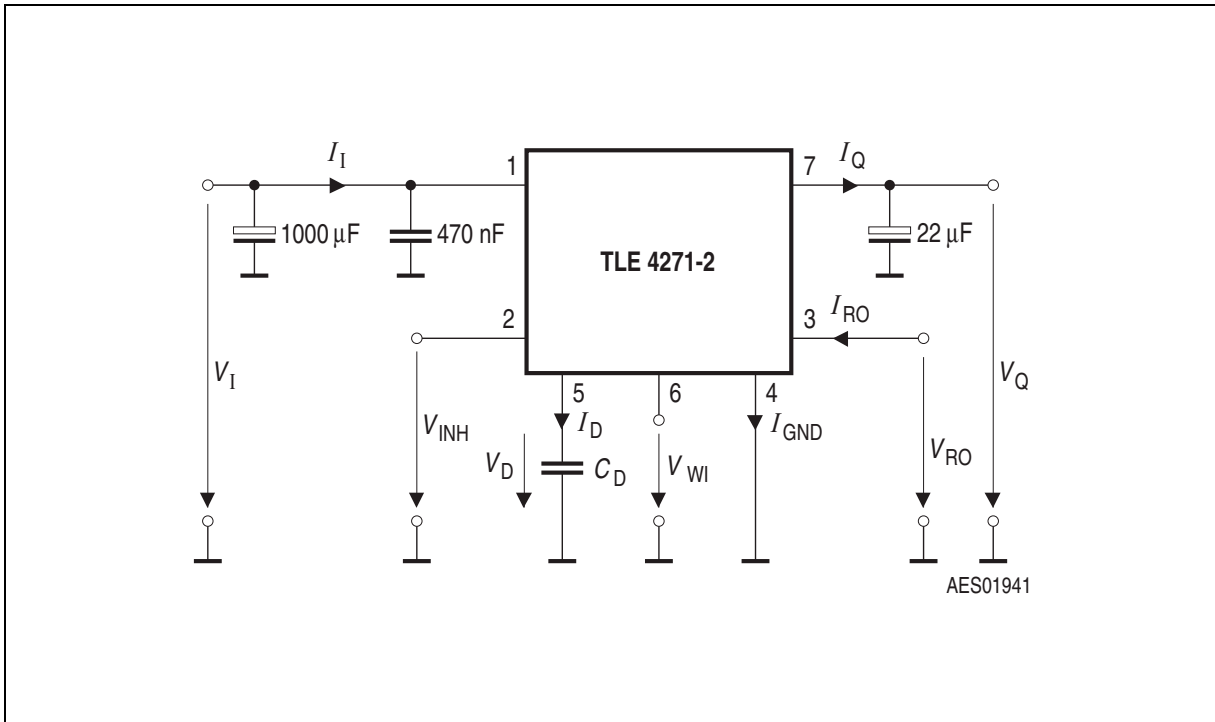


Figure 3 Test Circuit

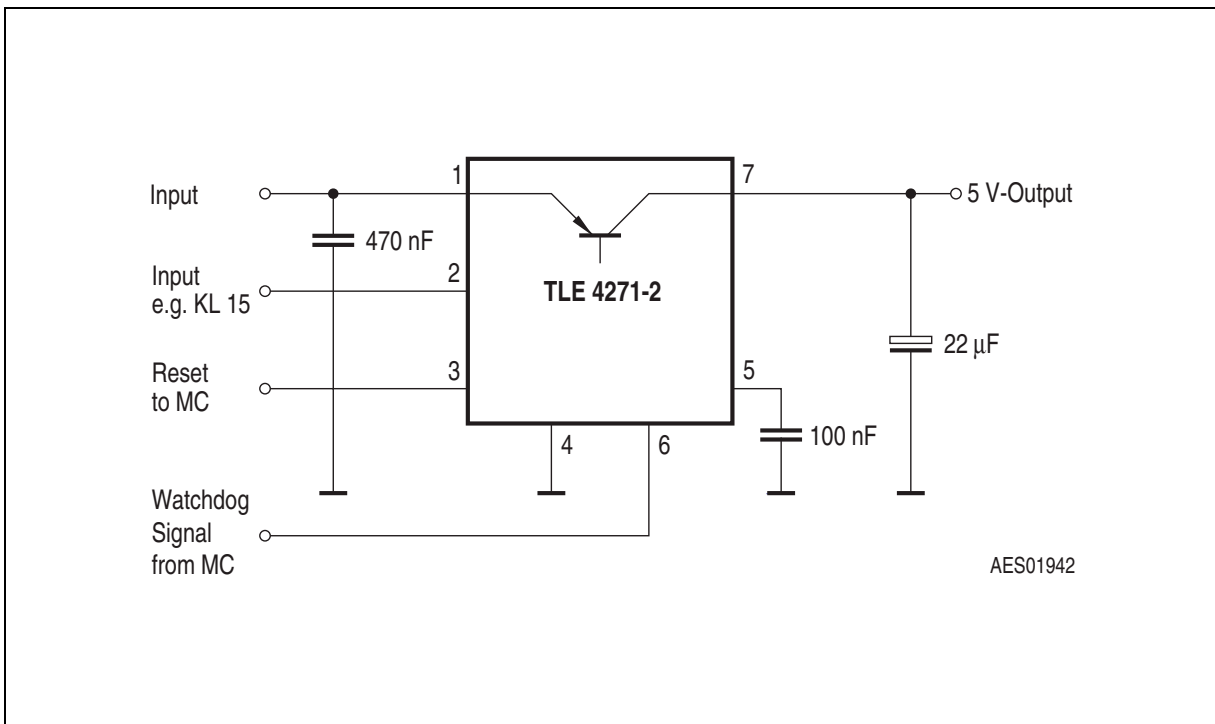


Figure 4 Circuit

Application Description

The IC regulates an input voltage in the range of $6\text{ V} < V_I < 40\text{ V}$ to $V_{Qnom} = 5.0\text{ V}$. Up to 26 V it produces a regulated output current of more than 550 mA . Above 26 V the save-operating-area protection allows operation up to 36 V with a regulated output current of more than 300 mA . Overvoltage protection limits operation at 42 V . The overvoltage protection hysteresis restores operation if the input voltage has dropped below 36 V . The IC can be switched off via the inhibit input, which causes the quiescent current to drop below $10\text{ }\mu\text{A}$. A reset signal is generated for an output voltage of $V_Q < 4.5\text{ V}$. The watchdog circuit monitors a connected controller. If there is no positive-going edge at the watchdog input within a fixed time, the reset output is set to low. The delay for power-on reset and the maximum permitted watchdog-pulse period can be set externally with a capacitor.

Design Notes for External Components

An input capacitor C_I is necessary for compensation of line influences. The resonant circuit consisting of lead inductance and input capacitance can be damped by a resistor of approx. $1\text{ }\Omega$ in series with C_I . An output capacitor C_Q is necessary for the stability of the regulating circuit. Stability is guaranteed at values of $C_Q \geq 22\text{ }\mu\text{F}$ and an ESR of $< 3\text{ }\Omega$.

Reset Circuitry

If the output voltage decreases below 4.5 V , an external capacitor C_D on pin D will be discharged by the reset generator. If the voltage on this capacitor drops below V_{DRL} , a reset signal is generated on pin RO, i.e. reset output is set low. If the output voltage rises above the reset threshold, C_D will be charged with constant current. After the power-on-reset time the voltage on the capacitor reaches V_{DU} and the reset output will be set high again. The value of the power-on-reset time can be set within a wide range depending of the capacitance of C_D .

Reset Timing

The power-on reset delay time is defined by the charging time of an external capacitor C_d which can be calculated as follows:

$$t_D = C_D \times \Delta V / I_D \quad (1)$$

Definitions:

- C_D = delay capacitor
- t_D = reset delay time
- I_D = charge current, typical $14\text{ }\mu\text{A}$
- $\Delta V = V_{UD}$, typical 1.8 V
- V_{UD} = upper delay timing threshold at C_D for reset delay time

The reset reaction time t_{rr} is the time it takes the voltage regulator to set the reset out LOW after the output voltage has dropped below the reset threshold. It is typically 1 μ s for delay capacitor of 47 nF. For other values for C_d the reaction time can be estimated using the following equation:

$$t_{RR} \approx 20 \text{ s/F} \times C_d \tag{2}$$

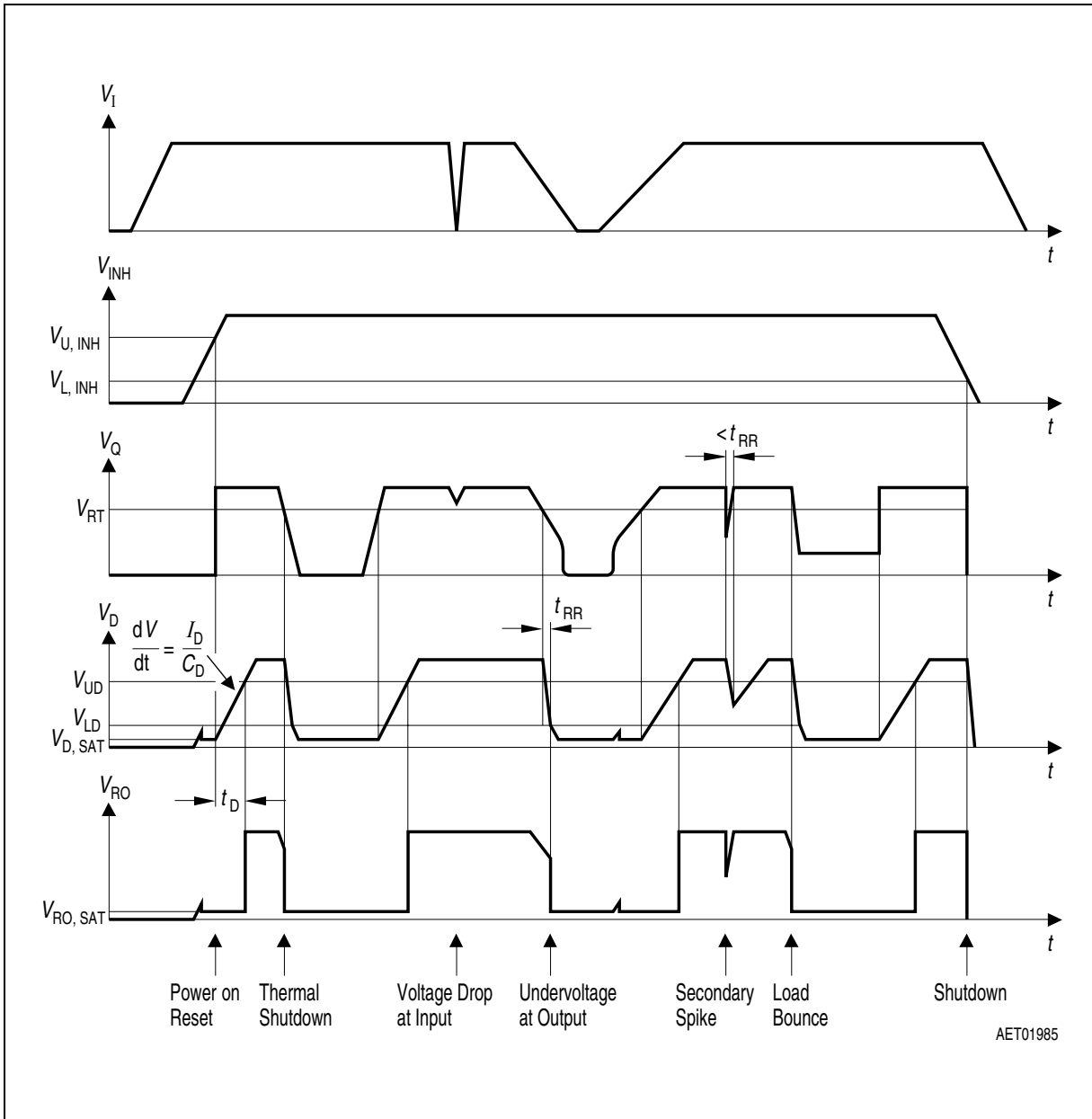


Figure 5 Time Response

Watchdog Timing

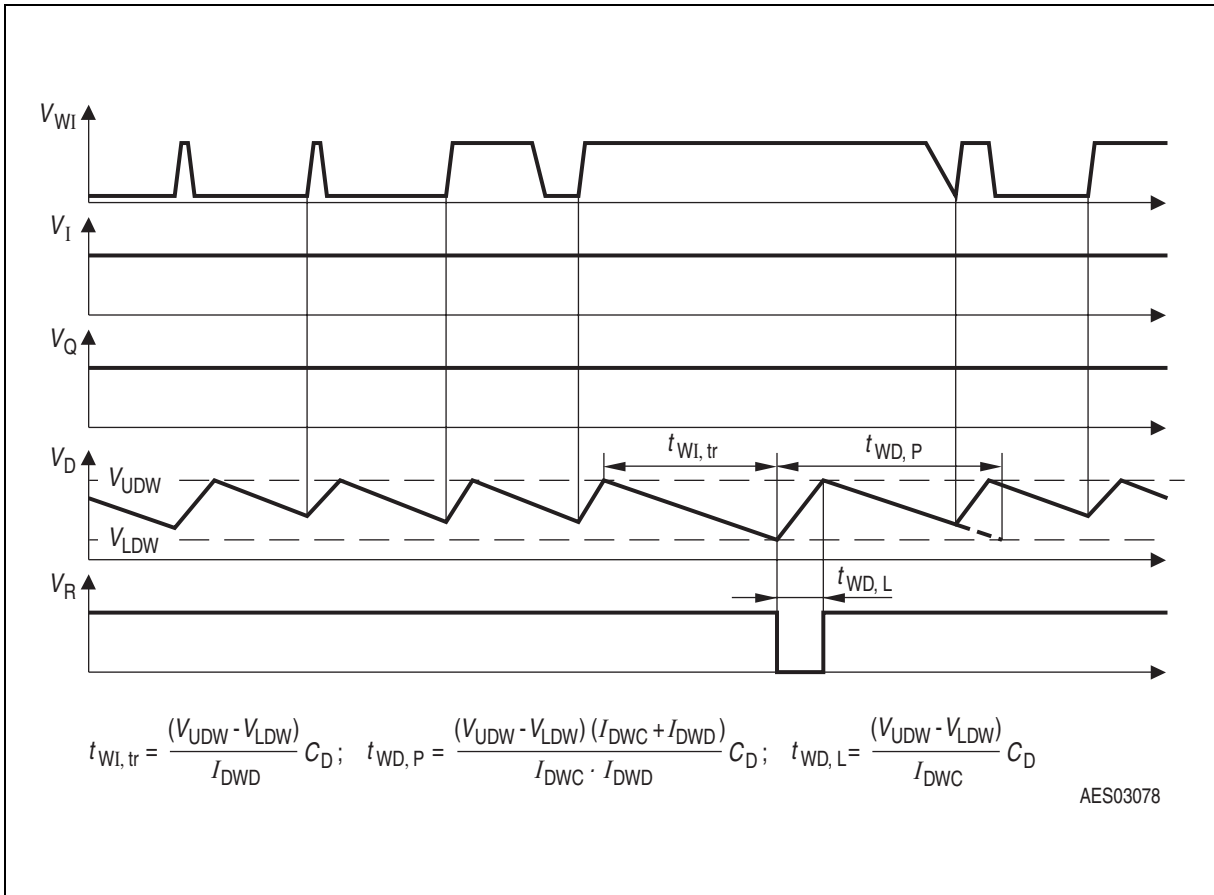
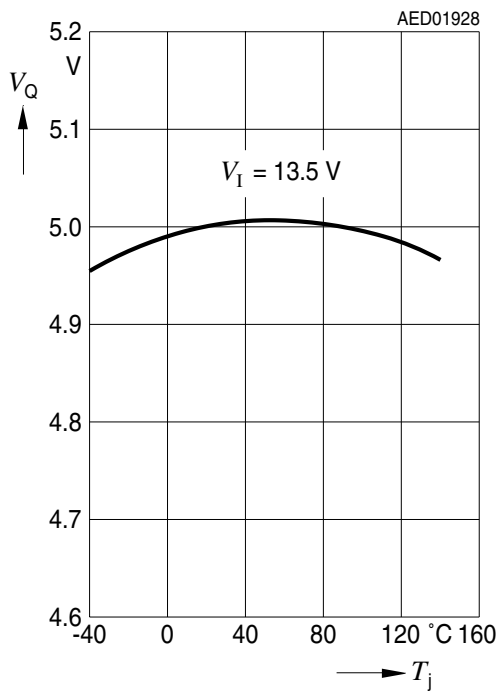


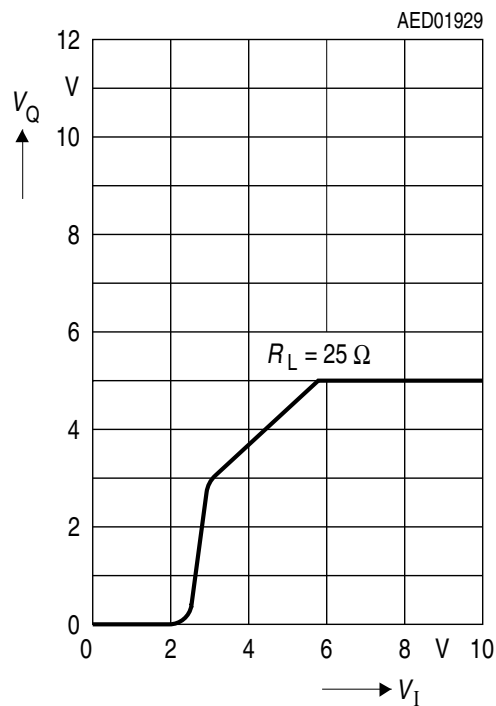
Figure 6 Time Response, Watchdog Behavior

Typical Performance Characteristics

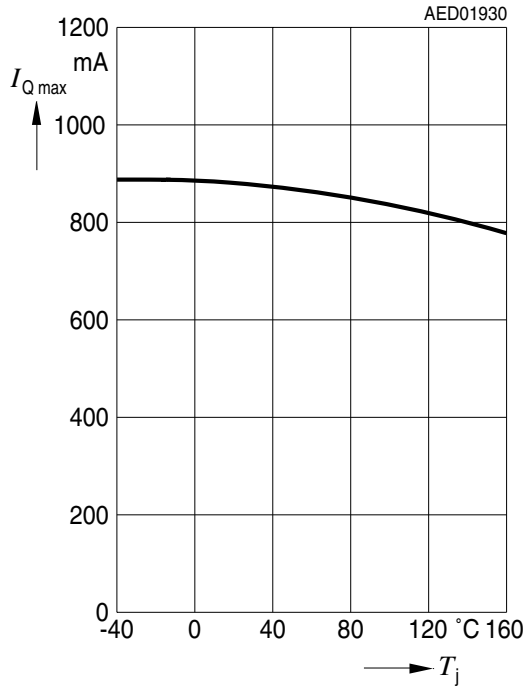
Output Voltage V_Q versus Temperature T_j



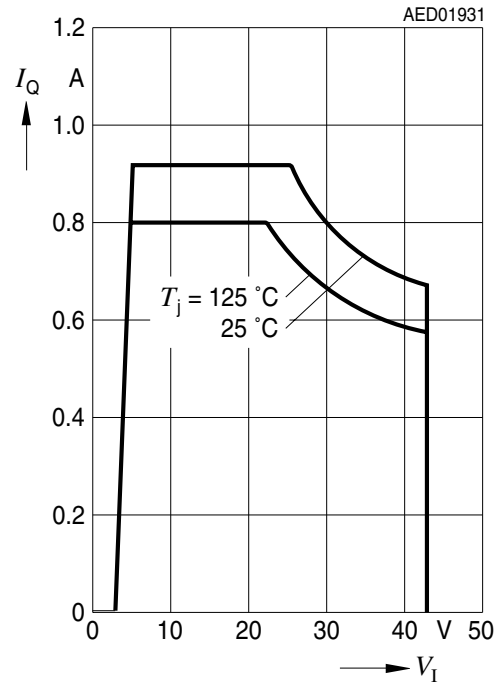
Output Voltage V_Q versus Input Voltage V_I ($V_{INH} = V_I$)



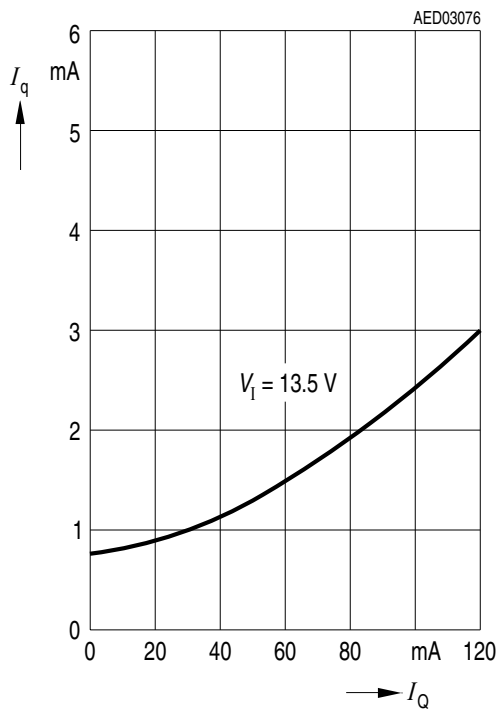
Output Current Limit I_Q versus Temperature T_j



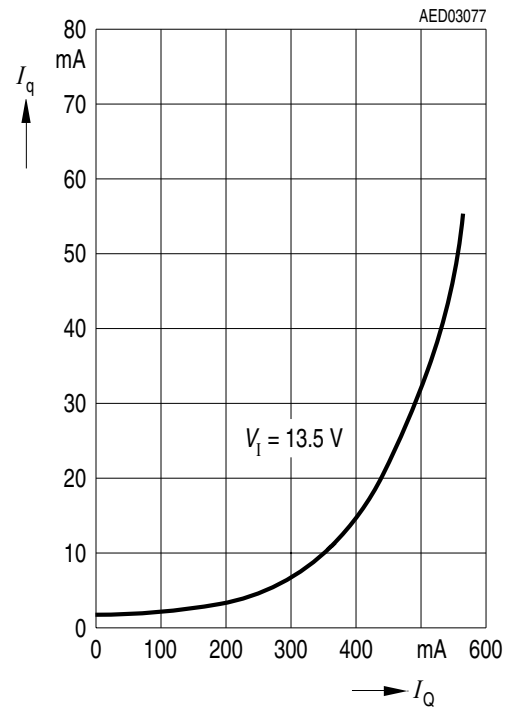
Output Current I_Q versus Input Voltage V_I



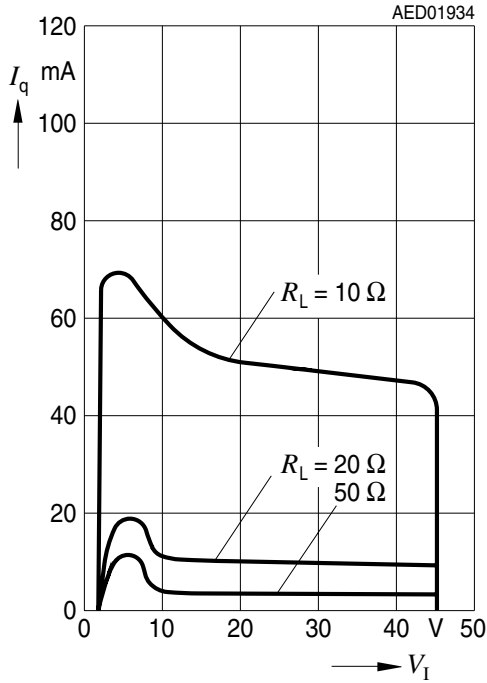
Current Consumption I_q versus Output Current I_Q



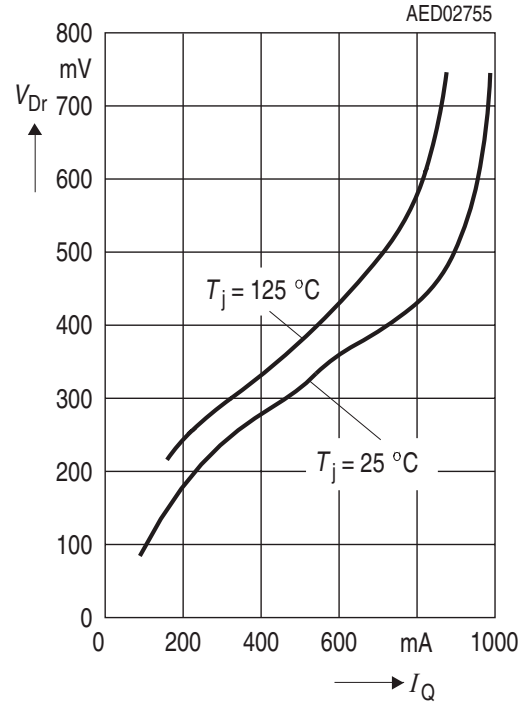
Current Consumption I_q versus Output Current I_Q



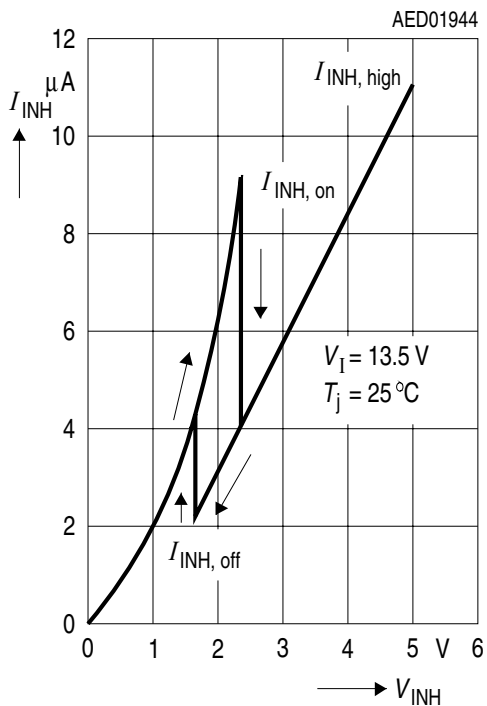
Current Consumption I_q versus Input Voltage V_I



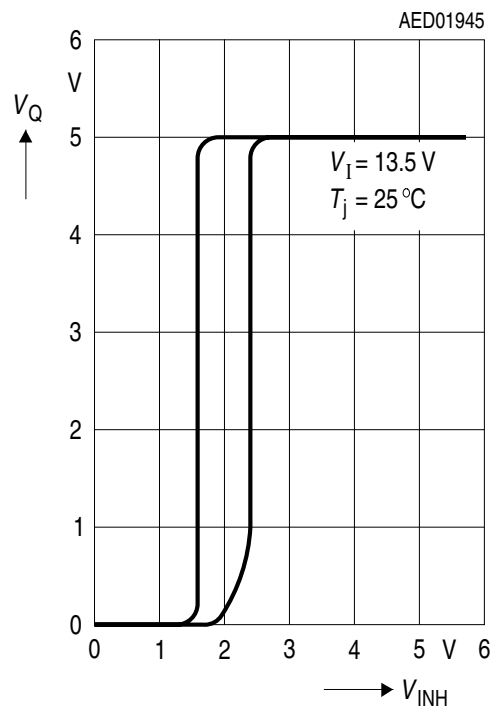
Drop Voltage V_{Dr} versus Output Current I_Q



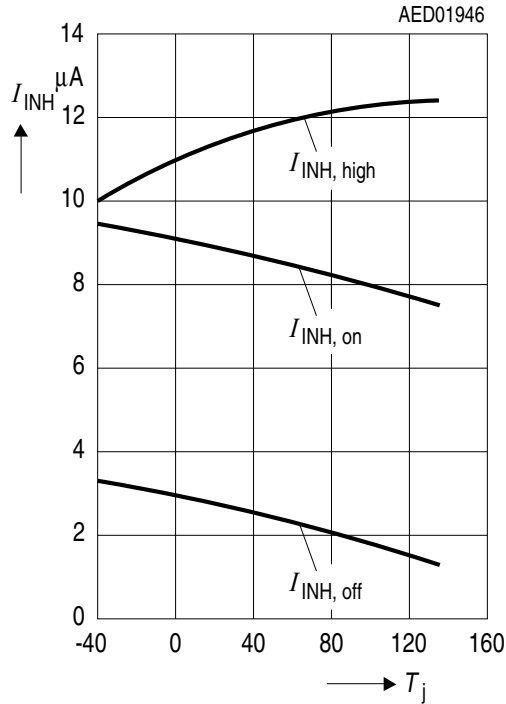
Inhibit Current I_{INH} versus Inhibit Voltage V_{INH}



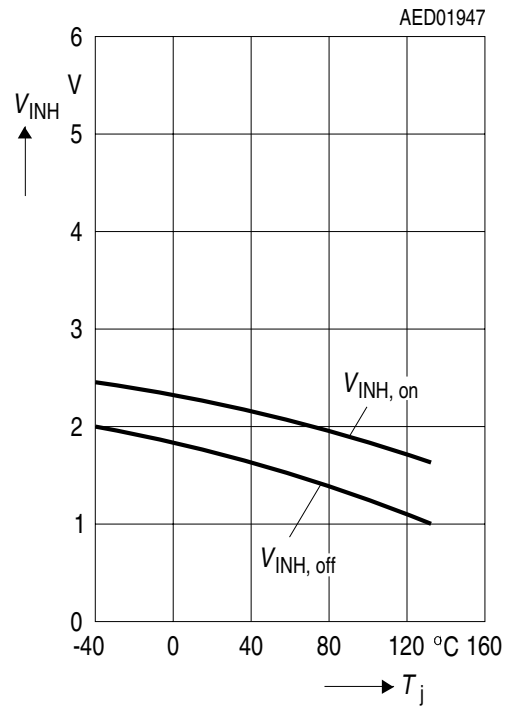
Output Voltage V_Q versus Inhibit Voltage V_{INH}



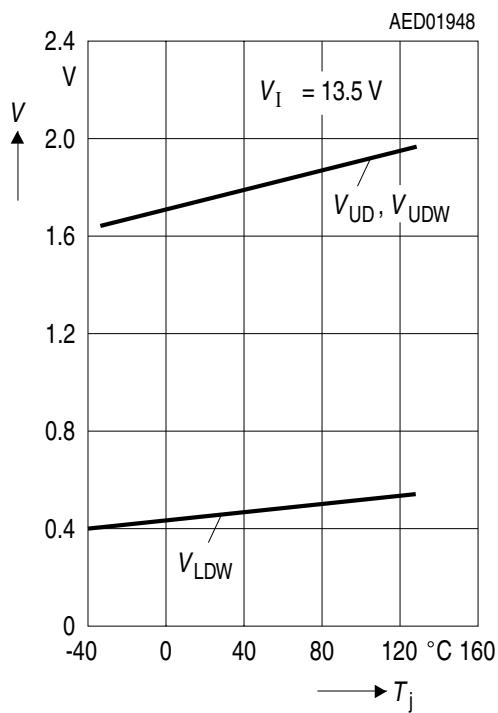
Inhibit Current Consumptions I_{INH} versus Temperature T_j



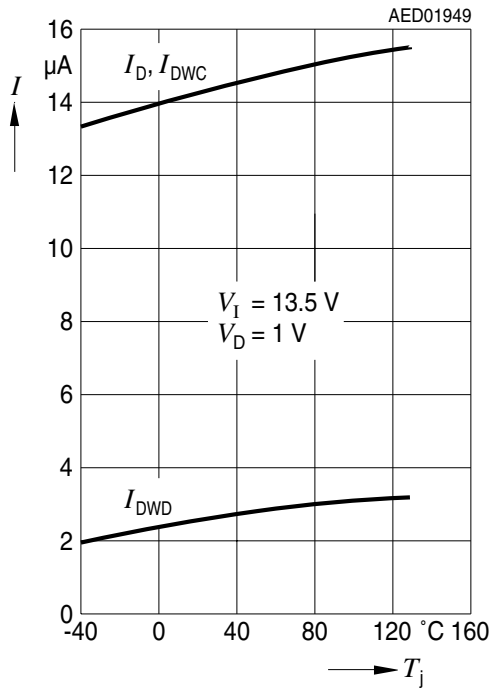
Inhibit Voltages V_{INH} versus Temperature T_j



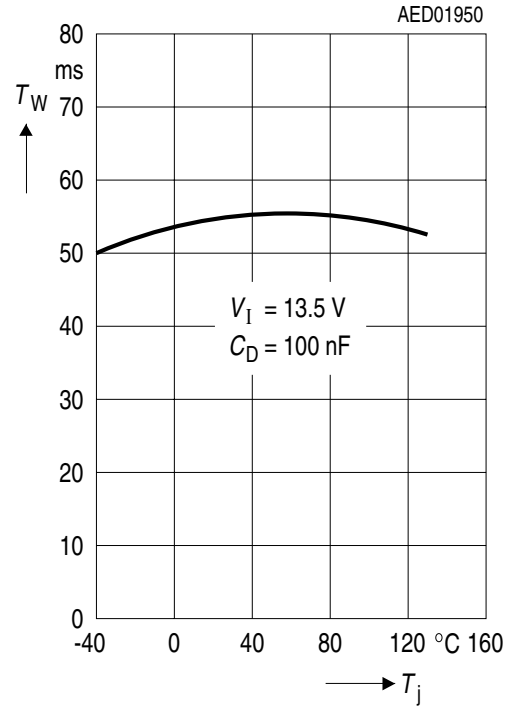
Switching Voltage V_{UD} and V_{LDW} versus Temperature T_j



Charge Current I_D , I_{DWC} and Discharge Current I_{DWD} versus Temperature T_j



Watchdog Pulse Time T_w versus Temperature T_j



Package Outlines

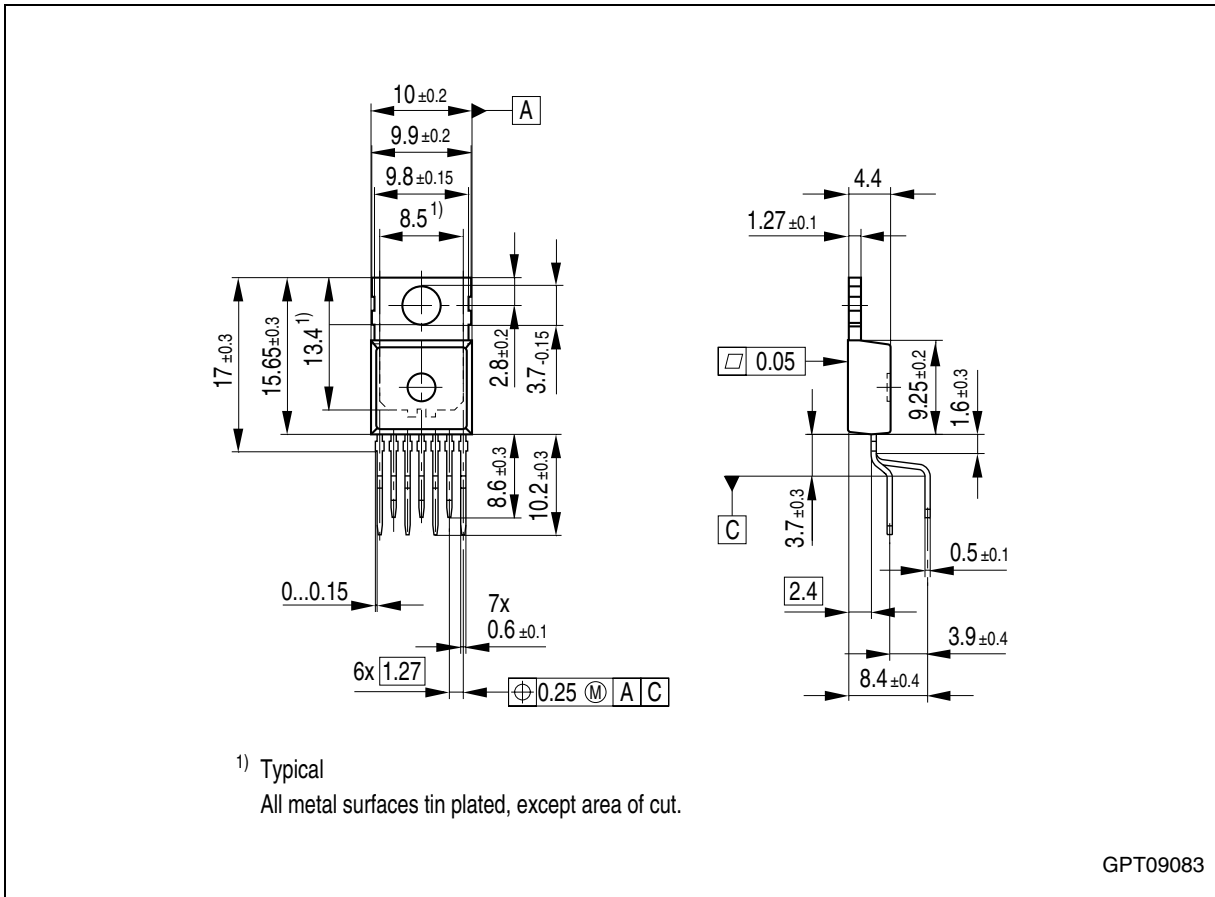


Figure 7 PG-TO220-7-11 (Plastic Transistor Single Outline)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

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SMD = Surface Mounted Device

Dimensions in mm

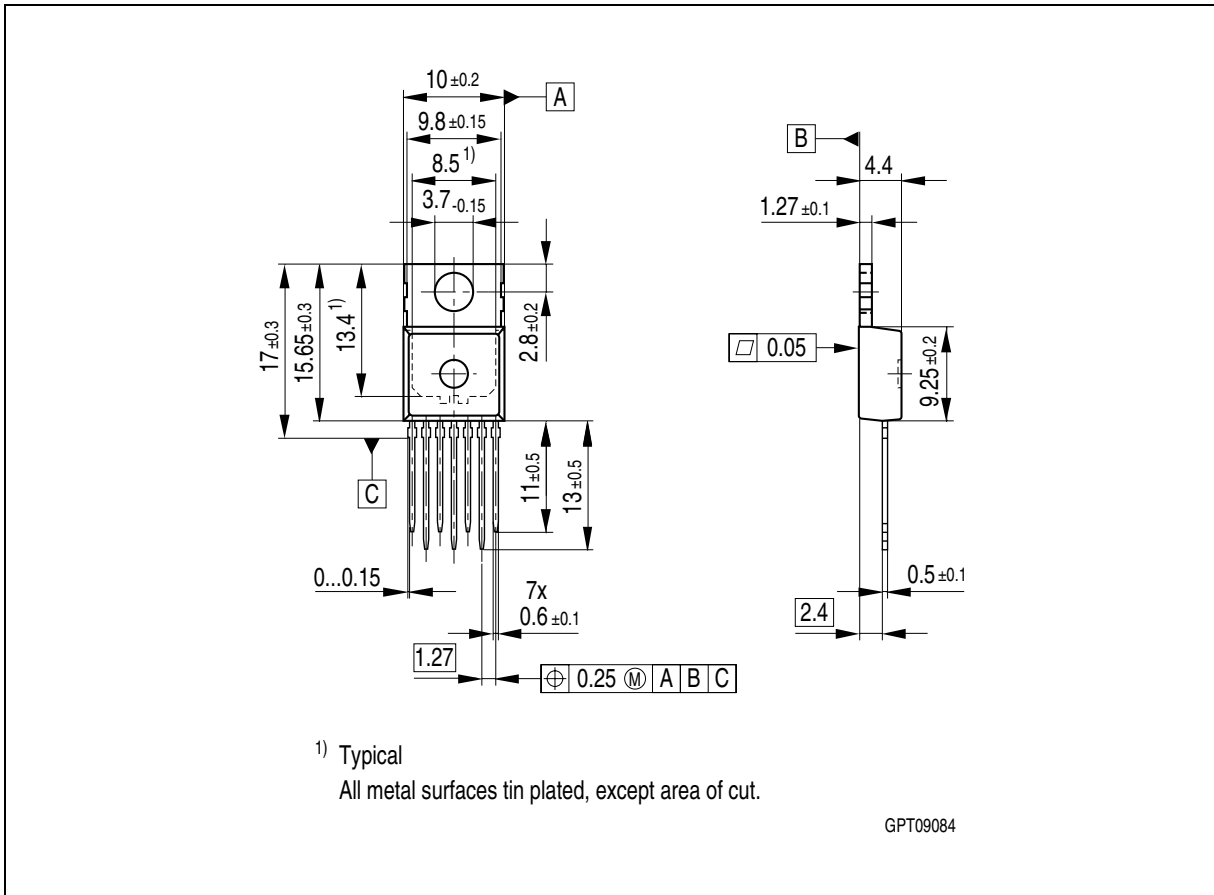


Figure 8 PG-TO220-7-12 (Plastic Transistor Single Outline)

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SMD = Surface Mounted Device

Dimensions in mm

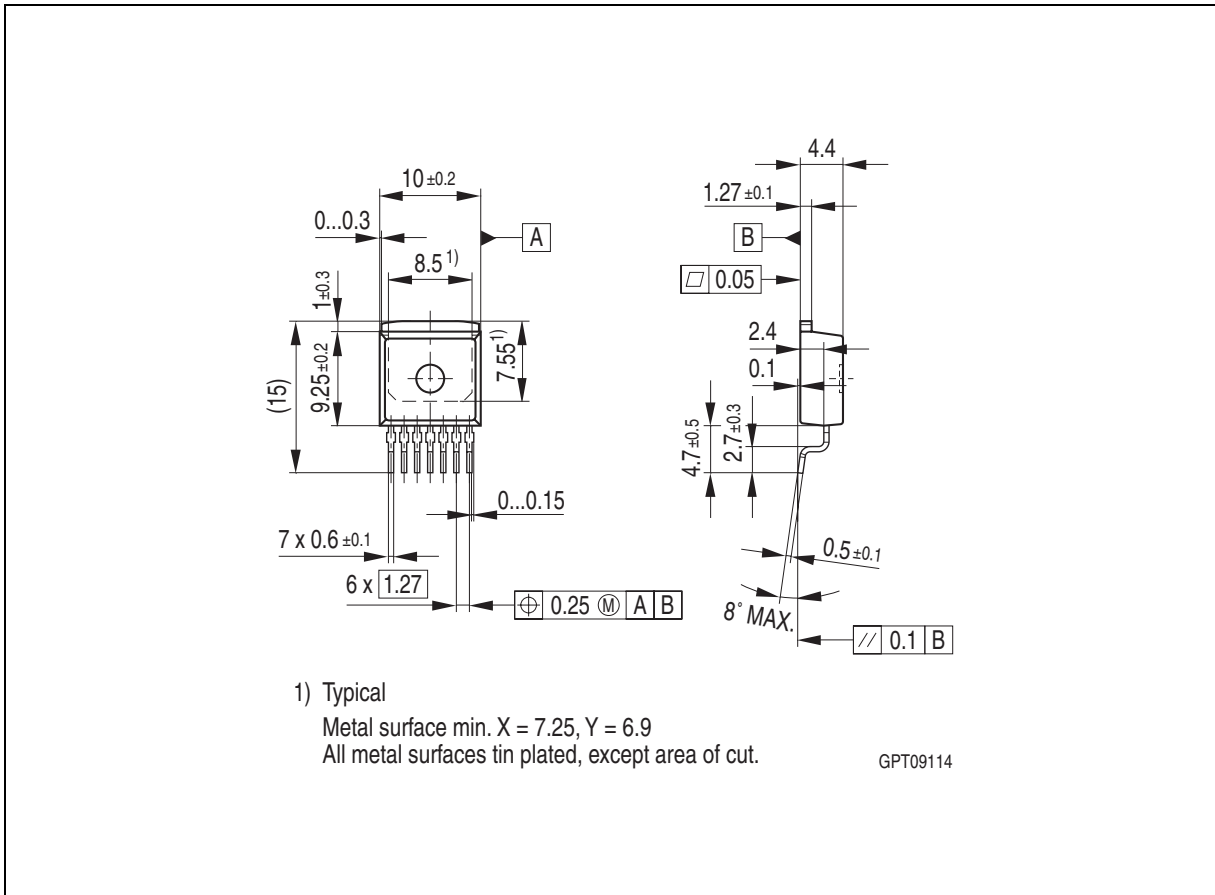


Figure 9 PG-T0263-7-1 (Plastic Transistor Single Outline)

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SMD = Surface Mounted Device

Dimensions in mm

Revision History

| Version | Date | Changes |
|----------|------------|---|
| Rev. 2.7 | 2007-03-20 | Initial version of RoHS-compliant derivate of TLE 4271-2 Page 1 : AEC certified statement added Page 1 and Page 19 ff: RoHS compliance statement and Green product feature added Page 1 and Page 19 ff: Package changed to RoHS compliant version Legal Disclaimer updated |

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