

## LP5526

# Lighting Management Unit with High Voltage Boost Converter with up to 150mA Serial FLASH LED Driver

### General Description

LP5526 is a Lighting Management Unit for portable applications. It is used to drive display backlights, keypad LEDs, RGB LEDs and camera flash LEDs. LP5526 can drive 2 separately connected strings of LEDs with high voltage boost converter. The RGB driver allows driving either individual color LEDs or RGB LED from separate supply power, or it can be used to drive series connector flash LEDs from high voltage boost converter.

The backlight drivers (MAIN and SUB pins) are both high resolution constant current mode drivers. The flash outputs can drive series connected flash LED with up to 150mA of current. External PWM control can be used for dimming any selected LED outputs or it can be used to trigger the flash. The flash has also 1-second safety timer.

The device is controlled through 2-wire low voltage I<sup>2</sup>C compatible interface that reduces the number of required connections.

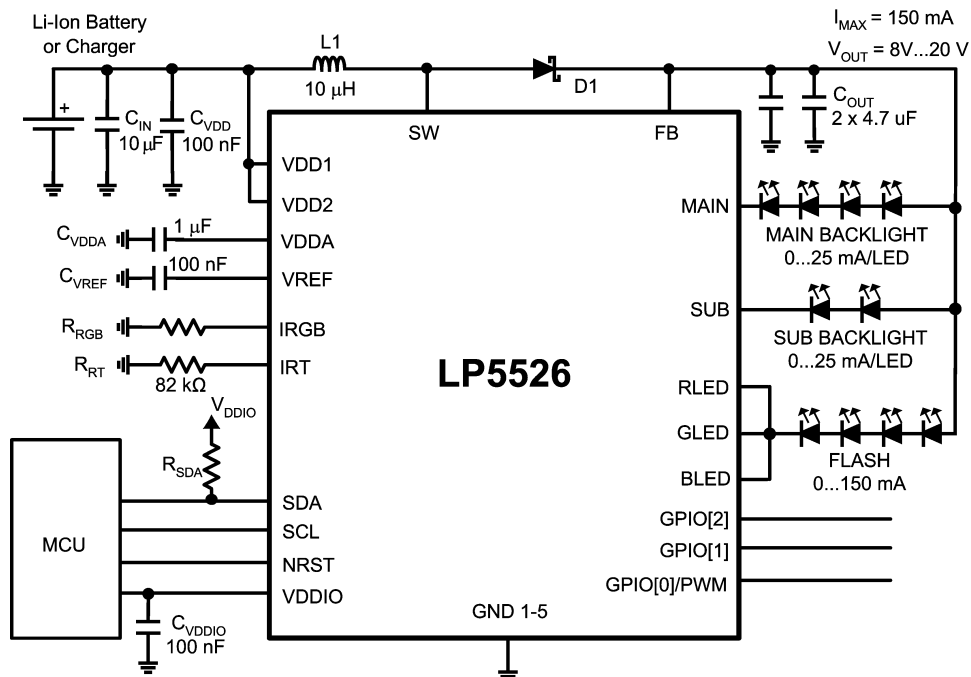
### Features

- High efficiency boost converter with programmable output voltage up to 20V
- 2 individual drivers for serial display backlight LEDs
- Automatic dimming controller
- Stand alone RGB controller
- Dedicated flash function
- Safety function to avoid prolonged flash
- 3 general purpose IO pins
- 25-bump micro SMD Package: (2.54mm x 2.54mm x 0.6mm)

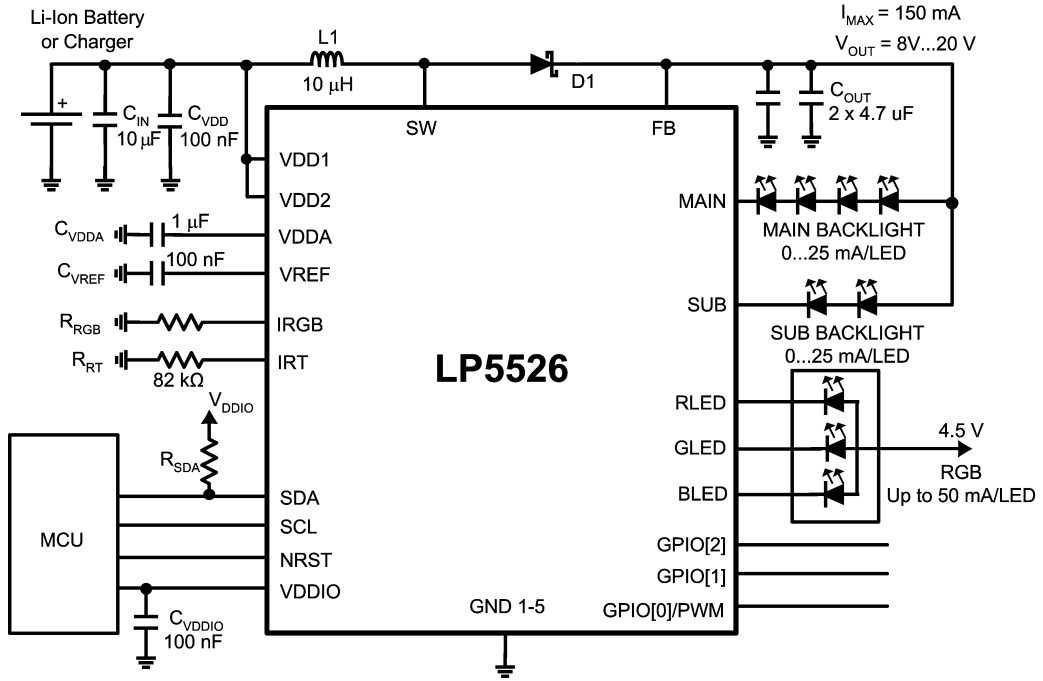
### Applications

- Cellular Phones and PDAs
- MP3 Players
- Digital Cameras

### Typical Application



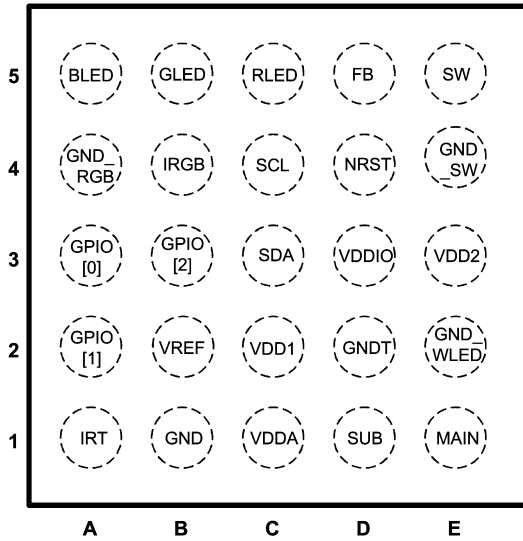
# Typical Application (Continued)



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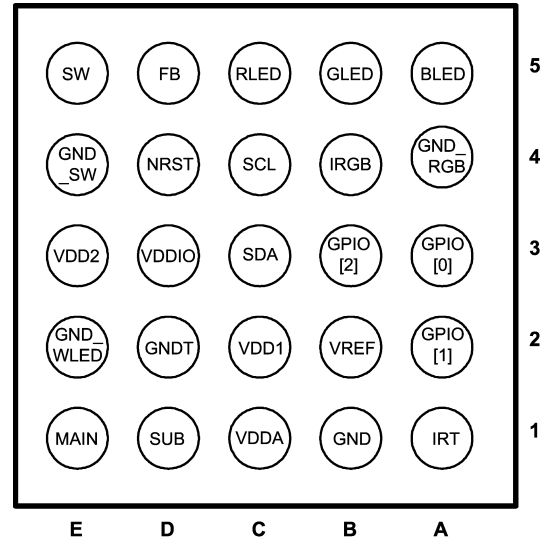
## Connection Diagrams

25-Bump Thin Micro SMD Package, Large Bump  
NS Package Number TLA25CCA



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Top View



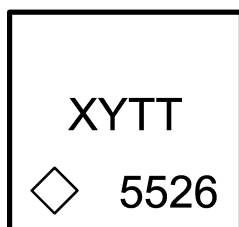
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Bottom View

## Pin Descriptions

Pin #	Name	Type	Description
5E	SW	Output	Boost Converter Power Switch
5D	FB	Input	Boost Converter Feedback
5C	RLED	Output	Red LED Output (Current Sink / Open Drain Switch)
5B	GLED	Output	Green LED Output (Current Sink / Open Drain Switch)
5A	BLED	Output	Blue LED Output (Current Sink / Open Drain Switch)
4E	GND_SW	Ground	Power Switch Ground
4D	NRST	Input	External Reset, Active Low
4C	SCL	Logic Input	Clock Input for I <sup>2</sup> C Compatible Interface
4B	IRGB	Input	External RGB LED Maximum Current Set Resistor
4A	GND_RGB	Ground	Ground for RGB LED Currents
3E	VDD2	Power	Supply Voltage 3.0...5.5 V
3D	VDDIO	Power	Supply Voltage for Digital Input/Output Buffers and Drivers
3C	SDA	Logic Input/Output	Data Input/Output for I <sup>2</sup> C Compatible Interface
3B	GPIO[2]	Logic Input/Output	General Purpose Logic Input/Output
3A	GPIO[0] / PWM	Logic Input/Output	General Purpose Logic Input/Output / External PWM Input
2E	GND_WLED	Ground	Ground for White LED Currents (MAIN and SUB Outputs)
2D	GNDT	Ground	Ground
2C	VDD1	Power	Supply Voltage 3.0...5.5 V
2B	VREF	Output	Reference Voltage (1.23V)
2A	GPIO[1]	Logic Input/Output	General Purpose Logic Input/Output
1E	MAIN	Output	MAIN Display White LED Current Output (Current Sink)
1D	SUB	Output	SUB Display White LED Current Output (Current Sink)
1C	VDDA	Output	Internal LDO Output (2.80V)
1B	GND	Ground	Ground for Core Circuitry
1A	IRT	Input	Oscillator Frequency Set Resistor

## Package Mark



XY = 2 Digit Date Code

TT = Die Traceability

5526 = Product Identification

◇ = Pin 1A

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## Ordering Information

Order Number	Package Marking	Supplied As	Spec/Flow
LP5526TL	5526	TNR 250	NoPb
LP5526TLX	5526	TNR 3000	NoPb

**Absolute Maximum Ratings** (Notes 1,

2)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

V (SW, FB, MAIN, SUB, RLED, GLED, BLED)	-0.3V to +23V
$V_{DD1}$ , $V_{DD2}$ , $V_{DDIO}$ , $V_{DDA}$	-0.3V to +6.0V
Voltage on $I_{RGB}$ , $I_{RT}$ , $V_{REF}$	-0.3V to $V_{DD1}+0.3V$ with 6.0V max
Voltage on Logic Pins	-0.3V to $V_{DDIO}+0.3V$ with 6.0V max
$I(V_{REF})$	10 $\mu$ A
$I(RLED, GLED, BLED)$	100mA
Continuous Power Dissipation (Note 3)	Internally Limited
Junction Temperature ( $T_{J-MAX}$ )	125°C
Storage Temperature Range	-65°C to +150°C
Maximum Lead Temperature (Soldering) (Note 4)	260°C
ESD Rating (Note 5)	
Human Body Model:	2kV
Machine Model:	200V

**Operating Ratings** (Notes 1, 2)

V (SW, FB, MAIN, SUB)	0 to +21V
$V_{DD1,2}$	3.0 to 5.5V
$V_{DDIO}$	1.65V to $V_{DD1}$
Recommended Load Current (RLED, GLED, BLED) CC Mode	0mA to 50mA/driver
Recommended Total Boost Converter Load Current	0mA to 150mA
Junction Temperature ( $T_J$ ) Range	-30°C to +125°C
Ambient Temperature ( $T_A$ ) Range (Note 6)	-30°C to +85°C

**Thermal Properties**

Junction-to-Ambient Thermal Resistance( $\theta_{JA}$ ), TLA25 Package (Note 7)	60 - 100°C/W
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## Electrical Characteristics (Notes 2, 8)

Limits in standard typeface are for  $T_J = 25^\circ\text{C}$ . Limits in **boldface** type apply over the operating ambient temperature range ( $-30^\circ\text{C} < T_A < +85^\circ\text{C}$ ). Unless otherwise noted, specifications apply to the LP5526 Block Diagram with:  $V_{DD1,2} = 3.0 \dots 5.5\text{V}$ ,  $C_{VDD} = C_{VDDIO} = 100\text{nF}$ ,  $C_{OUT} = 2 \times 4.7\mu\text{F}$ ,  $C_{IN} = 10\mu\text{F}$ ,  $C_{VDDA} = 1\mu\text{F}$ ,  $C_{VREF} = 100\text{nF}$ ,  $L1 = 10\mu\text{H}$ ,  $R_{RGB} = 2.4\text{k}\Omega$  and  $R_{RT} = 82\text{k}\Omega$  (Note 9).

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{VDD}$	Standby supply current ( $V_{DD1}, V_{DD2}$ )	NSTBY = L Register 0DH=08H (Note 10)		1.7	<b>7</b>	$\mu\text{A}$
	No-boost supply current ( $V_{DD1}, V_{DD2}$ )	NSTBY = H, EN_BOOST = L		300	<b>800</b>	$\mu\text{A}$
	No-load supply current ( $V_{DD1}, V_{DD2}$ )	NSTBY = H, EN_BOOST = H Autoload OFF		780	<b>1300</b>	$\mu\text{A}$
$V_{DDA}$	Output voltage of internal LDO	$I_{VDDA} = 1\text{mA}$		2.80		V
			<b>-3</b>		<b>+3</b>	%
$V_{REF}$	Reference voltage (Note 11)			1.23		V

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

**Note 2:** All voltages are with respect to the potential at the GND pins.

**Note 3:** Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at  $T_J=150^\circ\text{C}$  (typ.) and disengages at  $T_J=130^\circ\text{C}$  (typ.).

**Note 4:** For detailed soldering specifications and information, please refer to National Semiconductor Application Note AN1112 : Micro SMD Wafer Level Chip Scale Package

**Note 5:** The Human body model is a 100pF capacitor discharged through a 1.5k $\Omega$  resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin. MIL-STD-883 3015.7

**Note 6:** In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ( $T_{A-MAX}$ ) is dependent on the maximum operating junction temperature ( $T_{J-MAX-OP} = 125^\circ\text{C}$ ), the maximum power dissipation of the device in the application ( $P_{D-MAX}$ ), and the junction-to ambient thermal resistance of the part/package in the application ( $\theta_{JA}$ ), as given by the following equation:  $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$ .

**Note 7:** Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

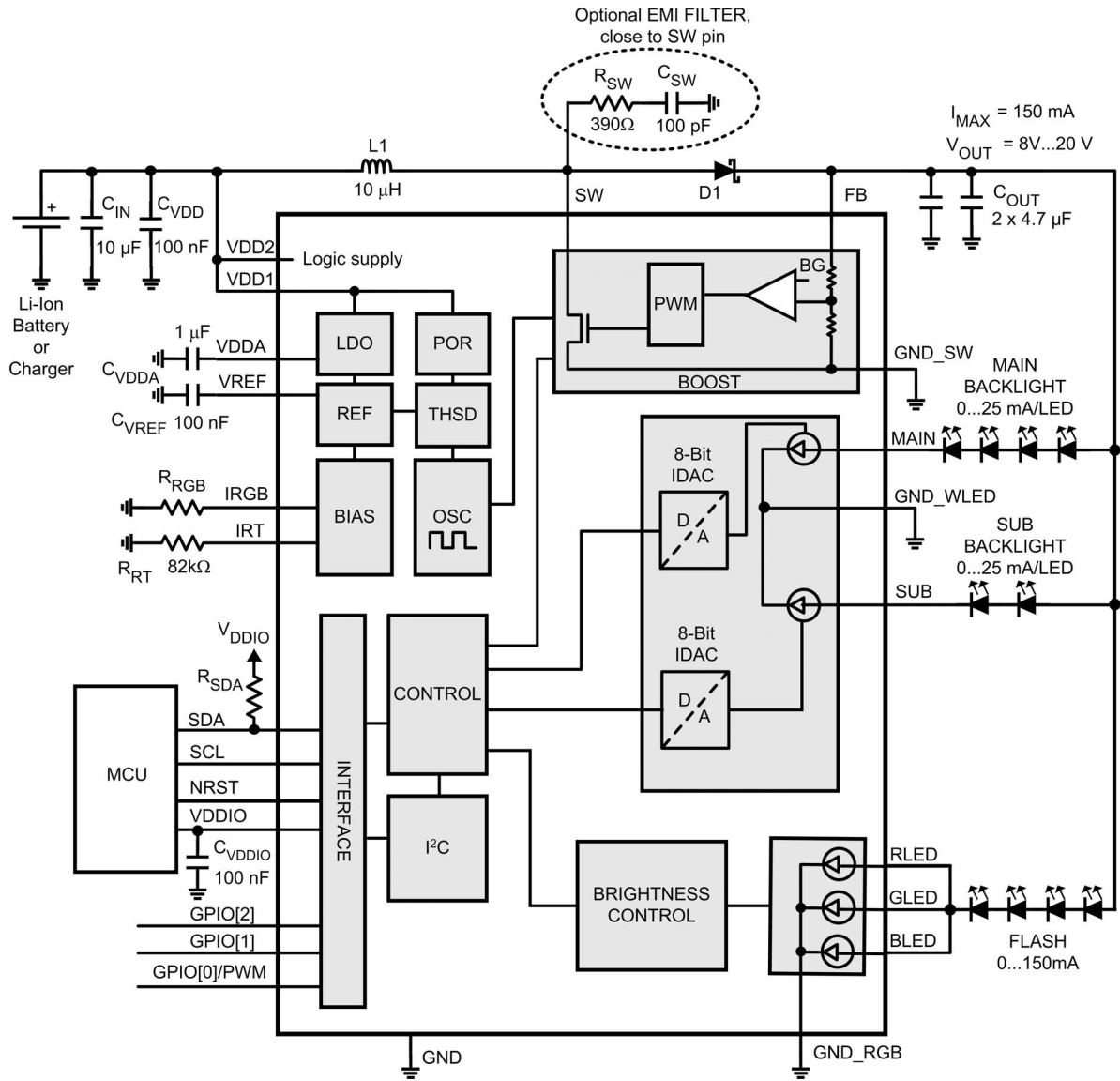
**Note 8:** Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.

**Note 9:** Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.

**Note 10:** Boost output voltage set to 8V (08H in register 0DH) to prevent any unnecessary current consumption.

**Note 11:** No external loading allowed for  $V_{REF}$  pin.

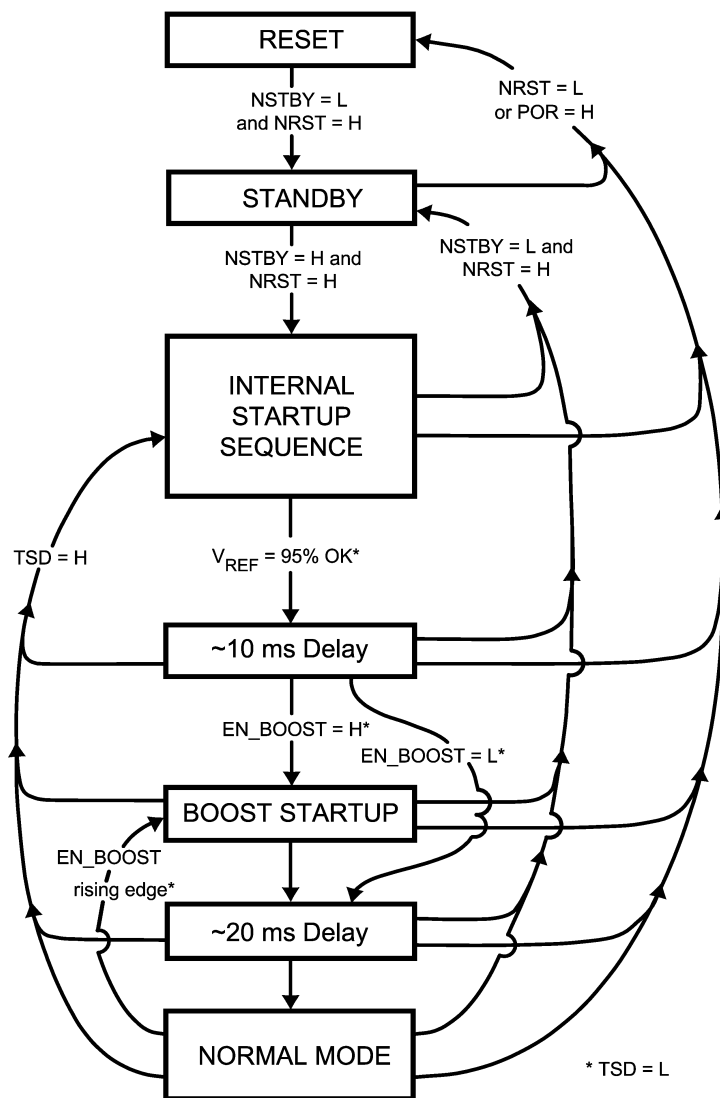
# Block Diagram



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## Modes of Operation

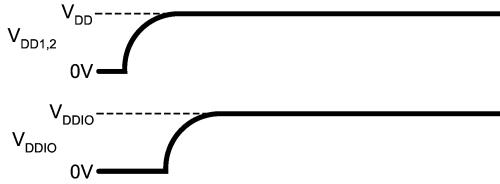
- RESET:** In the RESET mode all the internal registers are reset to the default values. Reset is entered always if input NRST is LOW or internal Power On Reset is active. Power On Reset (POR) will activate during the chip startup or when the supply voltages  $V_{DD1}$  and  $V_{DD2}$  fall below 1.5V. Once  $V_{DD1}$  and  $V_{DD2}$  rises above 1.5V, POR will inactivate and the chip will continue to the STANDBY mode. NSTBY control bit is low after POR by default.
- STANDBY:** The STANDBY mode is entered if the register bit NSTBY is LOW and Reset is not active. This is the low power consumption mode, when all circuit functions are disabled. Registers can be written in this mode and the control bits are effective immediately after start up.
- STARTUP:** When NSTBY bit is written high, the INTERNAL STARTUP SEQUENCE powers up all the needed internal blocks ( $V_{REF}$ , Bias, Oscillator etc.). To ensure the correct oscillator initialization, a 10ms delay is generated by the internal state-machine. If the chip temperature rises too high, the Thermal Shutdown (TSD) disables the chip operation and STARTUP mode is entered until no thermal shutdown event is present.
- BOOST STARTUP:** Soft start for boost output is generated in the BOOST STARTUP mode. The boost output is raised in low current PWM mode during the 20ms delay generated by the state-machine. All LED outputs are off during the 20ms delay to ensure smooth startup. The Boost startup is entered from Internal Startup Sequence if EN\_BOOST is HIGH or from Normal mode when EN\_BOOST is written HIGH.
- NORMAL:** During NORMAL mode the user controls the chip using the Control Registers. The registers can be written in any sequence and any number of bits can be altered in a register in one write.



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## Power-Up Sequence

When powering up the device,  $V_{DD1}$  and  $V_{DD2}$  should be greater than  $V_{DDIO}$  to prevent any damage to the device.



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## Magnetic Boost DC/DC Converter

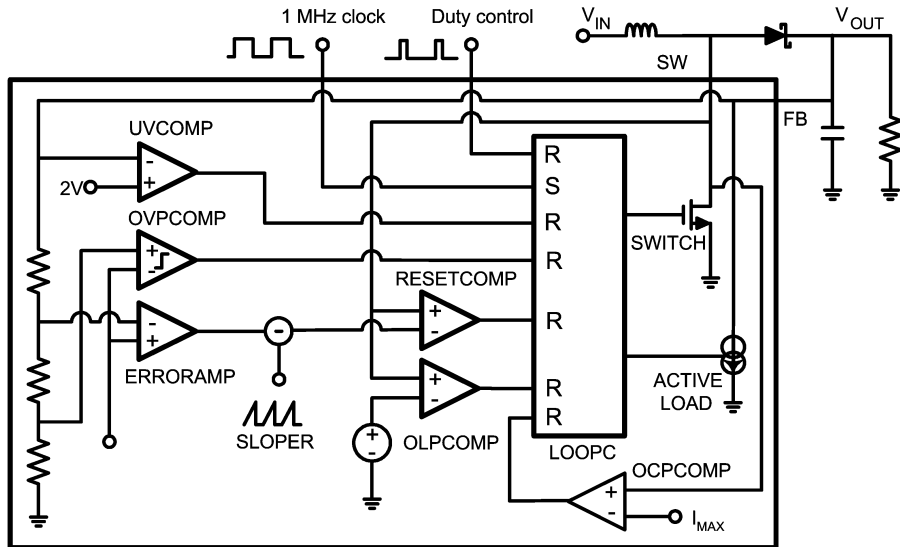
The LP5526 Boost DC/DC Converter generates an 8...20V supply voltage for the LEDs from single Li-Ion battery (3V...4.5V). The output voltage is controlled with an 8-bit register in 12 steps. The converter is a magnetic switching PWM mode DC/DC converter with a current limit. Switching frequency is 1MHz, when timing resistor  $R_T$  is 82k $\Omega$ . Timing resistor defines the internal oscillator frequency and thus directly affects boost frequency and RGB timings.

EMI filter ( $R_{SW}$  and  $C_{SW}$ ) on the SW pin can be used to suppress EMI caused by fast switching. These components should be as near as possible to the SW pin to ensure reliable operation. The LP5526 Boost Converter uses pulse-skipping elimination to stabilize the noise spectrum. Even with light load or no load a minimum length current pulse is fed to the inductor. An active load is used to remove the

excess charge from the output capacitor at very light loads. Active load can be disabled by writing the EN\_AUTOLOAD bit low. Disabling active load will increase slightly the efficiency at light loads, but the downside is that pulse skipping will occur. The Boost Converter should be stopped and set to 8V when there is no load to minimize the current consumption.

The topology of the magnetic boost converter is called CPM control, current programmed mode, where the inductor current is measured and controlled with the feedback. The user can program the output voltage of the boost converter. The output voltage control changes the resistor divider in the feedback loop. The following figure shows the boost topology with the protection circuitry. Four different protection schemes are implemented:

1. Over voltage protection, limits the maximum output voltage
  - Keeps the output below breakdown voltage.
  - Prevents boost operation if battery voltage is much higher than desired output.
2. Over current protection, limits the maximum inductor current
  - Voltage over switching NMOS is monitored; too high voltages turn the switch off.
3. Feedback break protection. Prevents uncontrolled operation if FB pin gets disconnected.
4. Duty cycle limiting, done with digital control.



Boost Converter Topology

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# Magnetic Boost DC/DC Converter (Continued)

## MAGNETIC BOOST DC/DC CONVERTER ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{LOAD}$	Maximum Non-Continuous Load Current	$3.0V \leq V_{IN} \leq 3.2V$ $V_{OUT} = 20V$			140	mA
		$3.2V < V_{IN}$ $V_{OUT} = 20V$			150	
$I_{LOAD}$	Maximum Continuous Load Current	$3.0V = V_{IN}$ $V_{OUT} = 20V$			100	
$V_{OUT}$	Output Voltage Accuracy (FB Pin)	$3.0V \leq V_{IN} \leq 5.5V$ $V_{OUT} = 20V$	-2.3 -1.7		+2.3 +1.7	%
$R_{DS(ON)}$	Switch ON Resistance	$I_{SW} = 0.5A$		0.15	0.3	$\Omega$
$f_{PWM}$	PWM Mode Switching Frequency	$RT = 82\text{ k}\Omega$		1.0		MHz
	Frequency Accuracy	$RT = 82\text{ k}\Omega$	-7 -9		+7 +9	%
$t_{PULSE}$	Switch Pulse Minimum Width	no load		45		ns
$t_{STARTUP}$	Startup Time	Boost startup from STANDBY to $V_{OUT} = 20V$ , no load		15		ms
$I_{MAX}$	SW Pin Current Limit			1500	1850	mA

**Note:** Maximum non-continuous currents rates as short pulses ( $t < 1s$ ). Exposure to maximum rating conditions for extended periods may affect device reliability.

### BOOST STANDBY MODE

User can set the Boost Converter to STANDBY mode by writing the register bit EN\_BOOST low. When EN\_BOOST is written high, the converter starts for 20ms in low current PWM mode and then goes to normal PWM mode. All LED outputs are off during the 20ms delay to ensure smooth startup.

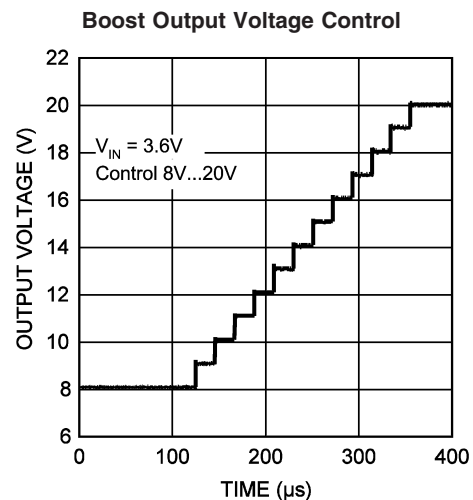
### BOOST OUTPUT VOLTAGE CONTROL

User can control the boost output voltage by Boost Output 8-bit register.

Boost Output [7:0] Register 0DH		Boost Output Voltage (typical)
Bin	Dec	
0000 1000	8	8.0V
0000 1001	9	9.0V
0000 1010	10	10.0V
0000 1011	11	11.0V
0000 1100	12	12.0V
0000 1101	13	13.0V
0000 1110	14	14.0V
0000 1111	15	15.0V
0001 0000	16	16.0V
0001 0001	17	17.0V
0001 0010	18	18.0V
0001 0011	19	19.0V
0001 0100	20	20.0V

If register value is lower than 8, then value of 8 is used internally.

If register value is higher than 20, then value of 20 is used internally.

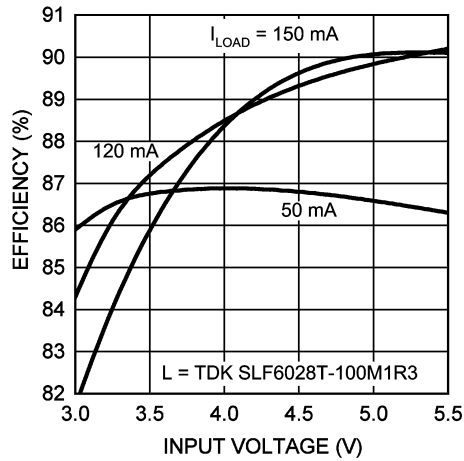


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# Boost Converter Typical Performance Characteristics

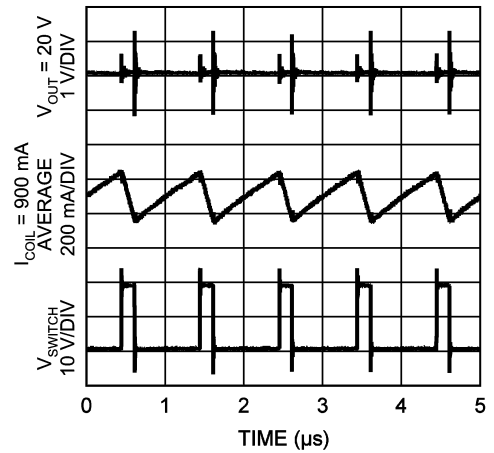
$V_{in} = 3.6V$ ,  $V_{out} = 20.0V$  if not otherwise stated

**Boost Converter Efficiency**



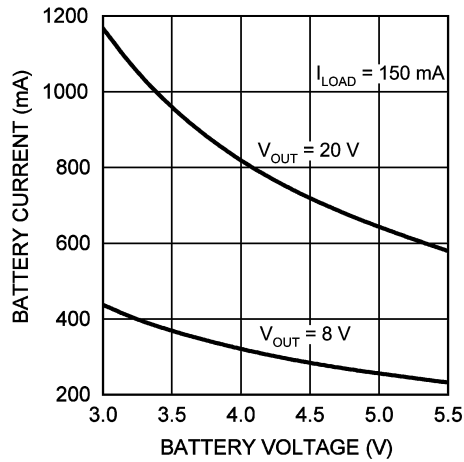
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**Boost Typical Waveforms at 150mA Load**



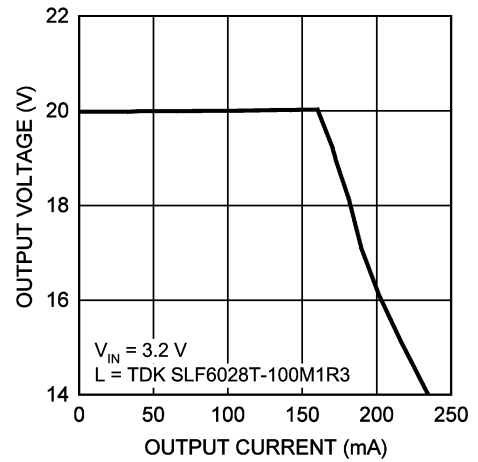
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**Battery Current vs Voltage**



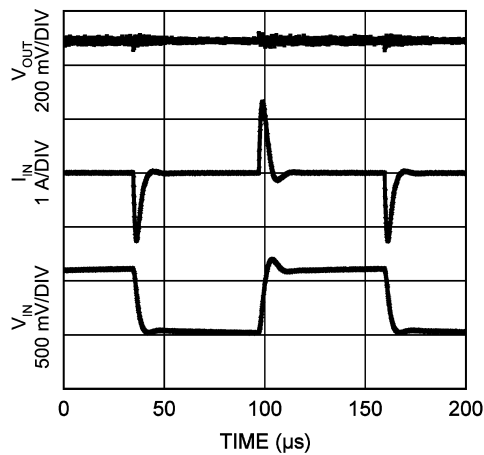
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**Boost Output Voltage vs. Current**



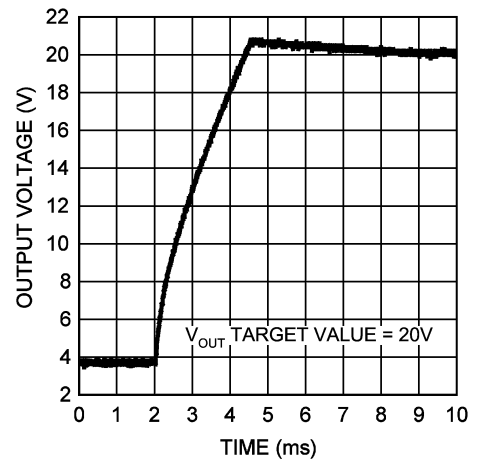
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**Boost Line Regulation 3.0V - 3.6V, no load**



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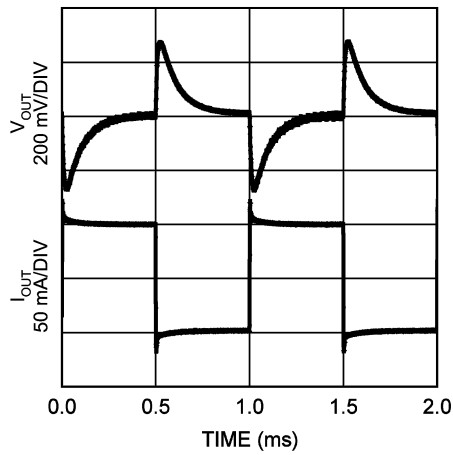
**Boost Turn On Time with No Load**



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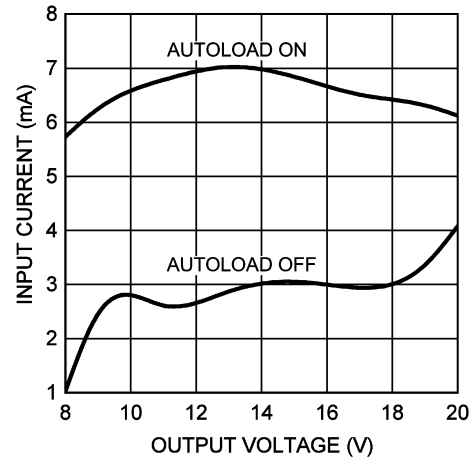
# Boost Converter Typical Performance Characteristics (Continued)

**Boost Load Transient Response 50mA – 150mA**



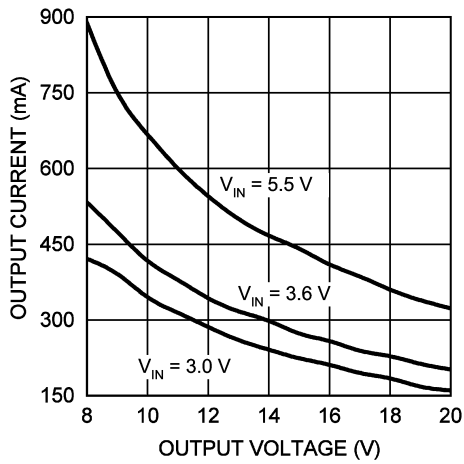
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**Autoload Effect on Input Current, No Load**



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**Boost Maximum Current vs. Output Voltage**



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## Functionality of Color LED Outputs (RLED, GLED, BLED)

LP5526 has one RGB/color LED output, consisting of three individual LED output pins. Output pins can be used in switch mode or constant current mode. Output mode can be selected with the control register (address 00H) bit CC\_SW. If the bit is set high, then RGB outputs are in switch mode, otherwise in constant current mode. These modes are described later in separate chapters.

RGB LED output control can be done in three ways:

1. Defining the expected color and brightness with internal PWM in RGB register (address 01H)
2. Direct setting each LED ON/OFF via RGB Control register (address 00H)
3. External PWM control

### 1. BRIGHTNESS CONTROL WITH RGB REGISTER

If the RGB LED output is used by defining the balance and brightness in the RGB register, then one needs to set EN\_RGB bit high and RGB\_PWM bit high in the Control register (address 00H). RSW, GSW and BSW are used to enable each LED output, enabled when written high. CC\_SW defines the LED output mode. A single register is used for defining the color and brightness for the RGB LED output. OVL bit selects overlapping/non-overlapping mode. Overlapping mode is selected when OVL = 1.

CONTROL REGISTER (00H)		
Name	Bit	Description
RGB_PWM	7	0 = Internal PWM control disabled 1 = Internal PWM control enabled
EN_RGB	6	0 = RGB outputs disabled 1 = RGB outputs enabled
CC_SW	5	0 = Constant current sink mode 1 = Switch mode
RSW	3	0 = RLED disabled 1 = RLED enabled
GSW	2	0 = GLED disabled 1 = GLED enabled
BSW	1	0 = BLED disabled 1 = BLED enabled
RGB REGISTER (01H)		
COLOR[3:0]	7:4	Color for RGB LED output
BRIGHT[2:0]	3:1	Brightness control
OVL	0	0 = Non-overlapping mode 1 = Overlapping mode

Brightness control is logarithmic and is programmed as follows:

Bright[2:0]	Brightness [%]	Ratio to max brightness
000	0	0
001	1.56	1/64
010	3.12	1/32
011	6.25	1/16
100	12.5	1/8
101	25	1/4
110	50	1/2
111	100	1/1

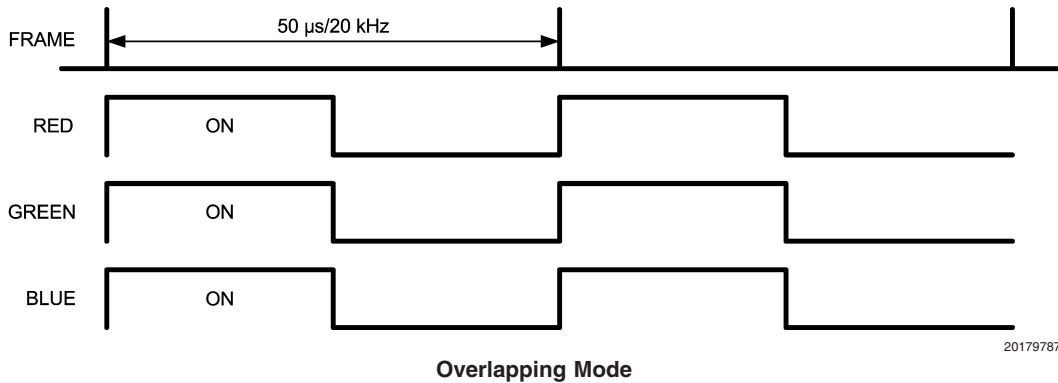
16 colors can be selected as follows. Please note that exact color depends on RGB LED current and type. Color setting is valid only in non-overlapping mode.

COLOR[3:0]	RED active [%]	GREEN active [%]	BLUE active [%]	RGB COLOR
0000	100	0	0	red
0001	0	100	0	green
0010	0	0	100	blue
0011	50	50	0	yellow
0100	0	50	50	cyan
0101	50	0	50	magenta
0110	33	33	33	white
0111	50	25	25	pink
1000	25	50	25	light green
1001	25	50	25	light blue
1010	25	25	50	orange
1011	75	25	0	deep pink
1100	0	75	25	spring green
1101	25	75	0	lawn green
1110	0	25	75	sky blue
1111	25	0	75	indigo

## Functionality of Color LED Outputs (RLED, GLED, BLED) (Continued)

### Overlapping Mode

In overlapping mode the brightness is controlled using PWM duty cycle based control method as the following figure shows.

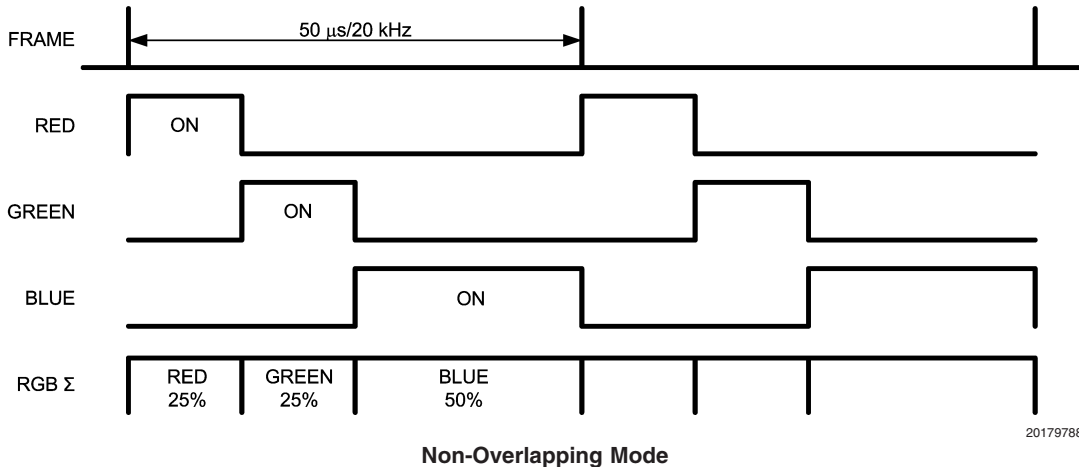


Since RGB outputs are on simultaneously, the maximum load peak current is:

$$I_{MAX} = I(RLED)_{MAX} + I(GLED)_{MAX} + I(BLED)_{MAX}$$

### Non-Overlapping Mode

The timing diagram shows the splitted R, G and B and brightness control effect to splitted parts. Full brightness is used in the diagram. If for example 1/2 brightness is used, the frame is still 50μs, but all LED outputs' ON time is 50% shorter and at the last 25μs all LED outputs are OFF.



The non-overlapping mode has 16 programmed colors (different R, G and B ratio -> different color). Since the R, G and B are split in to non-overlapping slots the output current through the RGB LED can be calculated with following equation:

$$I_{AVG} = (C_R \times I_R + C_G \times I_G + C_B \times I_B) \times B$$

where

C = Color [%] (see table of color control)

B = Brightness [%] (see table of brightness control)

### 2. LED ON/OFF CONTROL WITH RGB CONTROL REGISTER

Each LED output can be set ON by writing the corresponding bit high in the Control register (00H). RSW controls RLED, GSW controls GLED and BSW controls BLED output. Note that EN\_RGB bit must be high and RGB\_PWM bit low. In this mode, the RGB register (01H) does not have any effect. CC\_SW bit in Control register defines the LED output mode.

## Functionality of Color LED Outputs (RLED, GLED, BLED)

(Continued)

### Switch Mode / Constant Current Mode

Each RGB LED output can be set to act as a switch or a constant current sink. Selection of mode is done with the CC\_SW bit in the Control Register. If bit is set high, then the switch mode is selected. Default is switch mode.

### SWITCH MODE

In switch mode, the RGB LED outputs are low ohmic switches to ground. Resistance is typically  $3.2\Omega$ . **External ballast resistors must be used to limit the current through the LED.**

### CONSTANT CURRENT MODE

In constant current mode, the maximum output current is defined with a single external resistor ( $R_{RGB}$ ) and the maximum current control register (address 02H).

RGB MAX CURRENT REGISTER (02H)		
Name	Bit	Description
IR[1:0]	5:4	RLED maximum current
IG[1:0]	3:2	GLED maximum current
IB[1:0]	1:0	BLED maximum current

Maximum current for each LED output is adjusted with the RGB max current register in following way:

IR[1:0], IG[1:0], IB[1:0]	Maximum current / output
00	$0.25 \times I_{MAX}$
01	$0.50 \times I_{MAX}$
10	$0.75 \times I_{MAX}$
11	$1.00 \times I_{MAX}$

External ballast resistors are not needed in this mode. The maximum current for all RGB LED drivers is set with  $R_{RGB}$ . The equation for calculating the maximum current is:

$$I_{MAX} = 100 \times 1.23V / (R_{RGB} + 50 \Omega)$$

where

$I_{MAX}$  = maximum RGB current in any RGB output (during constant current mode)

1.23V = reference voltage

100 = internal current mirror multiplier

$R_{RGB}$  = resistor value in Ohms

$50 \Omega$  = Internal resistor in the  $I_{RGB}$  input

Table with example resistance values and corresponding output currents:

RGB resistor $R_{RGB}$ (k $\Omega$ )	Maximum current / output $I_{MAX}$ (mA)
2.4	50.2
2.7	44.7
3.0	40.3
3.3	36.7
3.6	33.7
3.9	31.1
4.3	28.3
4.7	25.9
5.1	23.9
5.6	21.8
6.2	19.7

Note that the LED output requires a minimum saturation voltage in order to act as a true constant current sink. The saturation voltage minimum is typically 230mV defined with 10% current drop. If the LED output voltage drops below 230mV, then the current will decrease significantly.

### 3. EXTERNAL PWM CONTROL

The GPIO[0]/PWM pin can be used to control the RGB output brightness or set RGB leds on/off. PWM function for the pin is selected by writing EN\_PWM\_PIN high in GPIO control register (address 06H). Note, that EN\_RGB bit must be set high. Each LED output can be enabled with RSW, GSW and BSW bits. EN\_EXT\_R\_PWM, EN\_EXT\_G\_PWM and EN\_EXT\_B\_PWM bits are used to select, which LED outputs are controlled with the external PWM input. Note that polarity of external PWM control is active high i.e. when pin is in high state, then LED output is enabled. If RGB\_PWM is set low, then each selected LED output is controlled directly with external PWM input. If RGB\_PWM is set high, then internal PWM control is modulated by the external PWM input. In latter case, internal PWM control is passed to LED when external PWM input is high.

## Functionality of Color LED Outputs (RLED, GLED, BLED)

(Continued)

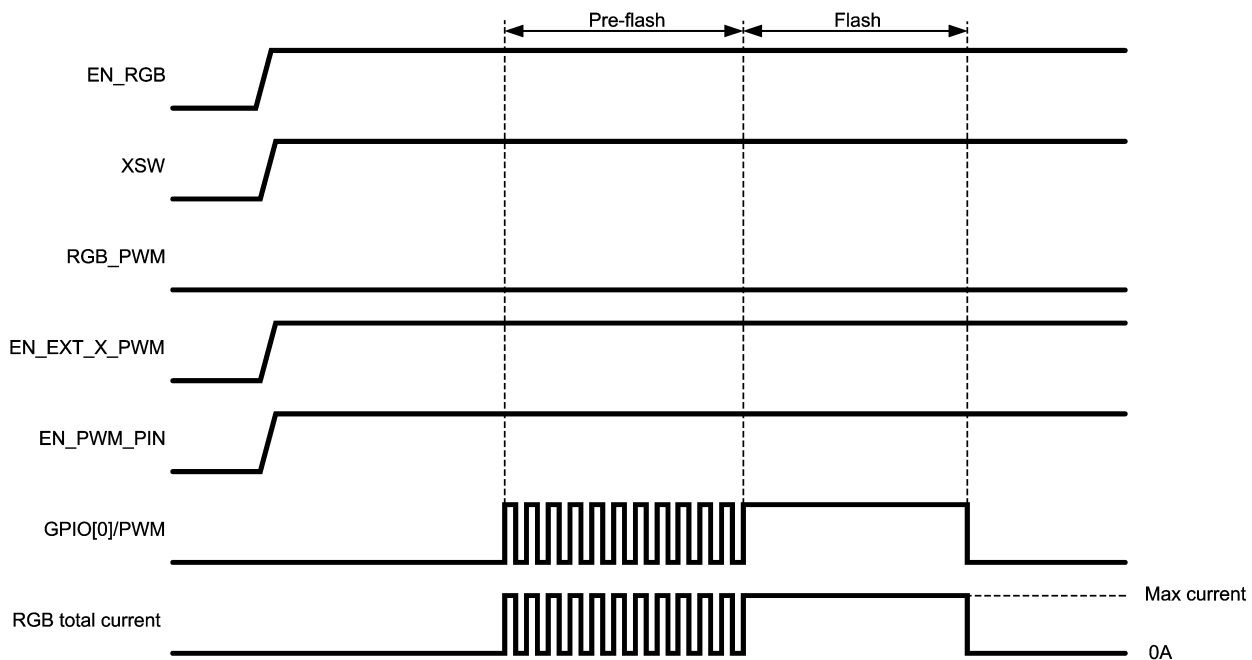
### FLASH LED DRIVING USING RGB DRIVERS

RGB drivers can be connected in parallel and used as a flash LED driver (see Typical application 2). Flash LEDs can be powered through the boost converter. Flash LEDs are controlled basically the same way as RGB LEDs controlling is previously described. Additional safety mode is introduced for FLASH LED driving to avoid prolonged flash and damage to application. FLASH can be done in 3 different ways:

1. Using external PWM control
2. Controlling RGB max current register values
3. Using Flash mode

#### 1. Using External PWM control

In this case pre-flash brightness is adjusted by adjusting the pulse width of PWM signal



Using External PWM Control for Flash

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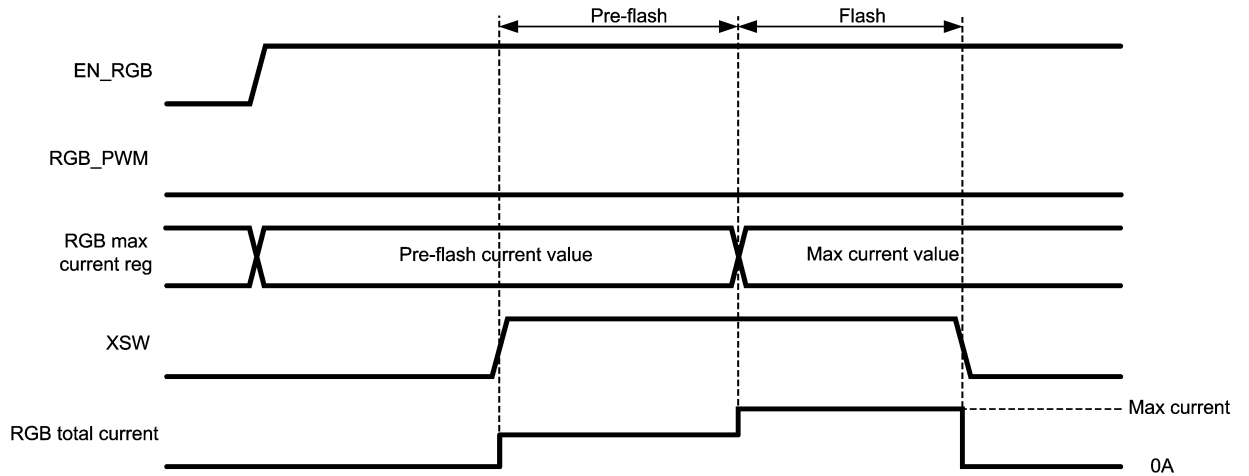
- Enable external PWM pin by writing EN\_PWM\_PIN bit high
- Use EN\_EXT\_R\_PWM, EN\_EXT\_G\_PWM and EN\_EXT\_B\_PWM bits to select, which LED outputs are controlled by the external PWM control. Output which external PWM control is not selected will be on constantly regardless of the state of the external PWM pin.
- Enable RGB constant current mode, if external ballast resistors are not used (CC\_SW = 0)
- Disable internal RGB PWM mode (RGB\_PWM = 0)
- Write wanted maximum current values for each output to RGB max current register (e.g. 11b for maximum current)
- Enable RGB functions (EN\_RGB = 1, RSW = 1, GSW = 1, BSW = 1)
- Use external PWM control pin (GPIO[0]/PWM) to introduce pre-flash and flash.

#### 2. Controlling RGB Max Current Register Values

In this case pre-flash brightness is adjusted by adjusting the current values in the RGB max current register. Note that in this mode flash control speed and timing depends on the I<sup>2</sup>C communication speed.

- Enable RGB functions and disable PWM mode (EN\_RGB = 1, RGB\_PWM = 0)
- Enable RGB constant current mode (CC\_SW = 0)
- Write pre-flash values for each output to RGB max current register (e.g. 00b for 25% of maximum current)
- Start pre-flash by switching on the LEDs (RSW = 1, GSW = 1, BSW = 1). Pre-flash brightness can be adjusted also by setting on only one or two LEDs during the pre-flash
- Start flash by writing each output maximum current values to RGB max current register
- Stop flash by switching off the LEDs (RSW = 0, GSW = 0, BSW = 0)

# Functionality of Color LED Outputs (RLED, GLED, BLED) (Continued)



Controlling RGB Max Current Values to Introduce Flash

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## Functionality of Color LED Outputs (RLED, GLED, BLED)

(Continued)

When RLED, GLED and BLED are connected together as in Typical Application 1, flash current can be adjusted with 8.33% step in constant current mode by changing RGB max current register values as seen on following table. Note that 0% means that appropriate output is turned off by setting RSW, GSW or BSW bit to 0.

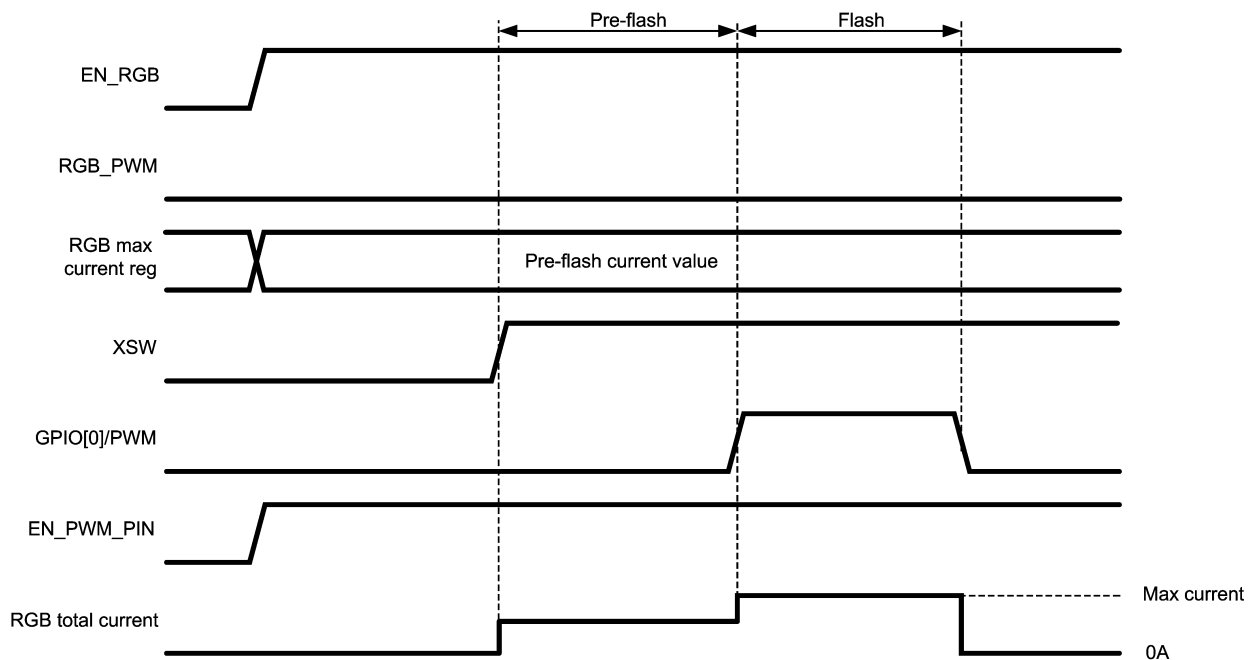
$I_R$ [%]	$I_G$ [%]	$I_B$ [%]	Total current [%]
0	0	25	8.33
0	0	50	16.67
0	0	75	25.00
0	0	100	33.33
0	25	100	41.67
0	50	100	50.00
0	75	100	58.33
0	100	100	66.67
25	100	100	75.00
50	100	100	83.33
75	100	100	91.67
100	100	100	100

### 3. Using Flash Mode

In this mode Flash is triggered with external PWM pin and pre-flash brightness is adjusted by adjusting the RGB max current values. After flash pulse flash led will be shut down.

- Write the pre-flash current values to RGB max current register
- Enable RGB functions and disable PWM mode (EN\_RGB = 1, RGB\_PWM = 0)
- Enable flash mode (EN\_FLASH = 1), make sure GPIO[0]/PWM pin is in low state
- Enable external PWM pin (EN\_PWM\_PIN = 1)
- Start pre-flash by switching on the LEDs (RSW = 1, GSW = 1, BSW = 1). Pre-flash brightness can be affected also by setting on only one or two LEDs
- Use EN\_EXT\_R\_PWM, EN\_EXT\_G\_PWM and EN\_EXT\_B\_PWM bits to select which LED outputs are used for flash
- Start flash pulse by setting GPIO[0]/PWM pin high and stop it by setting GPIO[0]/PWM pin low
- During the flash pulse the LED outputs with EN\_EXT\_x\_PWM bit enabled give out maximum current, regardless of RGB max current register value or XSW values

Note: EN\_FLASH bit must be set low, and then high again before it is possible to make a new flash pulse.



# Functionality of Color LED Outputs (RLED, GLED, BLED)

(Continued)

## FLASH SAFETY TIMER FUNCTION

Flash safety function can be used to prevent damages due to possible overheating when flash or RGB LEDs have been stuck on because of software or user error. Safety function has two operation modes:

1. Disabling selected RGB drivers when no writing has been done to the RGB max current register (address 02H) for 1 second
2. Disabling selected RGB drivers if the external flash trigger pulse is longer than 1 second

Flash safety function can be individually enabled for all RGB LED drivers (EN\_SAFETY\_R, EN\_SAFETY\_G, EN\_SAFETY\_B). The safety function operation mode depends on the state of EN\_FLASH bit.

1. EN\_FLASH = 0: Safety counter starts counting when at least one of the EN\_SAFETY\_X bits is enabled. Safety counter can be cleared by executing an I<sup>2</sup>C read or write sequence to address 02H. If safety counter reaches one second, the LEDs which have the safety function enabled, are switched off. Also the read-only bit SAFETY\_SET is set high.
2. EN\_FLASH = 1: Safety counter starts counting when the external flash trigger pulse starts (GPIO[0]/PWM goes high) and stops counting when flash pulse stops (GPIO[0]/PWM goes low). If flash pulse is longer than one second, the LEDs which have the safety function enabled, are switched off. Also the read-only bit SAFETY\_SET is set high.

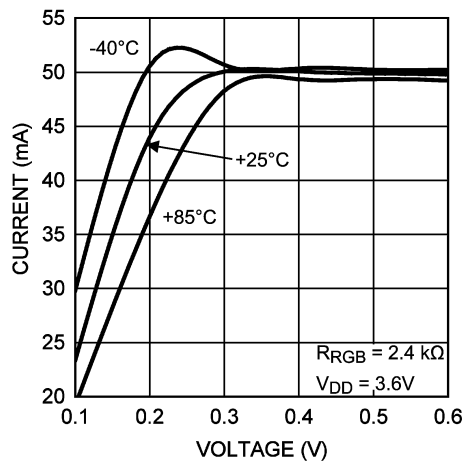
In both cases (EN\_FLASH = 0/1) after one second is reached and the LEDs which safety bit has been enabled are switched off, the LED state can be restored by disabling the safety function of the corresponding LED. Counter can be cleared only by disabling all safety bits (EN\_SAFETY\_R = 0, EN\_SAFETY\_G = 0, EN\_SAFETY\_B = 0), I<sup>2</sup>C read or write sequence to address 02H does not clear the counter when safety function has been activated.

## RGB LEDs Driver Performance Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I <sub>LEAKAGE</sub>	RLED, GLED, BLED pin leakage current				1	μA
I <sub>MAX(RGB)</sub>	Maximum recommended sink current	CC mode			50	mA
		SW mode			60	mA
	Accuracy @ 50mA	CC mode		5	12.5	%
	Current mirror ratio	CC mode		1:100		
	RGB current matching error	I <sub>RGB</sub> set to 50mA, CC mode		2		%
R <sub>SW</sub>	Switch resistance	SW mode		3.2		Ω
f <sub>RGB</sub>	RGB internal PMW switching frequency	Accuracy same as internal clock frequency accuracy		20		kHz
V <sub>SAT</sub>	Saturation voltage (current drop 10%)	+25°C, I <sub>RGB</sub> set to 50mA -30°C +85°C		230	350 300 430	mV

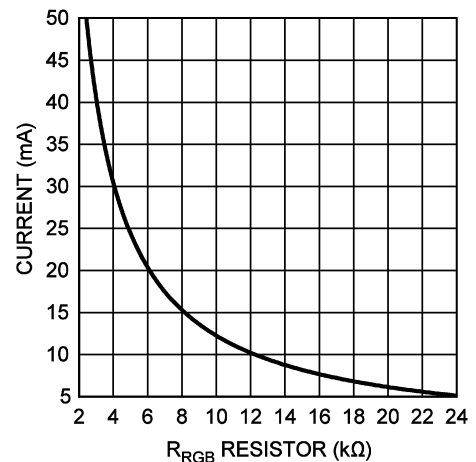
**Note:** RGB current should be limited as follows:  
**constant current mode** – limited by external R<sub>RGB</sub> resistor  
**switch mode** – limited by external ballast resistors

Output Current vs Pin Voltage (CC Mode)



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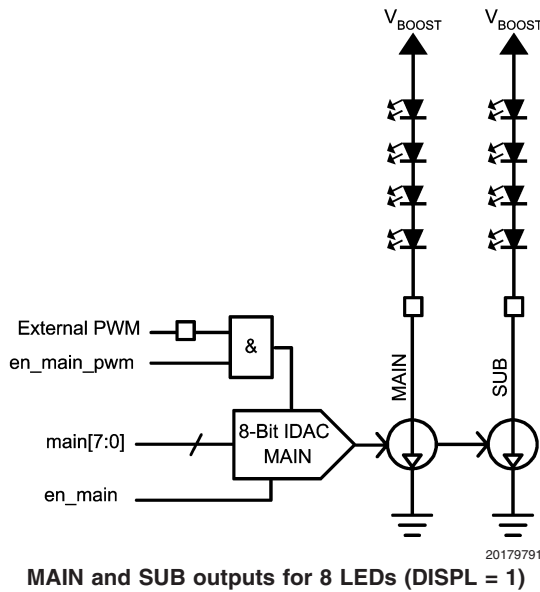
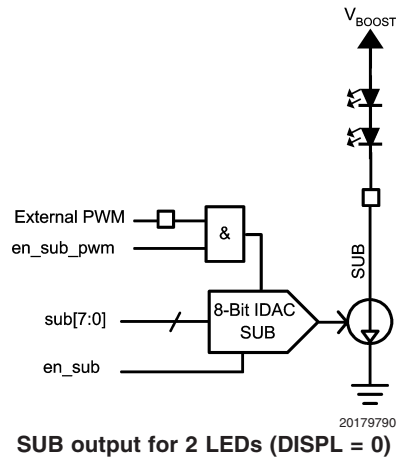
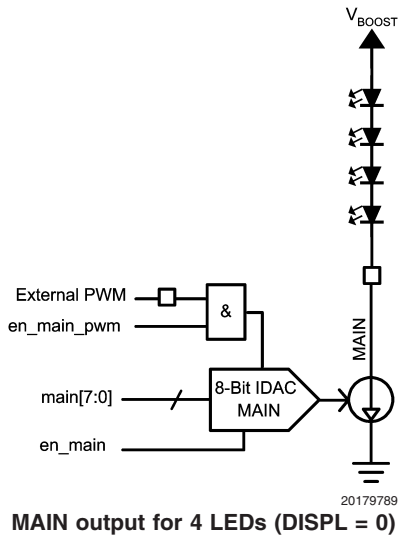
Output Current vs R<sub>RGB</sub> (CC Mode)



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## Backlight Drivers

LP5526 has 2 independent backlight drivers. Both drivers are regulated constant current sinks. LED current for both LED strings are controlled by the 8-bit current mode DACs with 0.1 mA step. MAIN and SUB LEDs can be also controlled with one DAC (MAIN) for better matching allowing the use of larger displays having up to 8 white LEDs by setting DISPL bit to 1.



### EXTERNAL PWM CONTROL

The GPIO[0]/PWM pin can be used to control the backlight drivers brightness or set leds on/off. External PWM control is enabled by writing 1 to EN\_MAIN\_PWM and/or EN\_SUB\_PWM bits in register address 2BH. GPIO[0]/PWM pin is used as external PWM input when EN\_PWM\_PIN is set high. PWM input is active high, i.e. LED is activated when in high state.

## Backlight Drivers (Continued)

### FADE IN / FADE OUT

LP5526 has an automatic fade in and out for main and sub backlight. The fade function is enabled with EN\_FADE bit. The slope of the fade curve is set by the SLOPE bit. Fade control for main and sub display is set by FADE\_SEL bit.

Recommended fading sequence:

1. Set SLOPE
2. Set FADE\_SEL
3. Set EN\_FADE = 1
4. Set EN\_MAIN / EN\_SUB = 1
5. Set target WLED value
6. Fading will be done either within 0.65s or 1.3s based on SLOPE selection

Fading times apply to full scale change i.e. from 0 to 100% or vice versa. If the current change does not correspond to full scale change, the time will be respectively shorter. See WLED Dimming diagrams for typical fade times.

WLED CONTROL REGISTER (03H)		
Name	Bit	Description
SLOPE	5	FADE execution time: 0 = 1.3s (full scale) 1 = 0.65s (full scale)
FADE_SEL	4	FADE selection: 0 = FADE controls MAIN 1 = FADE controls SUB
EN_FADE	3	FADE enable 0 = FADE disabled 1 = FADE enabled
DISPL	2	Display mode: 0 = MAIN and SUB individual control 1 = MAIN and SUB controlled with MAIN DAC
EN_MAIN	1	MAIN enable: 0 = disable 1 = enable
EN_SUB	0	SUB enable: 0 = disable 1 = enable

**Note:** if DISPL=1 and FADE\_SEL=0 then FADE effects MAIN and SUB

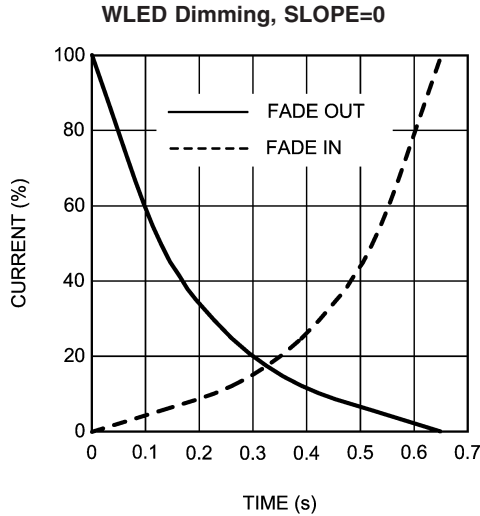
Adjustment is made with 04H (main current) and with 05H (sub current) registers:

MAIN CURRENT [7:0] SUB CURRENT [7:0]	Driver current, mA (typical)
0000 0000	0
0000 0001	0.1
0000 0010	0.2
0000 0011	0.3
...	...
...	...
1111 1101	25.3
1111 1110	25.4
1111 1111	25.5

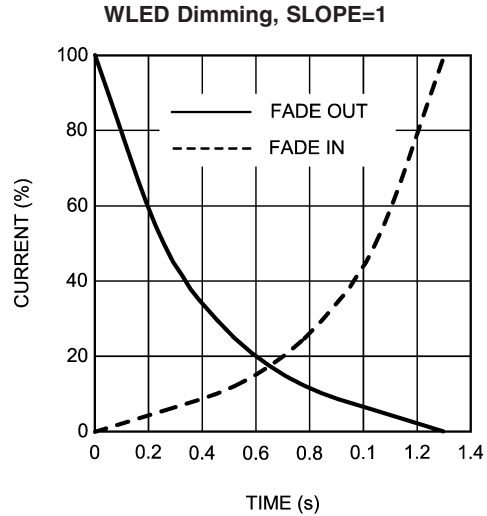
# Backlight Driver Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typical	Max	Units
$I_{MAX}$	Maximum Sink Current			25.5	<b>30</b>	mA
$I_{LEAKAGE}$	Leakage Current	$V_{SUB, MAIN} = 20V$		0.003	<b>1</b>	$\mu A$
$I_{MAIN}$ $I_{SUB}$	MAIN Current tolerance SUB Current tolerance	$I_{MAIN}$ and $I_{SUB}$ set to 12.8mA (80H)	<b>11.1</b>	12.8	<b>14.1</b>	%
$Match_{MAIN-SUB}$	Sink Current Matching Error	$I_{SINK}=12.8mA$ , DISPL=1		0.2		%
$Match_{MAIN-SUB}$	Sink Current Matching Error	$I_{SINK}=12.8mA$ , DISPL=0		5		%
$V_{SAT}$	95% Saturation Voltage	$I_{SINK}=25.5mA$		400	500 <b>650</b>	mV

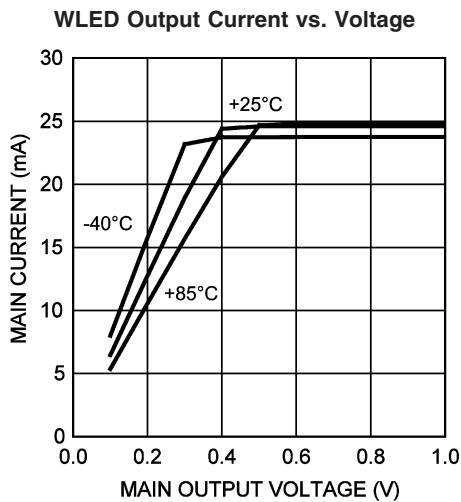
**Note:** Matching is the maximum difference from the average.



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## General Purpose I/O Functionality

LP5526 has three general purpose I/O pins: GPIO[0]/PWM, GPIO[1] and GPIO[2]. GPIO[0]/PWM can also be used as a PWM input for the external LED PWM controlling. GPIO bi-directional drivers are operating from the  $V_{DDIO}$  supply domain.

Registers for GPIO are as follows:

GPIO CONTROL (06H)		
Name	Bit	Description
EN_PWM_PIN	4	Enable PWM pin 0 = disable 1 = enable
OEN[2:0]	2:0	GPIO pin direction 0 = input 1 = output

## Logic Interface Characteristics

( $V_{DDIO} = 1.65V \dots V_{DD1,2}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>LOGIC INPUT SCL, SDA, GPIO[0:2]</b>						
$V_{IL}$	Input Low Level				$0.2xV_{DDIO}$	V
$V_{IH}$	Input High Level		$0.8xV_{DDIO}$			V
$I_I$	Logic Input Current		-1.0		1.0	$\mu A$
$f_{SCL}$	Clock Frequency				400	kHz
<b>LOGIC INPUT NRST</b>						
$V_{IL}$	Input Low Level				0.5	V
$V_{IH}$	Input High Level		1.2			V
$I_I$	Input Current		-1.0		1.0	$\mu A$
$t_{NRST}$	Reset Pulse Width		10			$\mu s$
<b>LOGIC OUTPUT SDA</b>						
$V_{OL}$	Output Low Level	$I_{SDA} = 3mA$		0.3	0.5	V
$V_{OH}$	Output High Level	$I_{SDA} = -3mA$	$V_{DDIO} - 0.5$	$V_{DDIO} - 0.3$		
$I_L$	Output Leakage Current	$V_{SDA} = 2.8V$			1.0	$\mu A$
<b>LOGIC OUTPUT GPIO[0:2]</b>						
$V_{OL}$	Output Low Level	$I_{GPIO} = 3 mA$		0.3	0.5	V
$V_{OH}$	Output High Level	$I_{GPIO} = -3 mA$	$V_{DDIO} - 0.5$	$V_{DDIO} - 0.3$		V
$I_L$	Output Leakage Current	$V_{GPIO} = 2.8V$			1.0	$\mu A$

GPIO DATA (07H)		
Name	Bit	Description
DATA[2:0]	2:0	Data bits

GPIO control register is used to set the direction of each GPIO pin. For example, by setting OEN0 bit high the GPIO[0]/PWM pin acts as a logic output pin with data defined DATA0 in GPIO data register. Note, that the EN\_PWM\_PIN bit overrides OEN0 state by forcing GPIO[0]/PWM to act as PWM input. GPIO[1] and GPIO[2] pins can be selected to be inputs or outputs, defined by OEN1 and OEN2 bit status. PWM functionality is valid only for GPIO[0]/PWM pin. GPIO data register contains the data of GPIO pins. When output direction is selected to GPIO pin, then GPIO data register defines the output pin state. When GPIO data register is read, it contains the state of the pin despite of the pin direction.

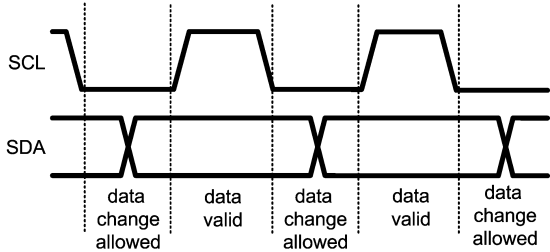
# I<sup>2</sup>C Compatible Interface

## I<sup>2</sup>C SIGNALS

The SCL pin is used for the I<sup>2</sup>C clock and the SDA pin is used for bidirectional data transfer. Both these signals need a pull-up resistor according to I<sup>2</sup>C specification.

## I<sup>2</sup>C DATA VALIDITY

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when CLK is LOW.

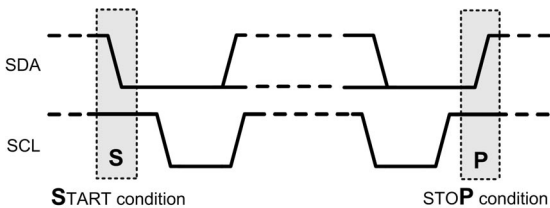


I<sup>2</sup>C Signals: Data Validity

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## I<sup>2</sup>C START AND STOP CONDITIONS

START and STOP bits classify the beginning and the end of the I<sup>2</sup>C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I<sup>2</sup>C master always generates START and STOP bits. The I<sup>2</sup>C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I<sup>2</sup>C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.



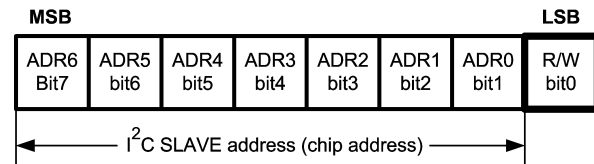
I<sup>2</sup>C Start and Stop Conditions

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## TRANSFERRING DATA

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9<sup>th</sup> clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received.

After the START condition, the I<sup>2</sup>C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LP5526 address is 59H (101 1001b). For the eighth bit, a "0" indicates a WRITE and a "1" indicates a READ. This means that the first byte is B2H for WRITE and B3H for READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

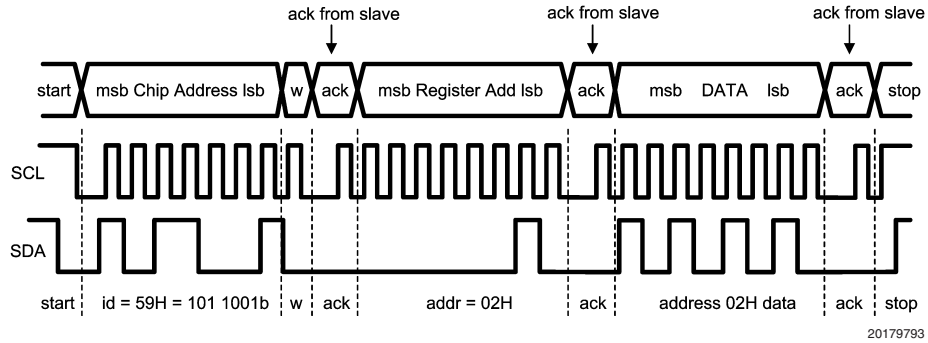


I<sup>2</sup>C Chip Address

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Register changes take an effect at the SCL rising edge during the last ACK from slave.

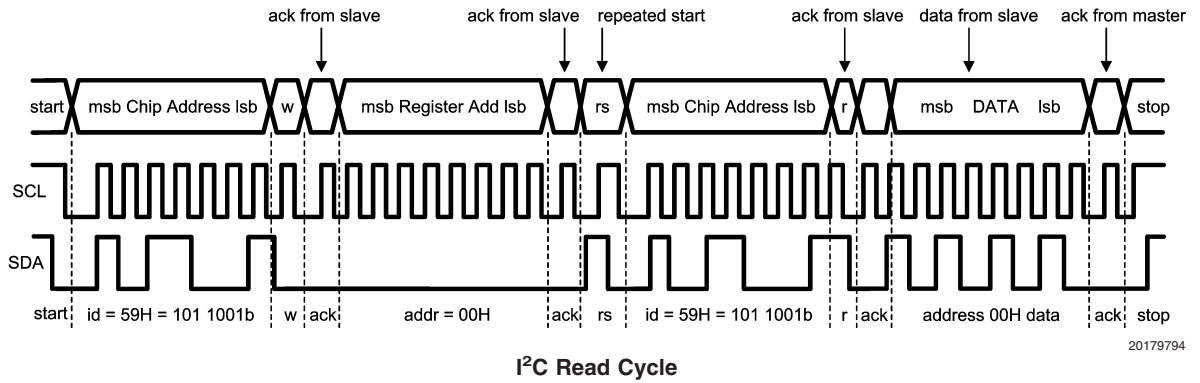
## I<sup>2</sup>C Compatible Interface (Continued)



w = write (SDA = "0")  
 r = read (SDA = "1")  
 ack = acknowledge (SDA pulled down by either master or slave)  
 rs = repeated start  
 id = 7-bit chip address, 59H (101 1001b) for LP5526.

### I<sup>2</sup>C Write Cycle

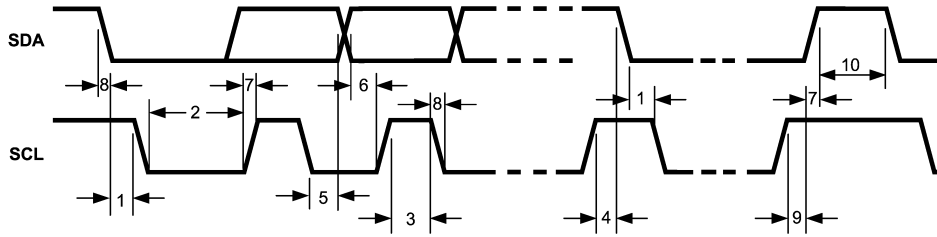
When a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in the Read Cycle waveform.



### I<sup>2</sup>C Read Cycle



## I<sup>2</sup>C Compatible Interface (Continued)



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I<sup>2</sup>C Timing Diagram

### I<sup>2</sup>C TIMING PARAMETERS ( $V_{DD1,2} = 3.0$ to $4.5V$ , $V_{DDIO} = 1.8V$ to $V_{DD1,2}$ )

Symbol	Parameter	Limit		Units
		Min	Max	
1	Hold Time (repeated) START Condition	0.6		$\mu s$
2	Clock Low Time	1.3		$\mu s$
3	Clock High Time	600		ns
4	Setup Time for a Repeated START Condition	600		ns
5	Data Hold Time (Output direction, delay generated by LP5526)	300	900	ns
5	Data Hold Time (Input direction, delay generated by Master)	0	900	ns
6	Data Setup Time	100		ns
7	Rise Time of SDA and SCL	$20+0.1C_b$	300	ns
8	Fall Time of SDA and SCL	$15+0.1C_b$	300	ns
9	Set-up Time for STOP condition	600		ns
10	Bus Free Time between a STOP and a START Condition	1.3		$\mu s$
$C_b$	Capacitive Load for Each Bus Line	10	200	pF

**NOTE:** Data guaranteed by design

## Recommended External Components

### OUTPUT CAPACITOR, $C_{OUT}$

The output capacitor  $C_{OUT}$  directly affects the magnitude of the output ripple voltage. In general, the higher the value of  $C_{OUT}$ , the lower the output ripple magnitude. Multilayer ceramic capacitors with low ESR are the best choice. At the lighter loads, the low ESR ceramics offer a much lower  $V_{OUT}$  ripple than the higher ESR tantalums of the same value. At the higher loads, the ceramics offer a slightly lower  $V_{OUT}$  ripple magnitude than the tantalums of the same value. However, the  $dv/dt$  of the  $V_{OUT}$  ripple with the ceramics is much lower than the tantalums under all load conditions. Capacitor voltage rating must be sufficient, 25V or greater is recommended. Examples of suitable capacitors are: TDK C3216X5R1E475K, Panasonic ECJ3YB1E475K, ECJMFB1E475K and ECJ4YB1E475K.

**Some ceramic capacitors, especially those in small packages, exhibit a strong capacitance reduction with the increased applied voltage (DC bias effect). The capacitance value can fall below half of the nominal capacitance. Too low output capacitance can make the boost converter unstable. Output capacitors DC bias effect should be better than -50% at 20V.**

### INPUT CAPACITOR, $C_{IN}$

The input capacitor  $C_{IN}$  directly affects the magnitude of the input ripple voltage and to a lesser degree the  $V_{OUT}$  ripple. A higher value  $C_{IN}$  will give a lower  $V_{IN}$  ripple. Capacitor voltage rating must be sufficient, 10V or greater is recommended.

### OUTPUT DIODE, $D_1$

A schottky diode should be used for the output diode. Peak repetitive current should be greater than inductor peak current (1500mA) to ensure reliable operation.

Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency in portable applications. Choose a reverse breakdown voltage of the schottky diode significantly larger (~30V) than the output voltage. Do not use ordinary rectifier diodes, since slow switching speeds and long recovery times cause the efficiency and the load regulation to suffer. Examples of suitable diodes are: Central Semiconductor CMMSH1-40, Infineon BAS52-02V.

### EMI FILTER COMPONENTS $C_{SW}$ , $R_{SW}$

EMI filter ( $R_{SW}$  and  $C_{SW}$ ) on the SW pin can be used to suppress EMI caused by fast switching. These components should be as near as possible to the SW pin to ensure reliable operation. 50V or greater voltage rating is recommended for capacitor.

### INDUCTOR, $L_1$

A 10uH shielded inductor is suggested for LP5526 boost converter. The inductor should have a saturation current rating higher than the rms current it will experience during circuit operation (1300mA). Less than 300mΩ ESR is suggested for high efficiency and sufficient output current. Open core inductors cause flux linkage with circuit components and interfere with the normal operation of the circuit. This should be avoided. For high efficiency, choose an inductor with a high frequency core material such as ferrite to reduce the core losses. To minimize radiated noise, use a toroid, pot core or shielded core inductor. The inductor should be connected to the SW pin as close to the IC as possible. Examples of suitable inductors are: TDK SLF6028T-100M1R3, Coilcraft MSS6122-103MLB.

### LIST OF RECOMMENDED EXTERNAL COMPONENTS

Symbol	Symbol explanation	Value	Unit	Type
$C_{VDD}$	C between VDD1,2 and GND	100	nF	Ceramic, X7R / X5R
$C_{VDDIO}$	C between VDDIO and GND	100	nF	Ceramic, X7R / X5R
$C_{VDDA}$	C between VDDA and GND	1	μF	Ceramic, X7R / X5R
$C_{OUT}$	C between FB and GND	2 x 4.7 or 1 x 10	μF	Ceramic, X7R / X5R, tolerance +/-10%
	Maximum DC bias effect @ 20V	-50	%	
$C_{IN}$	C between battery voltage and GND	10	μF	Ceramic, X7R / X5R
$L_1$	L between SW and $V_{BAT}$	10	μH	Shielded inductor, low ESR
	Saturation current	1300	mA	
$C_{VREF}$	C between $V_{REF}$ and GND	100	nF	Ceramic, X7R / X5R
$R_{RGB}$	R between $I_{RGB}$ and GND	2.4	kΩ	±1%
$R_{RT}$	R between $I_{RT}$ and GND	82	kΩ	±1%
$D_1$	Rectifying diode ( $V_f$ @ maxload)	0.3-0.5	V	Schottky diode
	Reverse voltage	30	V	
	Repetitive peak current	1500	mA	
$C_{SW}$	C in EMI filter	100	pF	Ceramic, X7R / X5R, 50V
$R_{SW}$	R in EMI filter	390	Ω	±1%
LEDs				User Defined

Note: See Application Note AN-1442 "Design and Programming Examples for Lighting Management Unit LP5526" for more information on how to design with LP5526

LP5526 Control Register Names and Default Values

ADDR (HEX)	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	
00	Control Register	RGB_PWM 0	EN_RGB 0	CC_SW 1		RSW 0	GSW 0	BSW 0		
01	RGB	COLOR[3:0]					BRIGHT[2:0]		OVL	
02	RGB max current	SAFETY_SET 0		IR[1:0] 0		IG[1:0] 0		IB[1:0] 0		
03	WLED Control			SLOPE 0	FADE_SEL 0	EN_FADE 0	DISPL 0	EN_MAIN 0	EN_SUB 0	
04	MAIN Current	MAIN[7:0]								
05	SUB Current	SUB[7:0]								
06	GPIO Control				EN_PWM_PIN 0			OEN[2:0] 0		
07	GPIO Data							DATA[2:0] 0		
0B	Enables		NSTBY 0	EN_BOOST 0		EN_FLASH 0	EN_AUTOLOAD 1			
0D	Boost Output	BOOST[7:0]								
2B	PWM Enable	EN_SAFETY_R 0	EN_SAFETY_G 0	EN_SAFETY_B 0	EN_EXT_R_PWM 0	EN_EXT_G_PWM 0	EN_EXT_B_PWM 0	EN_MAIN_PWM 0	EN_SUB_PWM 0	

## LP5526 Register Bit Explanations

Each register is shown with a key indicating the accessibility of the each individual bit, and the initial condition:

### Register Bit Accessibility and Initial Condition

Key	Bit Accessibility
RW	Read/write
R	Read only
-0,-1	Condition after POR

### CONTROL REGISTER (00H) – RGB LEDS CONTROL REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
<b>RGB_PWM</b>	<b>EN_RGB</b>	<b>CC_SW</b>		<b>RSW</b>	<b>GSW</b>	<b>BSW</b>	
RW - 0	RW - 0	RW - 1	R - 0	RW - 0	RW - 0	RW - 0	R - 0

<b>RGB_PWM</b>	Bit 7	0 - Internal RGB PWM control disabled 1 - Internal RGB PWM control enabled
<b>EN_RGB</b>	Bit 6	0 – RGB outputs disabled 1 – RGB outputs enabled
<b>CC_SW</b>	Bit 5	0 – Constant current sink mode 1 – Switch mode
<b>RSW</b>	Bit 3	0 – RLED disabled 1 – RLED enabled
<b>GSW</b>	Bit 2	0 – GLED disabled 1 – GLED enabled
<b>BSW</b>	Bit 1	0 – BLED disabled 1 – BLED enabled

### RGB (01H) – RGB COLOR AND BRIGHTNESS CONTROL REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
<b>COLOR[3:0]</b>				<b>BRIGHT[2:0]</b>			<b>OVL</b>
RW - 0	RW - 0	RW - 0	RW - 0	RW - 0	RW - 0	RW - 0	RW - 0

<b>COLOR[3:0]</b>	Bits 7-4	PWM color for RGB outputs
<b>BRIGHT[2:0]</b>	Bits 3-1	PWM brightness control for RGB outputs
<b>OVL</b>	Bit 0	0 – Overlapping mode disabled 1 – Overlapping mode enabled

## LP5526 Register Bit Explanations (Continued)

### RGB MAX CURRENT (02H) – MAXIMUM RGB CURRENT CONTROL REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
<b>SAFETY_SET</b>		<b>IR[1:0]</b>		<b>IG[1:0]</b>		<b>IB[1:0]</b>	
R - 0	R - 0	RW - 0	RW - 0	RW - 0	RW - 0	RW - 0	RW - 0

<b>SAFETY_SET</b>	Bit 7	0 – safety function not activated 1 – safety function activated
<b>IR[1:0]</b>	Bits 5-4	RLED maximum current
<b>IG[1:0]</b>	Bits 3-2	GLED maximum current
<b>IB[1:0]</b>	Bits 1-0	BLED maximum current

Maximum current for RGB driver	
IR,IG,IB[1:0]	Maximum output current
00	$0.25 \times I_{MAX}$
01	$0.50 \times I_{MAX}$
10	$0.75 \times I_{MAX}$
11	$1.00 \times I_{MAX}$

### WLED CONTROL (03H) – WLED CONTROL REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
		<b>SLOPE</b>	<b>FADE_SEL</b>	<b>EN_FADE</b>	<b>DISPL</b>	<b>EN_MAIN</b>	<b>EN_SUB</b>
R - 0	R - 0	RW - 0	RW - 0	RW - 0	RW - 0	RW - 0	RW - 0

<b>SLOPE</b>	Bit 5	0 – fade execution time 0.65 sec (full scale) 1 – fade execution time 1.3 sec (full scale)
<b>FADE_SEL</b>	Bit 4	0 – fade control for MAIN 1 – fade control for SUB
<b>EN_FADE</b>	Bit 3	0 – automatic fade disabled 1 – automatic fade enabled
<b>DISPL</b>	Bit 2	0 - MAIN and SUB individual control 1 - MAIN and SUB controlled with MAIN DAC
<b>EN_MAIN</b>	Bit 1	0 – MAIN output disabled 1 – MAIN output enabled
<b>EN_SUB</b>	Bit 0	0 – SUB output disabled 1 – SUB output enabled

## LP5526 Register Bit Explanations (Continued)

### MAIN CURRENT (04H) – MAIN CURRENT CONTROL REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
<b>MAIN[7:0]</b>							
RW - 0	RW - 0	RW - 0	RW - 0	RW - 0	RW - 0	RW - 0	RW - 0

### SUB CURRENT (05H) – SUB CURRENT CONTROL REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
<b>SUB[7:0]</b>							
RW - 0	RW - 0	RW - 0	RW - 0	RW - 0	RW - 0	RW - 0	RW - 0

MAIN, SUB current adjustment	
MAIN[7:0], SUB[7:0]	Typical driver current (mA)
0000 0000	0
0000 0001	0.1
0000 0010	0.2
0000 0011	0.3
0000 0100	0.4
...	...
1111 1101	25.3
1111 1110	25.4
1111 1111	25.5

### GPIO CONTROL (06H) – GPIO CONTROL REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
			<b>EN_PWM_PIN</b>	<b>OEN[2:0]</b>			
R - 0	R - 0	R - 0	RW - 0	R - 0	RW - 0	RW - 0	RW - 0

<b>EN_PWM_PIN</b>	Bit 4	0 – External PWM pin disabled 1 – External PWM pin enabled
<b>OEN[2:0]</b>	Bits 2-0	0 – GPIO pin set as a input 1 – GPIO pin set as a output

### GPIO DATA (07H) – GPIO DATA REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
					<b>DATA[2:0]</b>		
R - 0	R - 0	R - 0	R - 0	R - 0	RW - 0	RW - 0	RW - 0

<b>DATA[2:0]</b>	Bits 2-0	GPIO data register bits
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## LP5526 Register Bit Explanations (Continued)

### ENABLES (0BH) – ENABLES REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
	<b>NSTBY</b>	<b>EN_BOOST</b>		<b>EN_FLASH</b>	<b>EN_AUTOLOAD</b>		
R - 0	RW - 0	RW - 0	R - 0	RW - 0	RW - 1	R - 0	R - 0

<b>NSTBY</b>	Bit 6	0 – LP5526 standby mode 1 – LP5526 active mode
<b>EN_BOOST</b>	Bit 5	0 – Boost converter disabled 1 – Boost converter enabled
<b>EN_FLASH</b>	Bit 3	0 – Flash function disabled 1 – Flash function enabled
<b>EN_AUTOLOAD</b>	Bit 2	0 – Boost active load disabled 1 – Boost active load enabled

### BOOST OUTPUT (0DH) – BOOST OUTPUT VOLTAGE CONTROL REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
<b>BOOST[7:0]</b>							
RW - 0	RW - 0	RW - 0	RW - 0	RW - 1	RW - 0	RW - 0	RW - 0

<b>BOOST output voltage adjustment</b>	
<b>BOOST[7:0]</b>	<b>Typical boost output voltage (V)</b>
0000 1000	8.00
0000 1001	9.00
0000 1010	10.00
0000 1011	11.00
0000 1100	12.00
0000 1101	13.00
0000 1110	14.00
0000 1111	15.00
0001 0000	16.00
0001 0001	17.00
0001 0010	18.00
0001 0011	19.00
0001 0100	20.00

## LP5526 Register Bit Explanations (Continued)

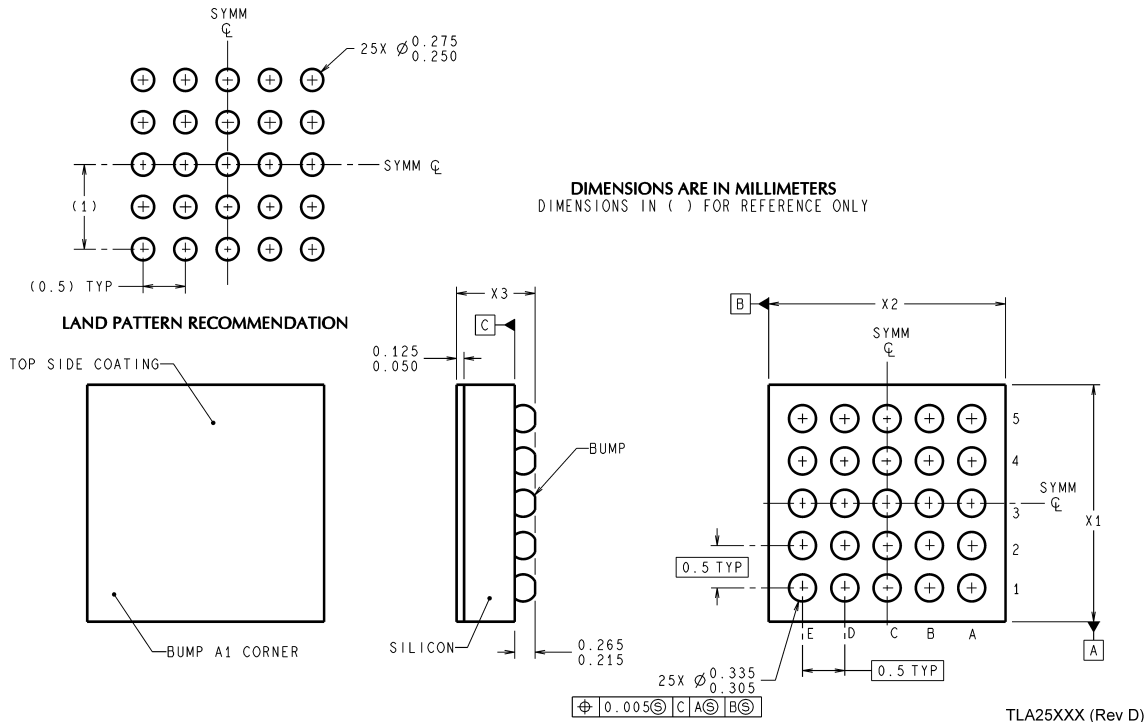
### PWM ENABLE (2BH) – EXTERNAL PWM CONTROL REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
<b>EN_SAFETY_R</b>	<b>EN_SAFETY_G</b>	<b>EN_SAFETY_B</b>	<b>EN_EXT_R_PWM</b>	<b>EN_EXT_G_PWM</b>	<b>EN_EXT_B_PWM</b>	<b>EN_MAIN_PWM</b>	<b>EN_SUB_PWM</b>
RW - 0	RW - 0	RW - 0	RW - 0	RW - 0	RW - 0	RW - 0	RW - 0

<b>EN_SAFETY_R</b>	Bit 7	0 – Safety function for RLED disabled 1 – Safety function for RLED enabled
<b>EN_SAFETY_G</b>	Bit 6	0 – Safety function for GLED disabled 1 – Safety function for GLED enabled
<b>EN_SAFETY_B</b>	Bit 5	0 – Safety function for BLED disabled 1 – Safety function for BLED enabled
<b>EN_EXT_R_PWM</b>	Bit 4	0 – External PWM control for RLED disabled 1 – External PWM control for RLED enabled
<b>EN_EXT_G_PWM</b>	Bit 3	0 – External PWM control for GLED disabled 1 – External PWM control for GLED enabled
<b>EN_EXT_B_PWM</b>	Bit 2	0 – External PWM control for BLED disabled 1 – External PWM control for BLED enabled
<b>EN_EXT_MAIN_PWM</b>	Bit 1	0 – External PWM control for MAIN disabled 1 – External PWM control for MAIN enabled
<b>EN_EXT_SUB_PWM</b>	Bit 0	0 – External PWM control for SUB disabled 1 – External PWM control for SUB enabled



**Physical Dimensions** inches (millimeters) unless otherwise noted



The dimension for X1, X2 and X3 are as given:

- X1=2.543mm ± 0.03mm
- X2=2.543mm ± 0.03mm
- X3=0.60mm ± 0.075mm

**25-bump micro SMD Package, 2.54 x 2.54 x 0.6mm, 0.5mm pitch  
NS Package Number TLA25CCA**

See Application note AN-1112 for PCB design and assembly instructions.

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English Tel: +44 (0) 870 24 0 2171  
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Asia Pacific Customer  
Support Center  
Email: [ap.support@nsc.com](mailto:ap.support@nsc.com)

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