SUN MICROELECTRONICS

STP2230SOP

July 1997

XB1

DATA SHEET — Crossbar Switch

DESCRIPTION

The STP2230SOP crossbar switch [1] acts as the bridge among three UltraSPARC UPA devices. One of the buses is dedicated to interfacing to system memory, while the other two are general-purpose buses. These buses are used for interfacing memory, a processor bus, and an I/O bus. In this particular configuration, eighteen XB1s are required per system implementation.

FEATURES

- Three-port crossbar
  - 16-bit data
  - 8-bit processor
  - 4-bit data ports
- Decoupled memory port; loading and unloading of memory data can take place in parallel with other operations
- Burst transfers operate on four bytes of data per slice
- Power-up safe buses; all buses power up tristated so there will be no bus contention with other parts which may be on the buses
- Implemented in 0.8-micron BiCMOS and housed in a 48-pin TSSOP package (also called DGG or “shrink-wide bus”)

1. The STP2230SOP crossbar switch is also referred to as BMX.

BLOCK, LOGIC, AND TYPICAL APPLICATION DIAGRAMS

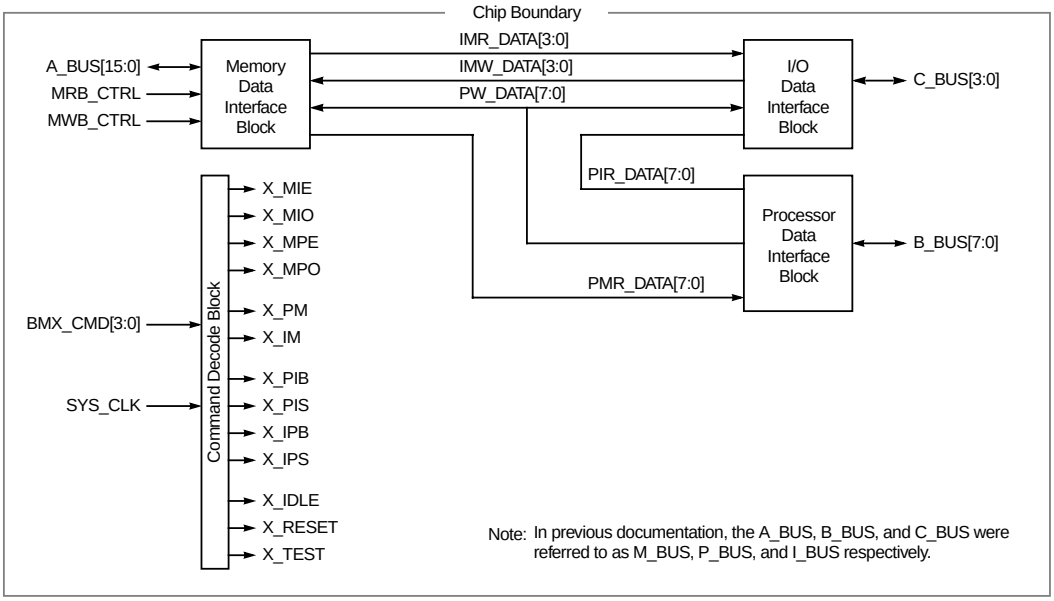


Figure 1. STP2230SOP Block Diagram

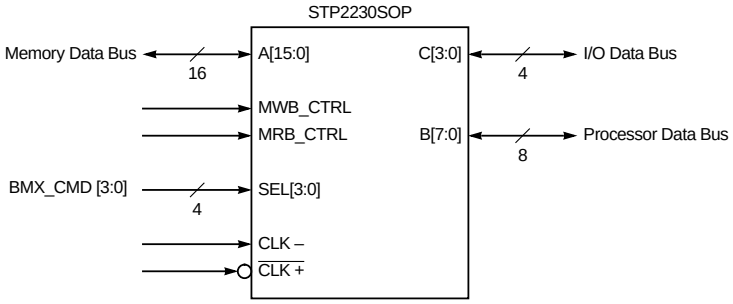


Figure 2. STP2230SOP Logic Diagram

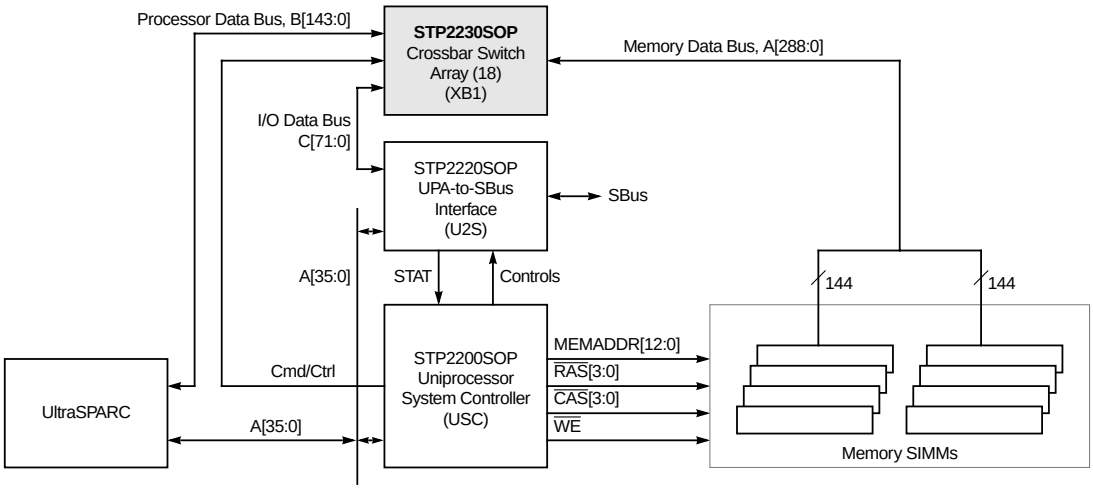


Figure 3. STP2230SOP Typical Application Diagram

SIGNAL DESCRIPTIONS

Signal	I/O	No. Pins	Description	I/F Type
A[15:0]	I/O	16	Bidirectional data from memory bus.	LV TTL, 5-volt tolerant
B[7:0]	I/O	8	Processor port, bidirectional, registered	LV TTL
C[3:0]	I/O	4	Input/output port, bidirectional, registered	LV TTL
MRB_CTRL	I	1	Memory read buffer control	LV TTL
MWB_CTRL	I	1	Memory write buffer control	LV TTL
CLK+, CLK–	I	2	Differential clock signals	3.3-V PECL
BMX_CMD[3:0]	I	4	Command input signals	LV TTL

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings [1]

Symbol	Parameter		Min	Max	Units
V_{DD}	DC supply voltage		– 0.5	4.6	V
V_{CC}	DC supply voltage		– 0.5	6.0	V
V_{IN}	Input voltage range		– 0.5	V_{DD} + 0.5	V
$V_{IN\_A\_BUS}$	Input voltage range (A_bus)		– 0.5	V_{CC} + 0.5	V
I_{IN}	DC input current			–18	mA
I_{OUT}	DC output current		– 50	50	mA
T_{ST}	Storage temperature		– 65	150	°C
F_{CLK}	Clock frequency	STP2230SOP-83	0.050	83.34	MHz
		STP2230SOP-100	0.050	100	MHz

1. Operation of the device at values in excess of those listed above will result in degradation or destruction of the device. All voltages are defined with respect to ground. Functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	DC supply voltage	3.15	3.3	3.45	V
V_{CC}	DC supply voltage	4.75	5.0	5.25	V
T_C	Case temperature	0	–	75	°C
T_J	Junction temperature	0	–	105	°C

Capacitance

Symbol	Parameter	Conditions	Min	Max	Units
C_{IN}	Input capacitance	Any input	–	6	pF
C_{OUT}	Output capacitance	Any output	–	8	pF
C_{IO}	Input/Output capacitance		–	10	pF

DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Voltage input low		–		0.8	V
V_{IH}	Voltage input high		2.0		–	V
V_{IL}	PECL clock voltage input low				1.6	V
V_{IH}	PECL clock voltage input high		2.4			V
V_{DIFF}	Input differential voltage (PECL inputs)		0.8			V
V_{OL}	Voltage output low	I_{OL} = 8 mA	–	0.2	0.5	V
V_{OH}	Voltage output high	I_{OH} = -8 mA	2.4		–	V
I_{CC}	$V_{CC\ input\ current}$		1		35	mA
I_{DD}	$V_{DD\ input\ current}$				35	mA

AC Characteristics

Symbol	Parameter	-83			-100			Unit
		Min	Typ	Max	Min	Typ	Max	
$t_{CO,UPA}$	Clock to output for processor and I/O ports [1]			5.4			5.4	ns
$t_{VO,UPA}$	Clock to output for processor and I/O ports	0.5			0.5			ns
$t_{CO,M}$	Clock to output for memory port			6			6	ns
$t_{VO,M}$	Clock to output valid for memory port			TBD			TBD	ns
t_{SPI}	Input setup time for processor and I/O ports	2.0			2.0			ns
t_{SM}	Input setup time for memory port	4.0			4.0			ns
t_{HPI}	Input hold time for processor and I/O ports	0.5			0.5			ns
t_{HM}	Input hold time for memory port	2.0			2.0			ns
t_{CYCLE}	Clock cycle time	12			10			ns
t_{WL}	Clock minimum low width	5.4			4.4			ns
t_{WH}	Clock minimum high width	5.4			4.4			ns

1. Note: t_{CO} is specified with a 50 pF loading. This timing improves with a 3.1 nS with a 25 pF loading.

AC Characteristics - Clock Signal

Symbol	Parameter	-83			-100			Unit
		Min	Typ	Max	Min	Typ	Max	
FCLK	Clock Frequency	0.1	-	83.4	0.1	-	100	MHz

Symbol	Parameter	-83			-100			Unit
		Min	Typ	Max	Min	Typ	Max	
t_{CYCLE}	Clock cycle time	12			10			ns
t_{WL}	Clock minimum low width	5.4			4.4			ns
t_{WH}	Clock minimum high width	5.4			4.4			ns
t_{E}	Clock rise/fall time	250		600	250		600	ps

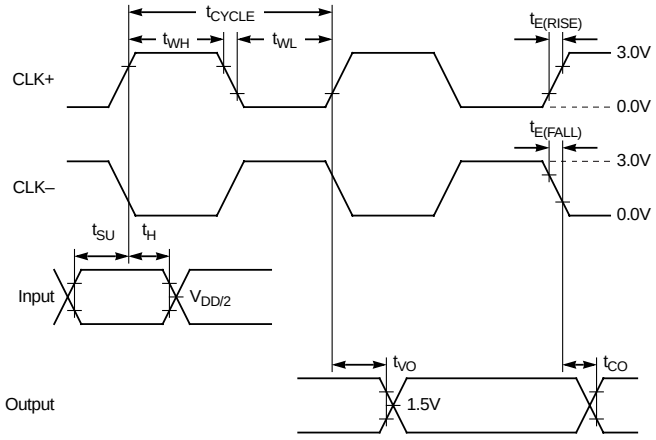


Figure 4. Signal Timing Definition

TIMING DIAGRAMS

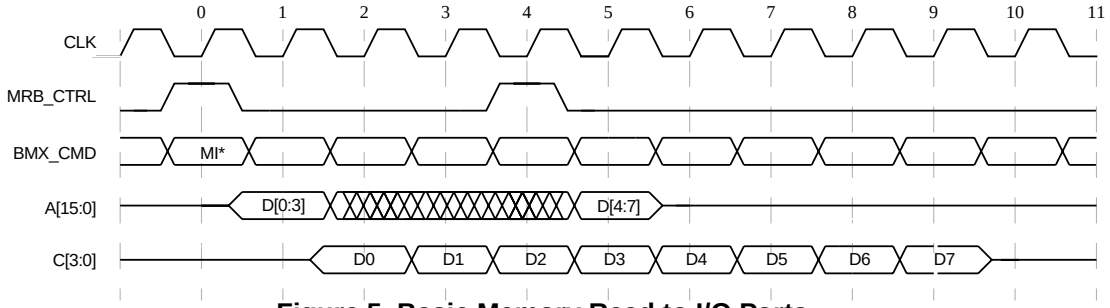


Figure 5. Basic Memory Read to I/O Ports

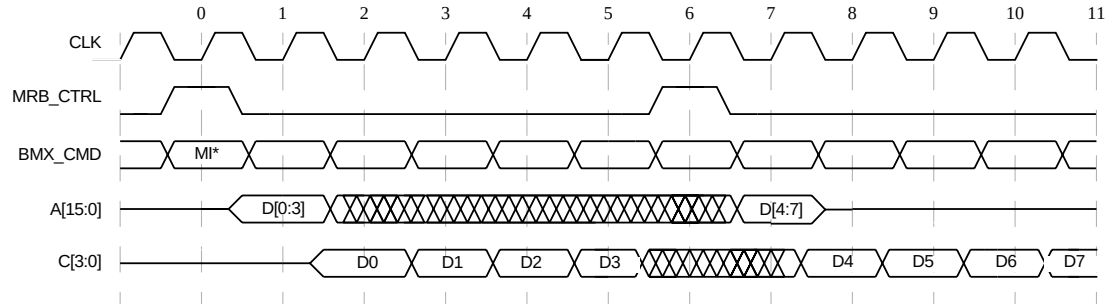


Figure 6. Memory Read to I/O Port Controlled by MRB_CTRL

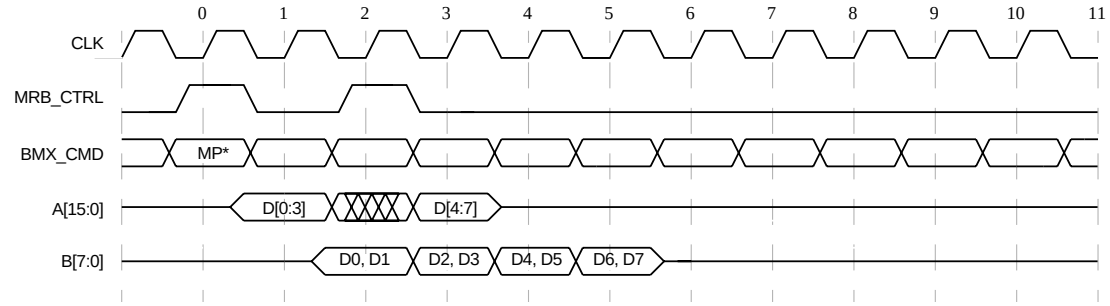


Figure 7. Basic Memory Read to Processor

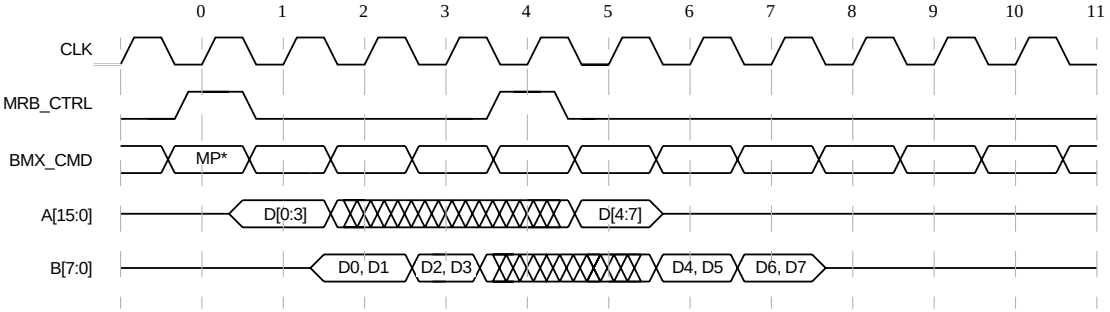


Figure 8. Memory Read to Processor Controlled by MRB_CTRL

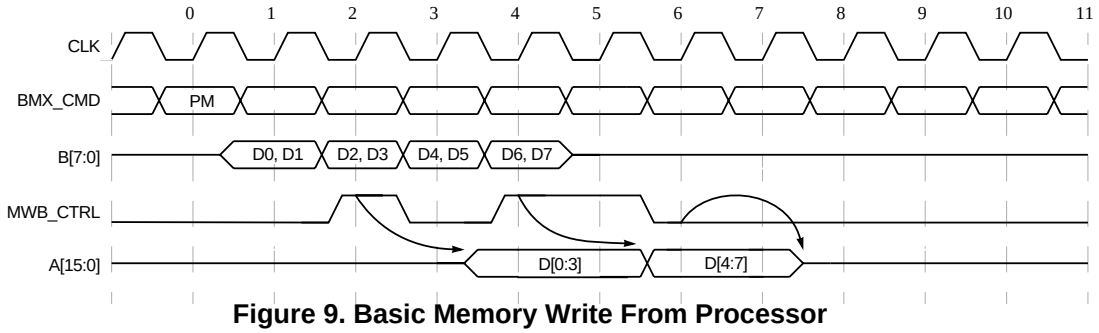


Figure 9. Basic Memory Write From Processor

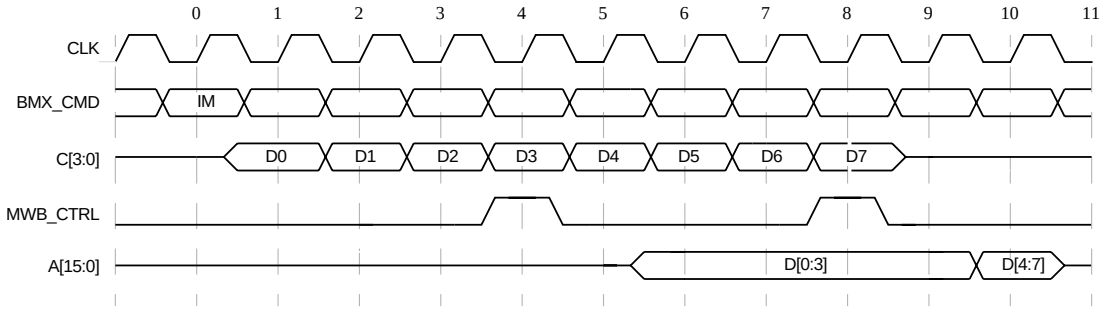


Figure 10. Basic Memory Write From I/O Ports

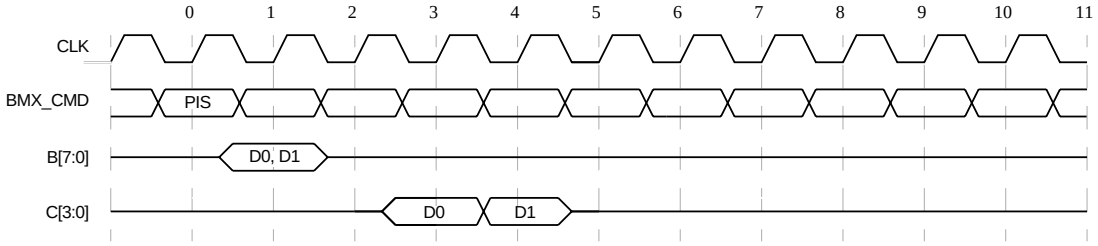


Figure 11. Single Transfer From Processor to I/O Port

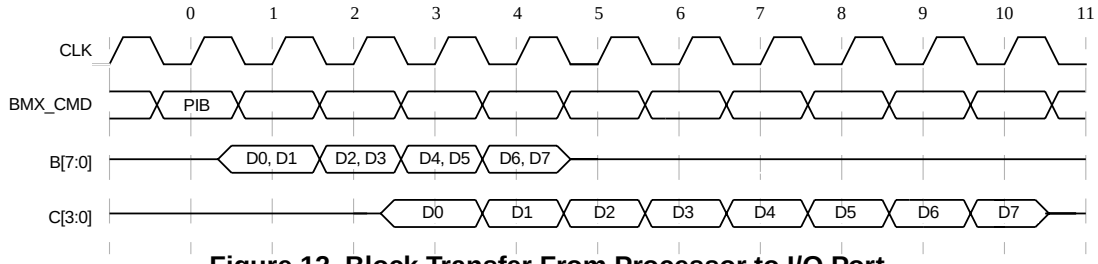


Figure 12. Block Transfer From Processor to I/O Port

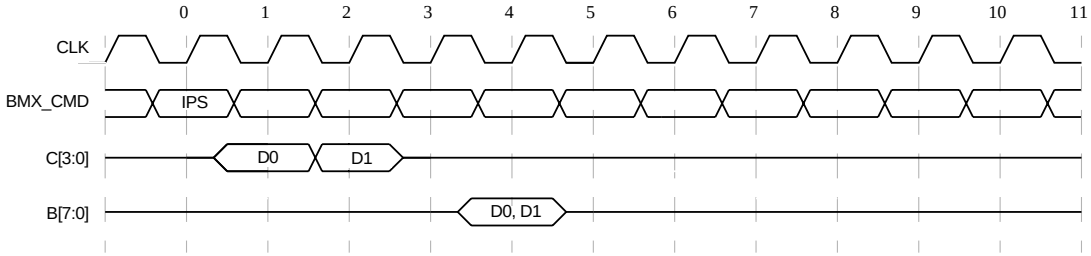


Figure 13. Single Transfer From I/O to Processor

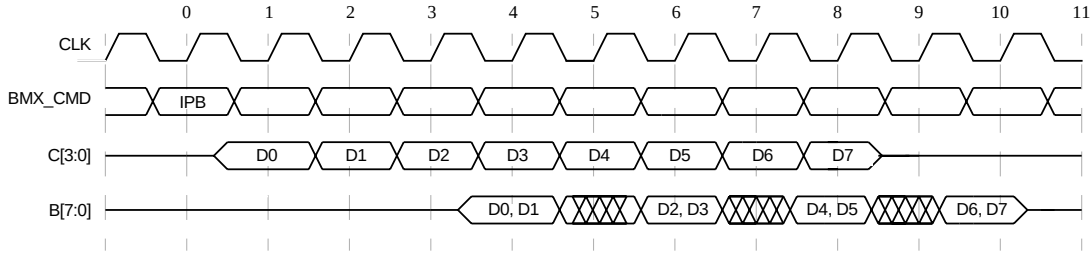


Figure 14. Block Transfer From I/O to Processor

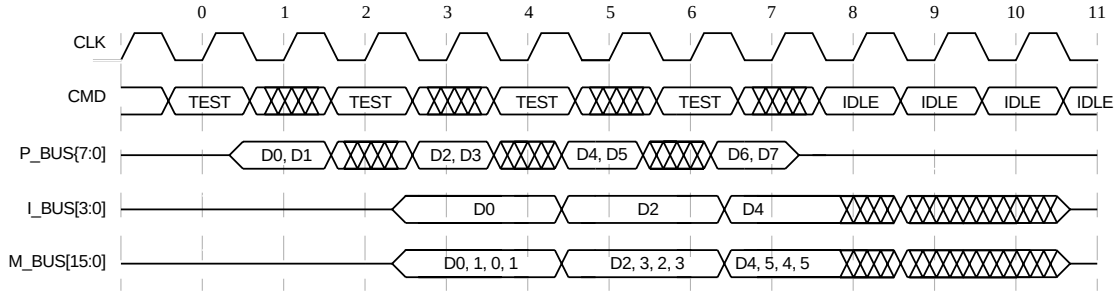


Figure 15. X_TEST Basic Timing

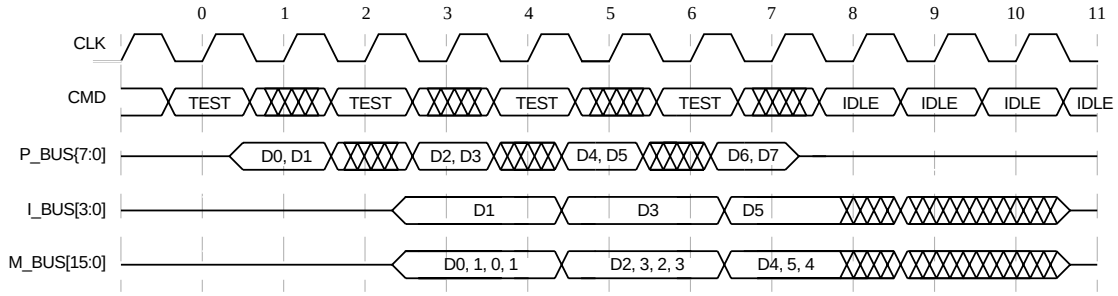


Figure 16. X_TEST2 Basic Timing

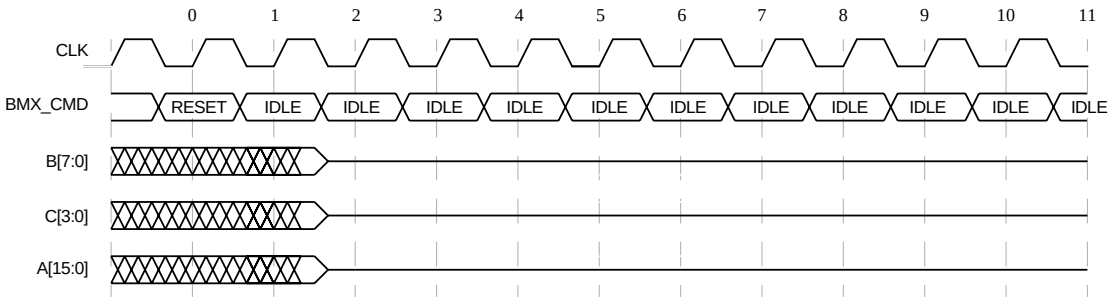
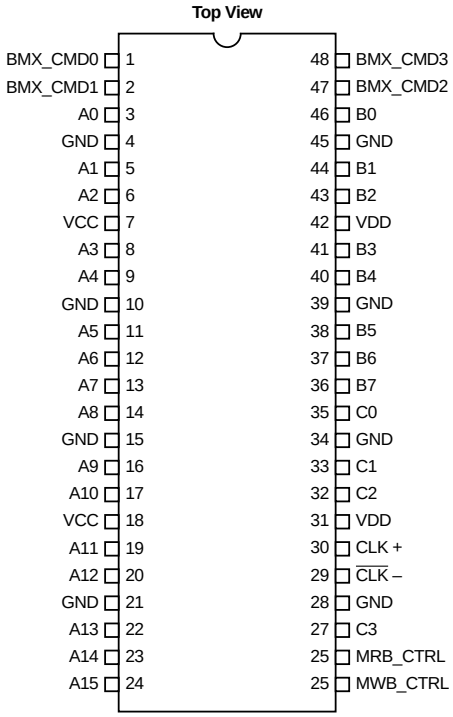


Figure 17. RESET Basic Timing

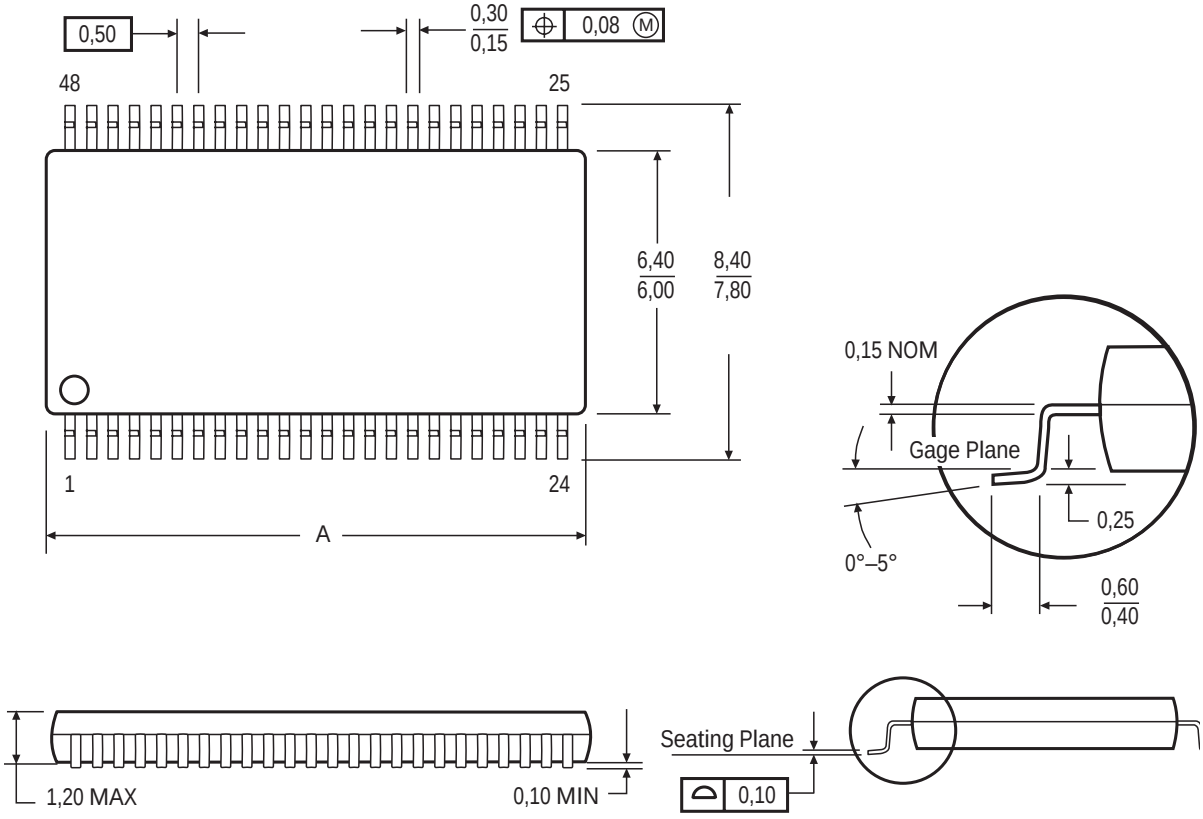
PACKAGE INFORMATION

48-Pin SOP Pin Assignments

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	BMX_CMD0	9	A4	17	A10	25	MWB_CTRL	33	C1	41	B3
2	BMX_CMD1	10	$_{GND}$	18	V_{CC}	26	MRB_CTRL	34	GND	42	V_{DD}
3	A0	11	A5	19	A11	27	C3	35	C0	43	$_{B2}$
4	GND	12	A6	20	A12	28	GND	36	B7	44	B1
5	A1	13	A7	21	$_{GND}$	29	$\overline{CLK}$ –	37	B6	45	GND
6	A2	14	A8	22	A13	30	CLK +	38	B5	46	B0
7	V_{CC}	15	GND	23	A14	31	V_{DD}	39	GND	47	BMX_CMD2
8	A3	16	A9	24	A15	32	C2	40	B4	48	BMX_CMD3



48-Pin SOP Package Dimensions



Dimension		mm
A	Max	12.80
	Min	12.40

Note:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions include mold flash or protrusion.

ORDERING INFORMATION

Part Number	Speed	Description
STP2230SOP	83 MHz	Crossbar switch for the UPA bus
STP2230SOP-100	100 MHz	Crossbar switch for the UPA bus

Documnet Part Number: 802-7955-02