DATA SHEET

TZA3034
SDH/SONET STM1/OC3 postamplifier

Product specification
Supersedes data of 1999 Mar 16
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Philips Semiconductors

FEATURES

- Pin compatible with the NE/SA5224 and NE/SA5225 but with extended power supply range and less external component count
- Wideband operation from 1.0 kHz to 150 MHz typical
- Applicable in 155 Mbits/s SDH/SONET receivers
- Single supply voltage from 3.0 to 5.5 V
- Positive Emitter Coupled Logic (PECL) compatible data outputs
- Programmable input signal level detection which can be adjusted using a single external resistor
- On-chip DC offset compensation without external capacitor.

APPLICATIONS

- Digital fibre optic receiver in short, medium and long haul optical telecommunications transmission systems or in high speed data networks
- Wideband RF gain block.

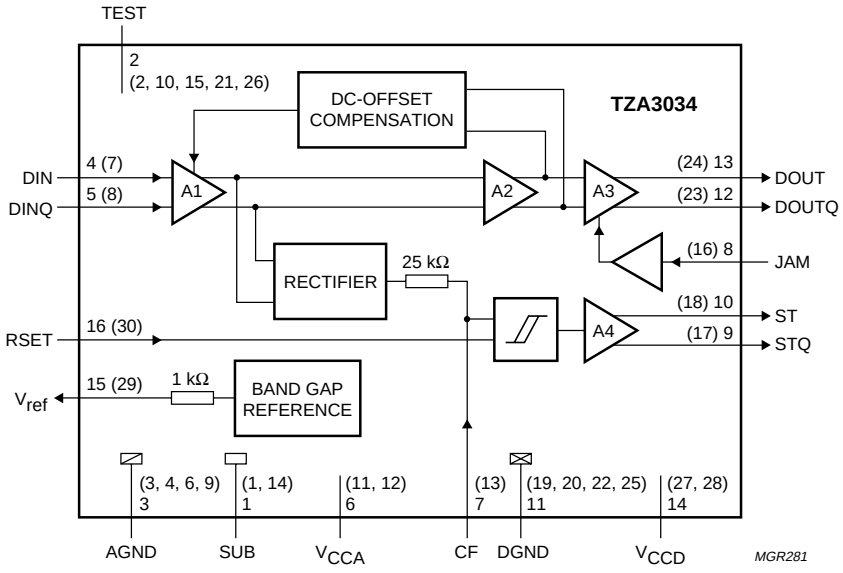
GENERAL DESCRIPTION

The TZA3034 is a high gain limiting amplifier that is designed to process signals from fibre optic preamplifiers like the TZA3033. It is pin compatible with the NE/SA5224 and NE/SA5225 but with extended power supply range, and needs less external components. Capable of operating at 155 Mbits/s, the chip has input signal level detection with a user-programmable threshold. The data and level detection status outputs are differential outputs for optimum noise margin and ease of use.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3034T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
TZA3034TT	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
TZA3034U	–	bare die in waffle pack carriers; die dimensions 1.55 × 1.55 mm	–

BLOCK DIAGRAM



The numbers in brackets refer to the pad numbers of the bare die version.

Fig.1 Block diagram.

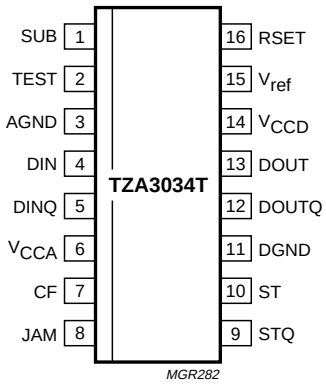


Fig.2 Pin configuration of TZA3034T.

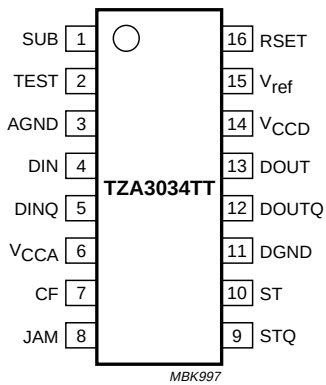


Fig.3 Pin configuration of TZA3034TT.

PINNING

SYMBOL	PIN TZA3034T TZA3034TT	PAD TZA3034U	TYPE[1]	DESCRIPTION
SUB	1	1, 14	S	substrate pin; must be at the same potential as pin AGND
TEST	2	2, 10, 15, 21, 26	–	for test purpose only; to be left open in the application
AGND	3	3, 4, 6, 9	S	analog ground; must be at the same potential as pin DGND
DIN	4	7	I	differential input; complementary to pin DINQ; DC bias level is set internally at approximately 2.1 V
DINQ	5	8	I	differential input; complementary to pin DIN; DC bias level is set internally at approximately 2.1 V
V_{CCA}	6	11, 12	S	analog supply voltage; must be at the same potential as pin V_{CCD}
CF	7	13	A	input for connection of capacitor to set time constant of level detector input filter (optional); the capacitor should be connected between V_{CCA} and pin CF
JAM	8	16	I	PECL-compatible input; controls the output buffers, pins DOUT and DOUTQ; when a LOW signal is applied, the output buffers will follow the input signal; when a HIGH signal is applied, the output buffers will latch into LOW and HIGH states respectively; when not connected, pin JAM is actively pulled LOW
STQ	9	17	O	PECL-compatible status output of the input signal level detector; when the input signal is below the user-programmed threshold level, this output is HIGH; complementary to pin ST
ST	10	18	O	PECL-compatible status output of the input signal level detector; when the input signal is below the user-programmed threshold level, this output is LOW; complementary to pin STQ
DGND	11	19, 20, 22, 25	S	digital ground; must be at the same potential as pin AGND
DOUTQ	12	23	O	PECL-compatible differential output; this pin will be forced into a HIGH condition when pin JAM is HIGH; complementary to pin DOUT
DOUT	13	24	O	PECL-compatible differential output; this pin will be forced into a LOW condition when pin JAM is HIGH; complementary to pin DOUTQ
V_{CCD}	14	27, 28	S	digital supply voltage; must be at the same potential as V_{CCA}
V_{ref}	15	29	O	band gap reference voltage; typical value is 1.2 V; internal series resistor of 1 kΩ
RSET	16	30	A	input signal level detector threshold setting; nominal DC voltage is V_{CCA} – 1.5 V; threshold level is set by connecting an external resistor between V_{CCA} and pin RSET or by forcing a current into pin RSET; default value for this resistor is 180 kΩ which corresponds with approximately 4 mV (p-p) differential input signal
n.c.	–	5, 31, 32	–	not connected

Note

1. Pin type abbreviations: O = Output, I = Input, S = power Supply and A = Analog function.

FUNCTIONAL DESCRIPTION

The TZA3034 accepts up to 155 Mbits/s SDH/SONET data streams, with amplitudes from 2 mV up to 1.5 V (p-p) single-ended. The input signal will be amplified and limited to differential PECL output levels (see Fig.1).

The input buffer A1 presents an impedance of approximately 4.5 kΩ to the data stream on the inputs pin DIN and pin DINQ. The input can be used both single-ended and differential, but differential operation is preferred for better performance.

Because of the high gain of the postamplifier, a very small offset voltage would shift the decision level in such a way that the input sensitivity decreases drastically. Therefore a DC offset compensation circuit is implemented in the TZA3034, which keeps the input of buffer A3 at its toggle point in the absence of any input signal.

An input signal level detection is implemented to check if the input signal is above the user-programmed level. The outcome of this test is available at the PECL outputs, pins ST and STQ. This flag can also be used to prevent the PECL outputs pins DOUT and DOUTQ from reacting to noise in the absence of a valid input signal, by connecting pin STQ to pin JAM. This guarantees that data will only be transmitted when the input signal-to-noise ratio is sufficient for low bit error rate system operation.

PECL logic

The logic level symbol definitions for PECL are shown in Fig.4.

Input biasing

The inputs, pins DIN and DINQ, are DC biased at approximately 2.1 V by an internal reference generator (see Fig.5). The TZA3034 can be DC coupled, but AC coupling is preferred. In case of DC coupling, the driving source must operate within the allowable input signal range (1.3 V to V_{CCA}). Also a DC offset voltage of more than a few millivolts should be avoided, since the internal DC offset compensation circuit has a limited correction range.

If AC coupling is used to remove any DC compatibility requirement, the coupling capacitors must be large enough to pass the lowest input frequency of interest. For example, 1 nF coupling capacitors react with the internal 4.5 kΩ input bias resistors to yield a lower −3 dB frequency of 35 kHz. This then sets a limit on the maximum number of consecutive pulses that can be sensed accurately at the system data rate. Capacitor tolerance and resistor variation must be included for an accurate calculation.

DC-offset compensation

A control loop connected between the inputs of buffer A3 and amplifier A1 (see Fig.1) will keep the input of buffer A3 at its toggle point in the absence of any input signal. Because of the active offset compensation which is integrated in the TZA3034, no external capacitor is required. The loop time constant determines the lower cut-off frequency of the amplifier chain, which is set at approximately 850 Hz.

Input signal level detection

The TZA3034 allows for user-programmable input signal level detection and can automatically disable the switching of the PECL outputs if the input signal is below a set threshold. This prevents the outputs from reacting to noise in the absence of a valid input signal, and insures that data will only be transmitted when the signal-to-noise ratio of the input signal is sufficient for low bit-error-rate system operation. Complementary PECL flags (pins ST and STQ) indicate whether the input signal is above or below the programmed threshold level.

The input signal is amplified and rectified before being compared to a programmable threshold reference. A filter is included to prevent noise spikes from triggering the level detector. This filter has a nominal 1 μs time constant and additional filtering can be achieved by using an external capacitor between V_{CCA} and pin CF (the internal driving impedance nominally is 25 kΩ). The resultant signal is then compared to a threshold current through pin RSET. This current can be set by connecting an external resistor between V_{CCA} and pin RSET, or by forcing a current into pin RSET (see Fig.6).

The relationship between the threshold current and the detected input voltage is approximately:

$$I_{RSET} = 0.0018 \times (V_{DIN} - V_{DINQ})[A] \quad (1)$$

In the formulas (1) and (3), the voltage on pin DIN and pin DINQ is measured as peak-to-peak value.

Since the voltage on pin RSET is held constant at 1.5 V below V_{CCA}, the current flowing into this pin will be:

$$I_{RSET} = \frac{1.5}{R_{ADJ}}[A] \quad (2)$$

Combining these two formulas results in a general formula to calculate R_{ADJ} for a given input signal level detection:

$$R_{ADJ} = \frac{830}{(V_{DIN} - V_{DINQ})}[\Omega] \quad (3)$$

Example: Detection should occur if the differential voltage of the input signals drops below 4 mV (p-p). In this case, a reference current of $0.0018 \times 0.004 = 7.2$ µA should flow into pin RSET. This can be set using a current source or simply by connecting a resistor of the appropriate value. The resistor must be connected between V_{CCA} and pin RSET. In this example the value would be:

$$R_{ADJ} = \frac{830}{0.004} = 207.5\ k\Omega$$

The hysteresis is fixed internally at 3 dB electrical. In the example of above, a differential level below 4 mV (p-p) of the input signal will drive pin ST to LOW, and an input signal level above 5.7 mV (p-p) will drive pin ST to HIGH.

A function is provided to automatically disable the signal transmission when the chip senses that the input signal is below the programmed threshold level. This function can be put into operation by connecting pin JAM with pin STQ. When the input signal is below the programmed threshold level, the data outputs are then forced to a predetermined state (pin DOUT = LOW and pin DOUTQ = HIGH).

Response time of the input signal level detection circuit is determined by the time constant of the input capacitors, together with the filter time constant (1 µs internal plus the additional capacitor at pin CF). For SDH/SONET applications, couple capacitors of 1.5 nF are recommended, leading to a high-pass frequency of approximately 30 kHz and a maximum assert time of 30 µs.

Dissipation

Since the thermal resistance from junction to ambient $R_{th(j-a)}$ of the TSSOP package is higher than the thermal resistance of the SO package (see Chapter “Thermal characteristics”), the dissipation should be considered when using the TZA3034TT version.

The formula to calculate the worst case die temperature is:

$$T_j = T_{amb} + R_{th(j-a)} \times P_{max} \quad (4)$$

where

T_j = junction temperature

T_{amb} = ambient temperature

$R_{th(j-a)}$ = thermal resistance from junction to ambient

P_{max} = maximum power dissipation.

For the TZA3034T (SO package), the worst case die temperature $T_j = 85 + 115 \times 0.3 = 119.5$ °C which is below the maximum operating temperature.

For the TZA3034TT (TSSOP package), the worst case die temperature $T_j = 85 + 150 \times 0.3 = 130$ °C which is higher than the maximum operating temperature, and therefore strongly discouraged. It is recommended to lower the thermal resistance from junction to ambient, e.g. by means of a dedicated board layout.

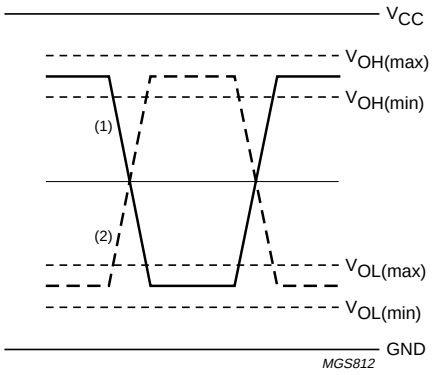
However, if the ambient temperature is limited to 75 °C or the power supply is limited to 3.3 ±0.3 V, the junction temperature will stay below the maximum value without further precautions.

PECL output circuits

The output circuit of ST and STQ is given in Fig.7.

The output circuit of DOUT and DOUTQ is given in Fig.8.

Some PECL termination schemes are given in Fig.9.



(1) Output signal on pins DOUT or ST; complementary to output signal (2).
(2) Output signal on pins DOUTQ or STQ; complementary to output signal (1)

Fig.4 Logic level symbol definitions for PECL outputs.

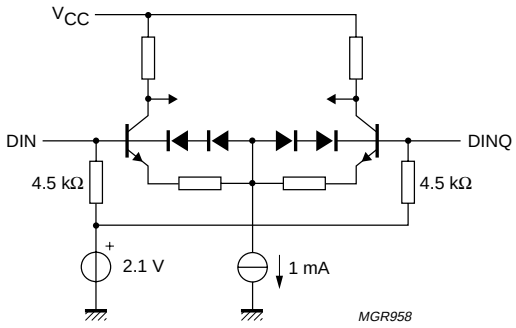
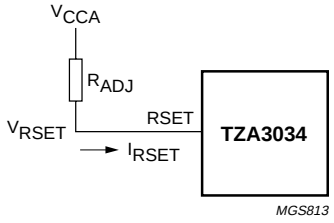
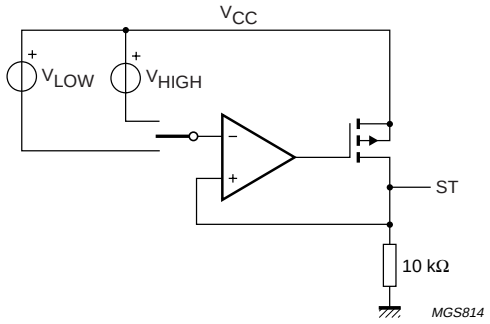


Fig.5 Data input circuit DIN and DINQ.



$V_{RSET} = V_{CCA} - 1.5$ V.

Fig.6 level detect input circuit RSET.



Output STQ is complementary to output ST.

Fig.7 PECL output circuit ST and STQ.

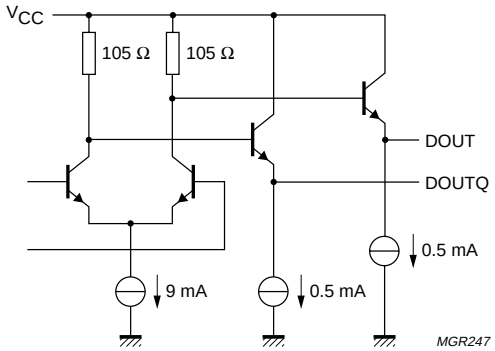
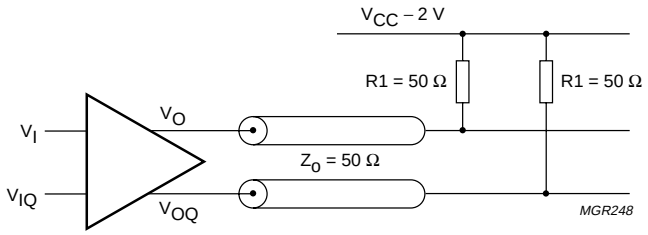
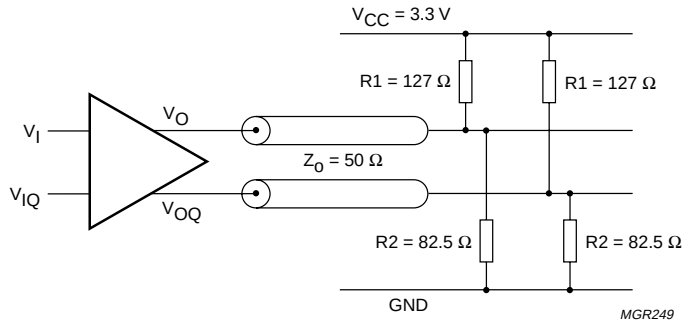


Fig.8 PECL output circuit DOUT and DOUTQ.





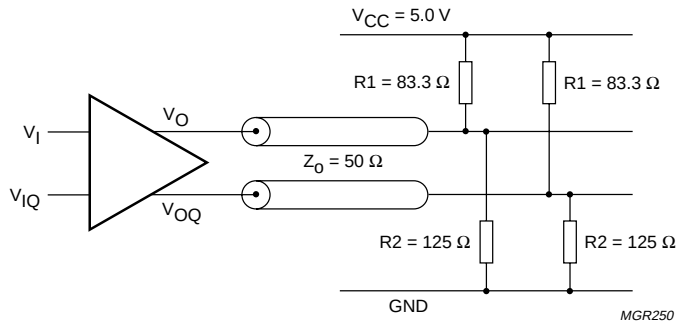


Fig.9 PECL output termination schemes.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–0.5	+6	V
V_n	DC voltage			
	pins DIN, DINQ, CF, JAM and RSET	–0.5	V_{CC} + 0.5	V
	pins STQ, ST, DOUTQ and DOUT	V_{CC} – 2	V_{CC} + 0.5	V
	pin V_{ref}	–0.5	+3.2	V
I_n	DC current			
	pins DIN, DINQ, CF and JAM	–1	+1	mA
	pins STQ, ST, DOUTQ and DOUT	–25	+10	mA
	pin V_{ref}	–2	+2.5	mA
	pin RSET	–2	+2	mA
P_{tot}	total power dissipation	–	300	mW
T_{stg}	storage temperature	–65	+150	°C
T_j	junction temperature	–	150	°C
T_{amb}	ambient temperature	–40	+85	°C

HANDLING

This device is ESD sensitive and should be handled with care. Precautions should be taken to avoid damage through electrostatic discharge. This is particularly important during assembly and handling of the bare die. Additional safety can be obtained by bonding the V_{CC} and GND pads first, the remaining pads may then be bonded to their external connections in any order.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	note 1		
	SO16 package		115	K/W
	TSSOP16 package		150	K/W

Note

1. Thermal resistance from junction to ambient is determined with the IC soldered on a standard single-sided $57 \times 57 \times 1.6$ mm FR4 epoxy printed-circuit board with 35 μm thick copper traces. The measurements are performed in still air.

CHARACTERISTICS

For typical values T_{amb} = 25 °C and V_{CC} = 3.3 V; minimum and maximum values are valid over the entire ambient temperature range and supply voltage range; all voltages are measured with respect to ground; unless otherwise specified.

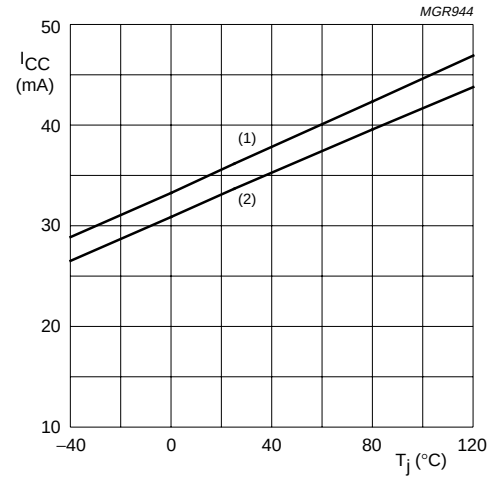
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC}	supply voltage		3	3.3	5.5	V
I_{CCD}	digital supply current	notes 1 and 2	–	18	31	mA
I_{CCA}	analog supply current	note 2	–	15	24	mA
P_{tot}	total power dissipation	notes 1 and 2	–	110	300	mW
T_j	junction temperature		–40	–	+125	°C
T_{amb}	ambient temperature		–40	+25	+85	°C
Input signal pins DIN and DINQ						
$V_{i(se)(p-p)}$	single-ended input signal voltage (peak-to-peak)	note 3	0.002	–	1.5	V
$V_{i(dif)(p-p)}$	differential input signal voltage (peak-to-peak)	note 3	0.004	–	3.0	V
$\lvert V_I \rvert$	absolute input signal voltage		1.3	2.1	V_{CCA}	V
$V_{IO(eq)}$	equivalent input signal offset voltage		–	–	50	µV
$V_{IO(cor)}$	input offset voltage correction	note 4; positive	–	3	–	mV
		note 4; negative	–	–3	–	mV
R_i	input resistance	single-ended	2.9	4.5	7.6	kΩ
C_i	input capacitance	single-ended; note 5	–	–	2.5	pF
$V_{n(i)(rms)}$	equivalent input RMS noise voltage	notes 5 and 6	–	40	60	µV
Input signal level detect pin RSET						
I_{RSET}	reference current	notes 5 and 7	5	–	60	µA
V_{RSET}	reference voltage	referred to V_{CCA}	V_{CCA} – 1.65	V_{CCA} – 1.5	V_{CCA} – 1.4	V
$V_{th(p-p)}$	threshold adjusting range (single-ended and peak-to-peak)	V_i = 155 Mbit/s PRBS 2^7 – 1 sequence; note 5	2	–	12	mV
hys	hysteresis	electrically measured	2	3	6	dB
R_F	filter resistance		14	25	41	kΩ
t_F	filter time constant	CF = 0; note 5	0.5	1.0	2.0	µs
PECL output pins DOUT and DOUTQ						
V_{OL}	LOW-level output voltage	note 8	V_{CC} – 1.84	–	V_{CC} – 1.6	V
V_{OH}	HIGH-level output voltage	note 8	V_{CC} – 1.1	–	V_{CC} – 0.9	V
t_r	rise time	20% to 80%; note 5	–	1.5	2.2	ns
t_f	fall time	80% to 20%; note 5	–	1.5	2.2	ns
t_{PWD}	pulse width distortion	note 5	–	–	0.3	ns
$f_{-3dB(l)}$	low frequency –3 dB point		–	0.85	1.5	kHz
$f_{-3dB(h)}$	high frequency –3 dB point		–	150	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PECL output pins ST and STQ						
V_{OL}	LOW-level output voltage	note 8	V_{CC} – 1.84	–	V_{CC} – 1.6	V
V_{OH}	HIGH-level output voltage	note 8	V_{CC} – 1.1	–	V_{CC} – 0.9	V
C_L	load capacitance	$R_L = \infty$	–	–	20	pF
		R_L = 1 kΩ	–	–	100	pF
		R_L = 50 Ω	–	–	1000	pF
PECL input pin JAM						
V_{IL}	LOW-level input voltage		–	–	V_{CC} – 1.49	V
V_{IH}	HIGH-level input voltage		V_{CC} – 1.165	–	–	V
$I_{I(JAM)}$	JAM input current	note 9	–20	–	+20	µA
Reference voltage output pin V_{ref}						
V_{ref}	reference voltage	note 10	1.165	1.20	1.235	V

Notes

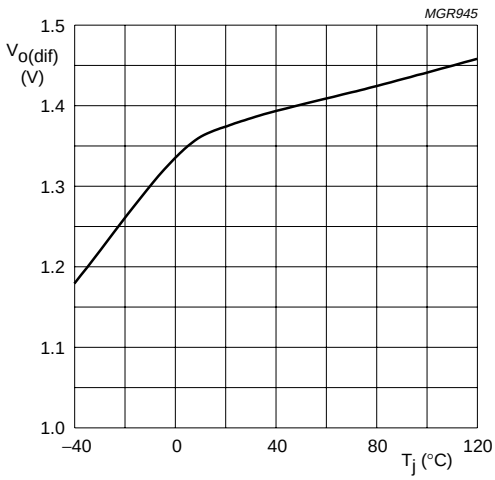
1. PECL outputs (pins DOUT, DOUTQ, ST and STQ) are not connected.
2. Maximum currents are specified at T_j = 125 °C, V_{CC} = 5.5 V and worst case processing.
3. 2 mV (p-p) single-ended is the minimum input signal to achieve full clipping of the output signal. Typical an input signal of 0.5 mV (p-p) single-ended results in a Bit Error Rate (BER) of less than 10^{-10}.
4. If the input is DC coupled, the preceding amplifier's output offset voltage should not exceed these limits, in order to avoid malfunctioning of the DC offset compensation circuit.
5. Specifications guaranteed by design and characterisation. Each device is tested at full operating speed to guarantee RF functionality.
6. $\text{Input RMS noise} = \frac{\text{total output RMS noise}}{\text{low frequency gain}}$
7. The reference current can be set by connecting a resistor between V_{CCA} and pin RSET. The corresponding input signal level detect range is from 2 to 12 mV (p-p) single-ended. See Section "Input signal level detection" for detailed information.
8. R_L = 50 Ω connected to a level of V_{CC} – 2 V (see Fig.9).
9. Internal pull-down resistor of 500 kΩ to DGND.
10. Internal series resistor of 1 kΩ.

TYPICAL PERFORMANCE CHARACTERISTICS



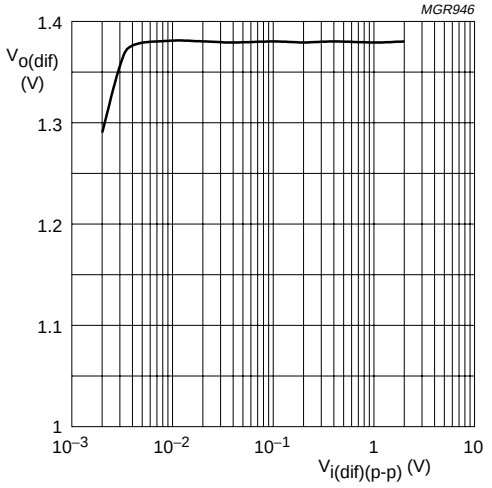
PECL outputs not connected.
(1) V_{CC} = 5.5 V.
(2) V_{CC} = 3.0 V.

Fig.10 Total power supply current as function of junction temperature.



$V_{o(dif)} = V_{DOUT} - V_{DOUTQ}$.

Fig.11 Differential output voltage as function of junction temperature.



$V_{o(dif)} = V_{DOUT} - V_{DOUTQ}$.

Fig.12 Differential output voltage as function of differential input voltage.

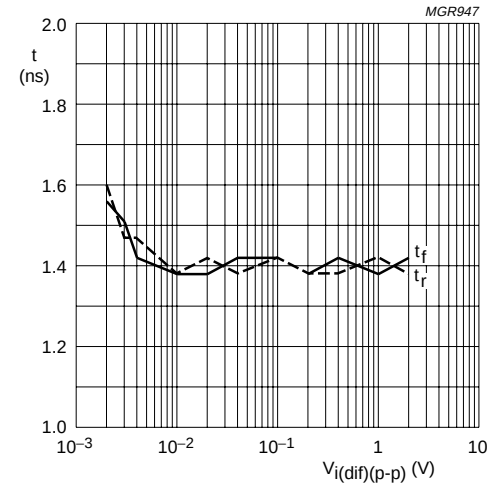


Fig.13 Differential output rise time and fall time as function of differential input voltage.

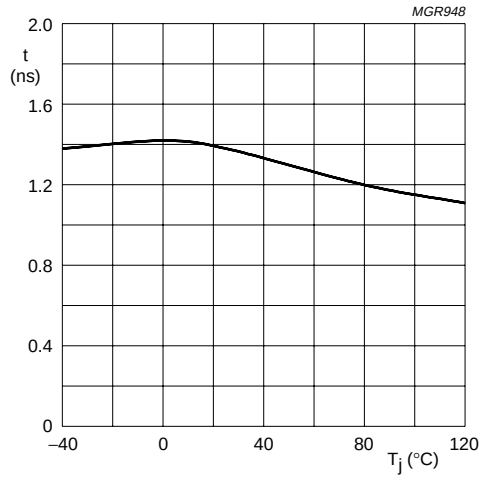
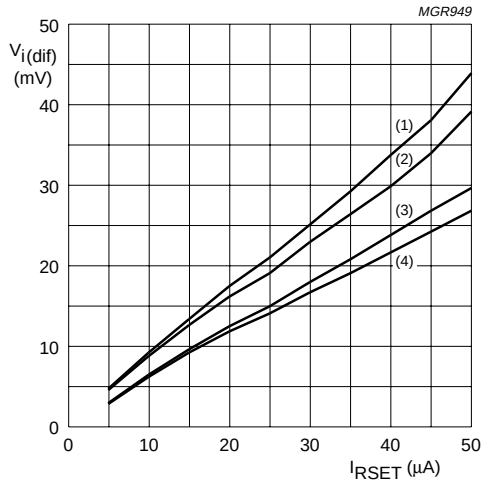


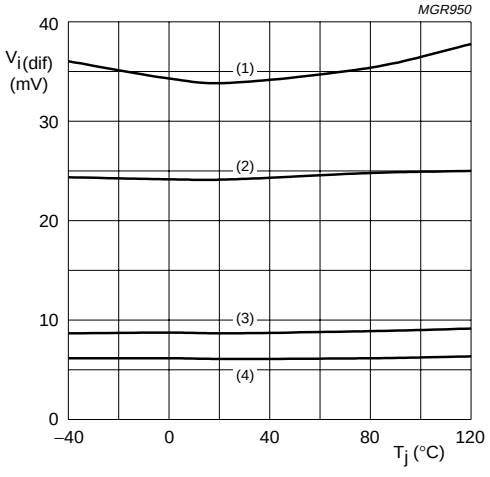
Fig.14 Differential output rise time and fall time as function of junction temperature.



$V_{i(dif)} = V_{DIN} - V_{DINQ}$.

(1) Input high threshold for 1 0 1 0 pattern (pin ST = HIGH).
(2) Input high threshold for $2^7 - 1$ PRBS pattern (pin ST = HIGH).
(3) Input low threshold for 1 0 1 0 pattern (pin ST = LOW).
(4) Input low threshold for $2^7 - 1$ PRBS pattern (pin ST = LOW).

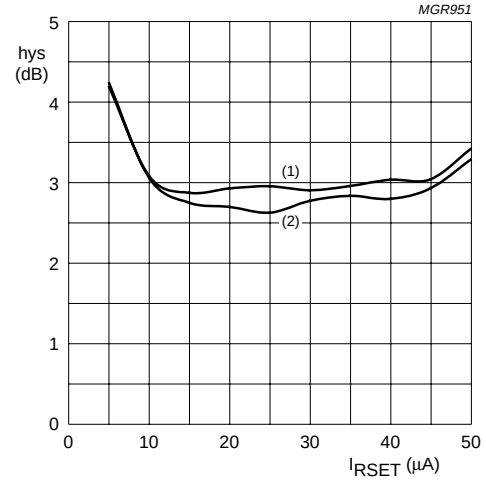
Fig.15 Status detect level as function of I_{RSET}.



$V_{i(dif)} = V_{DIN} - V_{DINQ}$.

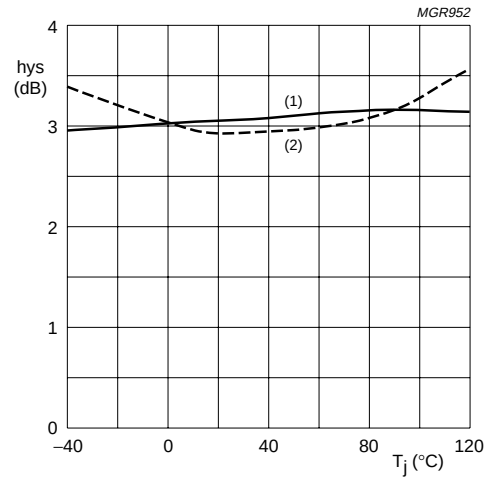
(1) Input high threshold for I_{RSET} = 45 μA (pin ST = HIGH).
(2) Input low threshold for I_{RSET} = 45 μA (pin ST = LOW).
(3) Input high threshold for I_{RSET} = 10 μA (pin ST = HIGH).
(4) Input low threshold for I_{RSET} = 10 μA (pin ST = LOW).

Fig.16 Status detect level as function of junction temperature.



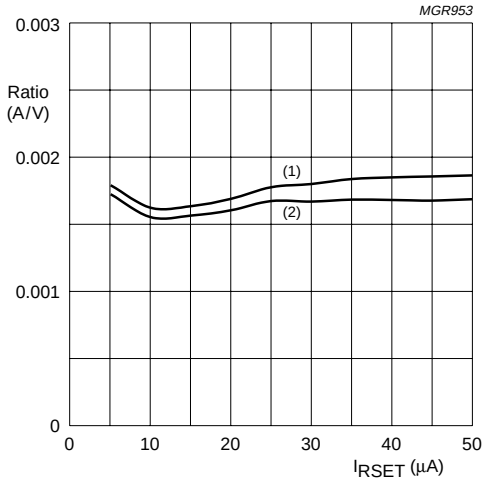
(1) 1 0 1 0 pattern.
(2) $2^7 - 1$ PRBS pattern.

Fig.17 Status detect hysteresis as function of I_{RSET}.



(1) I_{RSET} = 10 µA.
(2) I_{RSET} = 45 µA.

Fig.18 Status detect hysteresis as function of junction temperature.



Ratio = $\frac{I_{RSET}}{V_{i(dif)}}$ where $V_{i(dif)}$ = input low threshold (pin ST = LOW).

(1) $2^7 - 1$ PRBS pattern.
(2) 1 0 1 0 pattern.

Fig.19 Status detect ratio as function of I_{RSET}.

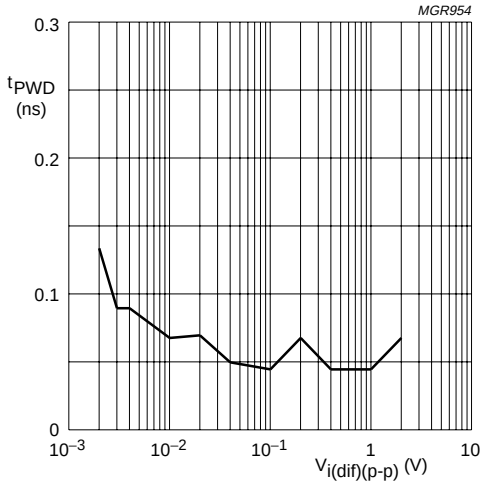
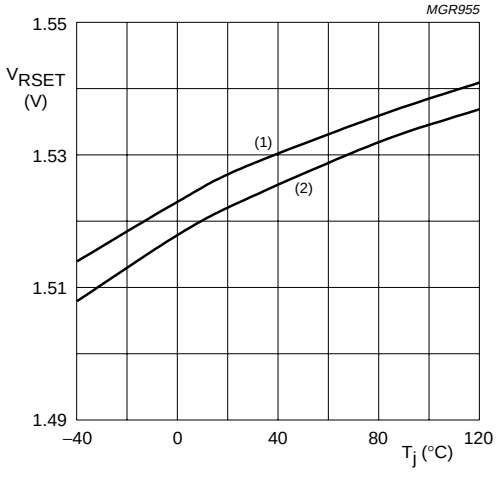


Fig.20 Pulse Width Distortion (t_{PWD}) as function of differential input voltage.



$V_{RSET} = V_{CCA} - 1.5$ V.
(1) V_{CC} = 5.5 V.
(2) V_{CC} = 3.0 V.

Fig.21 V_{RSET} as function of junction temperature.

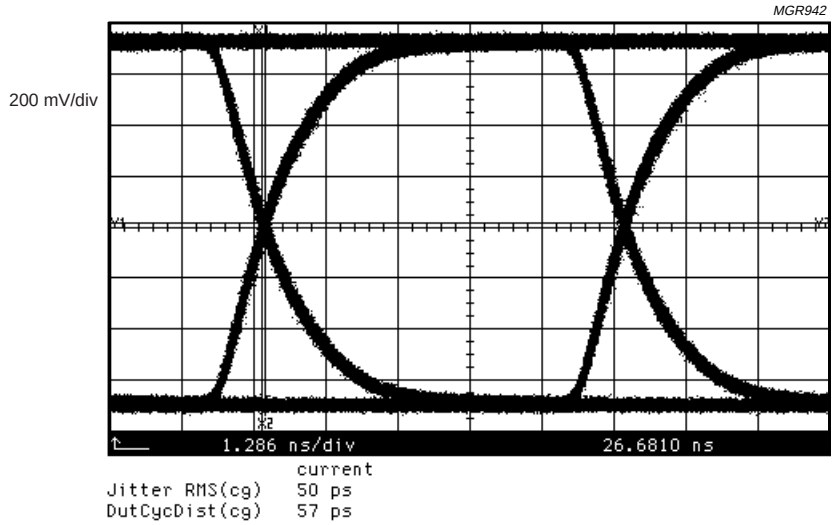


Fig.22 Differential output waveform with 4 mV differential input voltage.

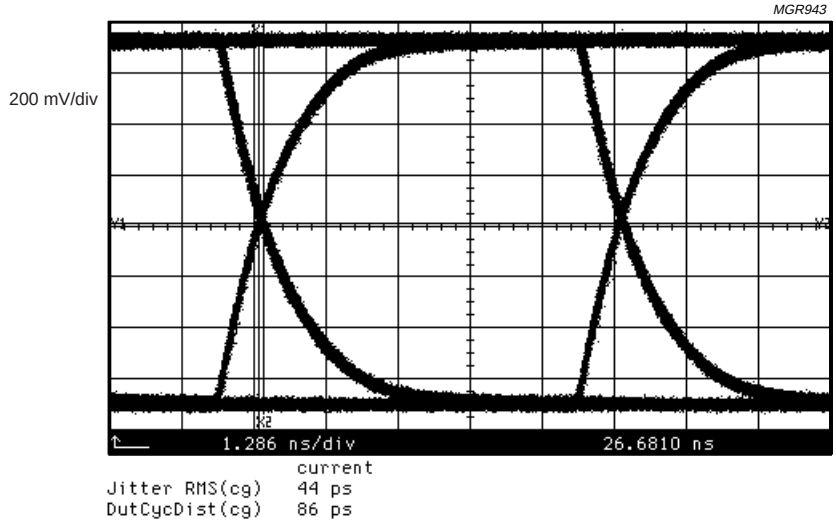
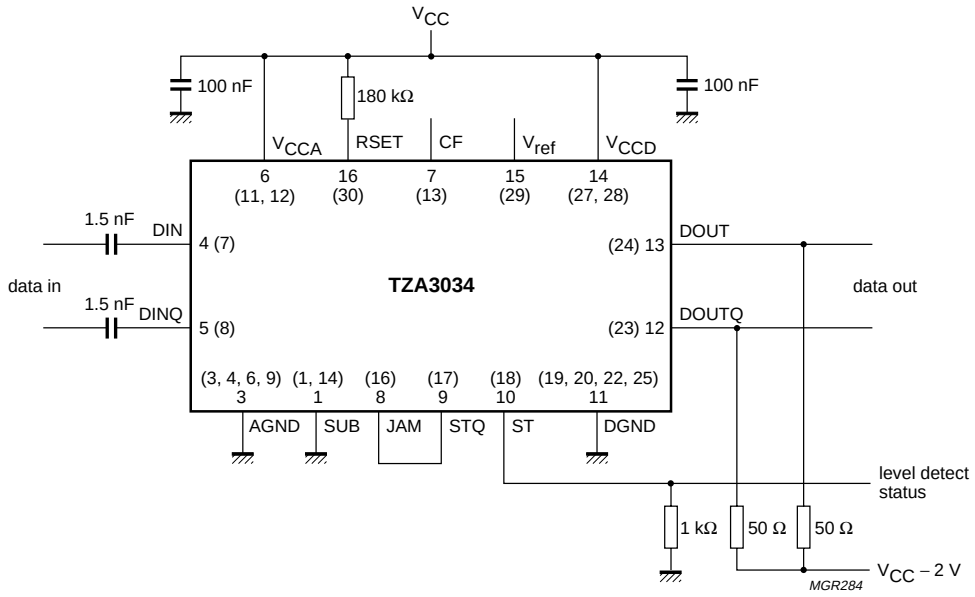


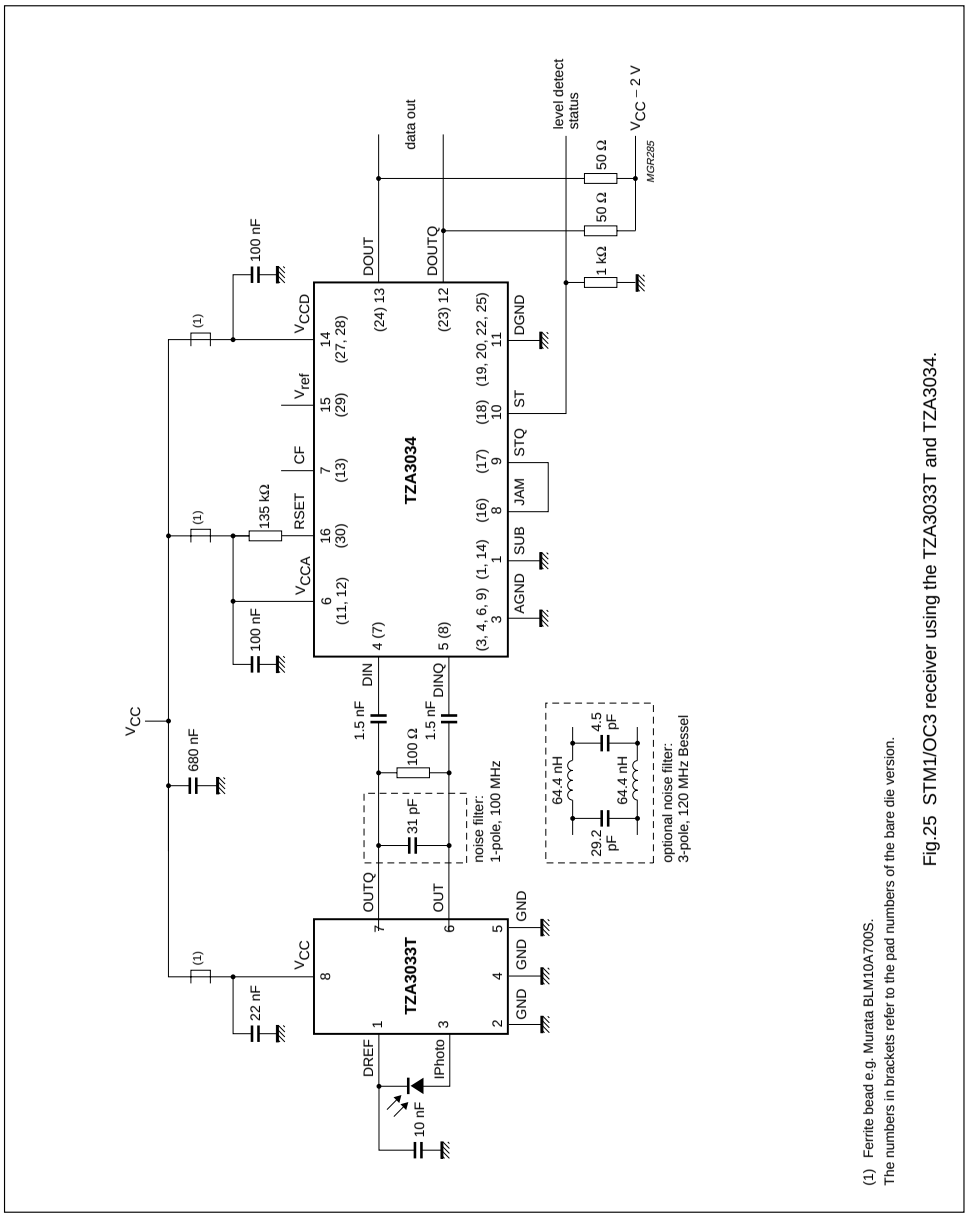
Fig.23 Differential output waveform with 2 V differential input voltage.

APPLICATION INFORMATION



The numbers in brackets refer to the pad numbers of the bare die version.

Fig.24 Application diagram.



(1) Ferrite bead e.g. Murata BLM10A700S.
The numbers in brackets refer to the pad numbers of the bare die version.

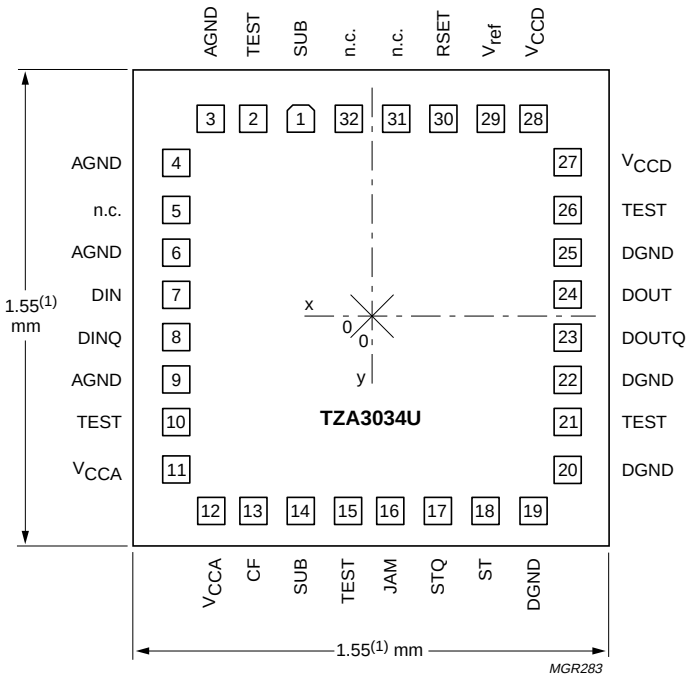
Fig.25 STM1/OC3 receiver using the TZA3033T and TZA3034.

BONDING PADS

SYMBOL	PAD	COORDINATES(1)	
		X	Y
SUB	1	–235.7	+647.8
TEST	2	–392.8	+647.8
AGND	3	–532.8	+647.8
AGND	4	–647.8	+507.1
n.c.	5	–647.8	+350.0
AGND	6	–647.8	+210.0
DIN	7	–647.8	+70.0
DINQ	8	–647.8	–70.0
AGND	9	–647.8	–210.0
TEST	10	–647.8	–350.0
V_{CCA}	11	–647.8	–507.1
V_{CCA}	12	–532.8	–647.8
CF	13	–392.8	–647.8
SUB	14	–235.7	–647.8
TEST	15	–78.6	–647.8
JAM	16	+61.4	–647.8
STQ	17	+218.5	–647.8
ST	18	+375.6	–647.8
DGND	19	+532.7	–647.8
DGND	20	+647.8	–507.1
TEST	21	+647.8	–350.0
DGND	22	+647.8	–210.0
DOUTQ	23	+647.8	–70.0
DOUT	24	+647.8	+70.0
DGND	25	+647.8	+210.0
TEST	26	+647.8	+350.0
V_{CCD}	27	+647.8	+507.1
V_{CCD}	28	+532.7	+647.8
V_{ref}	29	+392.7	+647.8
RSET	30	+235.6	+647.8
n.c.	31	+78.5	+647.8
n.c.	32	–78.6	+647.8

Note

1. The x and y coordinates represent the position of the centre of the pad with respect to the centre of the die (see Fig.26).



(1) Typical value.

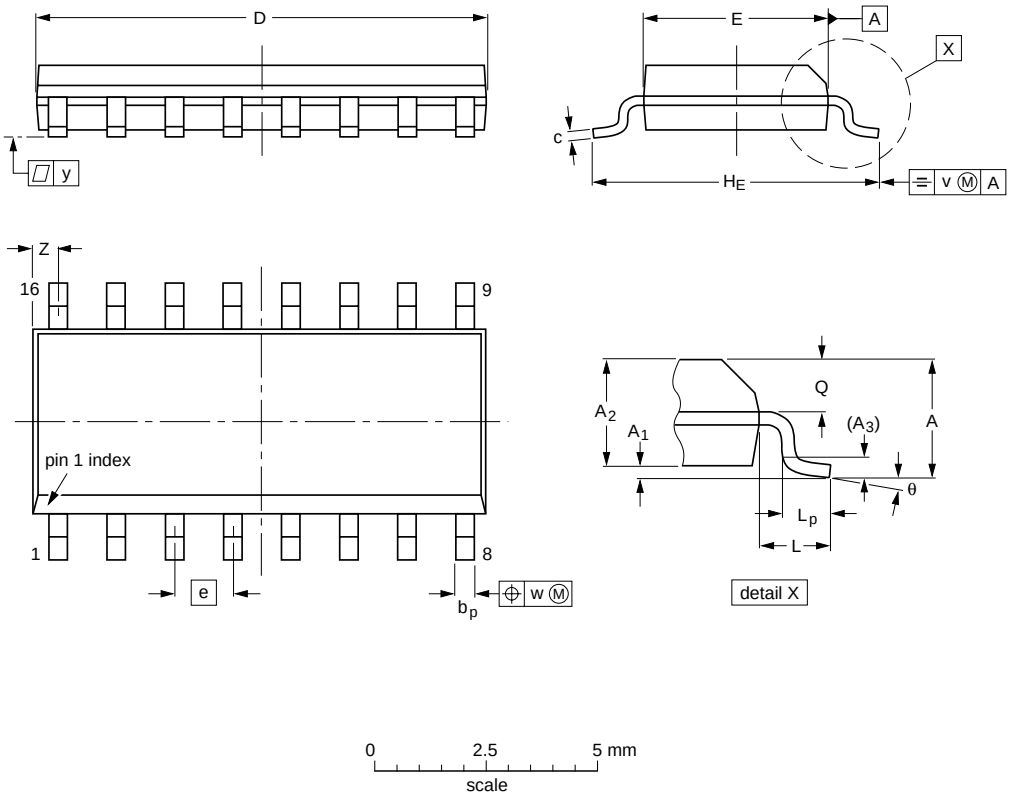
Fig.26 Bonding pad locations of TZA3034U.

Table 1 Physical characteristics of bare die

PARAMETER	VALUE
Glass passivation	2.1 μm PSG (PhosphoSilicate Glass) on top of 0.65 μm oxynitride
Bonding pad dimension	minimum dimension of exposed metallization is 90 × 90 μm (pad size = 100 × 100 μm)
Metallization	1.22 μm W/AlCu/TiW
Thickness	380 μm nominal
Size	1.55 × 1.55 mm (2.4 mm^2)
Backing	silicon; electrically connected to GND potential through substrate contacts
Attache temperature	<440 °C; recommended die attache is glue
Attache time	<15 s

PACKAGE OUTLINES

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

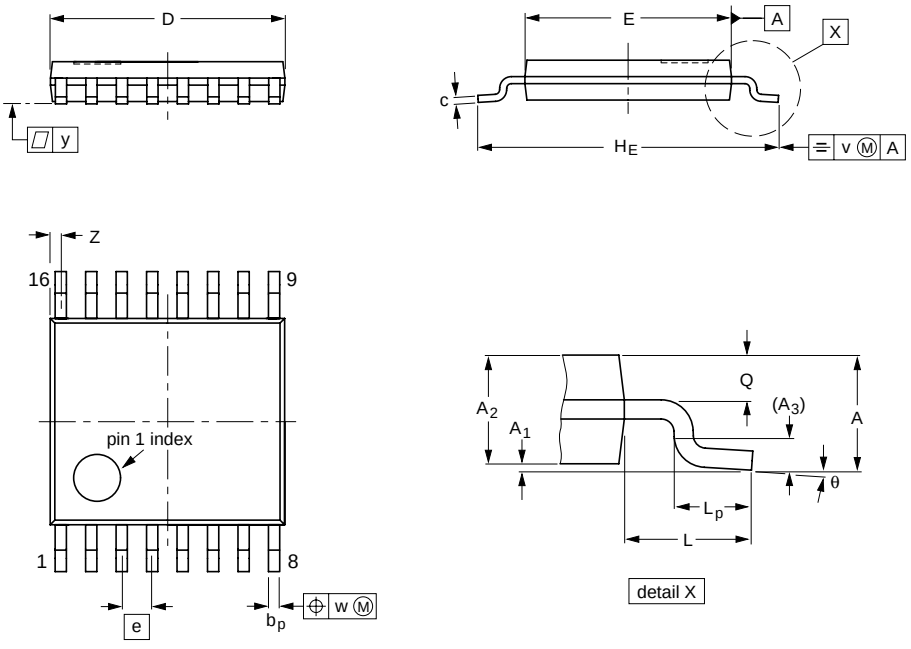
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

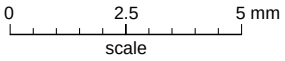
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~95-01-23~~ 97-05-22

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				~~94-07-12~~ 95-04-04

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
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NOTES

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