DATA SHEET

TZA3014

2.5 Gbits/s postamplifier with level detector

Product specification

Supersedes data of 2000 Aug 09

File under Integrated Circuits, IC19

2001 Jun 25

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2.5 Gbits/s postamplifier with level detector

TZA3014

FEATURES

- Single 3.3 V power supply
- Wideband operation from 50 kHz to 2.5 GHz (typical value)
- Fully differential
- On-chip DC-offset compensation without external capacitor
- Interfacing with supplied positive or negative logic
- Positive Emitter Coupled Logic (PECL) or Current-Mode Logic (CML) compatible data outputs adjustable from 200 to 800 mV (p-p) single-ended
- Power-down capability for unused output or detector
- Rise and fall times of 80 ps (typical value)
- Inverted output possible
- Input level detection circuit for Received Signal Strength Indicator (RSSI) and Loss Of Signal (LOS), programmable from 0.4 to 400 mV (p-p) single-ended, with open-drain comparator output for directly interfacing positive or negative logic
- Reference voltage for output level and LOS adjustment
- HTQFP32 and HBCC32 plastic packages with exposed pad
- Mute input.

APPLICATIONS

- Postamplifier for SDH/SONET transponder
- SDH/SONET wavelength converter
- PECL driver
- Fibre channel arbitrated loop
- Signal level detectors
- Swing converter CML 200 mV (p-p) to PECL 800 mV (p-p)
- 2.5 GHz clock amplification.

GENERAL DESCRIPTION

The TZA3014 is a low gain postamplifier with a LOS detector and a RSSI designed for use in critical signal path control applications, such as loop-through or Wavelength Division Multiplexing (WDM). The signal path is capable of operating from 50 kHz up to 2.5 GHz.

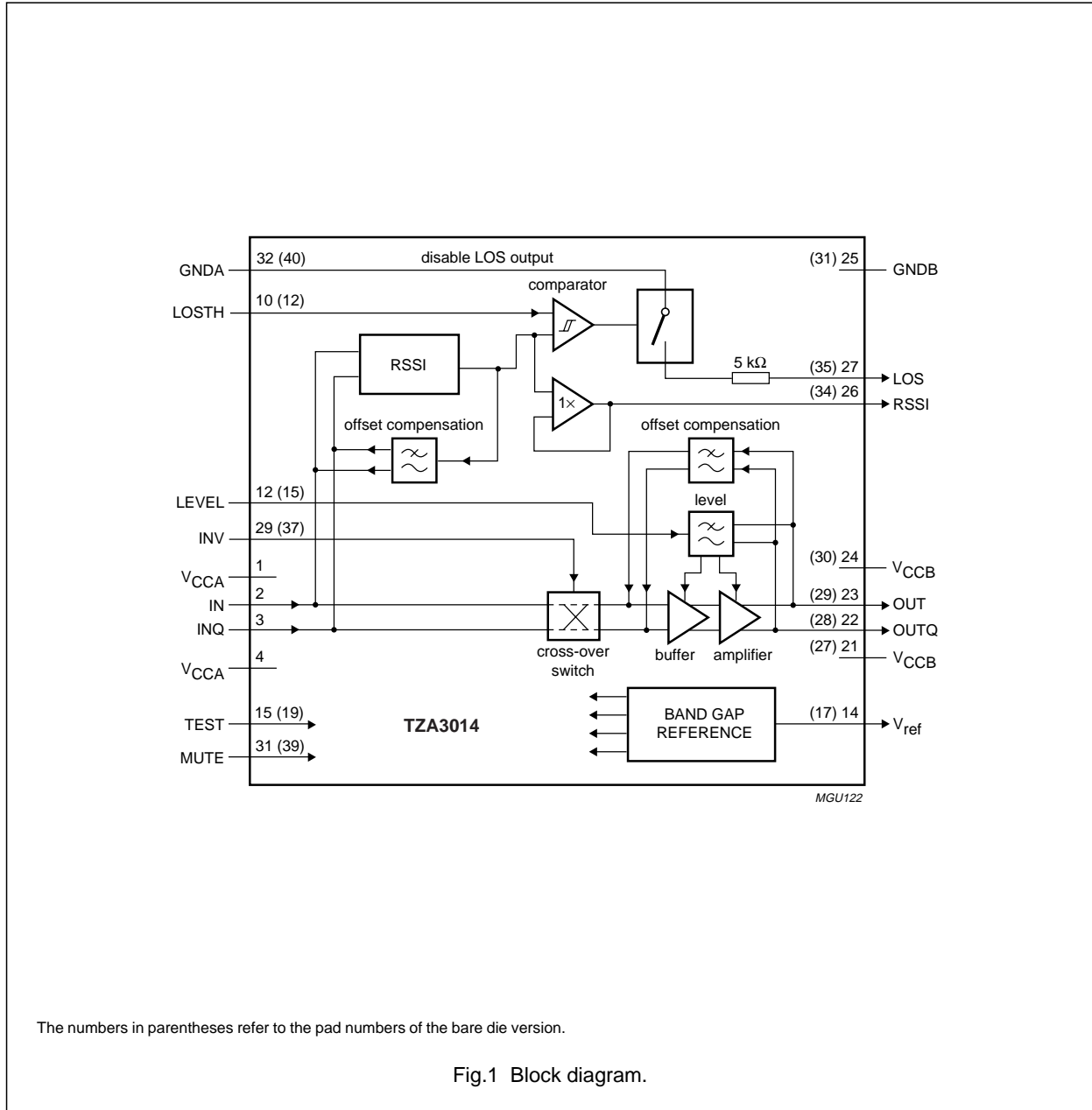The TZA3014 can be delivered in HTQFP32 and HBCC32 packages and as bare die.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3014HT	HTQFP32	plastic, heatsink thin quad flat package; 32 leads; body $5 \times 5 \times 1.0$ mm	SOT547-2
TZA3014VH	HBCC32	plastic, heatsink bottom chip carrier; 32 terminals; body $5 \times 5 \times 0.65$ mm	SOT560-1
TZA3014U	–	bare die; $2.22 \times 2.22 \times 0.28$ mm	–

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BLOCK DIAGRAM

The numbers in parentheses refer to the pad numbers of the bare die version.

Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	PAD	TYPE[1]	DESCRIPTION
V_{CCA}	1	1	S	supply voltage for input and LOS detector
IN	2	2	I	differential input; complimentary to pin INQ; DC bias level is set internally at approximately $V_{CC} - 0.33$ V
INQ	3	3	I	differential input; complimentary to pin IN; DC bias level is set internally at approximately $V_{CC} - 0.33$ V
V_{CCA}	4	4	S	supply voltage for input and LOS detector
n.c.	–	5	–	not connected
n.c.	–	6	–	not connected
n.c.	5	7	–	not connected
n.c.	6	8	I	not connected
n.c.	7	9	I	not connected
n.c.	8	10	S	not connected
n.c.	9	11	S	not connected
LOSTH	10	12	I	input for setting threshold level of LOS detector; threshold level is set by connecting external resistors between pins V_{CCA} and V_{ref}; when forced to GNDA or not connected, the LOS detector is switched off
n.c.	11	13	I	not connected
n.c.	–	14	–	not connected
LEVEL	12	15	I	input for setting AC level of the output circuit; output signal level is set by connecting external resistors between pins V_{CCA} and V_{ref}; when forced to V_{CCA} or not connected, pins OUT and OUTQ will be switched off
n.c.	13	16	I	not connected
V_{ref}	14	17	O	reference voltage for programming output level circuit and LOS threshold; typical value is $V_{CC} - 1.6$ V; no external capacitor allowed
n.c.	–	18	–	not connected
TEST	15	19	I	for test purposes only; to be left open-circuit in the application
n.c.	16	20	S	not connected
n.c.	17	21	S	not connected
n.c.	18	22	O	not connected
n.c.	19	23	O	not connected
n.c.	20	24	S	not connected
n.c.	–	25	–	not connected
n.c.	–	26	–	not connected
V_{CCB}	21	27	S	supply voltage for output circuit
OUTQ	22	28	O	PECL or CML compatible differential output; complimentary to pin OUT
OUT	23	29	O	PECL or CML compatible differential output; complimentary to pin OUTQ
V_{CCB}	24	30	S	supply voltage for output circuit
GNDB	25	31	S	ground for output circuit
n.c.	–	32	O	not connected
n.c.	–	33	O-DRN	not connected

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SYMBOL	PIN	PAD	TYPE[1]	DESCRIPTION
RSSI	26	34	O	RSSI output
LOS	27	35	O-DRN	output of LOS detector; direct drive to either positive or negative supplied logic via internal 5 kΩ resistor
n.c.	28	36	TTL	not connected
INV	29	37	TTL	input to invert the signal at pins OUT and OUTQ; supports positive or negative logic
n.c.	30	38	TTL	not connected
MUTE	31	39	TTL	input to mute the output signal on pins OUT ('0') and OUTQ ('1'); supports positive or negative logic
GNDA	32	40	S	ground for input and LOS detector
GNDp	pad	–	S	ground pad (exposed die pad)

Note

1. Pin type abbreviations: O = output, I = input, S = power supply, TTL = logic input and O-DRN = open-drain output.

Fig.2 Pin configuration HTQFP32 package.
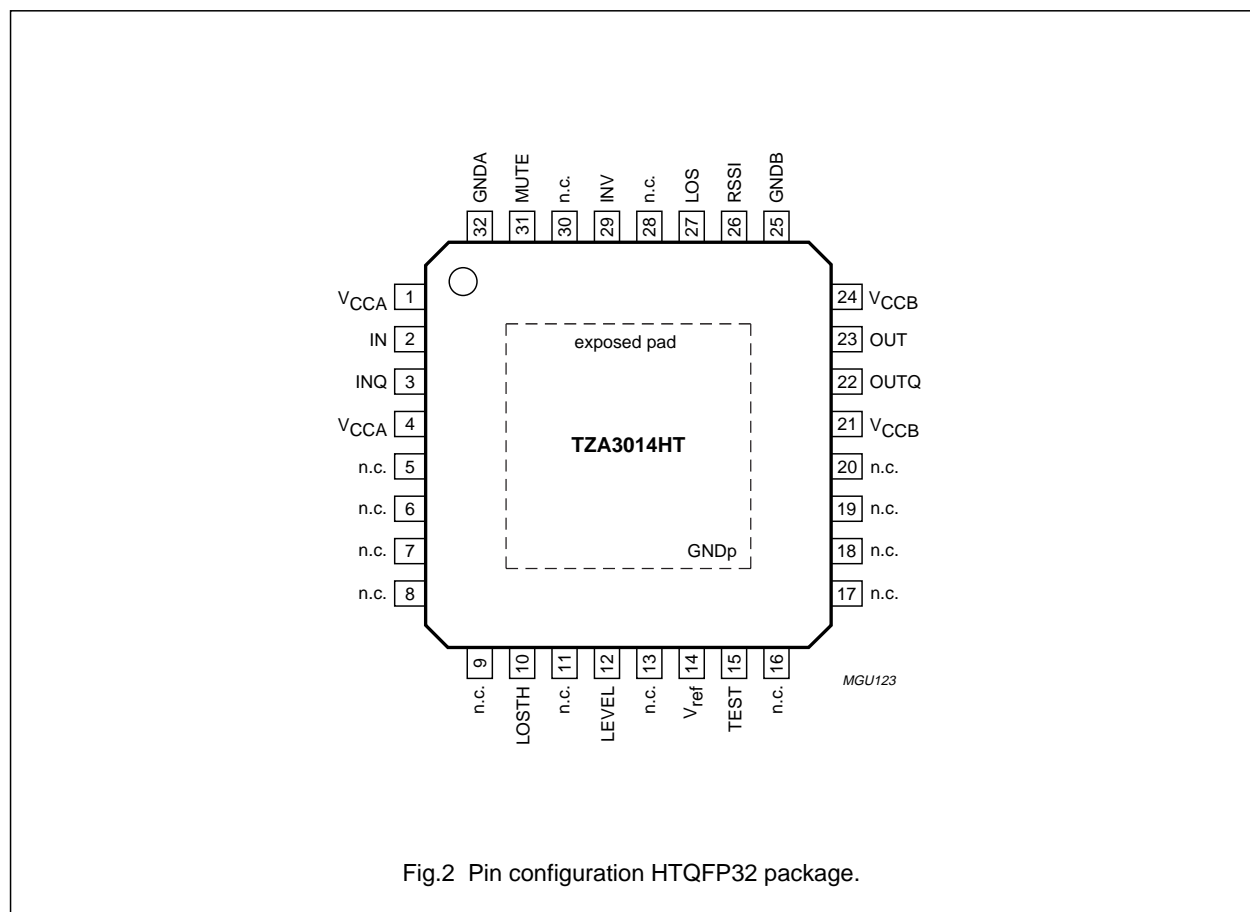
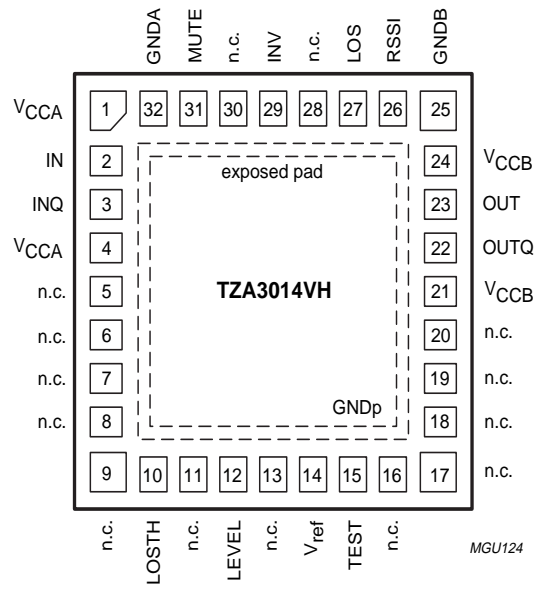## 2.5 Gbits/s postamplifier with level detector

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Fig.3 Pin configuration HBCC32 package.

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FUNCTIONAL DESCRIPTION

The TZA3014 is a postamplifier with a RSSI circuit to provide output signals for RSSI and LOS (see Fig.1). The input signal can be amplified to a programmable level. An active level control circuit ensures this level. The control voltage on pin INV inverts the outputs, so avoiding a required complicated Printed Circuit Board (PCB) layout. An offset compensation circuit minimizes the effect of any voltage offset present at the input.

The RSSI and LOS detector are based on a 7-stage 'successive detection' circuit which provides a logarithmic output. The LOS detector is followed by a comparator with a programmable threshold. The input signal level detection is implemented to check if the input signal is above the user-programmed level. The user can ensure that data will only be transmitted when the input signal-to-noise ratio is sufficient for low bit error rate system operation. A second offset compensation circuit minimizes the effect of any voltage offset present in the logarithmic amplifier.

RF input circuit

The input circuit contains internal 50 Ω resistors decoupled to V_{CCA} via an internal common mode 12 pF capacitor (see Fig.4).

The inputs IN and INQ are DC-biased at approximately $V_{CCA} - 0.33$ V by an internal reference generator. The TZA3014 can be DC-coupled, but AC coupling is preferred. When DC-coupled, the drive source must operate within the allowable input range ($V_{CCA} - 1.0$ V to $V_{CCA} + 0.3$ V). The DC-offset voltage should stay below a few millivolts since the internal DC-offset compensation circuit has a limited correction range. When AC-coupled, do not use capacitors that cause a 3 dB cut-off point at 50 kHz (postamplifier cut-off point) or at 1 MHz (RSSI cut-off point).

RF output circuit

Matching the outputs of the postamplifier (see Fig.5) is not mandatory. In most applications, the receiving end of the transmission line will be properly matched, causing very few reflections.

Matching the transmitting end of the transmission line to absorb reflections only, is recommended for very sensitive applications.

In such cases, 100 Ω pull-up resistors should be connected to V_{CCB} and pins OUT and OUTQ as close as possible to the IC. However, for most applications these matching resistors are not required.
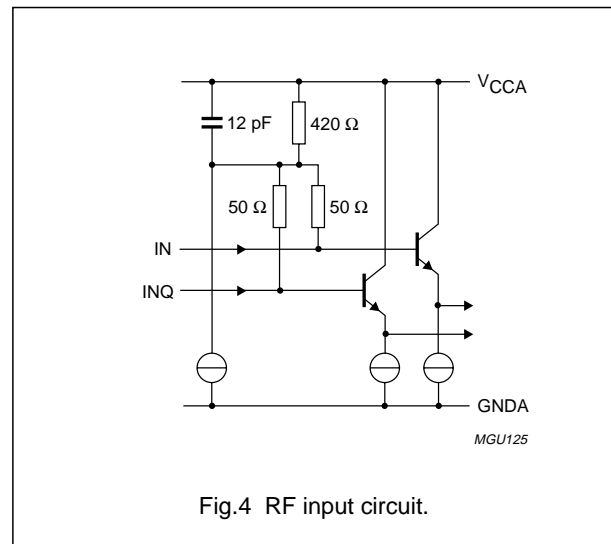

Fig.4 RF input circuit.

RF output level adjustment

The output level can be made compatible with CML or PECL by adjusting the voltage on pin LEVEL. The DC voltages on pins OUT and OUTQ relate to the DC voltage on pin LEVEL. Due to the effect of the 50 Ω load resistance at the receiving end, for a given peak-to-peak value on pins OUT and OUTQ, a different voltage is required on pin LEVEL in case the output is AC-coupled and when the output is DC-coupled (see Figs 5 and 6).
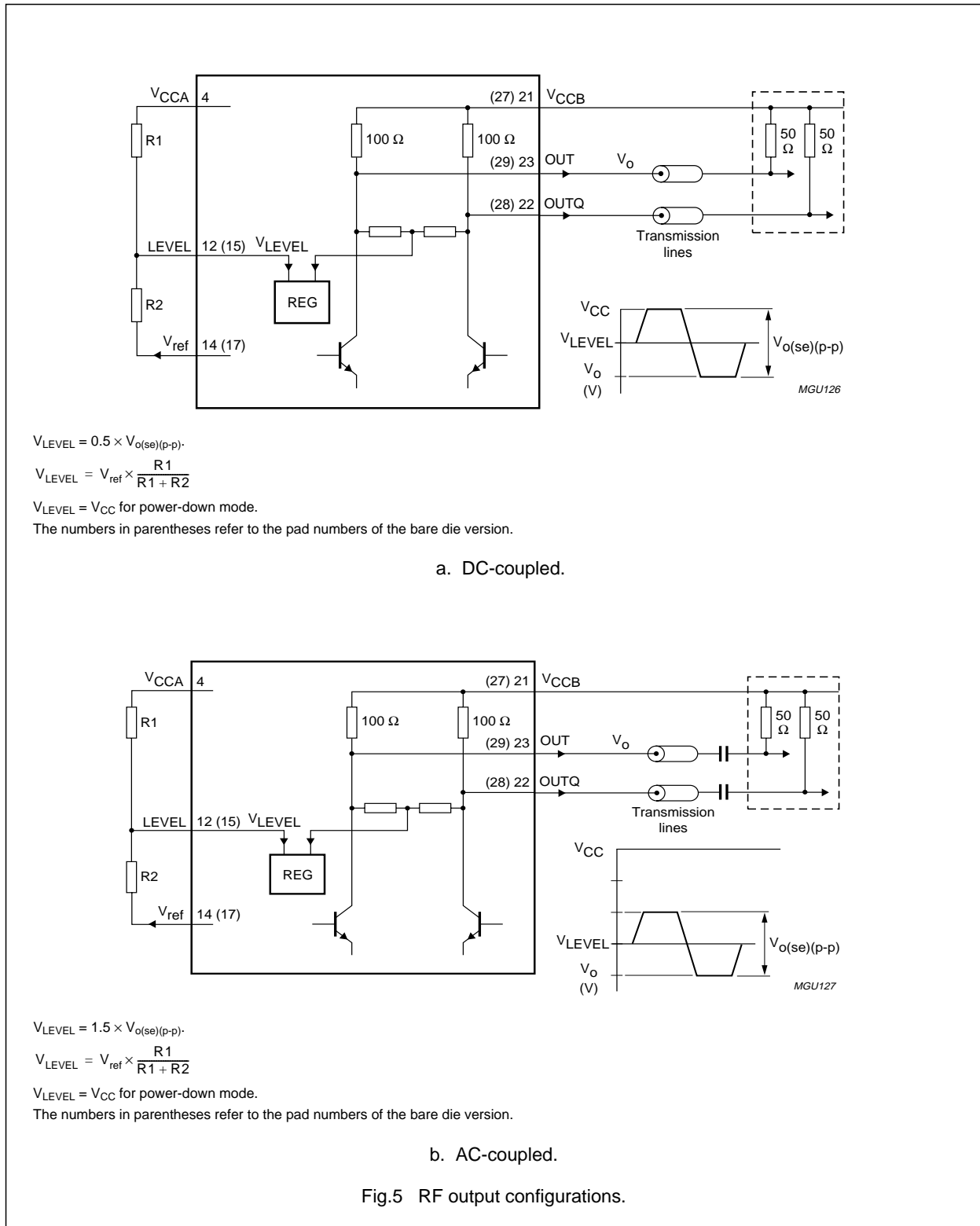
When pin LEVEL is not connected or connected to V_{CCA}, the postamplifier is in power-down state (see Fig.5).

DC-offset compensation loop

A DC-offset compensation loop connected between the amplifier output and the buffer input maintains the toggle point at the buffer input when there is no input signal (see Fig.1). This active control circuit is integrated and does not require an external capacitor. The loop time constant determines the lower cut-off frequency of the amplifier chain, and is internally fixed at approximately 5 kHz.

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$V_{LEVEL} = 0.5 \times V_{o(se)(p-p)}$.

$$V_{LEVEL} = V_{ref} \times \frac{R1}{R1 + R2}$$

$V_{LEVEL} = V_{CC}$ for power-down mode.

The numbers in parentheses refer to the pad numbers of the bare die version.

a. DC-coupled.

$V_{LEVEL} = 1.5 \times V_{o(se)(p-p)}$.

$$V_{LEVEL} = V_{ref} \times \frac{R1}{R1 + R2}$$

$V_{LEVEL} = V_{CC}$ for power-down mode.

The numbers in parentheses refer to the pad numbers of the bare die version.

b. AC-coupled.
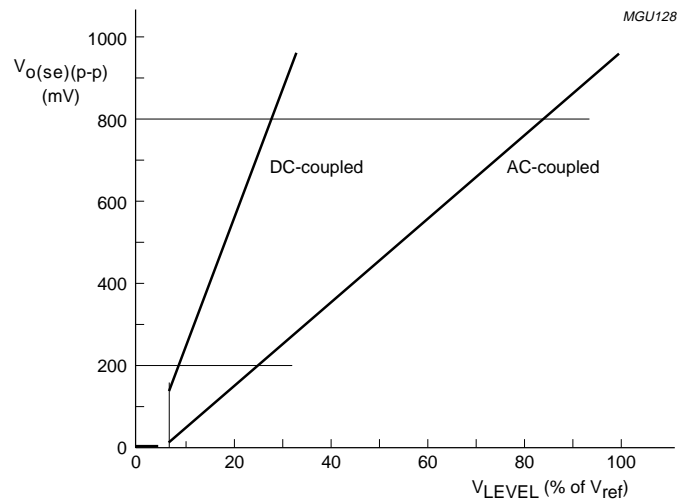
Fig.5   RF output configurations.

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Fig.6 Output signal as a function of V_{LEVEL}.

TTL logic inputs MUTE and INV

It should be noted that switch control voltages in positive logic are inverted in case a negative supply voltage is used (see Fig.7).

Output signal as a function of inputs MUTE and INV

The default logic level for inputs MUTE and INV is 0 in case these pins are not connected. See Tables 1 and 2.

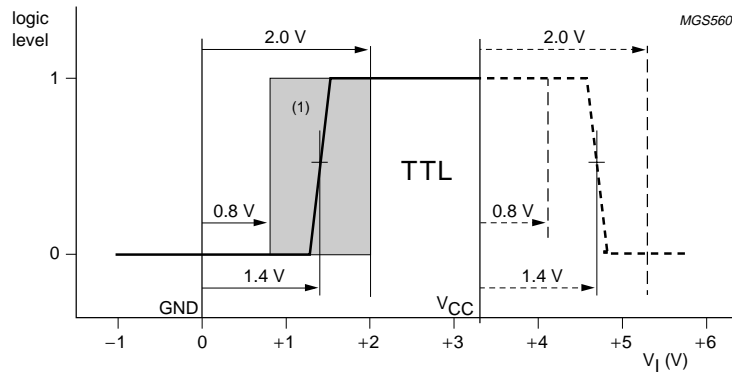**Table 1** OUT and OUTQ as a function of input MUTE

MUTE	OUT	OUTQ
0	IN	INQ
1	'0'	'1'

Table 2 OUT and OUTQ as a function of input INV
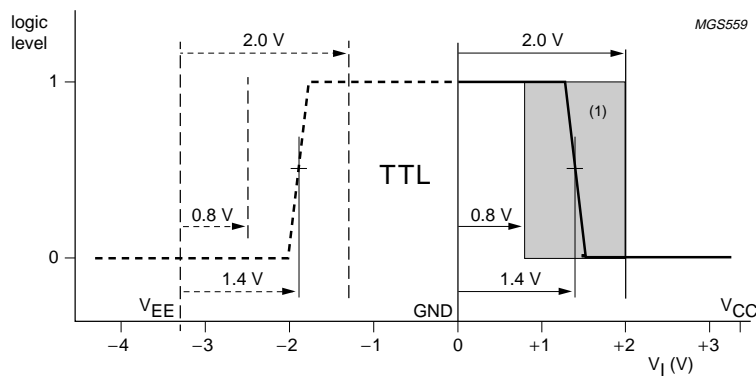
INV	OUT	OUTQ
0	IN	INQ
1	INQ	IN

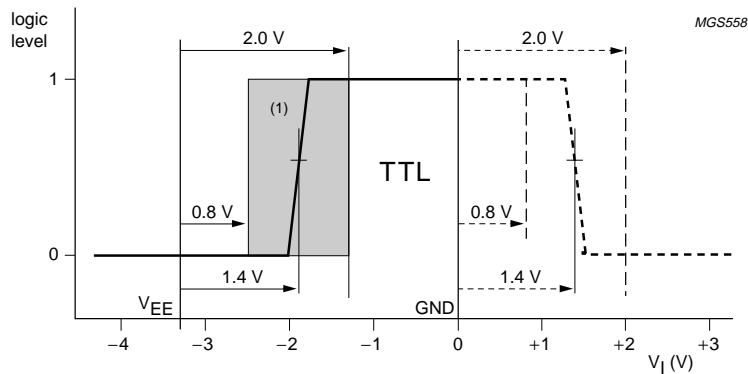## 2.5 Gbits/s postamplifier with level detector

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a. Positive supply voltage (V_{CC}) and positive input voltage (V_{CC}).

b. Negative supply voltage (V_{EE}) and positive input voltage (V_{CC}).

c. Negative supply voltage (V_{EE}) and negative input voltage (V_{EE}).

(1) Level not defined.

Fig.7 Logic levels on pins MUTE and INV as a function of the supply voltages.

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RSSI and LOS detection

The TZA3014 monitors the level of the input AC signal. This function can prevent the output circuit from reacting to noise in case there is no valid input signal, and can ensure that only data is transmitted when there is sufficient input signal for low bit error rate system operation.

The RSSI uses seven limiting amplifiers in a 'successive detection' topology to closely approximate a logarithmic response over a total range of 70 dB. The AC signal is full-wave rectified by a detector at each amplifier stage. Each detector output has a current driver followed by a low-pass filter providing the first stage in the recovery of the average value of the demodulated input signal. The total current from each detector output is converted to a voltage by an internal load resistor and then buffered. When the RSSI output is used, input pin LOSTH is not to be connected to GND (standby mode). The RSSI output follows the internal 3 dB hysteresis of the LOS comparator. The LOS comparator detects when the input signal level rises above a programmable fixed threshold. Then pin LOS gets a LOW-level. The threshold level is determined by the voltage on pin LOSTH and by the level of the input AC signal (see Fig.8). A filter with a nominal time constant of 1 μs prevents noise spikes from triggering the level detector.

The LOS comparator has an internal 3 dB hysteresis and drives an open-drain circuit with a 5 kΩ internal resistor allowing it to directly interface positive or negative logic circuits (see Fig.9).

Its response is independent of the input signal polarity due to the circuit design and to the demodulating action of the detector which transforms the alternating input voltage to a rectified and filtered quasi DC output signal. The logarithmic voltage slope of the TZA3014 is $\varphi = \frac{1}{12.5}$ dB/mV and mostly is independent of temperature and supply voltage due to four feedback loops in the reference circuit. The LOS detector output voltage is derived from V_{ref}.

The sensitivity of the LOS detector is affected by the RMS value of the input signal which, in its turn, depends on the frequency.

V_{LOSTH} can be calculated using the following formula:

$V_{LOSTH} = V_{RSSI} =$

$$V_{CC} + 0.458 - S_{RSSI} \times 20 \log\left(\frac{V_{i(p\text{-}p)}}{26E-8}\right) \qquad (1)$$

where S_{RSSI} in [mV/dB]; V_{LOSTH}, V_{RSSI} and $V_{i(p\text{-}p)}$ in [V].

(1) PRBS pattern input signal with a frequency <1 GHz.
(2) Linearity error typically 0.5 dB.
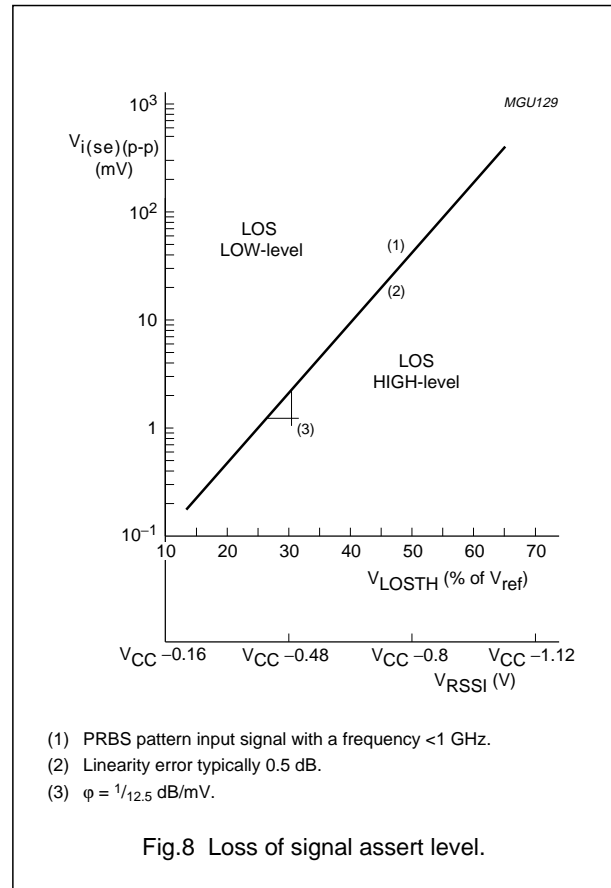(3) $\varphi = \frac{1}{12.5}$ dB/mV.

Fig.8 Loss of signal assert level.

Example: a 200 mV (p-p) single-ended 1.2 GB/s PRBS input signal will have a V_{RSSI} voltage of $V_{CC} - 1.013$ V.

If the offset voltage of the first stage increases above a certain level, the high DC gain of the amplifier circuit will cause successive stages to limit prematurely. This is prevented by the LOS detector offset control loop which extends the lower end of the amplifier's dynamic range. The offset is automatically and continuously compensated by a feedback path from the last stage. An offset at the output of the logarithmic converter is equivalent to a change of amplitude at the input.

Using DC-coupling, with signal absence, and V_{IN} not equal to V_{INQ} (mute), the LOS detector detects full signal. Only very small signals with an average value equal to zero, can result into a zero output.

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a. Positive supply and positive logic.   b. Negative supply and positive logic.

c. Negative supply and negative logic.

$V_{CC} - V_{EE} < 7$ V.

Fig.9 Loss of signal output pin LOS.
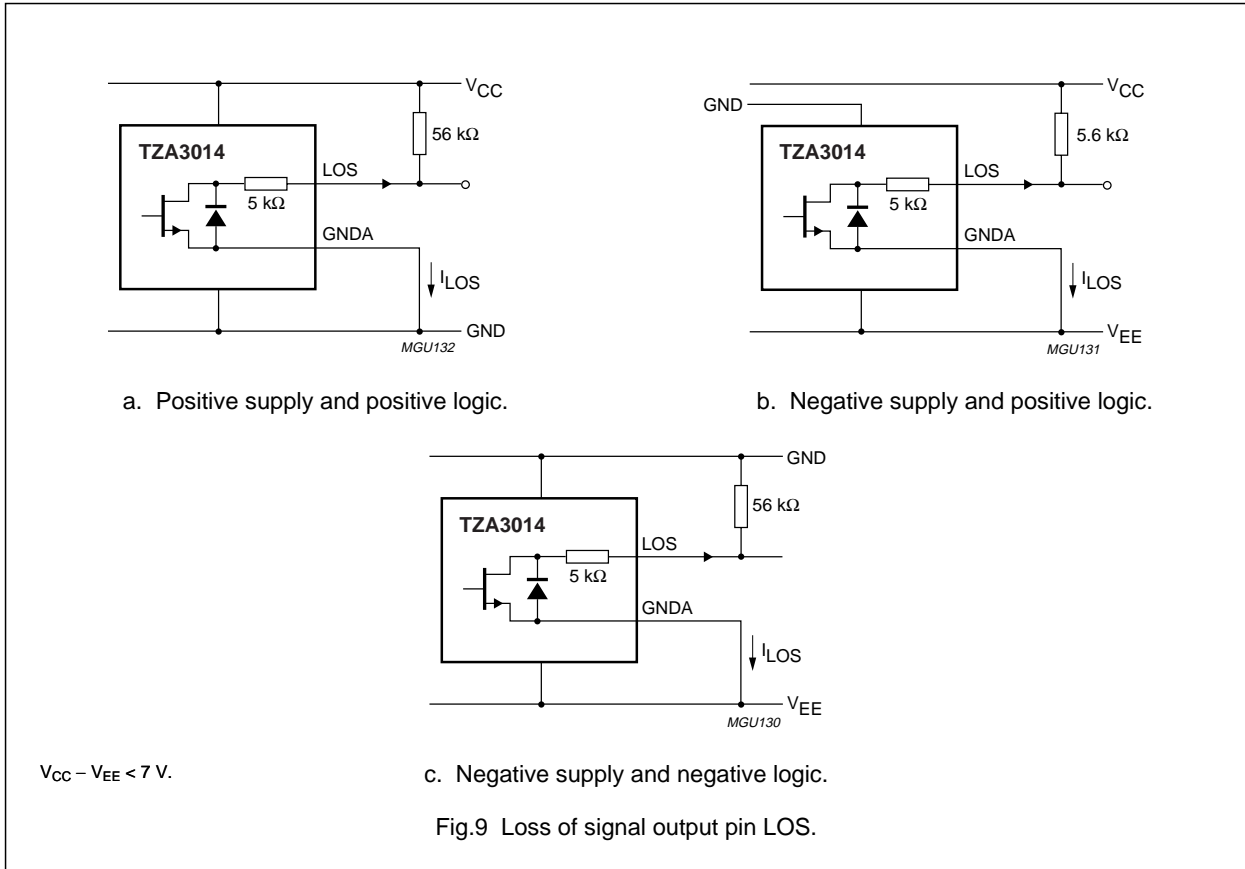
Supply current

For the supply current I_{CCB}, see Fig.10.

Using a positive supply voltage

Although the TZA3014 has been designed to use a single +3.3 V supply voltage (see Fig.11), some care should be taken with respect to RF transmission lines. The on-chip signals refer to the various V_{CC} pins. The external transmission lines will most likely be referred to the pins GNDA and GNDB, being the system ground.

The RF signals will change from one reference plane to another when interfacing the RF inputs and outputs. A positive supply application is very vulnerable to interference with respect to this point. For a successful +3.3 V application, special care should be taken when designing the PCB layout in order to reduce the influence of interference and to keep the positive supply voltage as clean as possible.

(1) $T_{amb} = 25$ °C.

Fig.10 Supply current as a function of the output voltage.
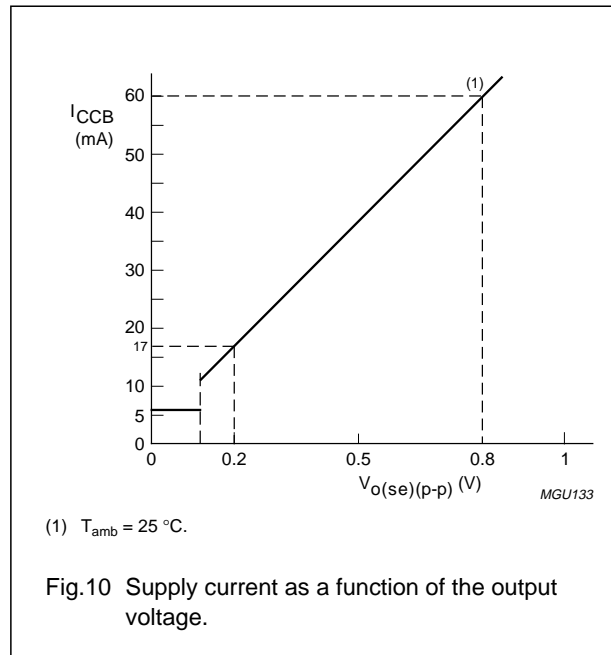
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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER		MIN.	MAX.	UNIT
V_{CC}	supply voltage		−0.5	+5.5	V
V_n	DC voltage				
	pins IN, INQ, LOSTH, LEVEL, V_{ref}, TEST, OUTQ, OUT, GNDp, V_{CCA} and V_{CCB}		−0.5	V_{CC} + 0.5	V
	pins LOS, INV and MUTE		−0.5	+7	V
I_n	DC current				
	pins IN and INQ		−20	+20	mA
	pins LOSTH and LEVEL		0	14	µA
	pins V_{ref}, TEST and LOS		−1	+1	mA
	pins OUT and OUTQ		−30	+30	mA
	pins INV and MUTE		0	20	µA
P_{tot}	total power dissipation		−	0.6	W
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		−	150	°C
T_{amb}	ambient temperature		−40	+85	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-s)}$	thermal resistance from junction to solder point (exposed die pad)	note 1	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	1s2p multi-layer test board; notes 1 and 2	33	K/W
$R_{th(s-a)}$	thermal resistance from solder point to ambient (exposed die pad)	1s2p multi-layer test board; notes 1 and 2	18	K/W
$R_{th(s-a)(req)}$	required thermal resistance from solder point to ambient	LOS detector switched on		
		V_o = 200 mV (p-p) single-ended	130	K/W
		V_o = 800 mV (p-p) single-ended	75	K/W

Notes

1. JEDEC standard.

2. HTQFP32 and HBCC32 packages.

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CHARACTERISTICS

Typical values at T_{amb} = 25 °C and V_{CC} = 3.3 V; minimum and maximum values are valid over the entire ambient temperature range and supply voltage range; all voltages referenced to ground; note 1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pins V$_{CCA}$ and V$_{CCB}$)						
V_{CC}	supply voltage		3.13	3.3	3.47	V
I_{CCA}	supply current A	LOS detector power-down	14	24	34	mA
		LOS detector switched on	24	40	56	mA
I_{CCB}	supply current B	amplifier power-down	2	6	10	mA
		V_o = 200 mV (p-p) single-ended	11	17	24	mA
		V_o = 800 mV (p-p) single-ended	43	60	77	mA
P_{tot}	total power dissipation	power-down	60	100	240	mW
		V_o = 200 mV (p-p) single-ended	120	190	270	mW
		V_o = 800 mV (p-p) single-ended	250	330	450	mW
TC	temperature coefficient	LOS detector switched on; I_{CCA}	−80	−50	−30	µA/K
		V_o = 800 mV (p-p) single-ended; I_{CCB}	−50	−30	−15	µA/K
T_j	junction temperature		−40	–	+125	°C
T_{amb}	ambient temperature		−40	+25	+85	°C
RF inputs in general (PECL or CML input pins IN and INQ)						
$V_{I(bias)}$	DC input bias voltage		V_{CC} − 0.4	V_{CC} − 0.33	V_{CC} − 0.28	V
V_I	DC and AC input window voltage	note 2	V_{CC} − 1.0	–	V_{CC} + 0.3	V
R_i	input resistance	single-ended	35	50	70	Ω
C_i	input capacitance	single-ended; note 2	0.6	0.8	1.2	pF
Cross-over switch and postamplifier						
PECL OR CML INPUT PINS IN AND INQ						
$V_{i(p-p)}$	input voltage swing (peak-to-peak value)	single-ended; notes 2 and 3	50	–	500	mV
$\alpha_{OS(red)}$	input offset reduction	V_o = 200 mV (p-p) single-ended; note 4	3.8	9	13.5	dB
		V_o = 800 mV (p-p) single-ended; note 4	6	14	22	dB
$V_{io(cor)}$	input offset voltage correction range (peak-to-peak value)	single-ended	−10	–	+10	mV
$V_{n(i)(eq)(rms)}$	equivalent input noise voltage (RMS value)	V_o = 800 mV (p-p) single-ended; note 2	–	75	170	µV
Fn	noise factor	note 2	–	5	12	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BUFFER AND AMPLIFIER						
G_v	small signal voltage gain	V_o = 200 mV (p-p) single-ended; note 5	9	15	20	dB
		V_o = 800 mV (p-p) single-ended; note 5	21	29	34	dB
f_D	signal path data rate	notes 6 and 7	–	2.5	–	Gbits/s
$f_{-3dB(l)}$	low −3 dB cut-off frequency DC compensation	note 2	2	5	10	kHz
$f_{-3dB(h)}$	high −3 dB cut-off frequency		–	2.0	–	GHz
t_{PD}	propagation delay	note 2	150	200	250	ps
Δt_{PD}	propagation delay difference	at the same signal levels; note 2	–	0	5	ps
J	total jitter	20 bits of the 28.5 kbits pattern; notes 2 and 8	–	8	–	ps
α_{ct}	crosstalk	note 9	–	110	–	dB
PECL OR CML OUTPUTS (PINS OUT AND OUTQ)						
$V_{o(se)(p-p)}$	single-ended output voltage (peak-to-peak value)	50 Ω load	200	–	800	mV
TC_{Vo}	temperature coefficient output voltage		−1	0	+1	mV/K
t_r	rise time	20% to 80%; notes 6 and 8	–	80	–	ps
t_f	fall time	80% to 20%; notes 6 and 8	–	80	–	ps
R_o	output resistance	single-ended	70	100	130	Ω
C_o	output capacitance	single-ended; note 2	0.6	0.8	1.2	pF
LEVEL CONTROL INPUT (PIN LEVEL)						
V_i	input voltage		$V_{CC} - V_{ref}$	–	V_{CC}	V
R_i	input resistance	referenced to V_{CC}	200	350	600	kΩ
SWITCH CIRCUIT						
t_a	assert time	multiplexer and inverter	–	100	–	ns
t_d	de-assert time	multiplexer and inverter	–	80	–	ns
TTL INPUT PINS MUTE AND INV						
V_{IL}	LOW-level input voltage	positive logic; note 10	−0.3	–	+0.8	V
V_{IH}	HIGH-level input voltage	positive logic; note 10	2	–	V_{CC} + 0.8	V
R_i	input resistance	referenced to GNDA	100	180	400	kΩ
I_i	input current		−40	–	+40	µA

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RSSI and LOS detector						
PECL OR CML INPUT PINS IN AND INQ						
$V_{i(p-p)}$	input voltage swing (peak-to-peak value)	single-ended	0.4	–	400	mV
$\alpha_{OS(red)}$	input offset reduction	notes 2 and 4	25	40	50	dB
$V_{io(cor)}$	on-chip DC-offset compensation correction range	peak-to-peak value; single-ended	–5	–	+5	mV
RSSI CIRCUIT						
$f_{-3dB(l)}$	low –3 dB cut-off frequency		0.5	1	2	MHz
$f_{-3dB(h)}$	high –3 dB cut-off frequency	note 11	1.5	2	2.5	GHz
DR	dynamic range		57	60	63	dB
S_{RSSI}	RSSI sensitivity	50 MHz, square; note 11	10	12.5	15	mV/dB
		620 MHz, square; note 11	10	12	14	mV/dB
		1.2 GHz, square; note 11	9	11	13.5	mV/dB
		100 MB/s PRBS ($2^{31} - 1$); note 11	9	12.5	15	mV/dB
		1.2 GB/s PRBS ($2^{31} - 1$); note 11	10	12	14.5	mV/dB
		2.4 GB/s PRBS ($2^{31} - 1$); note 11	10	12	14	mV/dB
TC_{sens}	temperature coefficient sensitivity		–2	0	+2	µV/dBK
LE	linearity error	see Fig.8; note 2	–	0.5	1	dB
LOS DETECTOR						
hys_{LOS}	LOS hysteresis	input signal waveform dependent	2.0	3.0	4.0	dB
t_a	assert time	note 2	–	–	5	µs
t_d	de-assert time	note 2	–	–	5	µs
INPUT PIN LOSTH						
V_i	input voltage		0	–	V_{CC}	V
R_i	input resistance	referenced to GNDA	150	350	600	kΩ
OUTPUT PIN LOS						
$I_{o(sink)}$	output sink current		–	–	1	mA
R_o	output resistance	internal output series resistance	3.5	5	6.5	kΩ

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
OUTPUT PIN RSSI						
V_o	output voltage		$V_{CC} - 1.2$	–	V_{CC}	V
I_o	output current		–1	–	+1	mA
Band gap reference circuit						
OUTPUT PIN V_{ref}						
V_{ref}	reference voltage		$V_{CC} - 1.85$	$V_{CC} - 1.6$	$V_{CC} - 1.45$	V
C_{ext}	allowed external capacitance		–	–	10	pF
$I_{o(sink)}$	output sink current		–	–	500	µA

Notes

1. It is assumed that both CML inputs carry a complementary signal with the specified peak-to-peak value (true differential excitation).

2. Guaranteed by design.

3. Minimum signal with limiting output.

4. $\alpha_{OS(red)} = \dfrac{G_{AC}}{G_{DC}}$

5. $G_V = \dfrac{V_o}{V_i}$

6. Based on −3 dB cut-off frequency and rise/fall time.

7. Low limit can go as low as DC if the input signal overrides the input offset voltage correction range.

8. V_i = 100 mV (p-p) single-ended, V_o = 800 mV (p-p) single-ended.

9. Crosstalk of IC only.

10. When using a negative supply voltage, positive or negative logic can be used. The values will be different, see Fig.7.

11. Sensitivity depends on the waveform and is therefore a function of −3 dB cut-off frequency; see Section "RSSI and LOS detection", Equation (1).

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APPLICATION INFORMATION

RF input and output connections

Striplines, or microstrips, with an odd mode characteristic impedance of $Z_o = 50 \, \Omega$ have to be used for the differential RF connections on the PCB. This applies to both signal inputs and signal outputs. Each pair of lines should have the same length.

Grounding and power supply decoupling

The PCB ground connection has to be a large area of copper connected to a common ground plane with an inductance as low as possible.
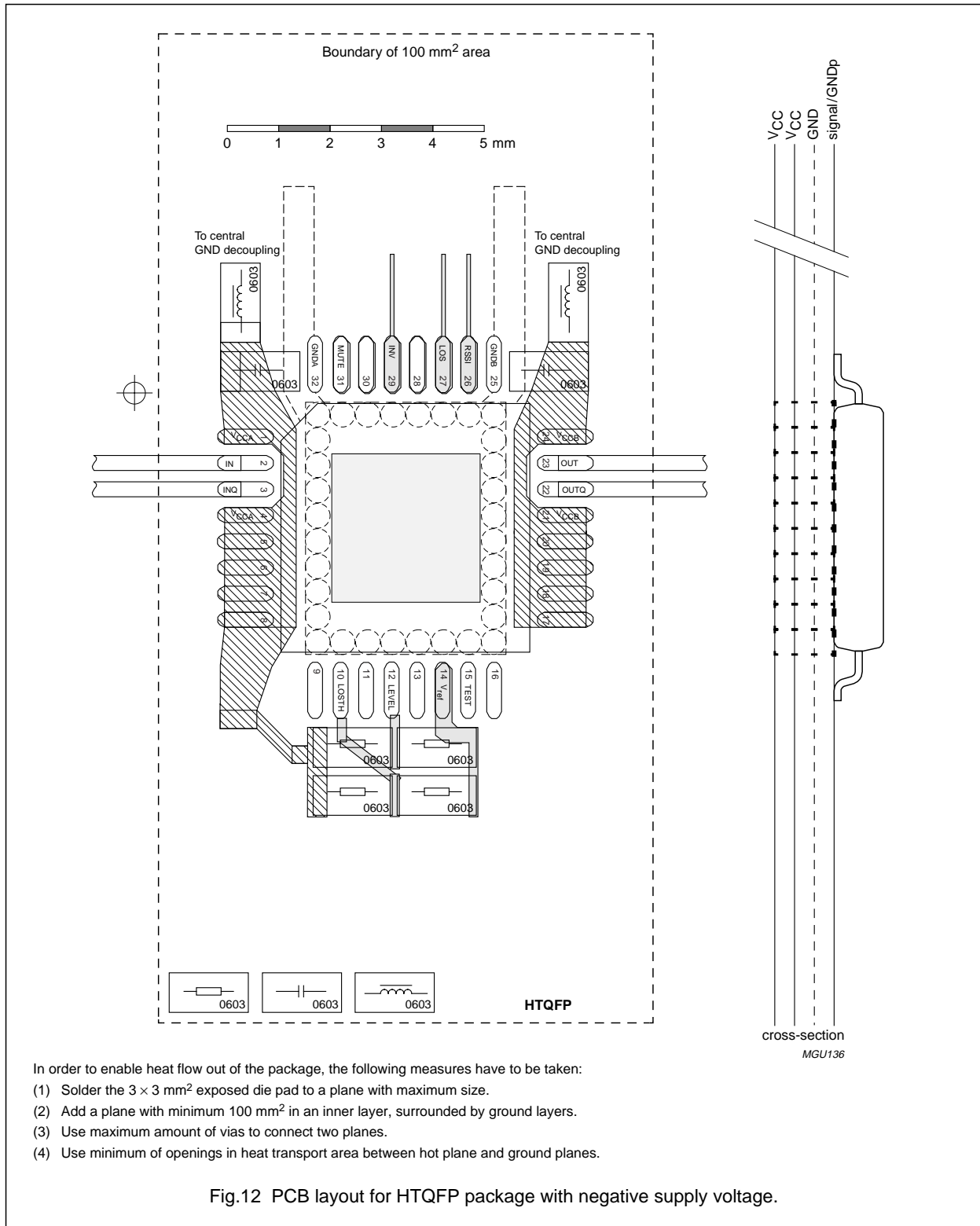
To minimize low frequency switching noise in the vicinity of the TZA3014, the power supply line should be filtered once using a beaded capacitor circuit having a low cut-off frequency.

The exposed die pad GNDp connection on the PCB must be a large area of copper to aid the transfer of heat from the IC to the PCB (see Figs 11 and 12).

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In order to enable heat flow out of the package, the following measures have to be taken:

(1) Solder the 3×3 mm^2 exposed die pad to a plane with maximum size.

(2) Add a plane with minimum 100 mm^2 in an inner layer, surrounded by ground layers.

(3) Use maximum amount of vias to connect two planes.

(4) Use minimum of openings in heat transport area between hot plane and ground planes.

Fig.11 PCB layout for HTQFP package with positive supply voltage.

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In order to enable heat flow out of the package, the following measures have to be taken:

(1) Solder the 3×3 mm^2 exposed die pad to a plane with maximum size.

(2) Add a plane with minimum 100 mm^2 in an inner layer, surrounded by ground layers.

(3) Use maximum amount of vias to connect two planes.

(4) Use minimum of openings in heat transport area between hot plane and ground planes.

Fig.12 PCB layout for HTQFP package with negative supply voltage.

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BONDING PAD INFORMATION

SYMBOL	PAD	COORDINATES[1]	
		x	y
V_{CCA}	1	−928	+710
IN	2	−928	+553
INQ	3	−928	+396
V_{CCA}	4	−928	+239
n.c.	5	−928	+81
n.c.	6	−928	−81
n.c.	7	−928	−239
n.c.	8	−928	−396
n.c.	9	−928	−553
n.c.	10	−928	−710
n.c.	11	−707	−928
LOSTH	12	−550	−928
n.c.	13	−393	−928
n.c.	14	−236	−928
LEVEL	15	−79	−928
n.c.	16	+79	−928
V_{ref}	17	+236	−928
n.c.	18	+393	−928
TEST	19	+550	−928
n.c.	20	+707	−928
n.c.	21	+928	−710
n.c.	22	+928	−553
n.c.	23	+928	−396
n.c.	24	+928	−239

SYMBOL	PAD	COORDINATES[1]	
		x	y
n.c.	25	+928	−81
n.c.	26	+928	+81
V_{CCB}	27	+928	+239
OUTQ	28	+928	+396
OUT	29	+928	+553
V_{CCB}	30	+928	+710
GNDB	31	+707	+928
n.c.	32	+550	+928
n.c.	33	+393	+928
RSSI	34	+236	+928
LOS	35	+79	+928
n.c.	36	−79	+928
INV	37	−236	+928
n.c.	38	−393	+928
MUTE	39	−550	+928
GNDA	40	−707	+928

Note

1. All x and y coordinates represent the position of the centre of the pad in μm with respect to the centre of the die (see Fig.13).

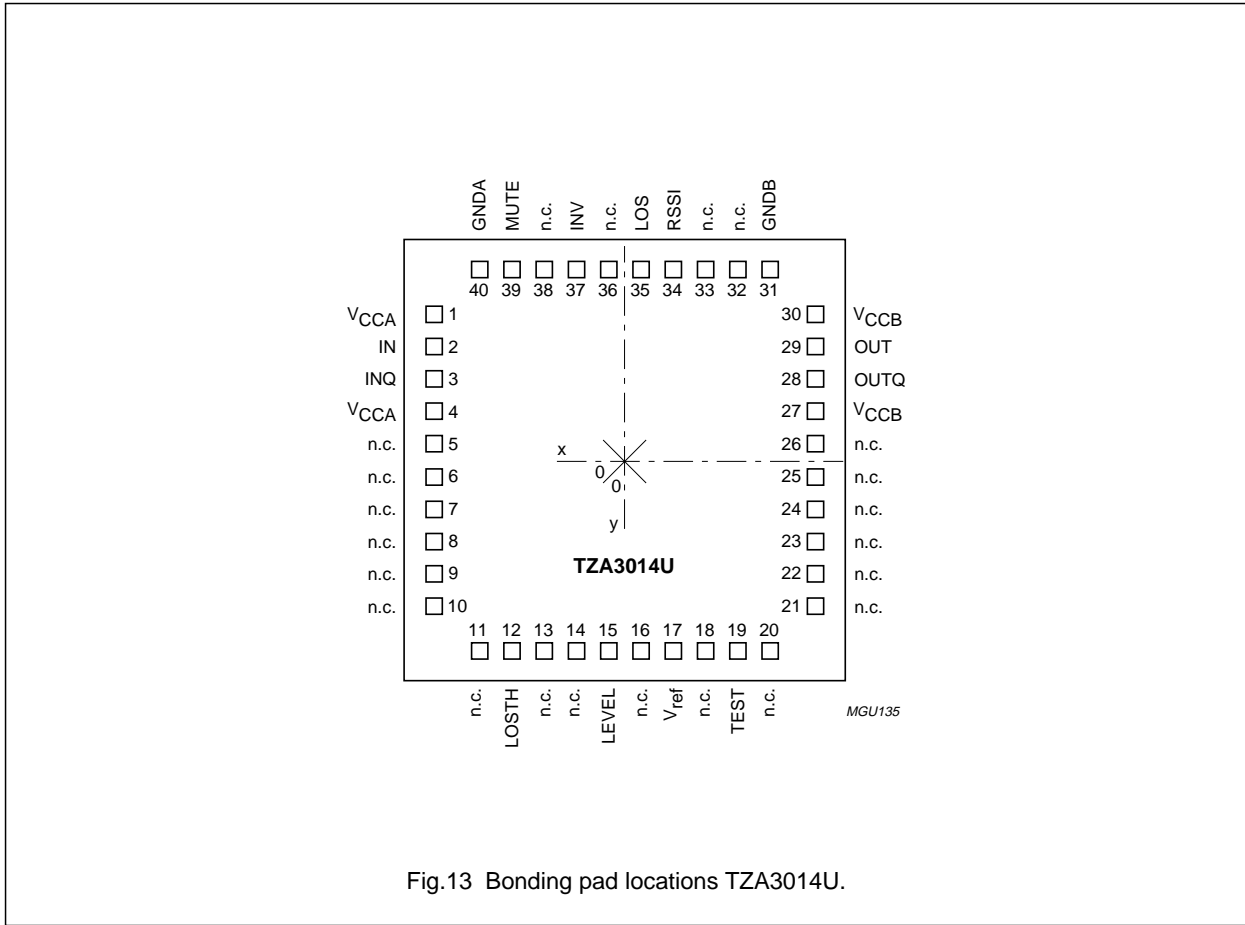## 2.5 Gbits/s postamplifier with level detector

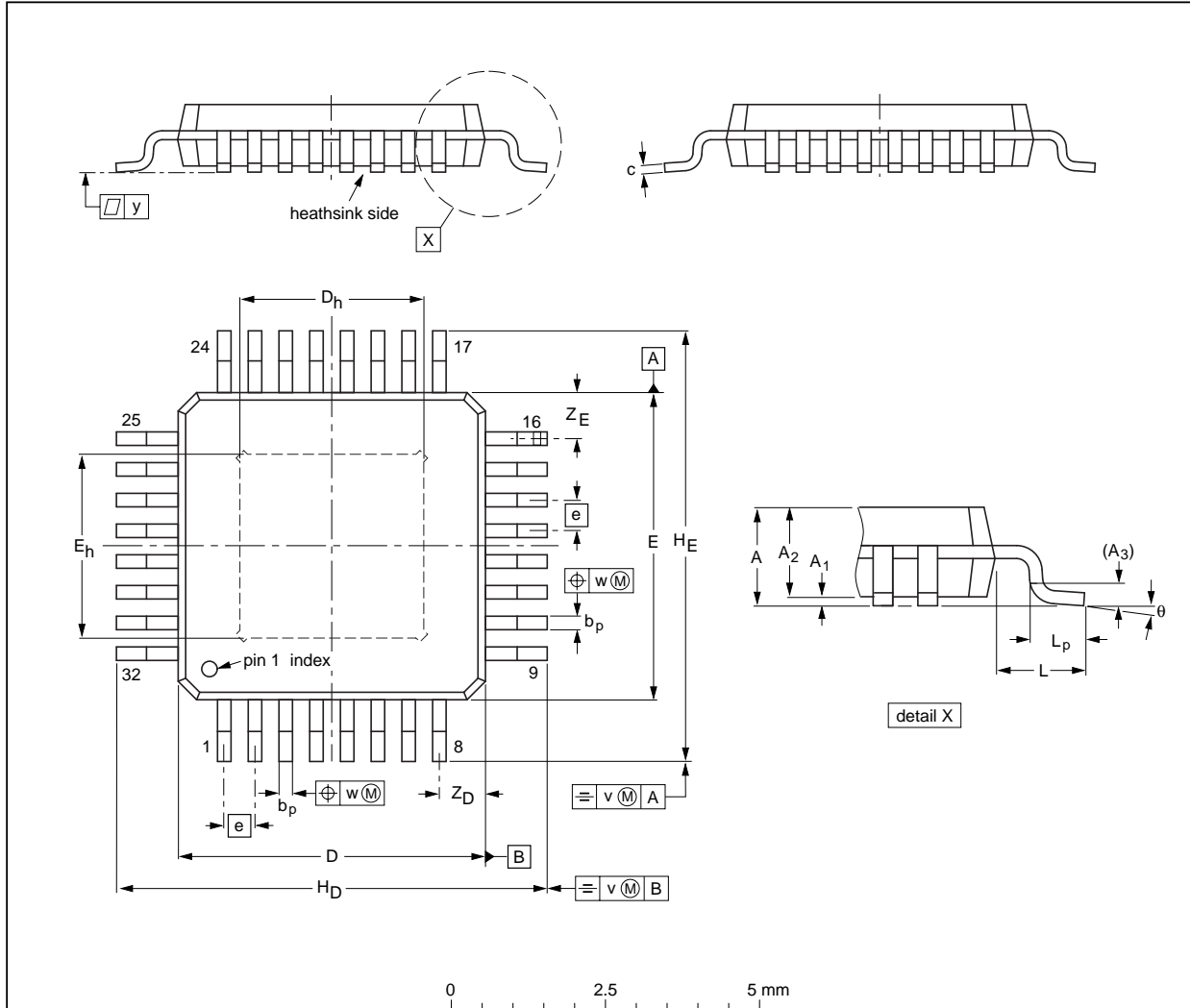## TZA3014

Fig.13 Bonding pad locations TZA3014U.

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PACKAGE OUTLINES

HTQFP32: plastic, heatsink thin quad flat package; 32 leads; body 5 x 5 x 1.0 mm   **SOT547-2**

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.27 0.17	0.20 0.09	5.1 4.9	3.1 2.7	5.1 4.9	3.1 2.7	0.5	7.1 6.9	7.1 6.9	1.0	0.75 0.45	0.2	0.08	0.08	0.89 0.61	0.89 0.61	7° 0°

Note

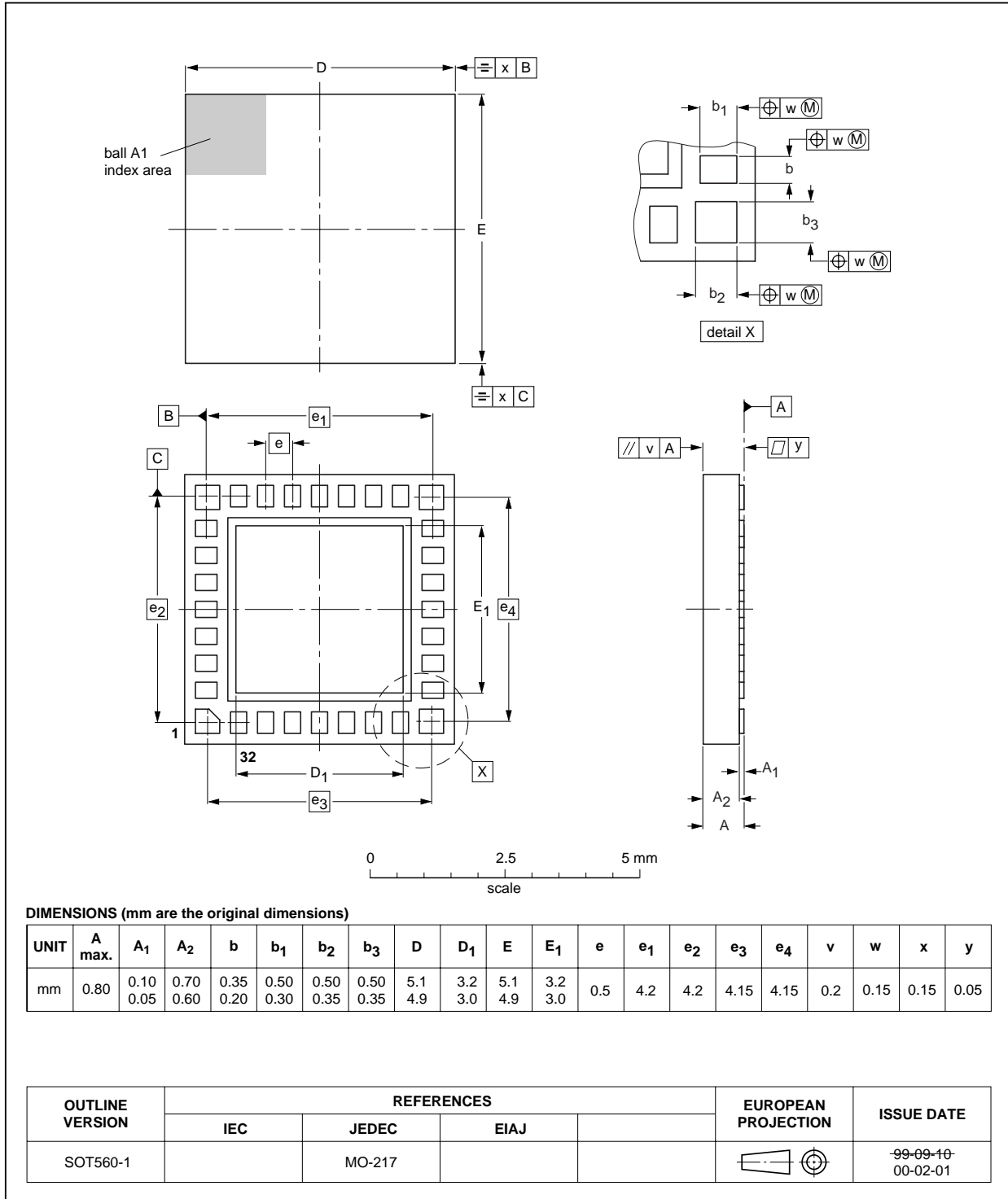1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT547-2						99-06-15

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HBCC32: plastic, heatsink bottom chip carrier; 32 terminals; body 5 x 5 x 0.65 mm

SOT560-1

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A₁	A₂	b	b₁	b₂	b₃	D	D₁	E	E₁	e	e₁	e₂	e₃	e₄	v	w	x	y
mm	0.80	0.10 0.05	0.70 0.60	0.35 0.20	0.50 0.30	0.50 0.35	0.50 0.35	5.1 4.9	3.2 3.0	5.1 4.9	3.2 3.0	0.5	4.2	4.2	4.15	4.15	0.2	0.15	0.15	0.05

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT560-1		MO-217				~~99-09-10~~ 00-02-01

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SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.

- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	**REFLOW**[1]
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.

2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).

3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
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Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 3 Figtree Drive, HOMEBUSH, NSW 2140,
Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

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Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V,
Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 7 - 9 Rue du Mont Valérien, BP317, 92156 SURESNES Cedex,
Tel. +33 1 4728 6600, Fax. +33 1 4728 6638

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Hungary: Philips Hungary Ltd., H-1119 Budapest, Fehervari ut 84/A,
Tel: +36 1 382 1700, Fax: +36 1 382 1800

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI),
Tel. +39 039 203 6838, Fax +39 039 203 6800

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

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Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

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Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Al.Jerozolimskie 195 B, 02-222 WARSAW,
Tel. +48 22 5710 000, Fax. +48 22 5710 001

Portugal: see Spain

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Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
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South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 5F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2451, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
60/14 MOO 11, Bangna Trad Road KM. 3, Bagna, BANGKOK 10260,
Tel. +66 2 361 7910, Fax. +66 2 398 3447

Turkey: Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

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Tel. +381 11 3341 299, Fax.+381 11 3342 553

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