STM8S103xx
STM8S105xx

Access line, STM8S 8-bit MCU, up to 32 Kbytes Flash, 10-bit ADC, timers, USART, SPI, I²C

Preliminary Data

Features

Core

- Max f_{CPU}: up to 16 MHz
- Advanced STM8 core with Harvard architecture and 3-stage pipeline
- Extended instruction set

Memories

- Program memory: Up to 32 Kbytes Flash; data retention 20 years at 85°C after 1 kcycles
- RAM: Up to 2 Kbytes

Clock, reset and supply management

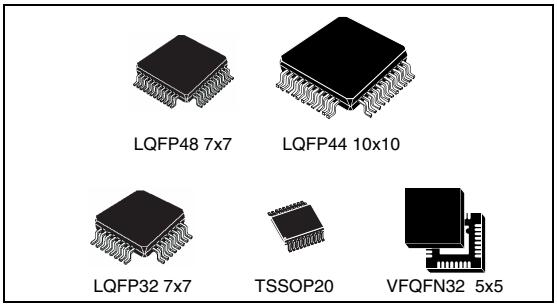
- 3.0 to 5.5 V operating voltage
- Flexible clock control, 4 master clock sources:
  - Low power crystal resonator oscillator
  - External clock input
  - Internal 16 MHz RC
  - Internal low power 128 kHz RC
- Clock security system with clock monitor
- Power management:
  - Low power modes (Wait, Active-halt, Halt)
  - Switch-off peripheral clocks individually
- Permanently active, low consumption power-on and power-down reset

Interrupt management

- Nested interrupt controller with 32 interrupts
- Up to 37 external interrupts on 6 vectors

Timers

- 2x 16-bit general purpose timers, with 2+3 CAPCOM channels (IC, OC or PWM)
- Advanced control timer: 16-bit, 4 CAPCOM channels, 3 complementary outputs, dead-time insertion and flexible synchronization
- 8-bit basic timer with 8-bit prescaler
- Auto wake-up timer
- 2 watchdog timers: Window watchdog and independent watchdog



Communications interfaces

- USART or LINUART with clock output for synchronous operation, smartcard mode, IrDA mode, LIN master mode
- SPI synchronous serial interface up to 8 Mbit/s
- I^2C interface up to 400 Kbit/s

Analog to digital converter (ADC)

- 10-bit, ±1 LSB ADC with up to 10 multiplexed channels, scan mode and analog watchdog

I/Os

- Up to 38 I/Os on a 48-pin package including 9 high sink outputs
- Highly robust I/O design, immune against current injection

Table 1. Device summary

Reference	Root part number
STM8S103xx	STM8S103K3
STM8S105xx	STM8S105C6, STM8S105C4, STM8S105K6, STM8S105K4, STM8S105S6, STM8S105S4,

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1 Introduction

This datasheet contains the description of the STM8S103/105 access line features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8S microcontroller memory, registers and peripherals, please refer to the STM8S microcontroller family reference manual (RM0016)
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8S Flash programming manual (PM0051)
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470)
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044)

2 Description

The STM8S103/105 access line 8-bit microcontrollers offer from 8 Kbytes up to 32 Kbytes of program memory.

All devices of the STM8S103/105 access line provide the following benefits:

- Reduced system cost
  - High system integration level with internal clock oscillators, watchdog and brown-out reset
- Performance and robustness
  - 16 MHz CPU clock frequency
  - Robust I/O, independent watchdogs with separate clock source
  - Clock security system
- Short development cycles
  - Applications scalability across a common family product architecture with compatible pinout, memory map and and modular peripherals.
  - Full documentation and a wide choice of development tools
- Product longevity
  - Advanced core and peripherals made in a state-of-the art technology
  - A family of products for applications with 3.0 V to 5.5 V operating supply

Table 2. STM8S103/105 access line features

Device	Pin count	No. of maximum GPIO (I/O)	Ext. Interrupt pins	Timer CAPCOM channels	Timer PWM channels	A/D Converter channels	Flash Program memory (bytes)	RAM (bytes)	Peripheral set	
STM8S105C6	48	38(1)	37	9	12	10	32K	2K	LINUART + extended features (synchronous comm. smartcard mode, IrdA mode), PWM timer (TIM3)	Multipurpose timer (TIM1), PWM timer (TIM2), 8-bit timer (TIM4), SPI, I^2C Window WDG, Independent WDG, ADC + extended features
STM8S105C4	48	38(1)	37	9	12	10	16K	2K		
STM8S105S6	44	34(1)	31	8	11	9	32K	2K		
STM8S105S4	44	34(1)	31	8	11	9	16K	2K		
STM8S105K6	32	25(1)	23	8	11	7	32K	2K		
STM8S105K4	32	25(1)	23	8	11	7	16K	2K		
STM8S103K3	32	28(2)	28	7	10	7	8	1K	USART with full features (synchronous comm. smartcard mode, IrdA mode and single wire mode)	

1. 9 high sink outputs
2. 8 high sink outputs

3 Block diagram

Figure 1. STM8S105 access line block diagram

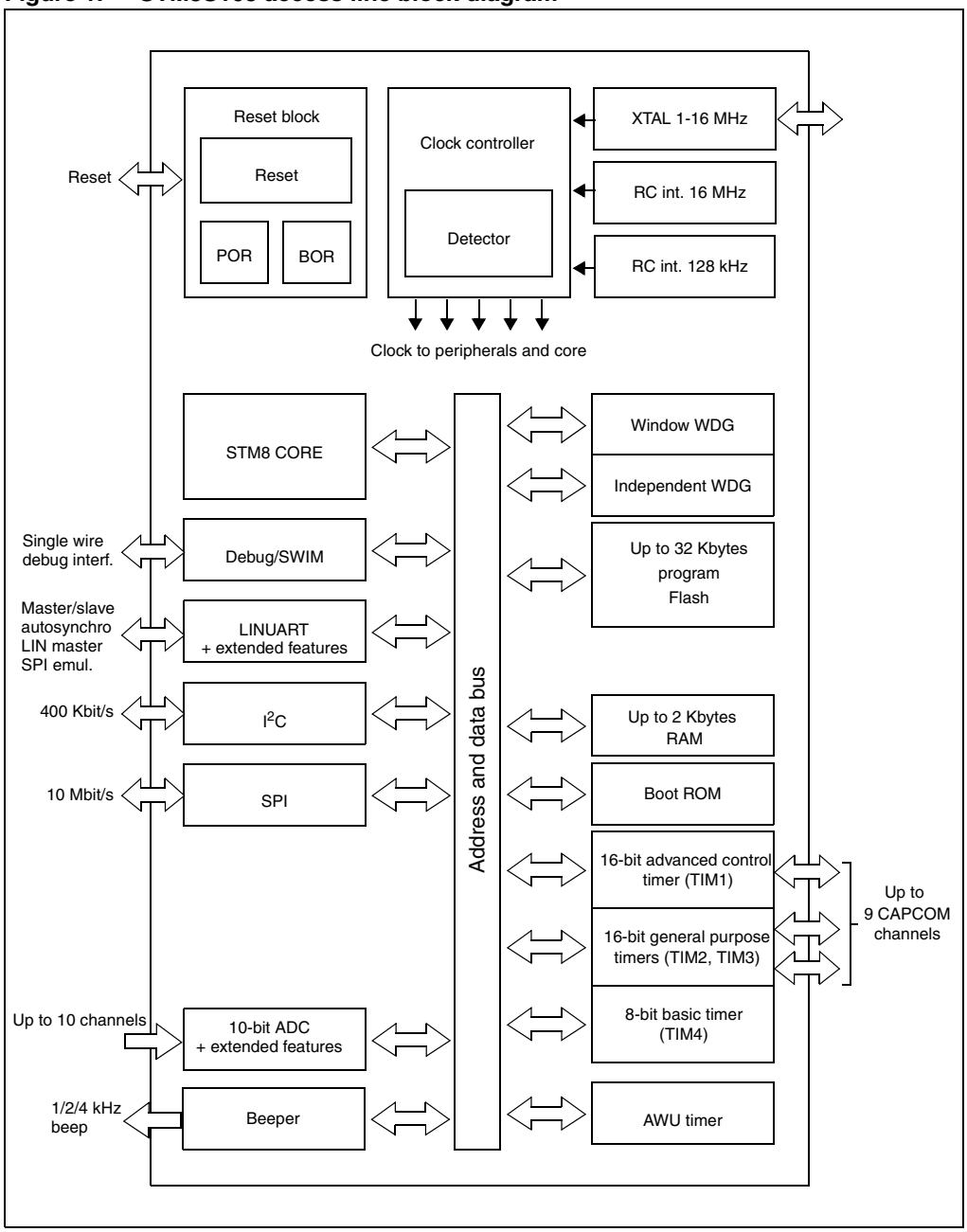
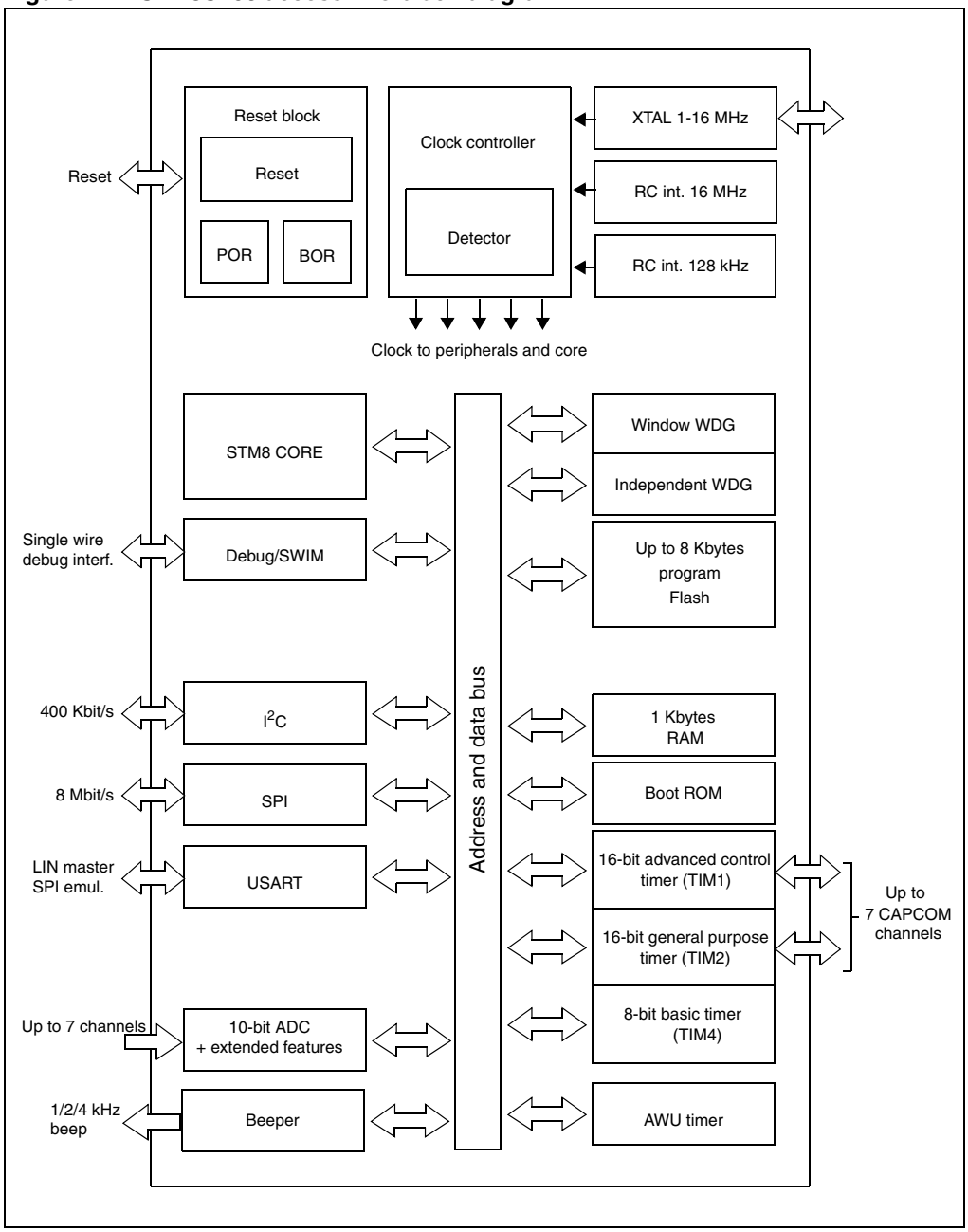


Figure 2. STM8S103 access line block diagram



4 Product overview

The following section intends to give an overview of the basic features of the STM8S103/105 access line functional modules and peripherals.

For more detailed information please refer to the corresponding family reference manual (RM0016).

4.1 Central processing unit STM8

The 8-bit STM8 core is designed for code efficiency and performance.

It contains 6 internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching for most instructions
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16-Mbyte linear memory space
- 16-bit stack pointer - access to a 64 K-level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction

Addressing

- 20 addressing modes
- Indexed indirect addressing mode for look-up tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

4.2 Single wire interface module (SWIM) and debug module (DM)

The single wire interface module and debug module and permit non-intrusive, real-time in-circuit debugging and fast memory programming.

SWIM

Single wire interface module for direct access to the debug module and memory programming. The interface can be activated in all device operation modes. The maximum data transmission speed is 145 bytes/ms.

Debug module

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, also CPU operation can be monitored in real-time by means of shadow registers.

- R/W to RAM and peripheral registers in real-time
- R/W access to all resources by stalling the CPU
- Breakpoints on all program-memory instructions (software breakpoints)
- 2 advanced breakpoints, 23 predefined configurations

4.3 Interrupt controller

- Nested interrupts with 3 software priority levels
- 32 interrupt vectors with hardware priority
- Up to 37 external interrupts on 6 vectors including TLI
- Trap and reset interrupts

4.4 Flash program memory

- Up to 32 Kbytes of program single voltage Flash memory
- User option byte area

Write protection (WP)

Write protection of Flash is provided to avoid unintentional overwriting of memory that could result from a user software malfunction.

There are two levels of write protection. The first level is known as MASS (Memory Access Security System). MASS is always enabled and protects the main Flash program memory and option bytes.

To perform In-Application Programming (IAP), this write protection can be removed by writing a MASS key sequence in a control register. This allows the application to modify the contents of main program memory or the device option bytes.

A second level of write protection, can be enabled to further protect a specific area of memory known as UBC (user boot code). Refer to *Figure 3.*

The size of the UBC is programmable through the UBC option byte (*Table 8.*), in increments of 1 page, by programming the UBC option byte in ICP mode.

This divides the program memory into two areas:

- Main program memory: Up to 32 Kbytes minus UBC
- User-specific boot code (UBC): Configurable up to 32 Kbytes

The UBC area remains write-protected during in-application programming. This means that the MASS keys do not unlock the UBC area. It protects the memory used to store the boot program, specific code libraries, reset and interrupt vectors, the reset routine and usually the IAP and communication routines.

Figure 3. Flash memory organization (STM8S105)

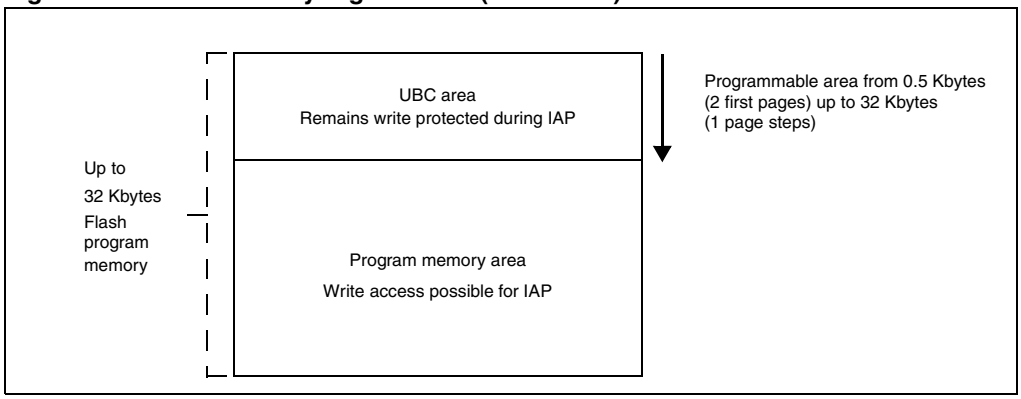
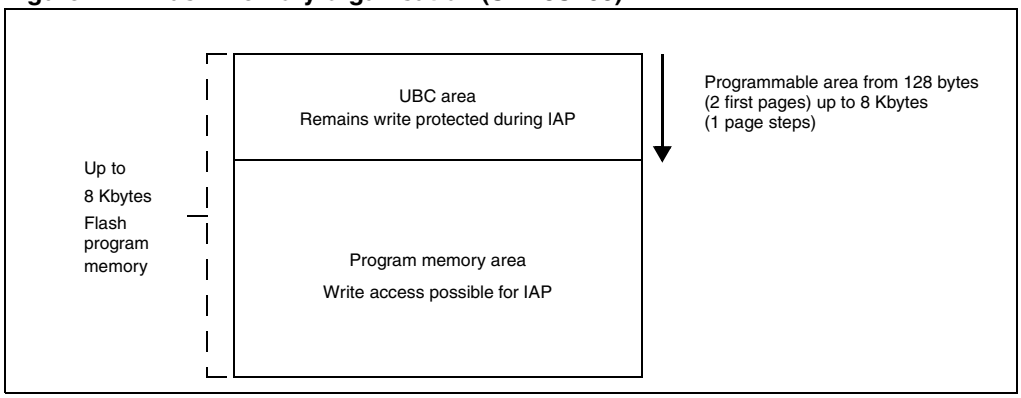


Figure 4. Flash memory organisation (STM8S103)



Read-out protection (ROP)

The read-out protection blocks reading and writing the Flash program memory in debug mode. Once the read-out protection is activated, any attempt to toggle its status triggers a global erase of the program and data memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

4.5 Clock controller

The clock controller distributes the system clock (f_{MASTER}) coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness.

Features

- **Clock prescaler:** to get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** Clock sources can be changed safely on the fly in run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- **Clock management:** To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **Master clock sources:** 4 different clock sources can be used to drive the master clock:
  - 1-16 MHz High Speed External crystal (HSE)
  - Up to 16 MHz High Speed user-external clock (HSE user-ext)
  - 16 MHz High Speed Internal RC oscillator (HSI)
  - 128 kHz Low Speed Internal RC (LSI)
- **Startup clock:** After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** This feature can be enabled by software. If an HSE clock failure occurs, the internal RC (16 MHz/8) is automatically selected by the CSS

and an interrupt can optionally be generated.

- **Configurable main clock output (CCO):** This outputs an external clock for use by the application. Available frequencies are 8 MHz, 4 MHz or 1 MHz.

4.6 Power management

For efficent power management, the application can be put in one four different low-power modes. You can configure each mode to obtain the best compromise between lowest power consumption, fastest start-up time and available wakeup sources.

- **Wait mode**: in this mode, the CPU is stopped, but peripherals are kept running. The wake-up is performed by an internal or external interrupt or reset.
- **Fast active halt mode**: in this mode, the CPU and peripheral clocks are stopped. An internal wake-up is generated at programmable intervals by the auto wake up unit (AWU). The main voltage regulator is kept powered on, so current consumption is more than in slow active halt mode, but the wake-up time is faster. Wake-up is triggered by the internal AWU interrupt, external interrupt or reset.
- **Slow active halt mode**: this mode is the same as fast active halt except that the main voltage regulator is powered off, so the wake up time is slower.
- **Halt mode**: in this mode the microcontroller uses the least power, CPU and peripheral clocks are stopped, the main voltage regulator is powered off. Wake-up is triggered by external interrupt or reset.

4.7 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

The WDG timer activity is controlled by option bytes. Once activated the watchdog can not be disabled by the user program without reset.

Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

The window function can be used to trim the watchdog behavior to match the application perfectly.

The application software must refresh the counter before time-out and during a limited time window.

A reset is generated in two situations:

1. Timeout: At 16 MHz CPU clock the time-out period can be adjusted between 75 µs up to 64 ms.
2. Refresh out of window: The downcounter is refreshed before its value is lower then the one stored in the window register.

Independent watchdog timer

The independent watchdog peripheral can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the 128 kHZ LSI internal RC clock source, and thus stays active even in case of a CPU clock failure

The IWDG time base spans from 60 µs to 1 s.

4.8 Auto wake-up counter

- Used for auto wake-up from active halt mode
- Clock source: internal 128 kHz internal low frequency RC oscillator or external clock

4.9 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

4.10 TIM1 - 16-bit advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver.

- 16-bit up, down and up/down autoreload counter with 16-bit prescaler
- 4 independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- Synchronization module to control the timer with external signal
- Break input to force the timer outputs into a defined state
- 3 complementary outputs with adjustable dead time
- Encoder mode
- Interrupt sources: x input capture/output compare, 1 x overflow/update, 1 x break

4.11 TIM2- 16-bit general purpose timer

- 16-bit autoreload (AR) up-counter
- 15-bit prescaler adjustable to fixed power of 2 ratios 1…32768
- Timers with 3 or 2 individually configurable capture/compare channels
- PWM mode
- Interrupt sources: 2 or 3 x input capture/output compare, 1 x overflow/update

4.12 TIM4 - 8-bit basic timer

- 8-bit autoreload, adjustable prescaler ratio to any power of 2 from 1 to 128
- Clock source: CPU clock
- Interrupt source: 1 x overflow/update

Table 3. STM8 TIM timer feature comparison

Timer	Counter size (bits)	Prescaler	Counting mode	CAPCOM channels	Complem. outputs	Ext. trigger	Timer synchr-onization/ chaining
TIM1	16	Any integer from 1 to 65536	Up/down	4	3	Yes	Yes
TIM2	16	Any power of 2 from 1 to 32768	Up	3	0	No	
TIM3	16	Any power of 2 from 1 to 32768	Up	2	0	No	
TIM4	8	Any power of 2 from 1 to 128	Up	0	0	No	

4.13 Analog/digital converter (ADC)

- STM8S103/105 access line products contain a 10-bit successive approximation A/D converter with up to 10 multiplexed input channels and the following general features:
  - Input voltage range: 0 to V_{DDA}
  - Dedicated voltage reference (VREF) pins available on 80 and 64-pin devices
  - Conversion time: 14 clock cycles
  - Single and continuous conversion modes
  - External trigger input
  - Trigger from TIM1 TRGO (STM8S105) or TIM2 TRGO (STM8S103)
  - End of conversion (EOC) interrupt

ADC extended features

- STM8S103/105 access line products contain a 10-bit successive approximation A/D converter with the following features:
  - Up to 10 (STM8S105x) or 7 (STM8S103x) multiplexed input channels
  - Single, continuous and buffered continuous conversion on a selected channel
  - Scan mode for single and continuous conversion of a sequence of channels
  - Analog watchdog capability with programmable upper and lower thresholds
  - Internal reference voltage on channel AIN7 (STM8S103 only)
  - Analog watchdog interrupt

4.14 Communication interfaces

The following communication interfaces are implemented:

- USART:
  - STM8S105: no USART
  - STM8S103: full feature UART, single wire mode, LIN2.1 master capability
- LINUART:
  - STM8S105: LIN2.1 master/slave capability, full feature UART, synchronous mode, SPI master mode, Smartcard mode, IrDA mode
  - STM8S103: No LINUART
- SPI - full and half-duplex, 8 Mbit/s
- I²C - up to 400 Kbit/s

4.14.1 USART

Main features

- 1 Mbit/s full duplex SCI
- LIN master capable
- SPI emulation
- High precision baud rate generator
- Smartcard emulation
- IrDA SIR encoder decoder
- Single wire half duplex mode

Asynchronous communication (UART mode)

- Full duplex communication - NRZ standard format (mark/space)
- Programmable transmit and receive baud rates up to 1 Mbit/s (f_{CPU}/16) and capable of following any standard baud rate regardless of the input frequency
- Separate enable bits for transmitter and receiver
- 2 receiver wakeup modes:
  - Address bit (MSB)
  - Idle line (interrupt)
- Transmission error detection with interrupt generation
- Parity control

LIN master capability

- Emission: Generates 13-bit synch break frame
- Reception: Detects 11-bit break frame

Synchronous communication

- Full duplex synchronous transfers
- SPI master operation
- 8-bit data communication
- Max. speed: 1 Mbit/s at 16 MHz (f_{CPU}/16)

4.14.2 LINUART

Main features

- LIN master/slave rev. 2.1 compliant
- Auto-synchronization in LIN slave mode
- High precision baud rate generator
- 1 Mbit full duplex SCI

LIN master

- Emission: Generates 13-bit synch break frame
- Reception: Detects 11-bit break frame

LIN slave

- Autonomous header handling - one single interrupt per valid message header
- Automatic baud rate synchronization - maximum tolerated initial clock deviation ±15 %
- Synch delimiter checking
- 11-bit LIN synch break detection - break detection always active
- Parity check on the LIN identifier field
- LIN error management
- Hot plugging support

Asynchronous communication (UART mode)

- Full duplex, asynchronous communications - NRZ standard format (mark/space)
- Independently programmable transmit and receive baud rates up to 500 Kbit/s
- Programmable data word length (8 or 9 bits)
- Low-power standby mode - 2 receiver wake-up modes:
  - Address bit (MSB)
  - Idle line
- Muting function for multiprocessor configurations
- Overrun, noise and frame error detection
- 6 interrupt sources
- Tx, Rx parity control

Note: In STM8S105, the LINUART also supports IrDA mode, Smartcard mode and synchronous communication (SPI master mode).

4.14.3 SPI

- Maximum speed: 8 Mbit/s ($f_{MASTER}/2$) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on 2 lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave/master selection input pin

4.14.4 I²C

- I²C master features:
  - Clock generation
  - Start and stop generation
- I²C slave features:
  - Programmable I²C address detection
  - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds:
  - Standard speed (up to 100 kHz),
  - Fast speed (up to 400 kHz)

5 Pinouts and pin description

5.1 Package pinouts

Figure 5. LQFP 48-pin pinout

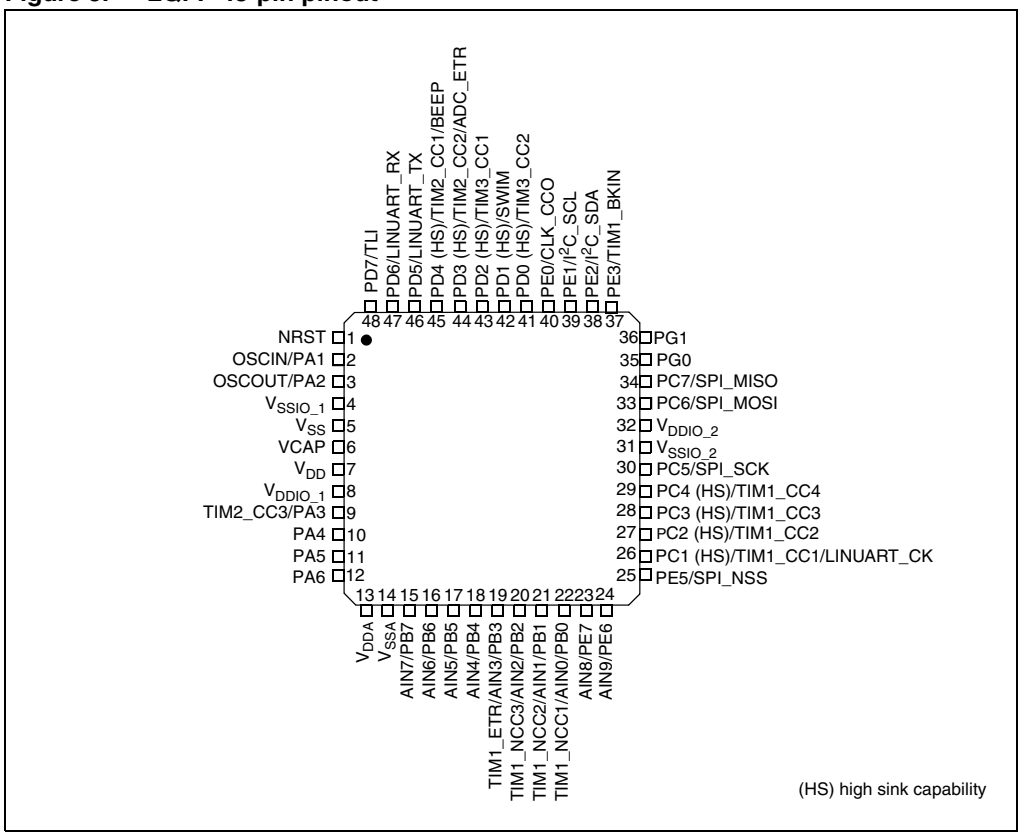


Figure 6. LQFP 44-pin pinout

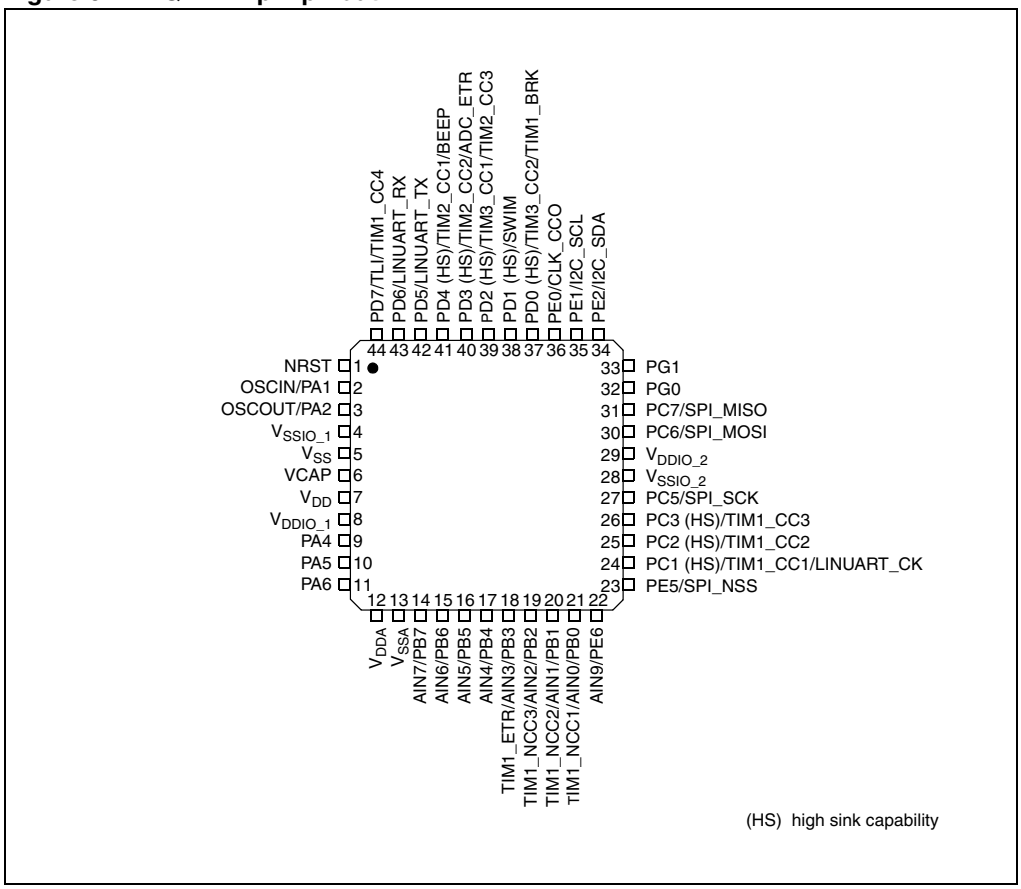


Figure 7. STM8S105 LQFP/VQFN 32-pin pinout

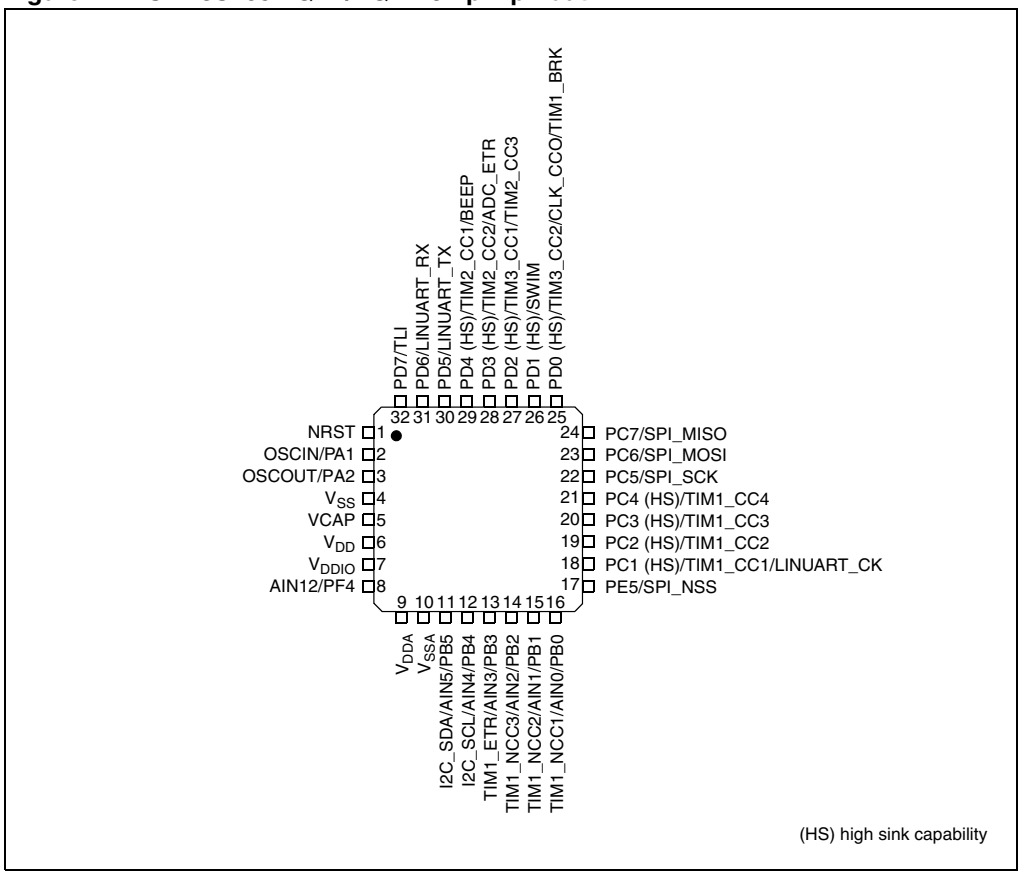


Figure 8. STM8S103 LQFP/VQFN 32-pin pinout

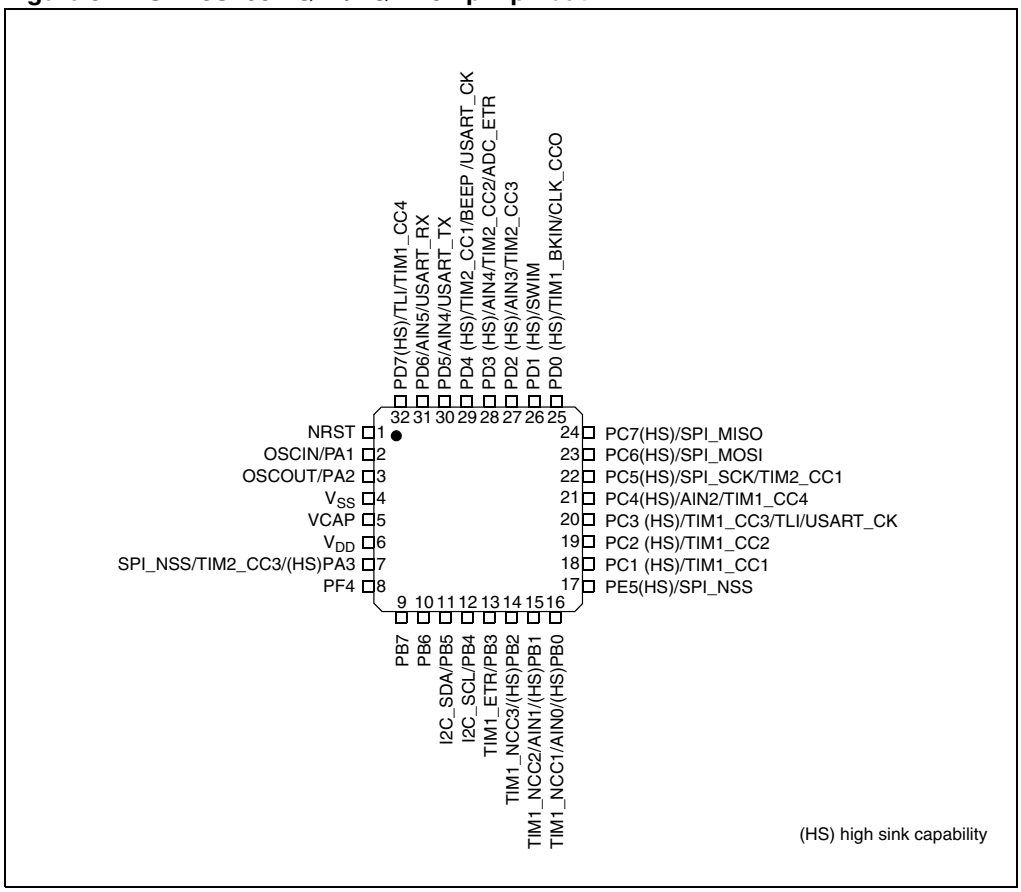
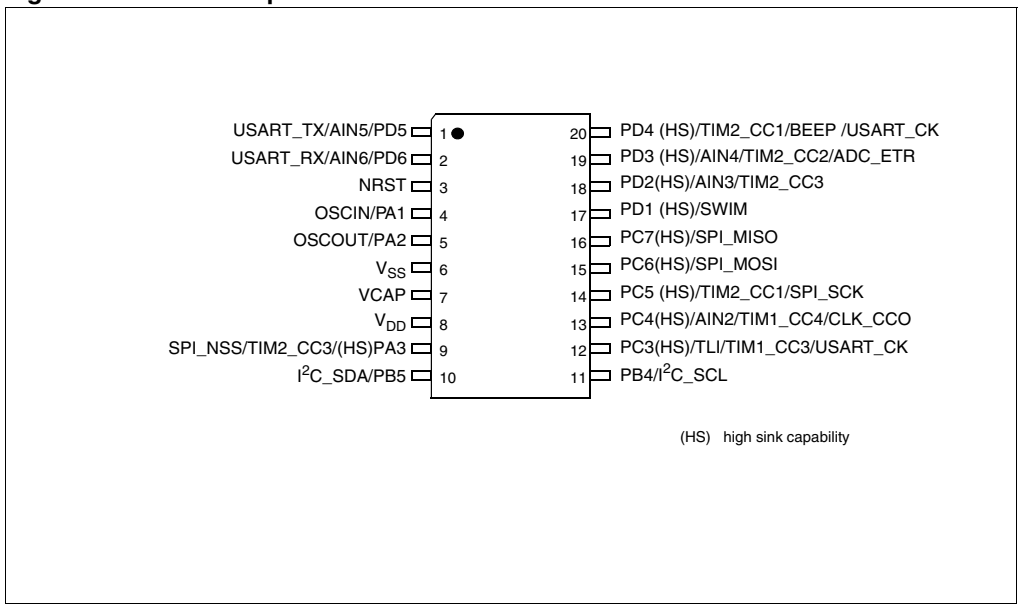


Figure 9. TSSOP20 pinout



5.2 Pin description

Table 4. Legend/abbreviations

Type	I= input, O = output, S = power supply	
Level	Input	CM = CMOS
	Output	HS = High sink
Output speed	O1 = Slow (up to 2 MHz) O2 = Fast (up to 10 MHz) O3 = Fast/slow programmability with slow as default state after reset O4 = Fast/slow programmability with fast as default state after reset	
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = true open drain, OD = open drain, PP = push pull

Reset state is shown in **bold**.

Table 5. Pin description for STM8S105 MCUs

Pin number			Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	LQFP44	LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
1	1	1	NRST	I/O		**X**						Reset		
2	2	2	PA1/OSCIN	I/O	**X**	X			O1	X	X	**Port A1**	Resonator/ crystal in	
3	3	3	PA2/OSCOUT	I/O	**X**	X	X		O1	X	X	**Port A2**	Resonator/ crystal out	
4	4	-	V_{SSIO_1}	S								I/O ground		
5	5	4	V_{SS}	S								Digital ground		
6	6	5	VCAP	S								1.8 V regulator capacitor		
7	7	6	V_{DD}	S								Digital power supply		
8	8	7	V_{DDIO_1}	S								I/O power supply		
-	-	8	PF4/AIN12	I/O	**X**	X			O1	X	X	**Port F4**	Analog input 12	
9	-	-	PA3/TIM2_CC3	I/O	**X**	X	X		O1	X	X	**Port A3**	Timer 2 - channel3	TIM3_CC1 [AFR1]
10	9	-	PA4	I/O	**X**	X	X		O3	X	X	**Port A4**		
11	10	-	PA5	I/O	**X**	X	X		O3	X	X	**Port A5**		
12	11	-	PA6	I/O	**X**	X	X		O3	X	X	**Port A6**		
13	12	9	V_{DDA}	S								Analog power supply		
14	13	10	V_{SSA}	S								Analog ground		
15	14	-	PB7/AIN7	I/O	**X**	X	X		O1	X	X	**Port B7**	Analog input 7	

Table 5. Pin description for STM8S105 MCUs (continued)

Pin number			Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	LQFP44	LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
16	15	-	PB6/AIN6	I/O	**X**	X	X		O1	X	X	**Port B6**	Analog input 6	
17	16	11	PB5/AIN5	I/O	**X**	X	X		O1	X	X	**Port B5**	Analog input 5	I^2C_SDA [AFR6]
18	17	12	PB4/AIN4	I/O	**X**	X	X		O1	X	X	**Port B4**	Analog input 4	I^2C_SCL [AFR6]
19	18	13	PB3/AIN3	I/O	**X**	X	X		O1	X	X	**Port B3**	Analog input 3	TIM1_ETR [AFR5]
20	19	14	PB2/AIN2	I/O	**X**	X	X		O1	X	X	**Port B2**	Analog input	TIM1_NCC3 [AFR5]
21	20	15	PB1/AIN1	I/O	**X**	X	X		O1	X	X	**Port B1**	Analog input 1	TIM1_NCC2 [AFR5]
22	21	16	PB0/AIN0	I/O	**X**	X	X		O1	X	X	**Port B0**	Analog input 0	TIM1_NCC1 [AFR5]
23	-	-	PE7/AIN8	I/O	**X**	X	X		O1	X	X	**Port E7**	Analog input 8	
24	22		PE6/AIN9	I/O	**X**	X	X		O1	X	X	**Port E7**	Analog input 9	
25	23	17	PE5/SPI_NSS	I/O	**X**	X	X		O1	X	X	**Port E5**	SPI master/slave select	
26	24	18	PC1/TIM1_CC1/ LINUART_CK	I/O	**X**	X	X	HS	O3	X	X	**Port C1**	Timer 1 - channel 1 / LINUART synchronous clock	
27	25	19	PC2/TIM1_CC2	I/O	**X**	X	X	HS	O3	X	X	**Port C2**	Timer 1- channel 2	
28	26	20	PC3/TIM1_CC3	I/O	**X**	X	X	HS	O3	X	X	**Port C3**	Timer 1 - channel 3	
29	-	21	PC4/TIM1_CC4	I/O	**X**	X	X	HS	O3	X	X	**Port C4**	Timer 1 - channel 4	
30	27	22	PC5/SPI_SCK	I/O	**X**	X	X		O3	X	X	**Port C5**	SPI clock	
31	28	-	V_{SSIO_2}	S								I/O ground		
32	29	-	V_{DDIO_2}	S								I/O power supply		
33	30	23	PC6/SPI_MOSI	I/O	**X**	X	X		O3	X	X	**Port C6**	SPI master out/ slave in	
34	31	24	PC7/SPI_MISO	I/O	**X**	X	X		O3	X	X	**Port C7**	SPI master in/ slave out	
35	32	-	PG0	I/O	**X**	X			O1	X	X	**Port G0**		
36	33	-	PG1	I/O	**X**	X			O1	X	X	**Port G1**		
37	-	-	PE3/TIM1_BKIN	I/O	**X**	X	X		O1	X	X	**Port E3**	Timer 1 - break input	
38	34	-	PE2/I^2C_SDA	I/O	**X**	X	X		O1	T(1)	X	**Port E2**	I^2C data	

Table 5. Pin description for STM8S105 MCUs (continued)

Pin number			Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	LQFP44	LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
39	35	-	PE1/I^{2}C_SCL	I/O	**X**	X	X		O1	T(1)	X	**Port E1**	I^{2}C clock	
40	36	-	PE0/CLK_CCO	I/O	**X**	X	X		O3	X	X	**Port E0**	Configurable clock output	
41	37	25	PD0/TIM3_CC2	I/O	**X**	X	X	HS	O3	X	X	**Port D0**	Timer 3 - channel 2	TIM1_BKIN [AFR3]/ CLK_CCO [AFR2]
42	38	26	PD1/SWIM	I/O	X	**X**	X	HS	O4	X	X	**Port D1**	SWIM data interface	
43	39	27	PD2/TIM3_CC1	I/O	**X**	X	X	HS	O3	X	X	**Port D2**	Timer 3 - channel 1	TIM2_CC3 [AFR1]
44	40	28	PD3/TIM2_CC2	I/O	**X**	X	X	HS	O3	X	X	**Port D3**	Timer 2 - channel 2	ADC_ETR [AFR0]
45	41	29	PD4/TIM2_CC1/BEEP	I/O	**X**	X	X	HS	O3	X	X	**Port D4**	Timer 2 - channel 1	BEEP output [AFR7]
46	42	30	PD5/ LINUART_TX	I/O	**X**	X	X		O1	X	X	**Port D5**	LINUART data transmit	
47	43	31	PD6/ LINUART_RX	I/O	**X**	X	X		O1	X	X	**Port D6**	LINUART data receive	
48	44	32	PD7/TLI	I/O	**X**	X	X		O1	X	X	**Port D7**	Top level interrupt	TIM1_CC4 [AFR4]

1. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer and protection diode to V_{DD} are not implemented)

Table 6. Pin description for STM8S103 MCUs

Pin number		Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
VQFN/LQFP32	TSSOP20			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
1	3	NRST	I/O		**X**						Reset		
2	4	PA1/OSCIN	I/O	**X**	X	X		O1	X	X	**Port A1**	Resonator/ crystal in	
3	5	PA2/OSCOUT	I/O	**X**	X	X		O1	X	X	**Port A2**	Resonator/ crystal out	
4	6	V_{SS}	S								Digital ground		
5	7	VCAP	S								1.8 V regulator capacitor		
6	8	V_{DD}	S								Digital power supply		
7	9	PA3/TIM2_CC3/SPI_NSS	I/O	**X**	X	X	HS	O3	X	X	**Port A3**	Timer 2 channel 3	SPI master/slave select
8	-	PF4	I/O	**X**	X	X		O1	X	X	**Port F4**		
9	-	PB7	I/O	**X**	X	X		O1	X	X	**Port B7**		
10	-	PB6	I/O	**X**	X	X		O1	X	X	**Port B6**		
11	10	PB5/I2C_SDA	I/O	**X**	X	X		O1	T(1)	X	**Port B5**	I^2C data	
12	11	PB4/I2C_SCL	I/O	**X**	X	X		O1	T(1)	X	**Port B4**	I^2C clock	
13	-	PB3/TIM1_ETR	I/O	**X**	X	X	HS	O3	X	X	**Port B3**	Timer 1 external trigger	
14	-	PB2/TIM1_NCC3	I/O	**X**	X	X	HS	O3	X	X	**Port B2**	Timer 1 - inverted channel 3	
15	-	PB1/AIN1/TIM1_NCC2	I/O	**X**	X	X	HS	O3	X	X	**Port B1**	Analog input 1/ Timer 1 - inverted channel 2	
16	-	PB0/AIN0/TIM1_NCC1	I/O	**X**	X	X	HS	O3	X	X	**Port B0**	Analog input 0/ Timer 1 - inverted channel 1	
17	-	PE5/SPI_NSS	I/O	**X**	X	X	HS	O3	X	X	**Port E5**	SPI master/slave select	
18	-	PC1/TIM1_CC1	I/O	**X**	X	X	HS	O3	X	X	**Port C1**	Timer 1 - channel 1	
19	-	PC2/TIM1_CC2	I/O	**X**	X	X	HS	O3	X	X	**Port C2**	Timer 1 - channel 2	
20	12	PC3/TLI/TIM1_CC3/ USART_CK	I/O	**X**	X	X	HS	O3	X	X	**Port C3**	Top level interrupt Timer 1 - channel 3	USART clock

Table 6. Pin description for STM8S103 MCUs (continued)

Pin number		Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
VQFN/LQFP32	TSSOP20			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
21	13	PC4/AIN2/TIM1_CC4/ CLK_CCO	I/O	**X**	X	X	HS	O3	X	X	**Port C4**	Analog input 2 / Timer 1 - channel 4	Con-figurable clock output
22	14	PC5/TIM2_CC1/SPI_SCK	I/O	**X**	X	X	HS	O3	X	X	**Port C5**	Timer 2 - channel 1	SPI clock
23	15	PC6/SPI_MOSI	I/O	**X**	X	X	HS	O3	X	X	**Port C6**	SPI master out/ slave in	
24	16	PC7/SPI_MISO	I/O	**X**	X	X	HS	O3	X	X	**Port C7**	SPI master in/ slave out	
25	-	PD0/TIM1_BKIN/CLK_CCO	I/O	**X**	X	X	HS	O3	X	X	**Port D0**	Timer 1 - break input	Con-figurable clock output
26	17	PD1/SWIM	I/O	X	**X**	X	HS	O4	X	X	**Port D1**	SWIM data interface	
27	18	PD2/AIN3/TIM2_CC3	I/O	**X**	X	X	HS	O3	X	X	**Port D2**	Analog input 3 / Timer 2 - channel 3	
28	19	PD3/AIN4/TIM2_CC2/ADC_ ETR	I/O	**X**	X	X	HS	O3	X	X	**Port D3**	Analog input 4 / Timer 2 - channel 2	ADC external trigger
29	20	PD4/TIM2_CC1/BEEP/ USART_CK	I/O	**X**	X	X	HS	O3	X	X	**Port D4**	Timer 2 - channel 1	USART clock/ BEEP output
30	1	PD5/AIN5/USART_TX	I/O	**X**	X	X		O1	X	X	**Port D5**	Analog input 5	USART data transmit
31	2	PD6/AIN6/USART_RX	I/O	**X**	X	X		O1	X	X	**Port D6**	Analog input 6	USART data receive
32	-	PD7/TLI/TIM1_CC4	I/O	**X**	X	X	HS	O3	X	X	**Port D7**	Top level interrupt/ Timer 1 - channel 4	

1. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer and protection diode to V_{DD} are not implemented)

5.2.1 Alternate function remapping

As shown in the rightmost column of the pin description table, some alternate functions can be remapped at different I/O ports by programming one of 8 AFR (alternate function remap) option bits. Refer to *Section 6: Option bytes on page 29*. When the remapping option is active, the default alternate function is no longer available.

To use an alternate function, the corresponding peripheral must be enabled in the peripheral registers.

Alternate function remapping does not effect GPIO capabilities of the I/O ports (see GPIO section of the family reference manual, RM0016).

6 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated block of the memory. Except for the ROP (read-out protection) byte, each option byte has to be stored twice, in a regular form (OPTx) and a complemented one (NOPTx) for redundancy.

Option bytes can be modified in ICP mode (via SWIM) by accessing the address shown in *Table 7: Option bytes* below.

Option bytes can also be modified 'on the fly' by the application in IAP mode, except the ROP and UBC options that can only be toggled in ICP mode (via SWIM).

Refer to the STM8S Flash programming manual (PM0051) and STM8 SWIM communication protocol and debug module user manual (UM0470) for information on SWIM programming procedures.

Table 7. Option bytes

Addr.	Option name	Option byte no.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
4800h	Read-out protection (ROP)	OPT0	ROP[7:0]								00h
4801h	User boot code(UBC)	OPT1	UBC[7:0]								00h
4802h		NOPT1	NUBC[7:0]								FFh
4803h	Alternate function remapping (AFR)	OPT2	AFR7	AFR6	AFR5	AFR4	AFR3	AFR2	AFR1	AFR0	00h
4804h		NOPT2	NAFR7	NAFR6	NAFR5	NAFR4	NAFR3	NAFR2	NAFR1	NAFR0	FFh
4805h	Watchdog option	OPT3	Reserved				LSI _EN	IWDG _HW	WWDG _HW	WWDG _HALT	00h
4806h		NOPT3	Reserved				NLSI _EN	NIWDG_ HW	NWWDG _HW	NWWG _HALT	FFh
4807h	Clock option	OPT4	Reserved				EXT CLK	CKAWU SEL	PRS C1	PRS C0	00h
4808h		NOPT4	Reserved				NEXT CLK	NCKAWUS EL	NPR SC1	NPR SC0	FFh
4809h	HSE clock startup	OPT5	HSECNT[7:0]								00h
480Ah		NOPT5	NHSECNT[7:0]								FFh
480Bh	Reserved	OPT6	Reserved								00h
480Ch		NOPT6	Reserved								FFh
480Dh	Flash wait states	OPT7	Reserved							Wait state	00h
480Eh		NOPT7	Reserved							Nwait state	FFh
487Eh	Bootloader	OPTBL	BL[7:0]								00h
487Fh		NOPTBL	NBL[7:0]								FFh

Table 8. Option byte description

Option byte no.	Description
OPT0	**ROP[7:0]** *Memory readout protection (ROP)* AAh: Enable readout protection (write access via SWIM protocol) *Note: Refer to the family reference manual (RM0016) section on Flash memory readout protection for details.*
OPT1	**UBC[7:0]** *User boot code area* For STM8S105 (page size 128 bytes): 00h: no UBC, no write-protection 01h: Page 0 and 1 defined as UBC, memory write-protected 02h to FFh: Pages 2 to 255 defined as UBC, memory write-protected For STM8S103 (page size 64 bytes): 00h: no UBC, no write-protection 01h: Page 0 and 1 defined as UBC, memory write-protected 02h to 7Fh: Pages 2 to 127 defined as UBC, memory write-protected *Note: Refer to the family reference manual (RM0016) section on Flash write protection for more details.*
OPT2	**Note :** This remapping applies to STM8S105. For STM8S103 alternate function remapping refer to *Table 9 on page 34*. **AFR7***Alternate function remapping option 7* 0: Port D4 alternate function = TIM2_CC1 1: Port D4 alternate function = BEEP **AFR6** *Alternate function remapping option 6* 0: Port B5 alternate function = AIN5, port B4 alternate function = AIN4 1: Port B5 alternate function = I^2C_SDA, port B4 alternate function = I^2C_SCL **AFR5** *Alternate function remapping option 5* 0: Port B3 alternate function = AIN3, port B2 alternate function = AIN2, port B1 alternate function = AIN1, port B0 alternate function = AIN0 1: Port B3 alternate function = TIM1_ETR, port B2 alternate function = TIM1_NCC3, port B1 alternate function = TIM1_NCC2, port B0 alternate function = TIM1_NCC1 **AFR4** *Alternate function remapping option 4* 0: Port D7 alternate function = TLI 1: Port D7 alternate function = TIM1_CC4 **AFR3** *Alternate function remapping option 3* 0: Port D0 alternate function = TIM3_CC2 1: Port D0 alternate function = TIM1_BKIN **AFR2** *Alternate function remapping option 2* 0: Port D0 alternate function = TIM3_CC2 1: Port D0 alternate function = CLK_CCO Note: AFR2 option has priority over AFR3 if both are activated
OPT2 (cont'd)	**AFR1** *Alternate function remapping option 1* 0: Port A3 alternate function = TIM2_CC3, port D2 alternate function TIM3_CC1 1: Port A3 alternate function = TIM3_CC1, port D2 alternate function TIM2_CC3 **AFR0** *Alternate function remapping option 0* 0: Port D3 alternate function = TIM2_CC2 1: Port D3 alternate function = ADC_ETR

Table 8. Option byte description (continued)

Option byte no.	Description
OPT3	**LSI_EN:** *Low speed internal clock enable* 0: LSI clock is not available as CPU clock source 1: LSI clock is available as CPU clock source
	IWDG_HW: *Independent watchdog* 0: IWDG Independent watchdog activated by software 1: IWDG Independent watchdog activated by hardware
	WWDG_HW: *Window watchdog activation* 0: WWDG window watchdog activated by software 1: WWDG window watchdog activated by hardware
	WWDG_HALT: *Window watchdog reset on halt* 0: No reset generated on halt if WWDG active 1: Reset generated on halt if WWDG active
OPT4	**EXTCLK:** *External clock selection* 0: External crystal connected to OSCIN/OSCOUT 1: External clock signal on OSCIN
	CKAWUSEL: *Auto wake-up unit/clock* 0: LSI clock source selected for AWU 1: HSE clock with prescaler selected as clock source for for AWU
	PRSC[1:0] AWU clock prescaler 00: Reserved 01: 16 MHz to 128 kHz prescaler 10: 8 MHz to 128 kHz prescaler 11: 4 MHz to 128 kHz prescaler
OPT5	**HSECNT[7:0]:** *HSE crystal oscillator stabilization time* This configures the stabilisation time to 0, 16, 256, 4096 HSE cycles.
OPT6	Reserved
OPT7	Reserved
OPTBL	**BL[7:0]** *Bootloader option byte* This option is checked by the boot ROM code after reset. Depending on content of addresses 487Eh, 487Fh and 8000h (reset vector) the CPU jumps to the bootloader or to the reset vector. Refer to STM8S bootloader manual for more details.

Table 9. STM8S103x alternate function remapping bits.

Option byte no.	Description
OPT2	**AFR7** *Alternate function remapping option 7* 0: TBD 1: TBD **AFR6** *Alternate function remapping option 6* 0: TBD 1: TBD **AFR5** *Alternate function remapping option 5* 0: TBD 1: Reserved **AFR4** *Alternate function remapping option 4* 0: TBD 1: TBD **AFR3** *Alternate function remapping option 3* 0: TBD 1: TBD **AFR2** *Alternate function remapping option 2* 0: TBD 1: TBD **AFR1** *Alternate function remapping option 1* 0: TBD 1: TBD **AFR0** *Alternate function remapping option 0* 0: TBD 1: TBD

7 Electrical characteristics

7.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

7.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100 % of the devices with an ambient temperature at T_A = 25 °C and $T_A = T_{Amax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3 Σ).

7.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 5.0 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ± 2 Σ).

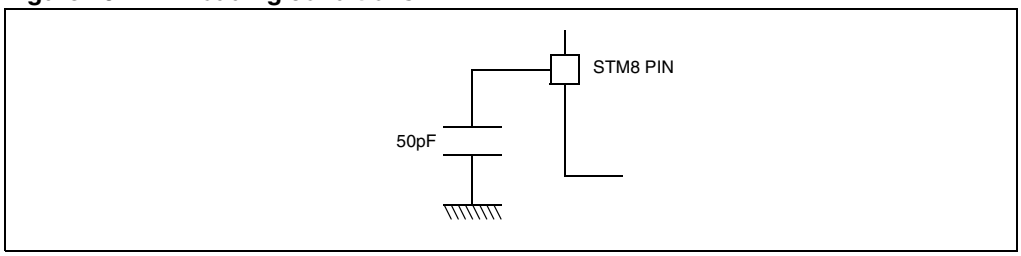
7.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

7.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 10*.

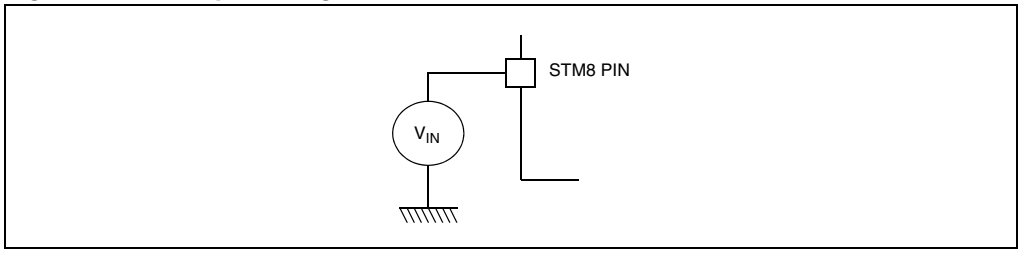
Figure 10. Pin loading conditions



7.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 11*.

Figure 11. Pin input voltage



7.2 Absolute maximum ratings

Stresses above those listed as 'absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 10. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DDx} - V_{SS}	Supply voltage (including V_{DDA} and V_{DDIO})(1)	-0.3	6.5	V
V_{IN}	Input voltage on true open drain pins (PE1, PE2)(2)	V_{SS} - 0.3	6.5	
	Input voltage on any other pin(2)	V_{SS} - 0.3	V_{DD} + 0.3	
$\lvert V_{DDx} - V_{SS} \rvert$	Variations between different power pins		50	mV
$\lvert V_{SSx} - V_{SS} \rvert$	Variations between all the different ground pins		50	

1. All power (V_{DD}, V_{DDIO}, V_{DDA}) and ground (V_{SS}, V_{SSIO}, V_{SSA}) pins must always be connected to the external power supply
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected

Table 11. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power lines (source)(1)	60	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	60	
I_{IO}	Output current sunk by any I/O and control pin	20	
	Output current source by any I/Os and control pin	- 20	
$I_{INJ(PIN)}$(2)(3)	Injected current on NRST pin	± 4	
	Injected current on OSCIN pin	± 4	
	Injected current on any other pin(4)	± 4	
$\Sigma I_{INJ(PIN)}$(2)	Total injected current (sum of all I/O and control pins)(4)	± 20	

1. All power (V_{DD}, V_{DDIO}, V_{DDA}) and ground (V_{SS}, V_{SSIO}, V_{SSA}) pins must always be connected to the external supply.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected
3. Negative injection disturbs the analog performance of the device.
4. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 12. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	150	

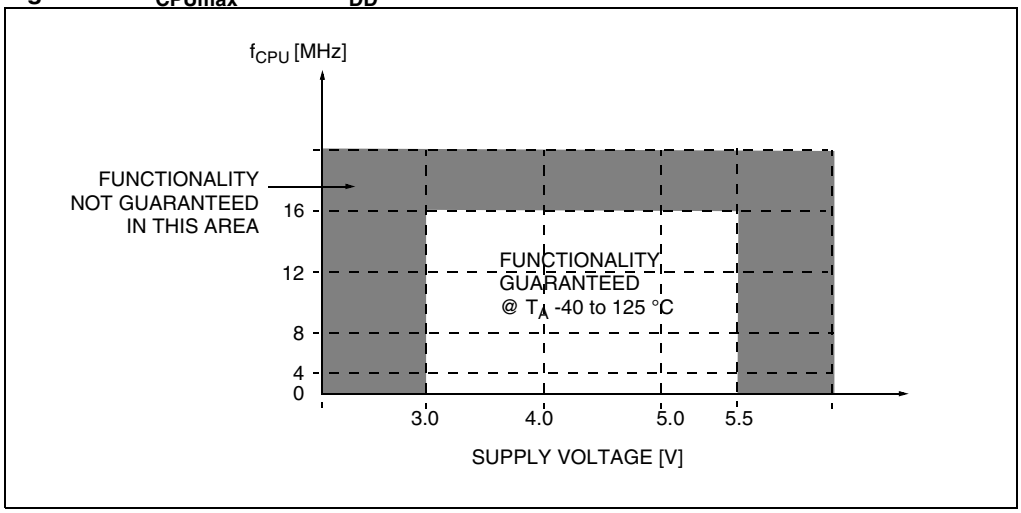
7.3 Operating conditions

Table 13. General operating conditions(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CPU}	Internal CPU clock frequency		0	16	MHz
V_{DD}/V_{DD_IO}	Standard operating voltage		3.0	5.5	V
P_D	Power dissipation at T_A= 85° C for suffix 6 or T_A= 125° C for suffix 3	LQFP48		TBD	mW
		LQFP44		TBD	
		LQFP32		TBD	
		VFQFN32		TBD	
		TSSOP20		TBD	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	-40	85	°C
		Low power dissipation(2)	-40	105	°C
	Ambient temperature for 3 suffix version	Maximum power dissipation	-40	125	°C
		Low power dissipation (2)	-40	TBD	°C
T_J	Junction temperature range	6 suffix version	-40	105	°C
		3 suffix version	-40	TBD	°C

1. TBD = to be determined.
2. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}

Figure 12. f_{CPUmax} versus V_{DD}



7.3.1 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 14. I/O static characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	V_{DD} = 5.0 V	-0.3 V		TBD	V
V_{IH}	Input high level voltage		0.7 x V_{DD}		V_{DD} + 0.3 V	V
V_{hys}	Hysteresis(2)			700		mV
R_{pu}	Pull-up resistor	V_{DD} = 5 V, V_{IN}=V_{SS}	30	45	60	kΩ
t_R, t_F	Rise and fall time (10% - 90%)	Fast I/Os Load = 50 pF			20 (3)	ns
		Standard and high sink I/Os Load = 50 pF			125 (3)	ns
I_{lkg}	Input leakage current, analog and digital	$V_{SS} \leq V_{IN} \leq V_{DD}$			±1 (3)	µA
$I_{lkg\ ana}$	Analog input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$			±250 (3)	nA
$I_{lkg(inj)}$	Leakage current in adjacent I/O(3)	Injection current ±4 mA			±1(3)	µA

1. TBD = to be determined.
2. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested in production.
3. Data based on characterization results, not tested in production.

Figure 13. Typical V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures

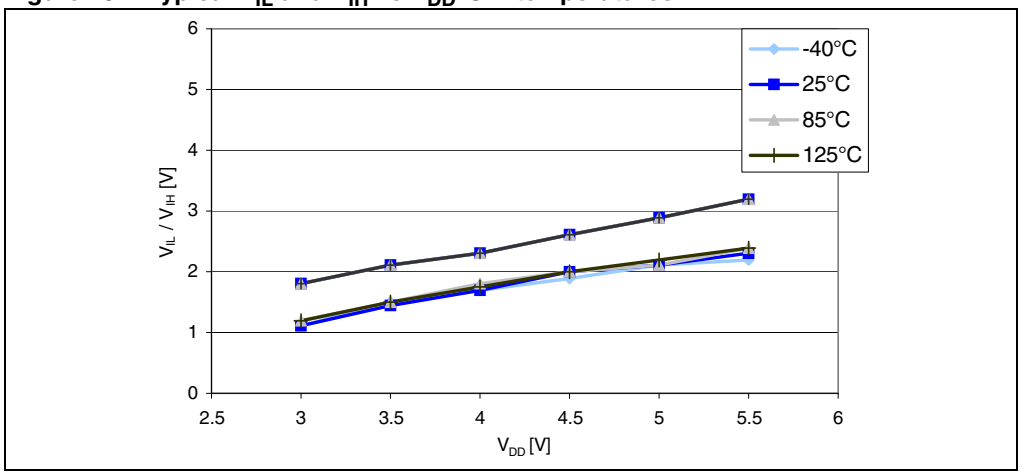


Figure 14. Typical pull-up resistance R_{PU} vs V_{DD} @ 4 temperatures

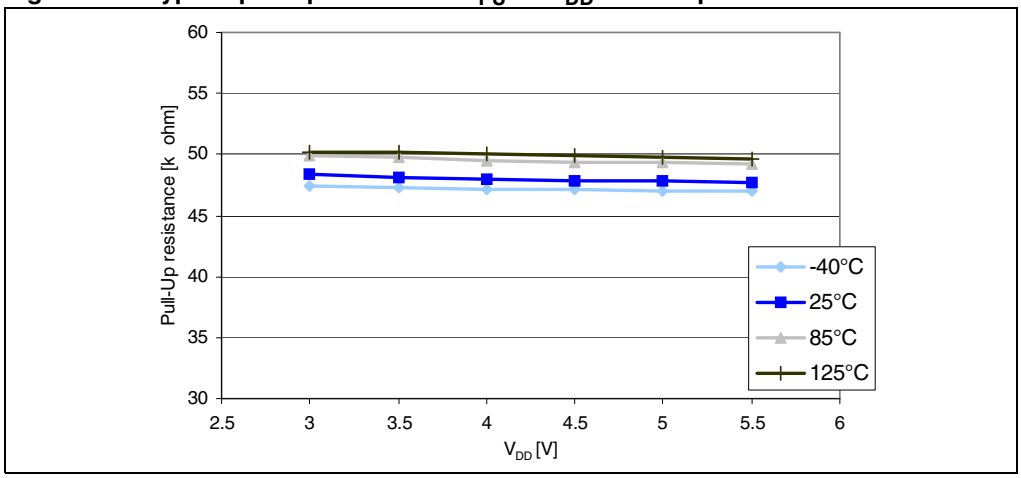
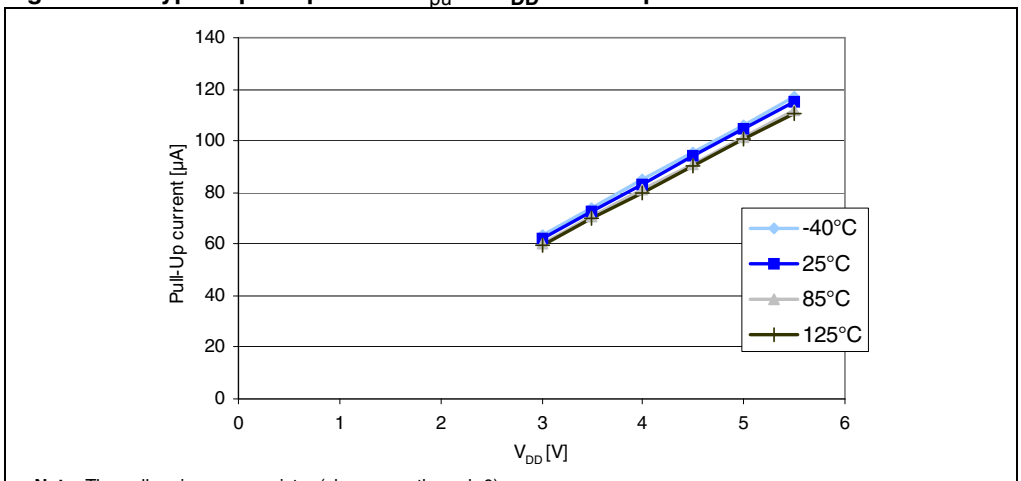


Figure 15. Typical pull-up current I_{pu} vs V_{DD} @ 4 temperatures



Note: The pull-up is a pure resistor (slope goes through 0).

Table 15. Output driving current (standard ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 4 pins sunk	I_{IO} = 4 mA,V_{DD} = 3.3 V		1000(1)	mV
	Output low level with 8 pins sunk	I_{IO}= 10 mA,V_{DD} = 5.0 V		2000	
V_{OH}	Output high level with 4 pins sourced	I_{IO} = 4 mA, V_{DD} = 3.3 V	2.1(1)		V
	Output high level with 8 pins sourced	I_{IO} = 10 mA, V_{DD} = 5.0 V	2.8		

1. Data based on characterization results, not tested in production

Table 16. Output driving current (true open drain ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 2 pins sunk	I_{IO} = 10 mA, V_{DD} = 3.3 V		1500(1)	mV
		I_{IO} = 10 mA, V_{DD} = 5.0 V		1000	
		I_{IO} = 20 mA, V_{DD} = 5.0 V		TBD(1)	

1. Data based on characterization results, not tested in production

Table 17. Output driving current (high sink ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 4 pins sunk	I_{IO} = 10 mA,V_{DD} = 3.3 V		1000(1)	mV
	Output low level with 8 pins sunk	I_{IO} = 10 mA,V_{DD} = 5.0 V		800	
	Output low level with 4 pins sunk	I_{IO} = 20 mA,V_{DD} = 5.0 V		1500(1)	
V_{OH}	Output high level with 4 pins sourced	I_{IO} = 10 mA, V_{DD} = 3.3 V	2.1(1)		V
	Output high level with 8 pins sourced	I_{IO} = 10 mA, V_{DD} = 5.0 V	4.0		
	Output high level with 4 pins sourced	I_{IO} = 20 mA, V_{DD} = 5.0 V	3.3(1)		

1. Data based on characterization results, not tested in production

Figure 16. Typ. V_{OL} @ V_{DD} = 3.3 V (standard ports)

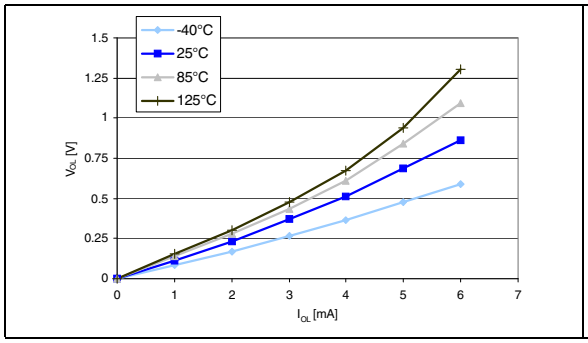


Figure 17. Typ. V_{OL} @ V_{DD} = 5.0 V (standard ports)

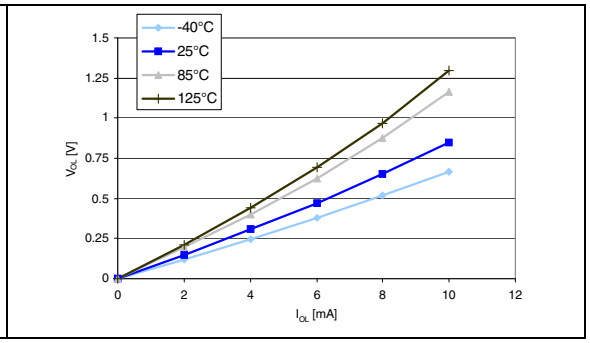


Figure 18. Typ. V_{OL} @ V_{DD} = 3.3 V (true open drain ports)

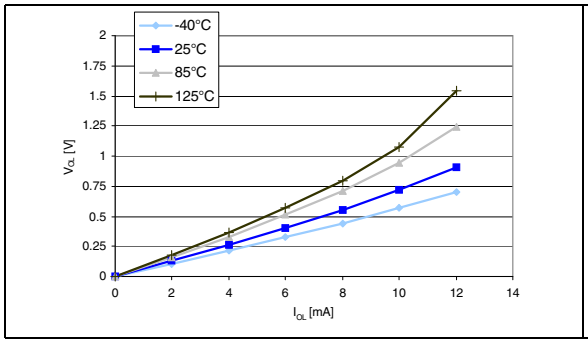


Figure 19. Typ. V_{OL} @ V_{DD} = 5.0 V (true open drain ports)

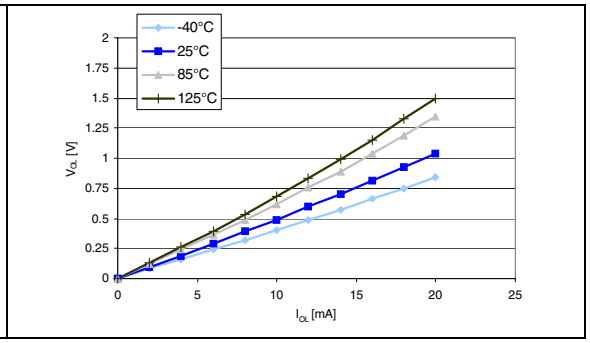


Figure 20. Typ. V_{OL} @ V_{DD} = 3.3 V (high sink ports)

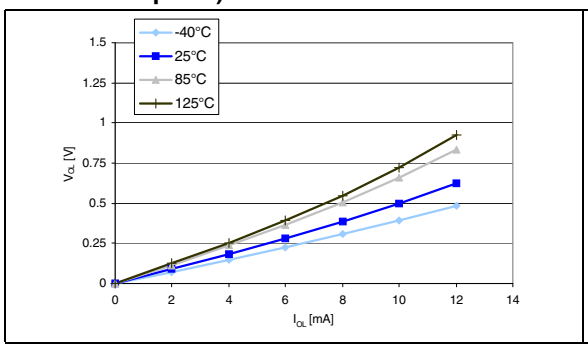


Figure 21. Typ. V_{OL} @ V_{DD} = 5.0 V (high sink ports)

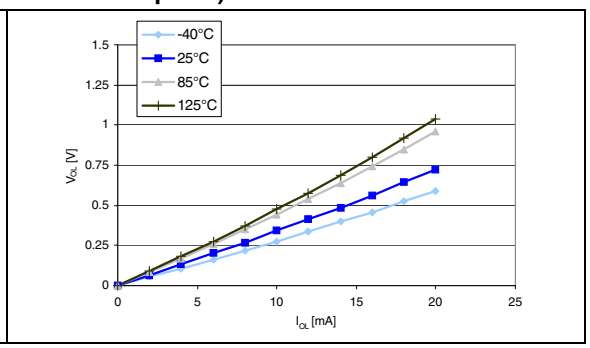


Figure 22. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (standard ports)

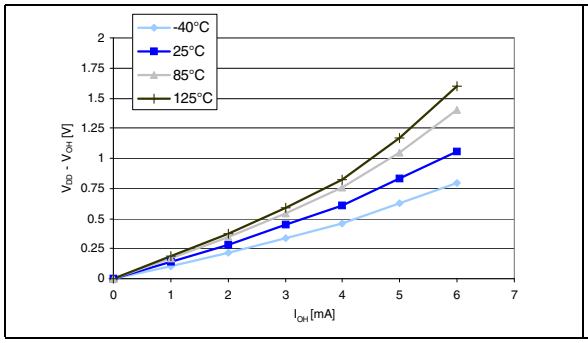


Figure 23. Typ. V_{DD} - V_{OH} @ V_{DD} = 5.0 V (standard ports)

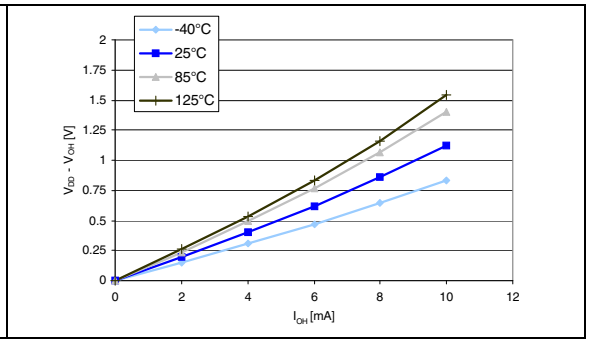


Figure 24. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (high sink ports)

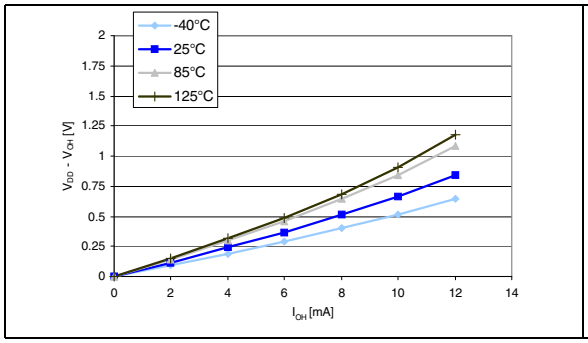
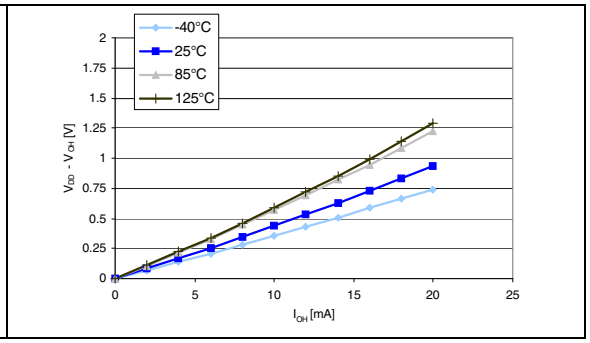


Figure 25. Typ. V_{DD} - V_{OH} @ V_{DD} = 5.0 V (high sink ports)



7.3.2 Reset pin characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 18. NRST pin characteristics(1)

Symbol	Parameter	Conditions	Min	Typ 1)	Max	Unit
$V_{IL(NRST)}$	NRST Input low level voltage (2)		V_{SS}		TBD	V
$V_{IH(NRST)}$	NRST Input high level voltage (2)		TBD		V_{DD}	
$V_{OL(NRST)}$	NRST Output low level voltage (2)	I_{OL}=TBD mA			TBD	
$R_{PU(NRST)}$	NRST Pull-up resistor (3)		30	40	60	kΩ
$V_{F(NRST)}$	NRST Input filtered pulse (4)			TBD		ns
$V_{NF(NRST)}$	NRST Input not filtered pulse (4)			TBD		µs

1. TBD = to be determined.
2. Data based on characterization results, not tested in production.
3. The R_{PU} pull-up equivalent resistor is based on a resistive transistor
4. Data guaranteed by design, not tested in production.

Figure 26. Typical NRST V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures

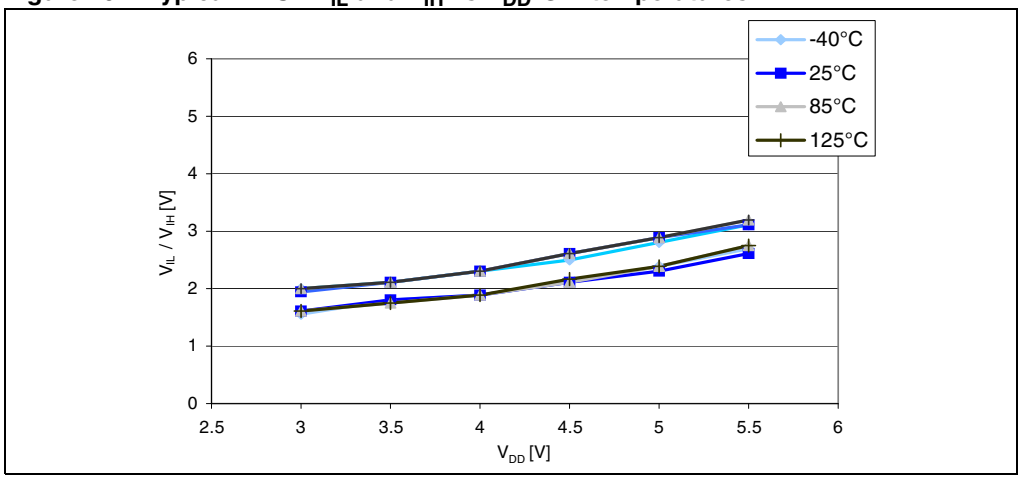


Figure 27. Typical NRST pull-up resistance R_{PU} vs V_{DD} @ 4 temperatures

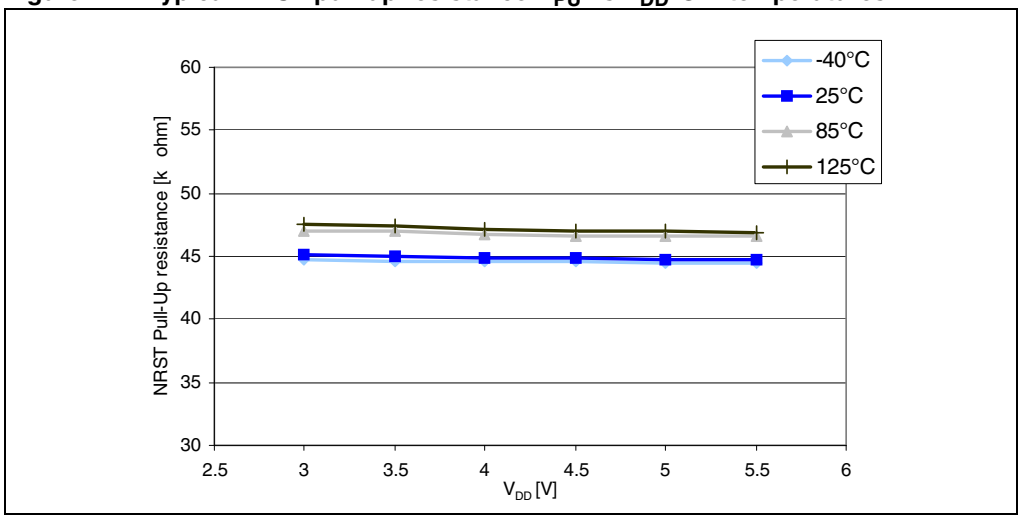
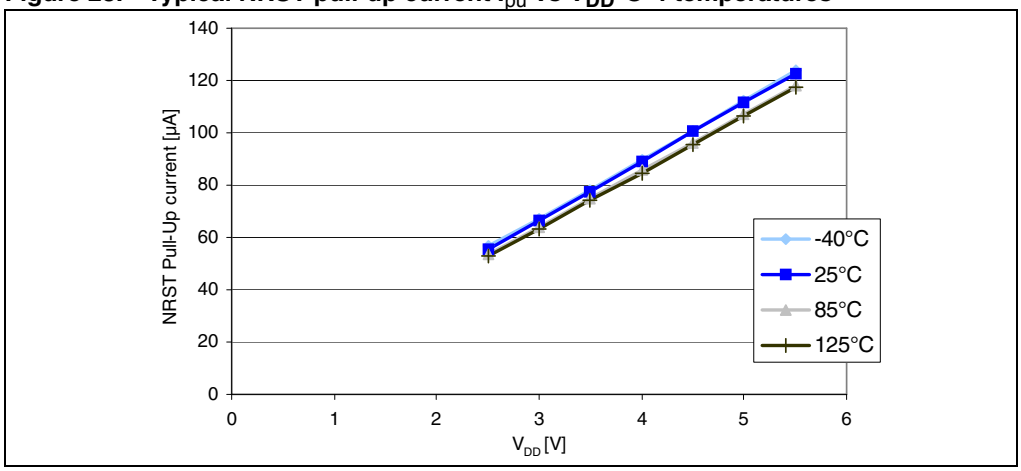
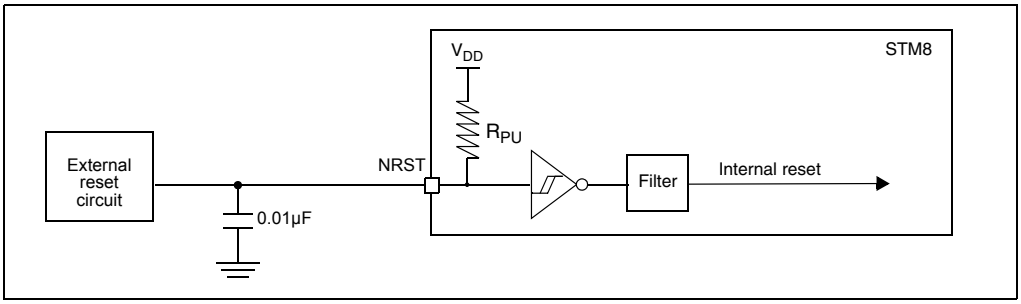


Figure 28. Typical NRST pull-up current I_{pu} vs V_{DD} @ 4 temperatures



The reset network shown in *Figure 29* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below the V_{IL} max. level specified in *Table 14*. Otherwise the reset is not taken into account internally.

Figure 29. Recommended reset pin protection



8 Package characteristics

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK® specifications are available at *www.st.com*.

8.1 Package mechanical data

8.1.1 LQFP package mechanical data

Figure 30. 48-pin low profile quad flat package (7 x 7)

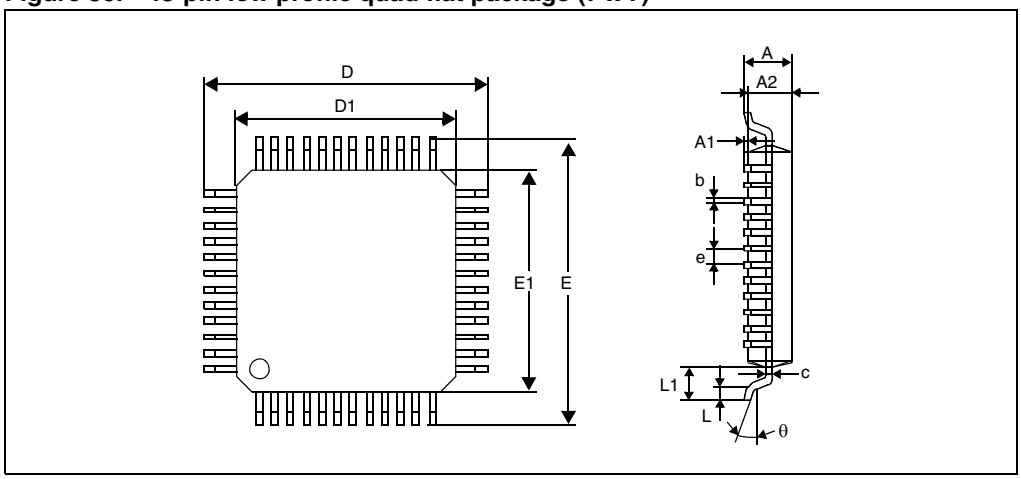


Table 19. 48-pin low profile quad flat package mechanical data

Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
C	0.09		0.20	0.0035		0.0079
D		9.00			0.3543	
D1		7.00			0.2756	
E		9.00			0.3543	
E1		7.00			0.2756	
e		0.50			0.0197	
q	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	

1. Values in inches are converted from mm and rounded to 4 decimal digits

Figure 31. 44-pin low profile quad flat package (10 x 10)

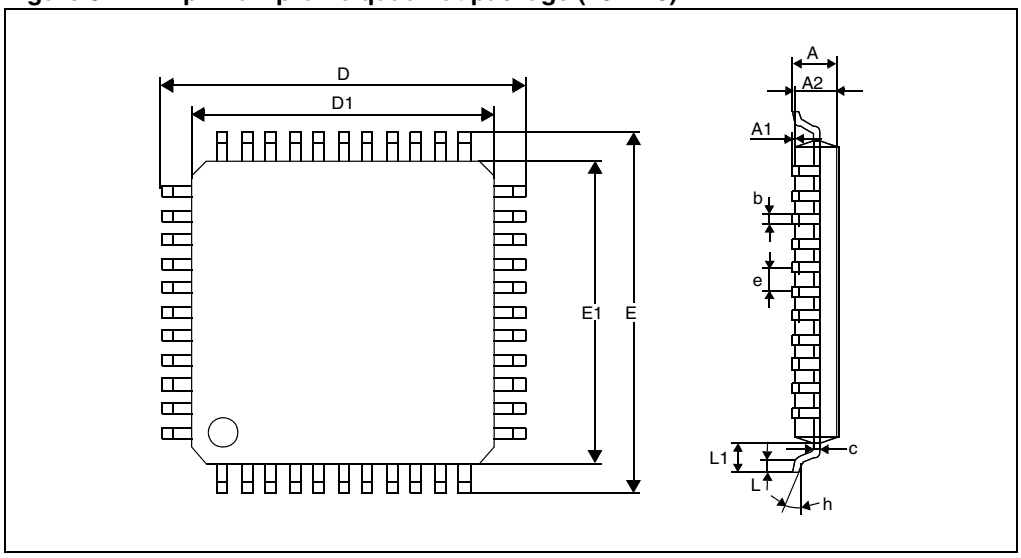


Table 20. 44-pin low profile quad flat package mechanical data

Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.30	0.37	0.45	0.0118	0.0146	0.0177
C	0.09		0.20	0.0035		0.0079
D		12.00			0.4724	
D1		10.00			0.3937	
E		12.00			0.4724	
E1		10.00			0.3937	
e		0.80			0.0315	
q	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	

1. Values in inches are converted from mm and rounded to 4 decimal digits

Figure 32. 32-pin low profile quad flat package (7 x 7)

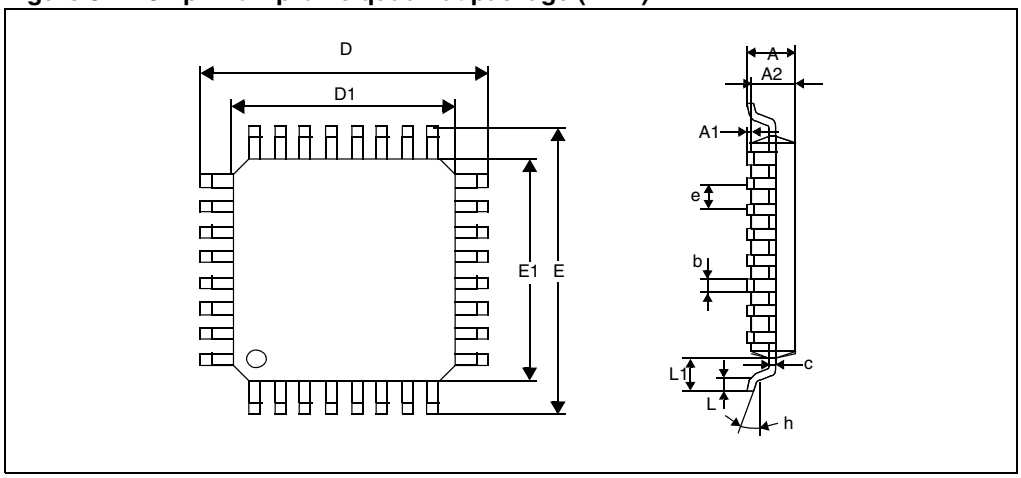


Table 21. 32-pin low profile quad flat package mechanical data

Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.30	0.37	0.45	0.0118	0.0146	0.0177
C	0.09		0.20	0.0035		0.0079
D		9.00			0.3543	
D1		7.00			0.2756	
E		9.00			0.3543	
E1		7.00			0.2756	
e		0.80			0.0315	
q	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	

1. Values in inches are converted from mm and rounded to 4 decimal digits

8.1.2 QFN package mechanical data

Figure 33. 32-lead very thin fine pitch quad flat no-lead package (5 x 5)

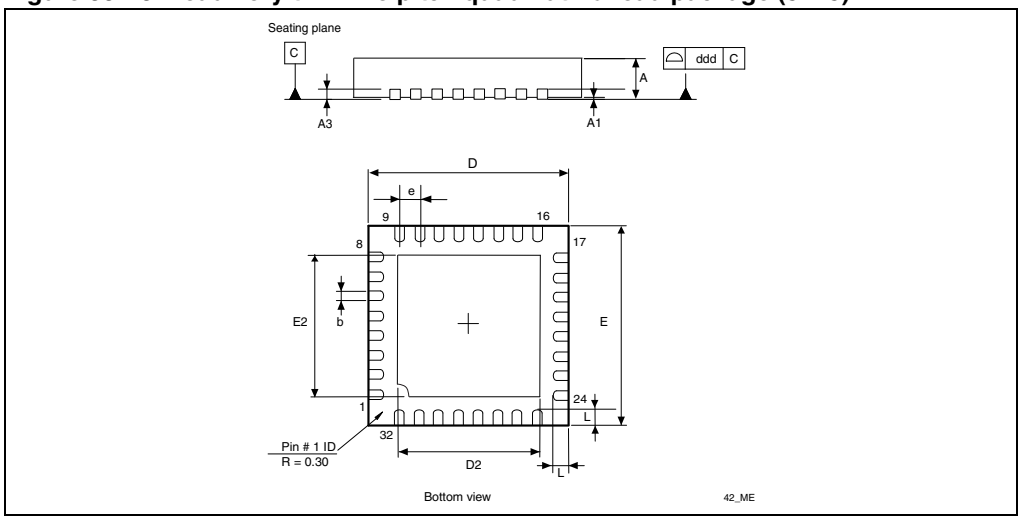


Table 22. 32-lead very thin fine pitch quad flat no-lead package mechanical data

Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1	0	0.02	0.05		0.0008	0.0020
A3		0.20			0.0079	
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
D	4.85	5.00	5.15	0.1909	0.1969	0.2028
D2	3.20	3.45	3.70	0.1260		0.1457
E	4.85	5.00	5.15	0.1909	0.1969	0.2028
E2	3.20	3.45	3.70	0.1260	0.1358	0.1457
e		0.50			0.0197	
L	0.30	0.40	0.50	0.0118	0.0157	0.0197
ddd			0.08			0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits

1. TBD = to be determined.

8.1.3 TSSOP package mechanical data

Figure 34. TSSOP 20-pin, 4.40 mm body, 0.65 mm pitch

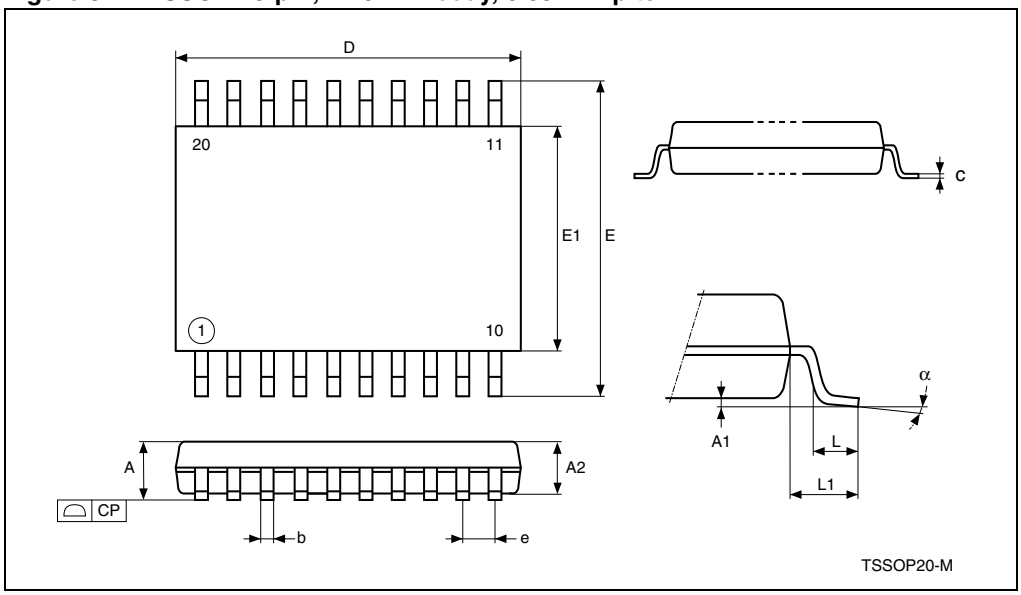


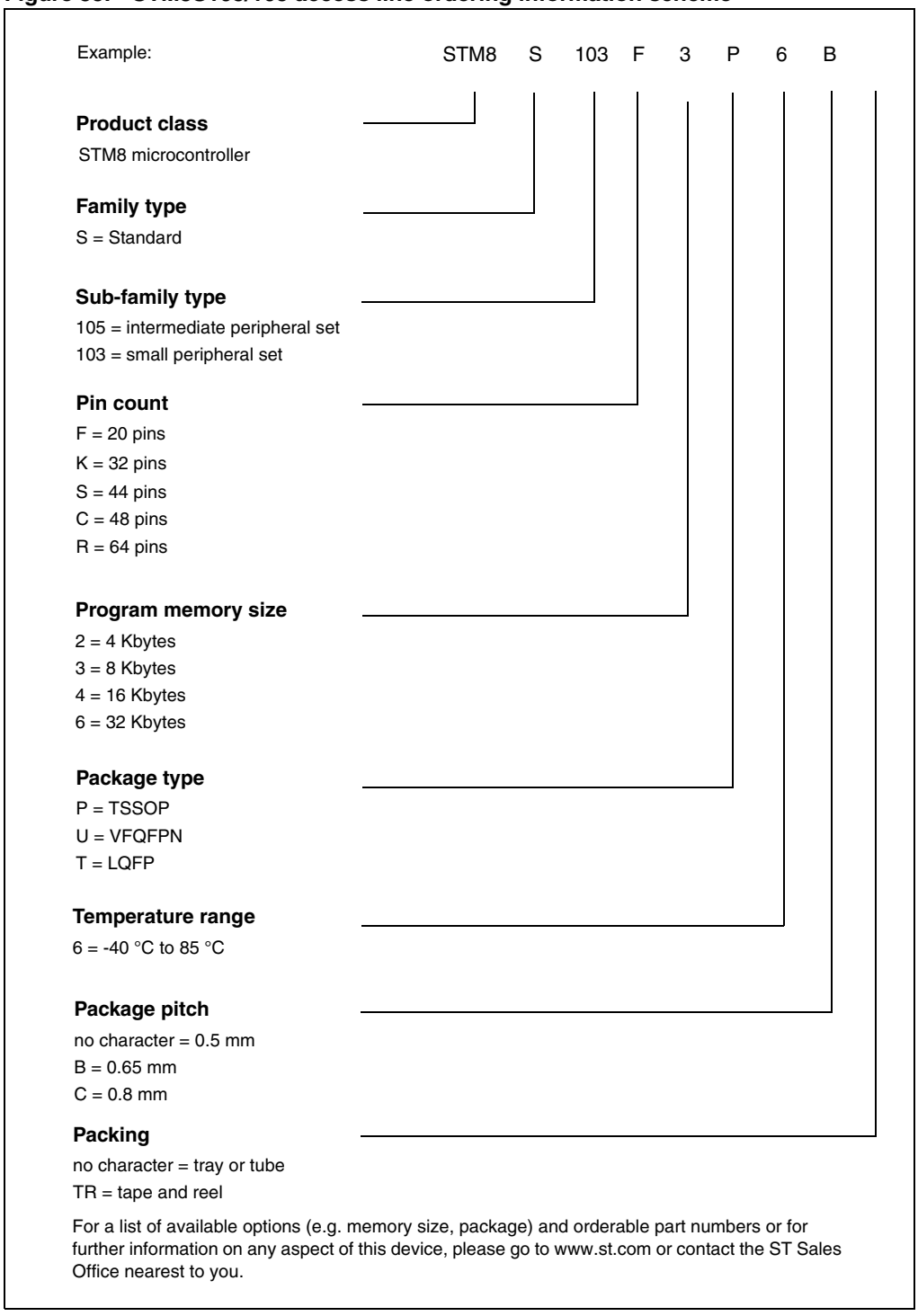
Table 23. TSSOP 20-pin, 4.40 mm body, 0.65 mm pitch mechanical data

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.2			0.0472
A1	0.05		0.15	0.002		0.0059
A2	0.8	1	1.05	0.0315	0.0394	0.0413
b	0.19		0.3	0.0075		0.0118
CP			0.1			0.0039
c	0.09		0.2	0.0035		0.0079
D	6.4	6.5	6.6	0.252	0.2559	0.2598
E	6.2	6.4	6.6	0.2441	0.252	0.2598
E1	4.3	4.4	4.5	0.1693	0.1732	0.1772
e	-	0.65	-	-	0.0256	-
L	0.45	0.6	0.75	0.0177	0.0236	0.0295
L1		1			0.0394	
a	0°		8°	0°		8°

1. Values in inches are converted from mm and rounded to 4 decimal digits

9 Ordering information

Figure 35. STM8S103/105 access line ordering information scheme



10 STM8 development tools

Development tools for the STM8 microcontrollers include the full-featured STice emulation system supported by a complete software tool package including C compiler, assembler and integrated development environment with high-level language debugger. In addition, the STM8 is to be supported by a complete range of tools including starter kits, evaluation boards and a low-cost in-circuit debugger/programmer.

10.1 Emulation and in-circuit debugging tools

The STM8 tool line includes the full-featured STice emulation system offering a complete range of emulation and in-circuit debugging features on a platform that is designed for versatility and cost-effectiveness. In addition, STM8 application development is supported by a low-cost in-circuit debugger/programmer.

The STice is the fourth generation of full featured emulators from STMicroelectronics. It offers new advanced debugging capabilities including profiling and coverage to help detect and eliminate bottlenecks in application execution and dead code when fine tuning an application.

In addition, STice offers in-circuit debugging and programming of STM8 microcontrollers via the STM8 single wire interface module (SWIM), which allows non-intrusive debugging of an application while it runs on the target microcontroller.

For improved cost effectiveness, STice is based on a modular design that allows you to order exactly what you need to meet your development requirements and to adapt your emulation system to support existing and future ST microcontrollers.

STice key features

- Occurrence and time profiling and code coverage (new features)
- Advanced breakpoints with up to 4 levels of conditions
- Data breakpoints
- Program and data trace recording up to 128 K records
- Read/write on the fly of memory during emulation
- In-circuit debugging/programming via SWIM protocol
- 8-bit probe analyzer
- 1 input and 2 output triggers
- Power supply follower managing application voltages between 1.62 to 5.5 V
- Modularity that allows you to specify the components you need to meet your development requirements and adapt to future requirements
- Supported by free software tools that include integrated development environment (IDE), programming software interface and assembler for STM8

10.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST visual develop (STVD) IDE and the ST visual programmer (STVP) software interface. STVD provides seamless integration of the cosmic C compiler for STM8, which is available in a free version that outputs up to 16 Kbytes of code.

10.2.1 STM8 toolset

STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at www.st.com/mcu. This package includes:

ST visual develop – Full-featured integrated development environment from ST, featuring

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

ST visual programmer (STVP) – Easy-to-use, unlimited graphical interface allowing read, write and verify of your STM8 microcontroller's Flash memory. STVP also offers project mode for saving programming configurations and automating programming sequences.

10.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of your application directly from an easy-to-use graphical interface.

Available toolchains include:

- **Cosmic C compiler for STM8** – Available in a free version that outputs up to 16 Kbytes of code. For more information, see www.cosmic-software.com.
- **Raisonance C compiler for STM8** – Available in a free version that outputs up to 16 Kbytes of code. For more information, see www.raisonance.com.
- **ST7/STM8 assembler linker** – Free assembly toolchain included in the ST7/STM8 toolset, which allows you to assemble and link your application source code.

10.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8 Flash microcontroller on your application board via the SWIM protocol. Additional tools are to include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for programming your STM8.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.

11 Revision history

Table 24. Document revision history

Date	Revision	Changes
05-Jun-2008	1	Initial release.
23-Jun-2008	2	Corrected number of high sink outputs to 9 in *I/Os on page 1*. Updated part numbers in *Table 2: STM8S103/105 access line features on page 7*.

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