

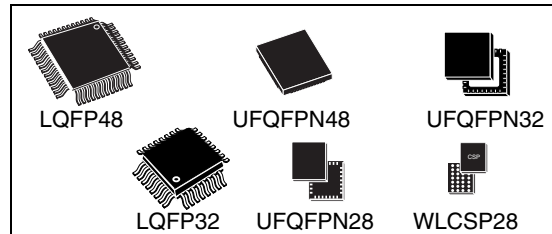


STM8L151x4, STM8L151x6, STM8L152x4, STM8L152x6

8-bit ultralow power MCU, up to 32 KB Flash, 1 KB Data EEPROM
RTC, LCD, timers, USART, I2C, SPI, ADC, DAC, comparators

Features

- Operating conditions
 - Operating power supply range 1.8 V to 3.6 V (down to 1.65 V at power down)
 - Temperature range: - 40 °C to 85 or 125 °C
- Low power features
 - 5 low power modes: Wait , Low power run (5.1 µA), Low power wait (3 µA), Active-halt with full RTC (1.3 µA), Halt (350 nA)
 - Dynamic consumption: 195 µA/MHz+440µA
 - Ultralow leakage per I/O: 50 nA
 - Fast wakeup from Halt: 4.7 µs
- Advanced STM8 core
 - Harvard architecture and 3-stage pipeline
 - Max freq. 16 MHz, 16 CISC MIPS peak
 - Up to 40 external interrupt sources
- Reset and supply management
 - Low power, ultrasafe BOR reset with 5 selectable thresholds
 - Ultralow power POR/PDR
 - Programmable voltage detector (PVD)
- Clock management
 - 1 to 16 MHz crystal oscillator
 - 32 kHz crystal oscillator
 - Internal 16 MHz factory-trimmed RC
 - Internal 38 kHz low consumption RC
 - Clock security system
- Low power RTC
 - BCD calendar with alarm interrupt
 - Auto-wakeup from Halt w/ periodic interrupt
- LCD: up to 4x28 segments w/ step-up converter
- Memories
 - Up to 32 KB of Flash program memory and 1 Kbyte of data EEPROM with ECC, RWW
 - Flexible write and read protection modes
 - Up to 2 Kbytes of RAM
- DMA
 - 4 channels; supported peripherals: ADC, DAC, SPI, I2C, USART, timers
 - 1 channel for memory-to-memory
- 12-bit DAC with output buffer



- 12-bit ADC up to 1 Msps/25 channels
 - T. sensor and internal reference voltage
- 2 Ultralow power comparators
 - 1 with fixed threshold and 1 rail to rail
 - Wakeup capability
- Timers
 - Two 16-bit timers with 2 channels (used as IC, OC, PWM), quadrature encoder
 - One 16-bit advanced control timer with 3 channels, supporting motor control
 - One 8-bit timer with 7-bit prescaler
 - 2 watchdogs: 1 Window, 1 Independent
 - Beeper timer with 1, 2 or 4 kHz frequencies
- Communication interfaces
 - Synchronous serial interface (SPI)
 - Fast I2C 400 kHz SMBus and PMBus
 - USART (ISO 7816 interface and IrDA)
- Up to 41 I/Os, all mappable on interrupt vectors
- Up to 16 capacitive sensing channels with free firmware
- Development support
 - Fast on-chip programming and non intrusive debugging with SWIM
 - Bootloader using USART
- 96-bit unique ID

Table 1. Device summary

| Reference | Part number |
|-----------------------------|--|
| STM8L151xx (without LCD) | STM8L151C6, STM8L151C4, STM8L151K6, STM8L151K4, STM8L151G6, STM8L151G4 |
| STM8L152xx (with LCD) | STM8L152C6, STM8L152C4, STM8L152K6, STM8L152K4 |

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1 Introduction

This document describes the STM8L15xxx family features, pinout, mechanical data and ordering information. The STM8L15xxx devices are referred to as medium-density devices in the STM8L15xxx reference manual (RM0031) and in the STM8L Flash programming manual (PM0054)

For more details on the whole STMicroelectronics ultralow power family please refer to [Section 2.2: Ultralow power continuum on page 12](#).

For information on the debug module and SWIM (single wire interface module), refer to the STM8 SWIM communication protocol and debug module user manual (UM0470). For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

The STM8L15xxx devices provide the following benefits:

- Integrated system
 - Up to 32 Kbytes of medium-density embedded Flash program memory
 - 1 Kbyte of data EEPROM
 - Internal high speed and low-power low speed RC.
 - Embedded reset
- Ultralow power consumption
 - 195 $\mu\text{A}/\text{MHZ}$ + 440 μA (dynamic consumption)
 - 0.9 μA with LSI in Active-halt mode
 - Clock gated system and optimized power management
 - Capability to execute from RAM for Low power wait mode and Low power run mode
- Advanced features
 - Up to 16 MIPS at 16 MHz CPU clock frequency
 - Direct memory access (DMA) for memory-to-memory or peripheral-to-memory access.
- Short development cycles
 - Application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals.
 - Wide choice of development tools

All devices offer 12-bit ADC, DAC, two comparators, Real-time clock three 16-bit timers, one 8-bit timer as well as standard communication interface such as SPI, I2C and USART. A 4x28-segment LCD is available on the STM8L152xx line. [Table 2: STM8L15x low power device features and peripheral counts](#) and [Section 3 on page 13](#) give an overview of the complete range of peripherals proposed in this family.

The STM8L15xxx microcontroller family is suitable for a wide range of applications:

- Medical and handheld equipment
- Application control and user interface
- PC peripherals, gaming, GPS and sport equipment
- Alarm systems, wired and wireless sensors

[Figure 1 on page 13](#) shows the general block diagram of the device family.

2 Description

The STM8L15xxx devices are members of the STM8L Ultralow power 8-bit family. The STM8L15xxx family operates from 1.8 V to 3.6 V (down to 1.65 V at power down) and is available in the -40 to +85 °C and -40 to +125 °C temperature ranges.

The STM8L15xxx Ultralow power family features the enhanced STM8 CPU core providing increased processing power (up to 16 MIPS at 16 MHz) while maintaining the advantages of a CISC architecture with improved code density, a 24-bit linear addressing space and an optimized architecture for low power operations.

The family includes an integrated debug module with a hardware interface (SWIM) which allows non-intrusive In-Application debugging and ultrafast Flash programming.

All STM8L15xxx microcontrollers feature embedded data EEPROM and low power low-voltage single-supply program Flash memory.

They incorporate an extensive range of enhanced I/Os and peripherals.

The modular design of the peripheral set allows the same peripherals to be found in different ST microcontroller families including 32-bit families. This makes any transition to a different family very easy, and simplified even more by the use of a common set of development tools.

Six different packages are proposed from 28 to 48 pins. Depending on the device chosen, different sets of peripherals are included. .

All STM8L Ultralow power products are based on the same architecture with the same memory mapping and a coherent pinout.

2.1 Device overview

Table 2. STM8L15x low power device features and peripheral counts

| Features | | STM8L151Gx | | STM8L15xKx | | STM8L15xCx | |
|---|------------------|---|----|--|----|---|----|
| Flash (Kbytes) | | 16 | 32 | 16 | 32 | 16 | 32 |
| Data EEPROM (Kbytes) | | 1 | | | | | |
| RAM-Kbytes | | 2 | | 2 | | 2 | |
| LCD | | No | | 4x17 ⁽¹⁾ | | 4x28 ⁽¹⁾ | |
| Timers | Basic | 1 (8-bit) | | 1 (8-bit) | | 1 (8-bit) | |
| | General purpose | 2 (16-bit) | | 2 (16-bit) | | 2 (16-bit) | |
| | Advanced control | 1 (16-bit) | | 1 (16-bit) | | 1 (16-bit) | |
| Communication interfaces | SPI | 1 | | 1 | | 1 | |
| | I2C | 1 | | 1 | | 1 | |
| | USART | 1 | | 1 | | 1 | |
| GPIOs | | 26 ⁽³⁾ | | 30 ⁽²⁾⁽³⁾ or 29 ⁽¹⁾⁽³⁾ | | 41 ⁽³⁾ | |
| 12-bit synchronized ADC (number of channels) | | 1 (18) | | 1 (22 ⁽²⁾ or 21 ⁽¹⁾) | | 1 (25) | |
| 12-Bit DAC (number of channels) | | 1 (1) | | 1 (1) | | 1 (1) | |
| Comparators COMP1/COMP2 | | 2 | | 2 | | 2 | |
| Others | | RTC, window watchdog, independent watchdog, 16-MHz and 38-kHz internal RC, 1- to 16-MHz and 32-kHz external oscillator | | | | | |
| CPU frequency | | 16 MHz | | | | | |
| Operating voltage | | 1.8 V to 3.6 V (down to 1.65 V at power down) | | | | | |
| Operating temperature | | -40 to +85 °C / -40 to +125 °C | | | | | |
| Packages | | UFQFPN28 (4x4; 0.6 mm thickness) WLCSP28 | | UFQFPN32 (5x5; 0.6 mm thickness) LQFP32(7x7) | | UFQFPN48 (4x4; 0.6 mm thickness) LQFP48 | |

1. STM8L152xx versions only
2. STM8L151xx versions only
3. The number of GPIOs given in this table includes the NRST/PA1 pin but the application can use the NRST/PA1 pin as general purpose output only (PA1).

2.2 Ultralow power continuum

The Ultralow power STM8L151xx and STM8L152xx are fully pin-to-pin, software and feature compatible. Besides the full compatibility within the family, the devices are part of STMicroelectronics microcontrollers UltraLowPower strategy which also includes STM8L101xx and STM32L15xxx. The STM8L and STM32L families allow a continuum of performance, peripherals, system architecture, and features.

They are all based on STMicroelectronics 0.13 μm ultralow leakage process.

- Note:
- 1 The STM8L151xx and STM8L152xx are pin-to-pin compatible with STM8L101xx devices.
 - 2 The STM32L family is pin-to-pin compatible with the general purpose STM32F family. Please refer to STM32L15x documentation for more information on these devices.

Performance

All families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM Cortex™-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the Ultralow power performance to range from 5 up to 33.3 DMIPs.

Shared peripherals

STM8L151xx/152xx and STM32L15xx share identical peripherals which ensure a very easy migration from one family to another:

- Analog peripherals: ADC1, DAC, and comparators COMP1/COMP2
- Digital peripherals: RTC and some communication interfaces

Common system strategy

To offer flexibility and optimize performance, the STM8L151xx/152xx and STM32L15xx devices use a common architecture:

- Same power supply range from 1.8 to 3.6 V, down to 1.65 V at power down
- Architecture optimized to reach ultralow consumption both in low power modes and Run mode
- Fast startup strategy from low power modes
- Flexible system clock
- Ultrasafe reset: same reset strategy for both STM8L15xxx and STM32L15xxx including power-on reset, power-down reset, brownout reset and programmable voltage detector.

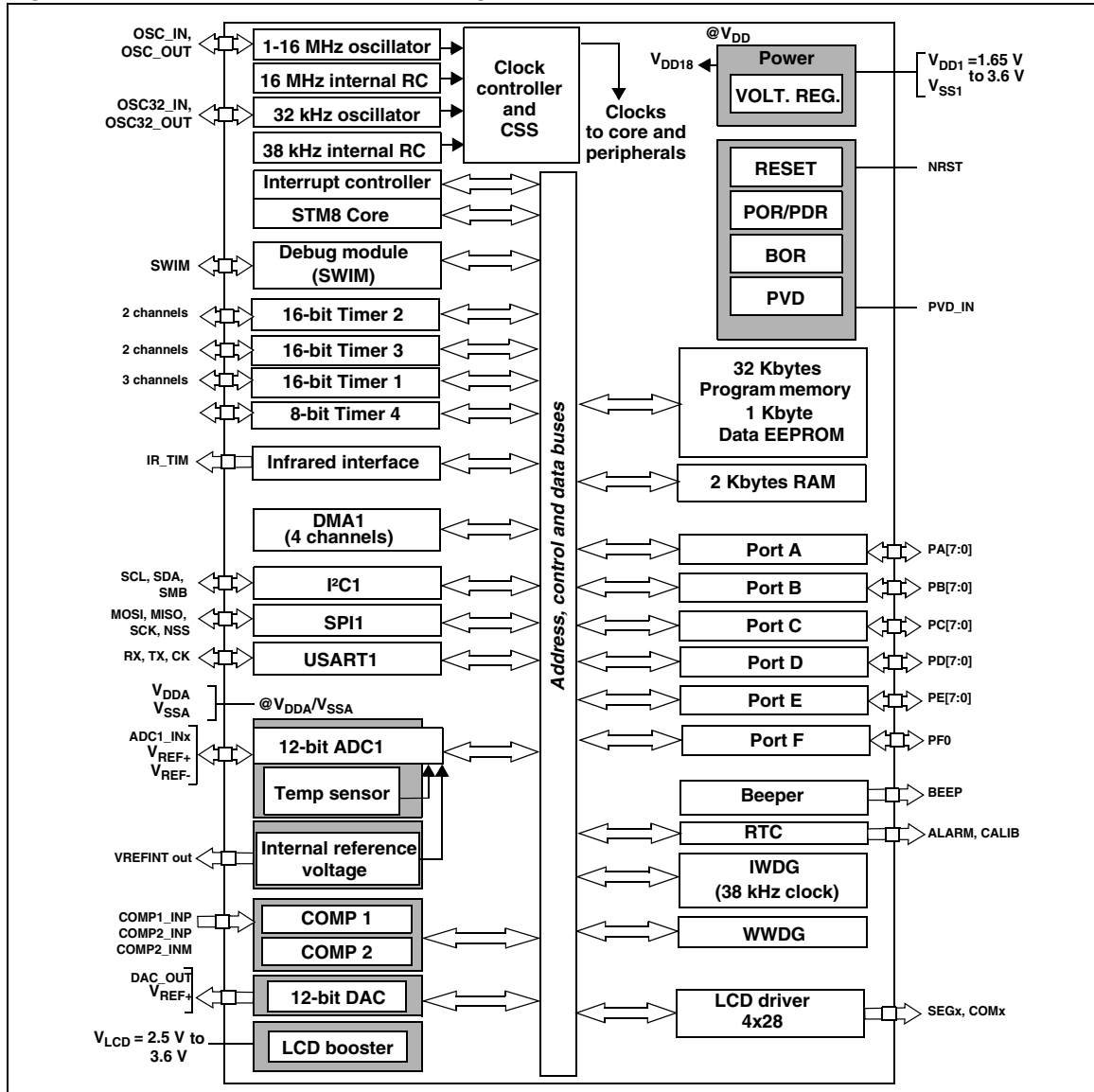
Features

ST UltraLowPower continuum also lies in feature compatibility:

- More than 10 packages with pin count from 20 to 100 pins and size down to 3 x 3 mm
- Memory density ranging from 4 to 128 Kbytes

3 Functional overview

Figure 1. STM8L15xxx device block diagram



1. **Legend:**
 ADC: Analog-to-digital converter
 BOR: Brownout reset
 DMA: Direct memory access
 DAC: Digital-to-analog converter
 I2C: Inter-integrated circuit multimaster interface
 IWDG: Independent watchdog
 LCD: Liquid crystal display
 POR/PDR: Power on reset / power down reset
 RTC: Real-time clock
 SPI: Serial peripheral interface
 SWIM: Single wire interface module
 USART: Universal synchronous asynchronous receiver transmitter
 WWDG: Window watchdog

3.1 Low power modes

The STM8L15xxx supports five low power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Wait mode:** CPU clock is stopped, but selected peripherals keep running. An internal or external interrupt or a Reset can be used to exit the microcontroller from Wait mode (WFE or WFI mode). Wait consumption: refer to [Table 20](#).
- **Low power run mode:** The CPU and the selected peripherals are running. Execution is done from RAM with a low speed oscillator (LSI or LSE). Flash and data EEPROM are stopped and the voltage regulator is configured in Ultralow power mode. The microcontroller enters Low power run mode by software and can exit from this mode by software or by a reset.
All interrupts must be masked. They cannot be used to exit the microcontroller from this mode. Low power run mode consumption: refer to [Table 21](#).
- **Low power wait mode:** This mode is entered when executing a Wait for event in Low power run mode. It is similar to Low power run mode except that the CPU clock is stopped. The wakeup from this mode is triggered by a Reset or by an internal or external event (peripheral event generated by the timers, serial interfaces, DMA controller (DMA1), comparators and I/O ports). When the wakeup is triggered by an event, the system goes back to Low power run mode.
All interrupts must be masked. They cannot be used to exit the microcontroller from this mode. Low power wait mode consumption: refer to [Table 22](#).
- **Active-halt mode:** CPU and peripheral clocks are stopped, except RTC. The wakeup can be triggered by RTC interrupts, external interrupts or reset. Active-halt consumption: refer to [Table 23](#) and [Table 24](#).
- **Halt mode:** CPU and peripheral clocks are stopped, the device remains powered on. The wakeup is triggered by an external interrupt or reset. A few peripherals have also a wakeup from Halt capability. Switching off the internal reference voltage reduces power consumption. Through software configuration it is also possible to wake up the device without waiting for the internal reference voltage wakeup time to have a fast wakeup time of 5 μ s. Halt consumption: refer to [Table 25](#).

3.2 Central processing unit STM8

3.2.1 Advanced STM8 Core

The 8-bit STM8 core is designed for code efficiency and performance with an Harvard architecture and a 3-stage pipeline.

It contains 6 internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing, and 80 instructions.

Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching most instructions
- X and Y 16-bit index registers - enabling indexed addressing modes with or without

offset and read-modify-write type data manipulations

- 8-bit accumulator
- 24-bit program counter - 16 Mbyte linear memory space
- 16-bit stack pointer - access to a 64 Kbyte level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction

Addressing

- 20 addressing modes
- Indexed indirect addressing mode for lookup tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

3.2.2 Interrupt controller

The STM8L15xxx features a nested vectored interrupt controller:

- Nested interrupts with 3 software priority levels
- 32 interrupt vectors with hardware priority
- Up to 40 external interrupt sources on 11 vectors
- Trap and reset interrupts

3.3 Reset and supply management

3.3.1 Power supply scheme

The device requires a 1.65 V to 3.6 V operating supply voltage (V_{DD}). The external power supply pins must be connected as follows:

- V_{SS1} ; V_{DD1} = 1.8 to 3.6 V, down to 1.65 V at power down: external power supply for I/Os and for the internal regulator. Provided externally through V_{DD1} pins, the corresponding ground pin is V_{SS1} .
- V_{SSA} ; V_{DDA} = 1.8 to 3.6 V, down to 1.65 V at power down: external power supplies for analog peripherals (minimum voltage to be applied to V_{DDA} is 1.8 V when the ADC1 is used). V_{DDA} and V_{SSA} must be connected to V_{DD1} and V_{SS1} , respectively.
- V_{SS2} ; V_{DD2} = 1.8 to 3.6 V, down to 1.65 V at power down: external power supplies for I/Os. V_{DD2} and V_{SS2} must be connected to V_{DD1} and V_{SS1} , respectively.
- V_{REF+} ; V_{REF-} (for ADC1): external reference voltage for ADC1. Must be provided externally through V_{REF+} and V_{REF-} pin.
- V_{REF+} (for DAC): external voltage reference for DAC must be provided externally through V_{REF+} .

3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR), coupled with a brownout reset (BOR) circuitry. At power-on, BOR is always active, and ensures proper operation starting from 1.8 V. After the 1.8 V BOR threshold is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently (in which case, the V_{DD} min value at power down is 1.65 V).

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Halt mode, it is possible to automatically switch off the internal reference voltage (and consequently the BOR) in Halt mode. The device remains under reset when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR} , without the need for any external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.3.3 Voltage regulator

The STM8L15xxx embeds an internal voltage regulator for generating the 1.8 V power supply for the core and peripherals.

This regulator has two different modes:

- Main voltage regulator mode (MVR) for Run, Wait for interrupt (WFI) and Wait for event (WFE) modes.
- Low power voltage regulator mode (LPVR) for Halt, Active-halt, Low power run and Low power wait modes.

When entering Halt or Active-halt modes, the system automatically switches from the MVR to the LPVR in order to reduce current consumption.

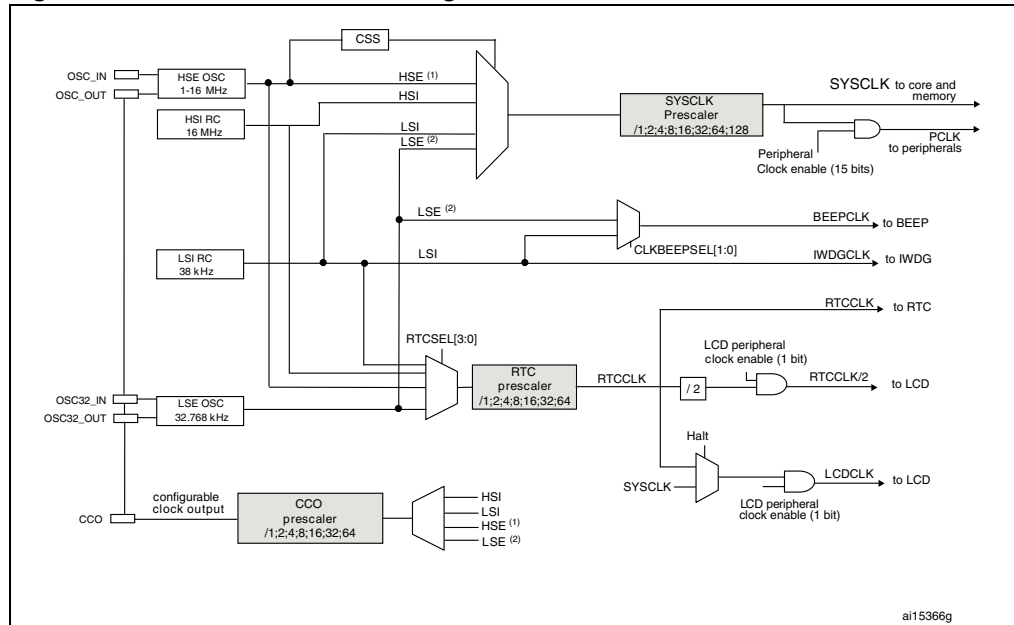
3.4 Clock management

The clock controller distributes the system clock (SYSCLK) coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness.

Features

- **Clock prescaler:** to get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** Clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock sources:** 4 different clock sources can be used to drive the system clock:
 - 1-16 MHz High speed external crystal (HSE)
 - 16 MHz High speed internal RC oscillator (HSI)
 - 32.768 Low speed external crystal (LSE)
 - 38 kHz Low speed internal RC (LSI)
- **RTC and LCD clock sources:** the above four sources can be chosen to clock the RTC and the LCD, whatever the system clock.
- **Startup clock:** After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** This feature can be enabled by software. If a HSE clock failure occurs, the system clock is automatically switched to HSI.
- **Configurable main clock output (CCO):** This outputs an external clock for use by the application.

Figure 2. STM8L15x clock tree diagram



1. The HSE clock source can be either an external crystal/ceramic resonator or an external source (HSE bypass). Refer to *Section HSE clock* in the STM8L15x reference manual (RM0031).
2. The LSE clock source can be either an external crystal/ceramic resonator or an external source (LSE bypass). Refer to *Section LSE clock* in the STM8L15x reference manual (RM0031).

3.5 Low power real-time clock

The real-time clock (RTC) is an independent binary coded decimal (BCD) timer/counter.

Six byte locations contain the second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day months are made automatically.

It provides a programmable alarm and programmable periodic interrupts with wakeup from Halt capability.

- Periodic wakeup time using the 32.768 kHz LSE with the lowest resolution (of 61 μ s) is from min. 122 μ s to max. 3.9 s. With a different resolution, the wakeup time can reach 36 hours
- Periodic alarms based on the calendar can also be generated from every second to every year

3.6 LCD (Liquid crystal display)

The liquid crystal display drives up to 4 common terminals and up to 28 segment terminals to drive up to 112 pixels.

- Internal step-up converter to guarantee contrast control whatever V_{DD} .
- Static 1/2, 1/3, 1/4 duty supported.
- Static 1/2, 1/3 bias supported.
- Phase inversion to reduce power consumption and EMI.
- Up to 4 pixels which can be programmed to blink.
- The LCD controller can operate in Halt mode.

Note: Unnecessary segments and common pins can be used as general I/O pins.

3.7 Memories

The STM8L15xxx devices have the following main features:

- Up to 2 Kbytes of RAM
- The non-volatile memory is divided into three arrays:
 - Up to 32 Kbytes of medium-density embedded Flash program memory
 - 1 Kbyte of Data EEPROM
 - Option bytes.

The EEPROM embeds the error correction code (ECC) feature. It supports the read-while-write (RWW): it is possible to execute the code from the program matrix while programming/erasing the data matrix.

The option byte protects part of the Flash program memory from write and readout piracy.

3.8 DMA

A 4-channel direct memory access controller (DMA1) offers a memory-to-memory and peripherals-from/to-memory transfer capability. The 4 channels are shared between the following IPs with DMA capability: ADC1, DAC, I2C1, SPI1, USART1, the 4 Timers.

3.9 Analog-to-digital converter

- 12-bit analog-to-digital converter (ADC1) with 25 channels (including 1 fast channel), temperature sensor and internal reference voltage
- Conversion time down to 1 μ s with $f_{SYSCLK} = 16$ MHz
- Programmable resolution
- Programmable sampling time
- Single and continuous mode of conversion
- Scan capability: automatic conversion performed on a selected group of analog inputs
- Analog watchdog
- Triggered by timer

Note: ADC1 can be served by DMA1.

3.10 Digital-to-analog converter (DAC)

- 12-bit DAC with output buffer
- Synchronized update capability using TIM4
- DMA capability
- External triggers for conversion
- Input reference voltage V_{REF+} for better resolution

Note: DAC can be served by DMA1.

3.11 Ultralow power comparators

The STM8L15x embeds two comparators (COMP1 and COMP2) sharing the same current bias and voltage reference. The voltage reference can be internal or external (coming from an I/O).

- One comparator with fixed threshold (COMP1).
- One comparator rail to rail with fast or slow mode (COMP2). The threshold can be one of the following:
 - DAC output
 - External I/O
 - Internal reference voltage or internal reference voltage submultiple (1/4, 1/2, 3/4)

The two comparators can be used together to offer a window function. They can wake up from Halt mode.

3.12 System configuration controller and routing interface

The system configuration controller provides the capability to remap some alternate functions on different I/O ports. TIM4 and ADC1 DMA channels can also be remapped.

The highly flexible routing interface allows application software to control the routing of different I/Os to the TIM1 timer input captures. It also controls the routing of internal analog signals to ADC1, COMP1, COMP2, DAC and the internal reference voltage V_{REFINT} . Finally, it provides a set of registers for efficiently managing a set of dedicated I/Os supporting up to 16 capacitive sensing channels using the ProxSense™ technology.

3.13 Timers

STM8L15xxx devices contain one advanced control timer (TIM1), two 16-bit general purpose timers (TIM2 and TIM3) and one 8-bit basic timer (TIM4).

All the timers can be served by DMA1.

Table 3 compares the features of the advanced control, general-purpose and basic timers.

Table 3. Timer feature comparison

| Timer | Counter resolution | Counter type | Prescaler factor | DMA1 request generation | Capture/compare channels | Complementary outputs |
|-------|--------------------|--------------|--------------------------------|-------------------------|--------------------------|-----------------------|
| TIM1 | 16-bit | up/down | Any integer from 1 to 65536 | Yes | 3 + 1 | 3 |
| TIM2 | | | Any power of 2 from 1 to 128 | | 2 | None |
| TIM3 | | | | | 0 | |
| TIM4 | 8-bit | up | Any power of 2 from 1 to 32768 | | | |

3.13.1 TIM1 - 16-bit advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver.

- 16-bit up, down and up/down autoreload counter with 16-bit prescaler
- 3 independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- 1 additional capture/compare channel which is not connected to an external I/O
- Synchronization module to control the timer with external signals
- Break input to force timer outputs into a defined state
- 3 complementary outputs with adjustable dead time
- Encoder mode
- Interrupt capability on various events (capture, compare, overflow, break, trigger)

3.13.2 16-bit general purpose timers

- 16-bit autoreload (AR) up/down-counter
- 7-bit prescaler adjustable to fixed power of 2 ratios (1...128)
- 2 individually configurable capture/compare channels
- PWM mode
- Interrupt capability on various events (capture, compare, overflow, break, trigger)
- Synchronization with other timers or external signals (external clock, reset, trigger and enable)

3.13.3 8-bit basic timer

The 8-bit timer consists of an 8-bit up auto-reload counter driven by a programmable prescaler. It can be used for timebase generation with interrupt generation on timer overflow or for DAC trigger generation.

3.14 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

3.14.1 Window watchdog timer

The window watchdog (WWDG) is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

3.14.2 Independent watchdog timer

The independent watchdog peripheral (IWDG) can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the internal LSI RC clock source, and thus stays active even in case of a CPU clock failure.

3.15 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

3.16 Communication interfaces

3.16.1 SPI

The serial peripheral interface (SPI1) provides half/ full duplex synchronous serial communication with external devices.

- Maximum speed: 8 Mbit/s ($f_{\text{SYSCLK}}/2$) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on 2 lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- Hardware CRC calculation
- Slave/master selection input pin

Note: SPI1 can be served by the DMA1 Controller.

3.16.2 I²C

The I²C bus interface (I²C1) provides multi-master capability, and controls all I²C bus-specific sequencing, protocol, arbitration and timing.

- Master, slave and multi-master capability
- Standard mode up to 100 kHz and fast speed modes up to 400 kHz.
- 7-bit and 10-bit addressing modes.
- SMBus 2.0 and PMBus support
- Hardware CRC calculation

Note: $\dot{P}C1$ can be served by the DMA1 Controller.

3.16.3 USART

The USART interface (USART1) allows full duplex, asynchronous communications with external devices requiring an industry standard NRZ asynchronous serial data format. It offers a very wide range of baud rates.

- 1 Mbit/s full duplex SCI
- SPI1 emulation
- High precision baud rate generator
- Smartcard emulation
- IrDA SIR encoder decoder
- Single wire half duplex mode

Note: USART1 can be served by the DMA1 Controller.

3.17 Infrared (IR) interface

The STM8L15x devices contain an infrared interface which can be used with an IR LED for remote control functions. Two timer output compare channels are used to generate the infrared remote control signals.

3.18 Development support

Development tools

Development tools for the STM8 microcontrollers include:

- The STice emulation system offering tracing and code profiling
- The STVD high-level language debugger including C compiler, assembler and integrated development environment
- The STVP Flash programming software

The STM8 also comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

Single wire data interface (SWIM) and debug module

The debug module with its single wire data interface (SWIM) permits non-intrusive real-time in-circuit debugging and fast memory programming.

The Single wire interface is used for direct access to the debugging module and memory programming. The interface can be activated in all device operation modes.

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, CPU operation can also be monitored in real-time by means of shadow registers.

Bootloader

A bootloader is available to reprogram the Flash memory using the USART1 interface.

4 Pin description

Figure 3. STM8L151Gx UFQFPN 28 package pinout

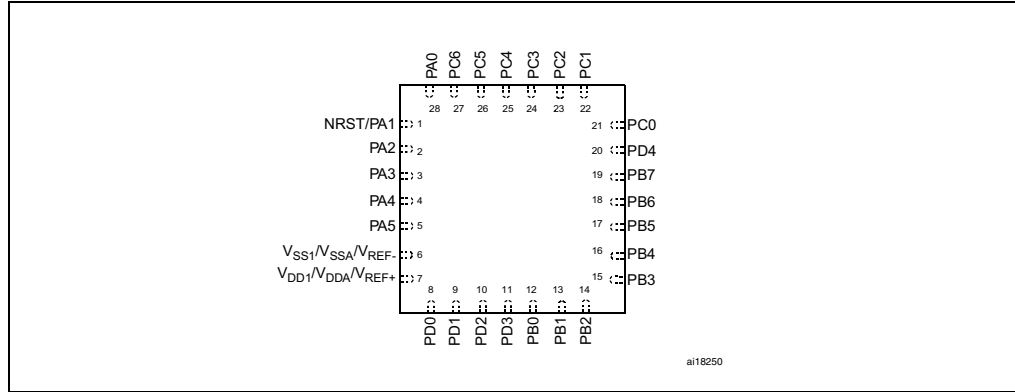


Figure 4. STM8L151Gx WLCSP28 package pinout

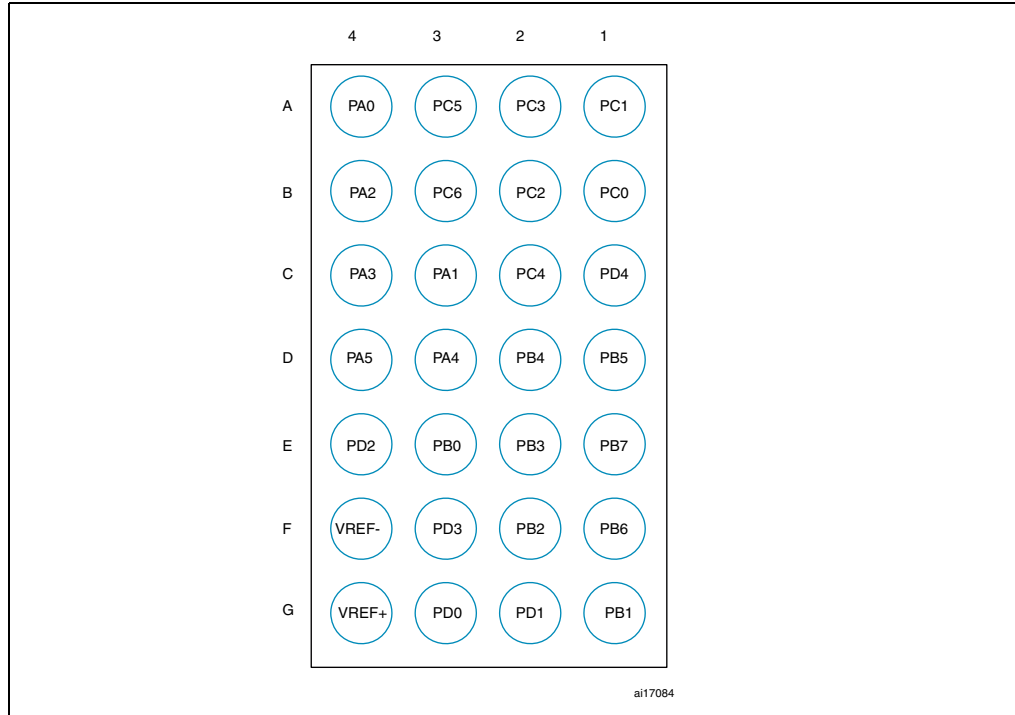
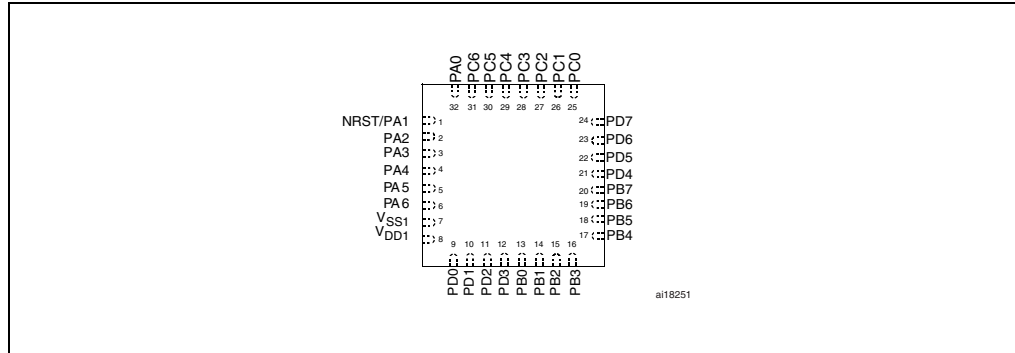
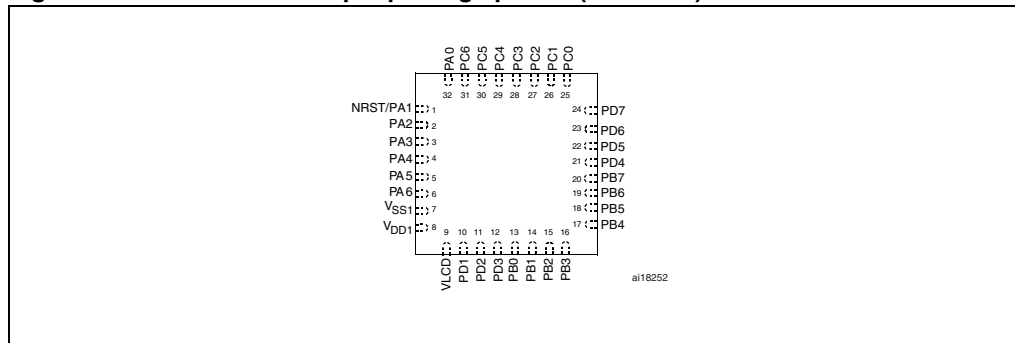


Figure 5. STM8L151Kx 32-pin package pinout (without LCD)



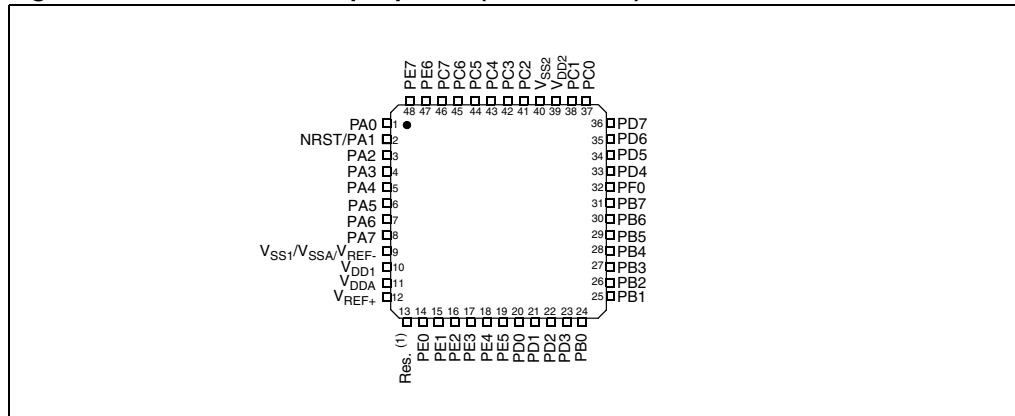
1. Example given for the UFQFPN32 package. The pinout is the same for the LQFP32 package.

Figure 6. STM8L152Kx 32-pin package pinout (with LCD)



1. Example given for the UFQFPN32 package. The pinout is the same for the LQFP32 package.

Figure 7. STM8L151Cx 48-pin pinout (without LCD)



1. Reserved. Must be tied to V_{DD} .

Figure 8. STM8L152Cx 48-pin pinout (with LCD)

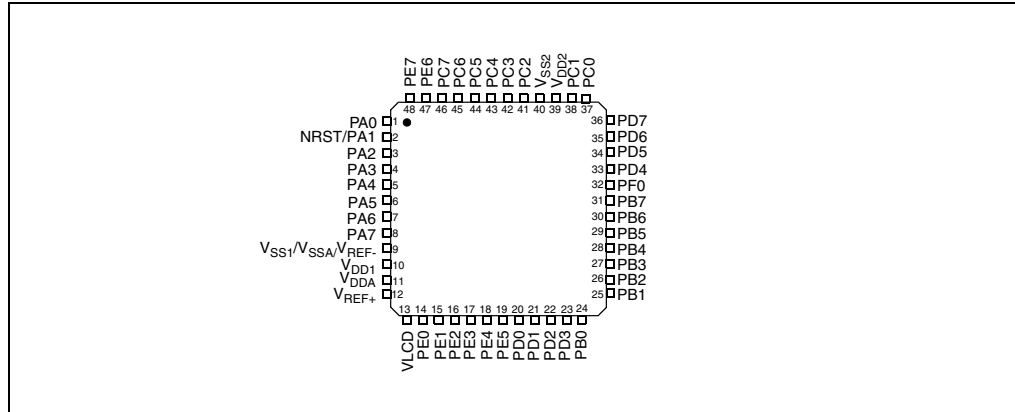


Table 4. Legend/abbreviation for table 5

| | | |
|---------------------------------------|--|--|
| Type | I= input, O = output, S = power supply | |
| Level | Input | CM = CMOS |
| | Output | HS = high sink/source (20 mA) |
| Port and control configuration | Input | float = floating, wpu = weak pull-up |
| | Output | T = true open drain, OD = open drain, PP = push pull |
| Reset state | Bold X (pin state after reset release). Unless otherwise specified, the pin state is the same during the reset phase (i.e. "under reset") and after internal reset release (i.e. at reset state). | |

Table 5. STM8L15x pin description

| Pin number | | | | Pin name | Type | I/O level | Input | | | Output | | | Main function (after reset) | Default alternate function |
|------------|----------|----------|---------|---|------|-----------|----------|-----|----------------|------------------|----|----|-----------------------------|---|
| | UFQFPN32 | UFQFPN28 | WLCSP28 | | | | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | |
| 2 | 1 | 1 | C3 | NRST/PA1 ⁽¹⁾ | I/O | | | X | | HS | X | X | Reset | PA1 |
| 3 | 2 | 2 | B4 | PA2/OSC_IN/ [USART1_TX] ⁽³⁾ / [SPI1_MISO] ⁽³⁾ | I/O | | X | X | X | HS | X | X | Port A2 | HSE oscillator input / [USART1 transmit] / [SPI1 master in- slave out] / |
| 4 | 3 | 3 | C4 | PA3/OSC_OUT/[USART1_RX] ⁽³⁾ / [SPI1_MOSI] ⁽³⁾ | I/O | | X | X | X | HS | X | X | Port A3 | HSE oscillator output / [USART1 receive]/[SPI1 master out/slave in] |
| 5 | - | - | - | PA4/TIM2_BKIN/ LCD_COM0 ⁽²⁾ /ADC1_IN2/ COMP1_INP | I/O | | X | X | X | HS | X | X | Port A4 | Timer 2 - break input / LCD_COM 0 / ADC1 input 2 / Comparator 1 positive input |
| - | 4 | 4 | D3 | PA4/TIM2_BKIN/ [TIM2_TRIG] ⁽³⁾ / LCD_COM0 ⁽²⁾ / ADC1_IN2/COMP1_INP | I/O | | X | X | X | HS | X | X | Port A4 | Timer 2 - break input / [Timer 2 - trigger] / LCD_COM 0 / ADC1 input 2 / Comparator 1 positive input |
| 6 | - | - | - | PA5/TIM3_BKIN/ LCD_COM1 ⁽²⁾ /ADC1_IN1/ COMP1_INP | I/O | | X | X | X | HS | X | X | Port A5 | Timer 3 - break input / LCD_COM 1 / ADC1 input 1/ Comparator 1 positive input |

Table 5. STM8L15x pin description (continued)

| Pin number | | | | Pin name | Type | I/O level | Input | | | Output | | | Main function (after reset) | Default alternate function |
|---------------------|----------|----------|---------|---|------|-----------|------------------|------------------|----------------|------------------|----|----|-----------------------------|--|
| UFQFPN48 and LQFP48 | UFQFPN32 | UFQFPN28 | WLCSP28 | | | | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | |
| | | | | | | | | | | | | | | |
| - | 5 | 5 | D4 | PA5/TIM3_BKIN/ [TIM3_TRIG ⁽³⁾]/ LCD_COM1 ⁽²⁾ /ADC1_IN1/ COMP1_INP | I/O | | X | X | X | HS | X | X | Port A5 | Timer 3 - break input / [Timer 3 - trigger] / LCD_COM 1 / ADC1 input 1 / Comparator 1 positive input |
| 7 | 6 | - | - | PA6/[ADC1_TRIG ⁽³⁾]/ LCD_COM2 ⁽²⁾ /ADC1_IN0/ COMP1_INP | I/O | | X | X | X | HS | X | X | Port A6 | [ADC1 - trigger] / LCD_COM2 / ADC1 input 0 / Comparator 1 positive input |
| 8 | - | - | - | PA7/LCD_SEG0 ⁽²⁾⁽⁴⁾ | I/O | FT | X | X | X | HS | X | X | Port A7 | LCD segment 0 |
| 24 | 13 | 12 | E3 | PB0 ⁽⁵⁾ /TIM2_CH1/ LCD_SEG10 ⁽²⁾ / ADC1_IN18/COMP1_INP | I/O | | X ⁽⁵⁾ | X ⁽⁵⁾ | X | HS | X | X | Port B0 | Timer 2 - channel 1 / LCD segment 10 / ADC1_IN18 / Comparator 1 positive input |
| 25 | 14 | 13 | G1 | PB1/TIM3_CH1/ LCD_SEG11 ⁽²⁾ / ADC1_IN17/COMP1_INP | I/O | | X | X | X | HS | X | X | Port B1 | Timer 3 - channel 1 / LCD segment 11 / ADC1_IN17 / Comparator 1 positive input |
| 26 | 15 | 14 | F2 | PB2/TIM2_CH2/ LCD_SEG12 ⁽²⁾ / ADC1_IN16/COMP1_INP | I/O | | X | X | X | HS | X | X | Port B2 | Timer 2 - channel 2 / LCD segment 12 / ADC1_IN16/ Comparator 1 positive input |
| 27 | - | - | - | PB3/TIM2_TRIG/ LCD_SEG13 ⁽²⁾ / ADC1_IN15/COMP1_INP | I/O | | X | X | X | HS | X | X | Port B3 | Timer 2 - trigger / LCD segment 13/ADC1_IN15 / Comparator 1 positive input |
| - | 16 | - | - | PB3/[TIM2_TRIG ⁽³⁾]/ TIM1_CH2N/LCD_SEG13 ⁽²⁾ / ADC1_IN15/ COMP1_INP | I/O | | X | X | X | HS | X | X | Port B3 | [Timer 2 - trigger] / Timer 1 inverted channel 2 / LCD segment 13 / ADC1_IN15 / Comparator 1 positive input |

Table 5. STM8L15x pin description (continued)

| Pin number | | Pin name | Type | I/O level | Input | | | Output | | | Main function (after reset) | Default alternate function | | |
|---------------------|----------|----------|------|---|----------|---------|------------------|------------------|----------------|------------------|-----------------------------|----------------------------|----------------|--|
| UFQFPN48 and LQFP48 | UFQFPN32 | | | | UFQFPN28 | WLCSP28 | floating | wpu | Ext. interrupt | High sink/source | | | OD | PP |
| - | - | 15 | E2 | PB3/[TIM2_TRIG] ⁽³⁾ / TIM1_CH1N/ LCD_SEG13 ⁽²⁾ / ADC1_IN15/RTC_ALARM/ COMP1_INP | I/O | | X | X | X | HS | X | X | Port B3 | [Timer 2 - trigger] / Timer 1 inverted channel 1 / LCD segment 13 / ADC1_IN15 / RTC alarm/ Comparator 1 positive input |
| 28 | - | - | - | PB4 ⁽⁵⁾ /[SPI1_NSS] ⁽³⁾ / LCD_SEG14 ⁽²⁾ / ADC1_IN14/COMP1_INP | I/O | | X ⁽⁵⁾ | X ⁽⁵⁾ | X | HS | X | X | Port B4 | [SPI1 master/slave select] / LCD segment 14 / ADC1_IN14 / Comparator 1 positive input |
| - | 17 | 16 | D2 | PB4 ⁽⁵⁾ /[SPI1_NSS] ⁽³⁾ / LCD_SEG14 ⁽²⁾ / ADC1_IN14/ COMP1_INP/DAC_OUT | I/O | | X ⁽⁵⁾ | X ⁽⁵⁾ | X | HS | X | X | Port B4 | [SPI1 master/slave select] / LCD segment 14 / ADC1_IN14 / DAC output / Comparator 1 positive input |
| 29 | - | - | - | PB5/[SPI1_SCK] ⁽³⁾ / LCD_SEG15 ⁽²⁾ / ADC1_IN13/COMP1_INP | I/O | | X | X | X | HS | X | X | Port B5 | [SPI1 clock] / LCD segment 15 / ADC1_IN13 / Comparator 1 positive input |
| - | 18 | 17 | D1 | PB5/[SPI1_SCK] ⁽³⁾ / LCD_SEG15 ⁽²⁾ / ADC1_IN13/DAC_OUT/ COMP1_INP | I/O | | X | X | X | HS | X | X | Port B5 | [SPI1 clock] / LCD segment 15 / ADC1_IN13 / DAC output / Comparator 1 positive input |
| 30 | - | - | - | PB6/[SPI1_MOSI] ⁽³⁾ / LCD_SEG16 ⁽²⁾ / ADC1_IN12/COMP1_INP | I/O | | X | X | X | HS | X | X | Port B6 | [SPI1 master out/slave in] / LCD segment 16 / ADC1_IN12 / Comparator 1 positive input |
| - | 19 | 18 | F1 | PB6/[SPI1_MOSI] ⁽³⁾ / LCD_SEG16 ⁽²⁾ / ADC1_IN12/COMP1_INP/ DAC_OUT | I/O | | X | X | X | HS | X | X | Port B6 | [SPI1 master out] / slave in / LCD segment 16 / ADC1_IN12 / DAC output / Comparator 1 positive input |

Table 5. STM8L15x pin description (continued)

| Pin number | | | | Pin name | Type | I/O level | Input | | | Output | | | Main function (after reset) | Default alternate function |
|---------------------|----------|----------|---------|---|------|-----------|----------|-----|----------------|------------------|------------------|----|-----------------------------|--|
| UFQFPN48 and LQFP48 | UFQFPN32 | UFQFPN28 | WLCSP28 | | | | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | |
| | | | | | | | | | | | | | | |
| 31 | 20 | 19 | E1 | PB7/[SPI1_MISO] ⁽³⁾ / LCD_SEG17 ⁽²⁾ / ADC1_IN11/COMP1_INP | I/O | | X | X | X | HS | X | X | Port B7 | [SPI1 master in- slave out] / LCD segment 17 / ADC1_IN11 / Comparator 1 positive input |
| 37 | 25 | 21 | B1 | PC0 ⁽⁴⁾ /I2C1_SDA | I/O | FT | X | | X | | T ⁽⁶⁾ | | Port C0 | I2C1 data |
| 38 | 26 | 22 | A1 | PC1 ⁽⁴⁾ /I2C1_SCL | I/O | FT | X | | X | | T ⁽⁶⁾ | | Port C1 | I2C1 clock |
| 41 | 27 | 23 | B2 | PC2/[USART1_RX] ⁽³⁾ / LCD_SEG22/ADC1_IN6/ COMP1_INP/VREF_OUT | I/O | | X | X | X | HS | X | X | Port C2 | [USART1 receive] / LCD segment 22 / ADC1_IN6 / Comparator 1 positive input / Voltage reference output |
| 42 | 28 | 24 | A2 | PC3/[USART1_TX] ⁽³⁾ / LCD_SEG23 ⁽²⁾ / ADC1_IN5/COMP1_INP/ COMP2_INM | I/O | | X | X | X | HS | X | X | Port C3 | [USART1 transmit] / LCD segment 23 / ADC1_IN5 / Comparator 1 positive input / Comparator 2 negative input |
| 43 | 29 | 25 | C2 | PC4/[USART1_CK] ⁽³⁾ / I2C1_SMB/CCO/ LCD_SEG24 ⁽²⁾ / ADC1_IN4/COMP2_INM/ COMP1_INP | I/O | | X | X | X | HS | X | X | Port C4 | [USART1 synchronous clock] / I2C1_SMB / Configurable clock output / LCD segment 24 / ADC1_IN4 / Comparator 2 negative input / Comparator 1 positive input |
| 44 | 30 | 26 | A3 | PC5/OSC32_IN /[SPI1_NSS] ⁽³⁾ / [USART1_TX] ⁽³⁾ | I/O | | X | X | X | HS | X | X | Port C5 | LSE oscillator input / [SPI1 master/slave select] / [USART1 transmit] |
| 45 | 31 | 27 | B3 | PC6/OSC32_OUT/ [SPI1_SCK] ⁽³⁾ / [USART1_RX] ⁽³⁾ | I/O | | X | X | X | HS | X | X | Port C6 | LSE oscillator output / [SPI1 clock] / [USART1 receive] |

Table 5. STM8L15x pin description (continued)

| Pin number | | | | Pin name | Type | I/O level | Input | | | Output | | | Main function (after reset) | Default alternate function |
|---------------------|----------|----------|---------|---|------|-----------|----------|-----|----------------|------------------|----|----|------------------------------|--|
| UFQFPN48 and LQFP48 | UFQFPN32 | UFQFPN28 | WLCSP28 | | | | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | |
| 46 | - | - | - | PC7/LCD_SEG25 ⁽²⁾ / ADC1_IN3/COMP2_INM/ COMP1_INP | I/O | | X | X | X | HS | X | X | Port C7 | LCD segment 25 /ADC1_IN3/ Comparator negative input / Comparator 1 positive input |
| 20 | - | 8 | G3 | PD0/TIM3_CH2/ [ADC1_TRIG] ⁽³⁾ / LCD_SEG7 ⁽²⁾ /ADC1_IN2 2/COMP2_INP/ COMP1_INP | I/O | | X | X | X | HS | X | X | Port D0 | Timer 3 - channel 2 / [ADC1_Trigger] / LCD segment 7 / ADC1_IN22 / Comparator 2 positive input / Comparator 1 positive input |
| - | 9 | - | - | PD0/TIM3_CH2/ [ADC1_TRIG] ⁽³⁾ / ADC1_IN22/COMP2_INP/ COMP1_INP | I/O | | X | X | X | HS | X | X | Port D0⁽⁷⁾ | Timer 3 - channel 2 / [ADC1_Trigger] / ADC1_IN22 / Comparator 2 positive input / Comparator 1 positive input |
| 21 | - | - | - | PD1/TIM3_TRIG/ LCD_COM3 ⁽²⁾ / ADC1_IN21/COMP2_INP/ COMP1_INP | I/O | | X | X | X | HS | X | X | Port D1 | Timer 3 - trigger / LCD_COM3 / ADC1_IN21 / comparator 2 positive input / Comparator 1 positive input |
| - | 10 | - | - | PD1/TIM1_CH3N/[TIM3_T RIG] ⁽³⁾ / LCD_COM3 ⁽²⁾ / ADC1_IN21/COMP2_INP/ COMP1_INP | I/O | | X | X | X | HS | X | X | Port D1 | [Timer 3 - trigger]/ TIM1 inverted channel 3 / LCD_COM3/ ADC1_IN21 / Comparator 2 positive input / Comparator 1 positive input |
| - | - | 9 | G2 | PD1/TIM1_CH3/[TIM3_TR IG] ⁽³⁾ /LCD_COM3 ⁽²⁾ / ADC1_IN21/COMP2_INP/ COMP1_INP | I/O | | X | X | X | HS | X | X | Port D1 | Timer 1 channel 3 / [Timer 3 - trigger] / LCD_COM3/ ADC1_IN21 / Comparator 2 positive input / Comparator 1 positive input |

Table 5. STM8L15x pin description (continued)

| Pin number | | | | Pin name | Type | I/O level | Input | | | Output | | | Main function (after reset) | Default alternate function |
|---------------------|----------|----------|---------|---|------|-----------|----------|-----|----------------|------------------|----|----|-----------------------------|--|
| UFQFPN48 and LQFP48 | UFQFPN32 | UFQFPN28 | WLCSP28 | | | | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | |
| 22 | 11 | 10 | E4 | PD2/TIM1_CH1 /LCD_SEG8 ⁽²⁾ / ADC1_IN20/COMP1_INP | I/O | | X | X | X | HS | X | X | Port D2 | Timer 1 - channel 1 / LCD segment 8 / ADC1_IN20 / Comparator 1 positive input |
| 23 | 12 | - | - | PD3/ TIM1_TRIG/ LCD_SEG9 ⁽²⁾ /ADC1_IN19/COMP1_INP | I/O | | X | X | X | HS | X | X | Port D3 | Timer 1 - trigger / LCD segment 9 / ADC1_IN19 / Comparator 1 positive input |
| - | - | 11 | F3 | PD3/ TIM1_TRIG/ LCD_SEG9 ⁽²⁾ / ADC1_IN19/TIM1_BKIN/ COMP1_INP/ RTC_CALIB | I/O | | X | X | X | HS | X | X | Port D3 | Timer 1 - trigger / LCD segment 9 / ADC1_IN19 / Timer 1 break input / RTC calibration / Comparator 1 positive input |
| 33 | 21 | 20 | C1 | PD4/TIM1_CH2 /LCD_SEG18 ⁽²⁾ / ADC1_IN10/COMP1_INP | I/O | | X | X | X | HS | X | X | Port D4 | Timer 1 - channel 2 / LCD segment 18 / ADC1_IN10/ Comparator 1 positive input |
| 34 | 22 | - | - | PD5/TIM1_CH3 /LCD_SEG19 ⁽²⁾ / ADC1_IN9/COMP1_INP | I/O | | X | X | X | HS | X | X | Port D5 | Timer 1 - channel 3 / LCD segment 19 / ADC1_IN9/ Comparator 1 positive input |
| 35 | 23 | - | - | PD6/TIM1_BKIN /LCD_SEG20 ⁽²⁾ / ADC1_IN8/RTC_CALIB/ VREF_OUT/ COMP1_INP | I/O | | X | X | X | HS | X | X | Port D6 | Timer 1 - break input / LCD segment 20 / ADC1_IN8 / RTC calibration / Voltage reference output / Comparator 1 positive input |
| 36 | 24 | - | - | PD7/TIM1_CH1N /LCD_SEG21 ⁽²⁾ / ADC1_IN7/RTC_ALARM/ VREF_OUT/ COMP1_INP | I/O | | X | X | X | HS | X | X | Port D7 | Timer 1 - inverted channel 1/ LCD segment 21 / ADC1_IN7 / RTC alarm / Voltage reference output /Comparator 1 positive input |
| 14 | - | - | - | PE0 ⁽⁴⁾ /LCD_SEG1 ⁽²⁾ | I/O | FT | X | X | X | HS | X | X | Port E0 | LCD segment 1 |

Table 5. STM8L15x pin description (continued)

| Pin number | | | | Pin name | Type | I/O level | Input | | | Output | | | Main function (after reset) | Default alternate function |
|------------|---------------------|----------|----------|---|------|-----------|---------|----------|-----|----------------|------------------|----|-----------------------------|---|
| | UFQFPN48 and LQFP48 | UFQFPN32 | UFQFPN28 | | | | WLCSP28 | floating | wpu | Ext. interrupt | High sink/source | OD | | |
| 15 | - | - | - | PE1/TIM1_CH2N /LCD_SEG2 ⁽²⁾ | I/O | | X | X | X | HS | X | X | Port E1 | Timer 1 - inverted channel 2 / LCD segment 2 |
| 16 | - | - | - | PE2/TIM1_CH3N /LCD_SEG3 ⁽²⁾ | I/O | | X | X | X | HS | X | X | Port E2 | Timer 1 - inverted channel 3 / LCD segment 3 |
| 17 | - | - | - | PE3/LCD_SEG4 ⁽²⁾ | I/O | | X | X | X | HS | X | X | Port E3 | LCD segment 4 |
| 18 | - | - | - | PE4/LCD_SEG5 ⁽²⁾ | I/O | | X | X | X | HS | X | X | Port E4 | LCD segment 5 |
| 19 | - | - | - | PE5/LCD_SEG6 ⁽²⁾ / ADC1_IN23/COMP2_INP/COMP1_INP | I/O | | X | X | X | HS | X | X | Port E5 | LCD segment 6 / ADC1_IN23 / Comparator 2 positive input / Comparator 1 positive input |
| 47 | - | - | - | PE6/LCD_SEG26 ⁽²⁾ / PVD_IN | I/O | | X | X | X | HS | X | X | Port E6 | LCD segment 26/PVD_IN |
| 48 | - | - | - | PE7/LCD_SEG27 ⁽²⁾ | I/O | | X | X | X | HS | X | X | Port E7 | LCD segment 27 |
| 32 | - | - | - | PF0/ADC1_IN24/ DAC_OUT | I/O | | X | X | X | HS | X | X | Port F0 | ADC1_IN24 / DAC_OUT |
| 13 | 9 | - | - | VLCD ⁽²⁾ | S | | | | | | | | | LCD booster external capacitor |
| 13 | - | - | - | Reserved ⁽⁷⁾ | | | | | | | | | | Reserved. Must be tied to V _{DD} |
| 10 | - | - | - | V _{DD} | S | | | | | | | | | Digital power supply |
| 11 | - | - | - | V _{DDA} | S | | | | | | | | | Analog supply voltage |
| 12 | - | - | - | V _{REF+} | S | | | | | | | | | ADC1 and DAC positive voltage reference |
| - | 8 | 7 | G4 | V _{DD1} /V _{DDA} /V _{REF+} | S | | | | | | | | | Digital power supply / Analog supply voltage / ADC1 positive voltage reference |
| 9 | 7 | 6 | F4 | V _{SS1} /V _{SSA} /V _{REF-} | S | | | | | | | | | I/O ground / Analog ground voltage / ADC1 negative voltage reference |
| 39 | - | - | - | V _{DD2} | S | | | | | | | | | IOs supply voltage |

Table 5. STM8L15x pin description (continued)

| Pin number | | | | Pin name | Type | I/O level | Input | | | Output | | | Main function (after reset) | Default alternate function |
|---------------------|----------|----------|---------|---|------|-----------|------------------|-----|-------------------|------------------|----|---------|---|----------------------------|
| UFQFPN48 and LQFP48 | UFQFPN32 | UFQFPN28 | WLCSP28 | | | | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | |
| | | | | | | | | | | | | | | |
| 40 | - | - | - | V _{SS2} | S | | | | | | | | IOs ground voltage | |
| 1 | 32 | 28 | A4 | PA0 ⁽⁸⁾ /[USART1_CK] ⁽³⁾ /SWIM/BEEP/IR_TIM ⁽⁹⁾ | I/O | X | X ⁽⁸⁾ | X | HS ⁽⁹⁾ | X | X | Port A0 | [USART1 synchronous clock] ⁽³⁾ / SWIM input and output / Beep output / Infrared Timer output | |

- At power-up, the PA1/NRST pin is a reset input pin with pull-up. To be used as a general purpose pin (PA1), it can be configured only as output open-drain or push-pull, not as a general purpose input. Refer to Section *Configuring NRST/PA1 pin as general purpose output* in the STM8L15x reference manual (RM0031).
- Available on STM8L152xx devices only.
- [] Alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).
- In the 5 V tolerant I/Os, protection diode to V_{DD} is not implemented.
- A pull-up is applied to PB0 and PB4 during the reset phase. These two pins are input floating after reset release.
- In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer and protection diode to V_{DD} are not implemented).
- Available on STM8L151xx devices only.
- The PA0 pin is in input pull-up during the reset phase and after reset release.
- High Sink LED driver capability available on PA0.

4.1 System configuration options

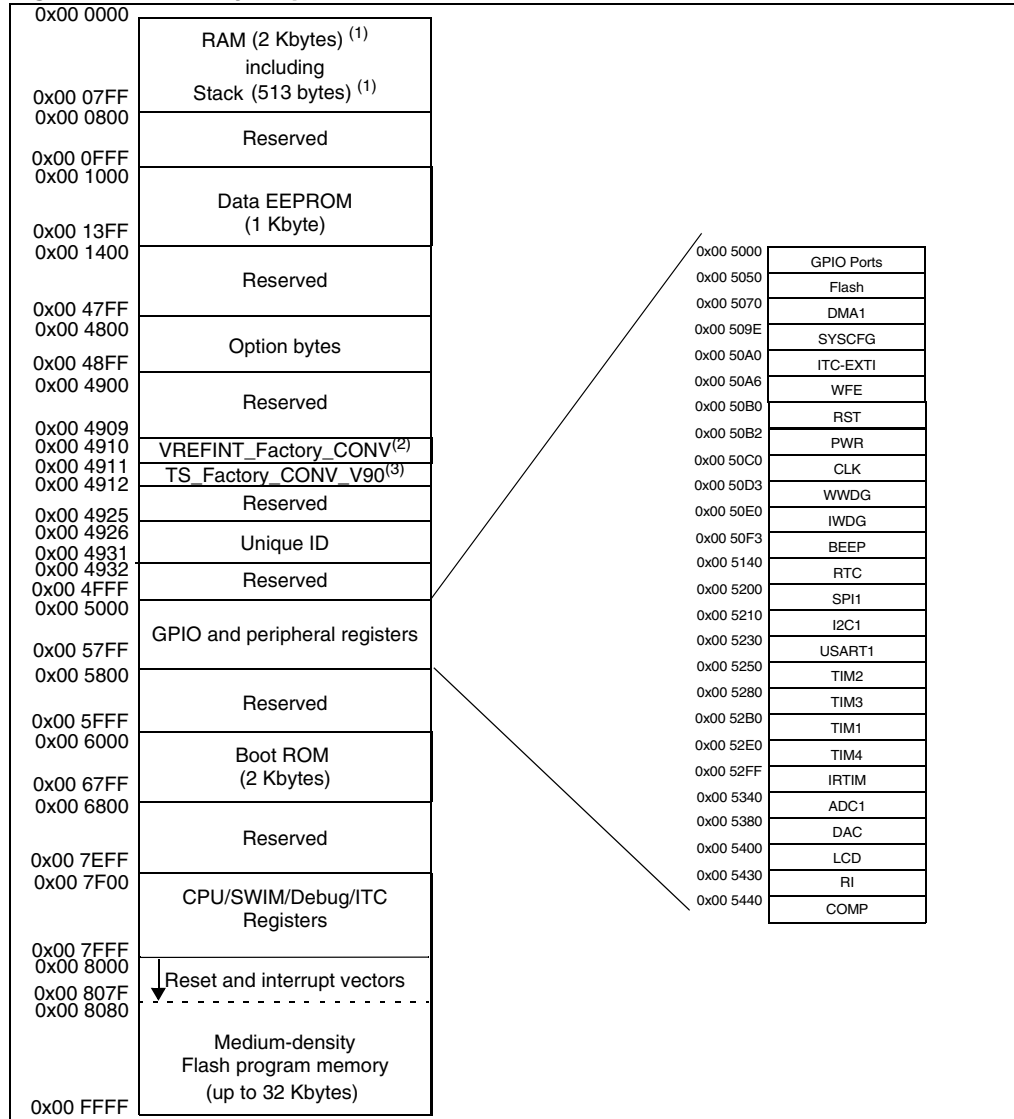
As shown in [Table 5: STM8L15x pin description](#), some alternate functions can be remapped on different I/O ports by programming one of the two remapping registers described in the “Routing interface (RI) and system configuration controller” section in the STM8L15xxx reference manual (RM0031).

5 Memory and register map

5.1 Memory mapping

The memory map is shown in [Figure 9](#).

Figure 9. Memory map



1. [Table 6](#) lists the boundary addresses for each memory size. The top of the stack is at the RAM end address.
2. The VREFINT_Factory_CONV byte represents the LSB of the V_{REFINT} 12-bit ADC conversion result. The MSB have a fixed value: 0x6.
3. The TS_Factory_CONV_V90 byte represents the LSB of the V₉₀ 12-bit ADC conversion result. The MSB have a fixed value: 0x3.
4. Refer to [Table 8](#) for an overview of hardware register mapping, to [Table 7](#) for details on I/O port hardware registers, and to [Table 9](#) for information on CPU/SWIM/debug module controller registers.

Table 6. Flash and RAM boundary addresses

| Memory area | Size | Start address | End address |
|----------------------|-----------|---------------|-------------|
| RAM | 2 Kbytes | 0x00 0000 | 0x00 07FF |
| Flash program memory | 16 Kbytes | 0x00 8000 | 0x00 BFFF |
| | 32 Kbytes | 0x00 8000 | 0x00 FFFF |

5.2 Register map

Table 7. I/O port hardware register map

| Address | Block | Register label | Register name | Reset status |
|-----------|--------|----------------|-----------------------------------|--------------|
| 0x00 5000 | Port A | PA_ODR | Port A data output latch register | 0x00 |
| 0x00 5001 | | PA_IDR | Port A input pin value register | 0xxx |
| 0x00 5002 | | PA_DDR | Port A data direction register | 0x00 |
| 0x00 5003 | | PA_CR1 | Port A control register 1 | 0x01 |
| 0x00 5004 | | PA_CR2 | Port A control register 2 | 0x00 |
| 0x00 5005 | Port B | PB_ODR | Port B data output latch register | 0x00 |
| 0x00 5006 | | PB_IDR | Port B input pin value register | 0xxx |
| 0x00 5007 | | PB_DDR | Port B data direction register | 0x00 |
| 0x00 5008 | | PB_CR1 | Port B control register 1 | 0x00 |
| 0x00 5009 | | PB_CR2 | Port B control register 2 | 0x00 |
| 0x00 500A | Port C | PC_ODR | Port C data output latch register | 0x00 |
| 0x00 500B | | PC_IDR | Port C input pin value register | 0xxx |
| 0x00 500C | | PC_DDR | Port C data direction register | 0x00 |
| 0x00 500D | | PC_CR1 | Port C control register 1 | 0x00 |
| 0x00 500E | | PC_CR2 | Port C control register 2 | 0x00 |
| 0x00 500F | Port D | PD_ODR | Port D data output latch register | 0x00 |
| 0x00 5010 | | PD_IDR | Port D input pin value register | 0xxx |
| 0x00 5011 | | PD_DDR | Port D data direction register | 0x00 |
| 0x00 5012 | | PD_CR1 | Port D control register 1 | 0x00 |
| 0x00 5013 | | PD_CR2 | Port D control register 2 | 0x00 |
| 0x00 5014 | Port E | PE_ODR | Port E data output latch register | 0x00 |
| 0x00 5015 | | PE_IDR | Port E input pin value register | 0xxx |
| 0x00 5016 | | PE_DDR | Port E data direction register | 0x00 |
| 0x00 5017 | | PE_CR1 | Port E control register 1 | 0x00 |
| 0x00 5018 | | PE_CR2 | Port E control register 2 | 0x00 |

Table 7. I/O port hardware register map (continued)

| Address | Block | Register label | Register name | Reset status |
|-----------|--------|----------------|-----------------------------------|--------------|
| 0x00 5019 | Port F | PF_ODR | Port F data output latch register | 0x00 |
| 0x00 501A | | PF_IDR | Port F input pin value register | 0xxx |
| 0x00 501B | | PF_DDR | Port F data direction register | 0x00 |
| 0x00 501C | | PF_CR1 | Port F control register 1 | 0x00 |
| 0x00 501D | | PF_CR2 | Port F control register 2 | 0x00 |

Table 8. General hardware register map

| Address | Block | Register label | Register name | Reset status |
|------------------------------|--------------------------|----------------|--|--------------|
| 0x00 501E to 0x00 5049 | Reserved area (44 bytes) | | | |
| 0x00 5050 | Flash | FLASH_CR1 | Flash control register 1 | 0x00 |
| 0x00 5051 | | FLASH_CR2 | Flash control register 2 | 0x00 |
| 0x00 5052 | | FLASH_PUKR | Flash program memory unprotection key register | 0x00 |
| 0x00 5053 | | FLASH_DUKR | Data EEPROM unprotection key register | 0x00 |
| 0x00 5054 | | FLASH_IAPSR | Flash in-application programming status register | 0x00 |
| 0x00 5055 to 0x00 506F | Reserved area (27 bytes) | | | |

Table 8. General hardware register map (continued)

| Address | Block | Register label | Register name | Reset status | |
|------------------------|-------|-------------------------|--|--------------|--|
| 0x00 5070 | DMA1 | DMA1_GCSR | DMA1 global configuration & status register | 0xFC | |
| 0x00 5071 | | DMA1_GIR1 | DMA1 global interrupt register 1 | 0x00 | |
| 0x00 5072 to 0x00 5074 | | Reserved area (3 bytes) | | | |
| 0x00 5075 | | DMA1_C0CR | DMA1 channel 0 configuration register | 0x00 | |
| 0x00 5076 | | DMA1_C0SPR | DMA1 channel 0 status & priority register | 0x00 | |
| 0x00 5077 | | DMA1_C0NDTR | DMA1 number of data to transfer register (channel 0) | 0x00 | |
| 0x00 5078 | | DMA1_C0PARH | DMA1 peripheral address high register (channel 0) | 0x52 | |
| 0x00 5079 | | DMA1_C0PARL | DMA1 peripheral address low register (channel 0) | 0x00 | |
| 0x00 507A | | Reserved area (1 byte) | | | |
| 0x00 507B | | DMA1_C0M0ARH | DMA1 memory 0 address high register (channel 0) | 0x00 | |
| 0x00 507C | | DMA1_C0M0ARL | DMA1 memory 0 address low register (channel 0) | 0x00 | |
| 0x00 507D to 0x00 507E | | Reserved area (2 bytes) | | | |
| 0x00 507F | | DMA1_C1CR | DMA1 channel 1 configuration register | 0x00 | |
| 0x00 5080 | | DMA1_C1SPR | DMA1 channel 1 status & priority register | 0x00 | |
| 0x00 5081 | | DMA1_C1NDTR | DMA1 number of data to transfer register (channel 1) | 0x00 | |
| 0x00 5082 | | DMA1_C1PARH | DMA1 peripheral address high register (channel 1) | 0x52 | |
| 0x00 5083 | | DMA1_C1PARL | DMA1 peripheral address low register (channel 1) | 0x00 | |

Table 8. General hardware register map (continued)

| Address | Block | Register label | Register name | Reset status | |
|---------------------------|-------|-------------------------|--|----------------------|------|
| 0x00 5084 | DMA1 | Reserved area (1 byte) | | | |
| 0x00 5085 | | DMA1_C1M0ARH | DMA1 memory 0 address high register (channel 1) | 0x00 | |
| 0x00 5086 | | DMA1_C1M0ARL | DMA1 memory 0 address low register (channel 1) | 0x00 | |
| 0x00 5087 0x00 5088 | | Reserved area (2 bytes) | | | |
| 0x00 5089 | | DMA1_C2CR | DMA1 channel 2 configuration register | 0x00 | |
| 0x00 508A | | DMA1_C2SPR | DMA1 channel 2 status & priority register | 0x00 | |
| 0x00 508B | | DMA1_C2NDTR | DMA1 number of data to transfer register (channel 2) | 0x00 | |
| 0x00 508C | | DMA1_C2PARH | DMA1 peripheral address high register (channel 2) | 0x52 | |
| 0x00 508D | | DMA1_C2PARL | DMA1 peripheral address low register (channel 2) | 0x00 | |
| 0x00 508E | | Reserved area (1 byte) | | | |
| 0x00 508F | | DMA1_C2M0ARH | DMA1 memory 0 address high register (channel 2) | 0x00 | |
| 0x00 5090 | | DMA1_C2M0ARL | DMA1 memory 0 address low register (channel 2) | 0x00 | |
| 0x00 5091 0x00 5092 | | Reserved area (2 bytes) | | | |
| 0x00 5093 | | DMA1_C3CR | DMA1 channel 3 configuration register | 0x00 | |
| 0x00 5094 | | DMA1_C3SPR | DMA1 channel 3 status & priority register | 0x00 | |
| 0x00 5095 | | DMA1_C3NDTR | DMA1 number of data to transfer register (channel 3) | 0x00 | |
| 0x00 5096 | | DMA1_C3PARH_C3M1ARH | DMA1 peripheral address high register (channel 3) | 0x40 | |
| 0x00 5097 | | DMA1_C3PARL_C3M1ARL | DMA1 peripheral address low register (channel 3) | 0x00 | |
| 0x00 5098 | | Reserved area (1 byte) | | | |
| 0x00 5099 | | DMA1_C3M0ARH | DMA1 memory 0 address high register (channel 3) | 0x00 | |
| 0x00 509A | | DMA1_C3M0ARL | DMA1 memory 0 address low register (channel 3) | 0x00 | |
| 0x00 509B to 0x00 509D | | Reserved area (3 bytes) | | | |
| 0x00 509E | | SYSCFG | SYSCFG_RMPCR1 | Remapping register 1 | 0x00 |
| 0x00 509F | | | SYSCFG_RMPCR2 | Remapping register 2 | 0x00 |

Table 8. General hardware register map (continued)

| Address | Block | Register label | Register name | Reset status |
|------------------------------|--------------------------|----------------|---|--------------|
| 0x00 50A0 | ITC - EXTI | EXTI_CR1 | External interrupt control register 1 | 0x00 |
| 0x00 50A1 | | EXTI_CR2 | External interrupt control register 2 | 0x00 |
| 0x00 50A2 | | EXTI_CR3 | External interrupt control register 3 | 0x00 |
| 0x00 50A3 | | EXTI_SR1 | External interrupt status register 1 | 0x00 |
| 0x00 50A4 | | EXTI_SR2 | External interrupt status register 2 | 0x00 |
| 0x00 50A5 | | EXTI_CONF1 | External interrupt port select register 1 | 0x00 |
| 0x00 50A6 | WFE | WFE_CR1 | WFE control register 1 | 0x00 |
| 0x00 50A7 | | WFE_CR2 | WFE control register 2 | 0x00 |
| 0x00 50A8 | | WFE_CR3 | WFE control register 3 | 0x00 |
| 0x00 50A9 to 0x00 50AF | Reserved area (7 bytes) | | | |
| 0x00 50B0 | RST | RST_CR | Reset control register | 0x00 |
| 0x00 50B1 | | RST_SR | Reset status register | 0x01 |
| 0x00 50B2 | PWR | PWR_CSR1 | Power control and status register 1 | 0x00 |
| 0x00 50B3 | | PWR_CSR2 | Power control and status register 2 | 0x00 |
| 0x00 50B4 to 0x00 50BF | Reserved area (12 bytes) | | | |
| 0x00 50C0 | CLK | CLK_DIVR | Clock master divider register | 0x03 |
| 0x00 50C1 | | CLK_CRTCR | Clock RTC register | 0x00 |
| 0x00 50C2 | | CLK_ICKR | Internal clock control register | 0x11 |
| 0x00 50C3 | | CLK_PCKENR1 | Peripheral clock gating register 1 | 0x00 |
| 0x00 50C4 | | CLK_PCKENR2 | Peripheral clock gating register 2 | 0x80 |
| 0x00 50C5 | | CLK_CCOR | Configurable clock control register | 0x00 |
| 0x00 50C6 | | CLK_ECKR | External clock control register | 0x00 |
| 0x00 50C7 | | CLK_SCSR | System clock status register | 0x01 |
| 0x00 50C8 | | CLK_SWR | System clock switch register | 0x01 |
| 0x00 50C9 | | CLK_SWCR | Clock switch control register | 0bxxxx0000 |
| 0x00 50CA | | CLK_CSSR | Clock security system register | 0x00 |
| 0x00 50CB | | CLK_CBEEP | Clock BEEP register | 0x00 |
| 0x00 50CC | | CLK_HSICALR | HSI calibration register | 0xxx |
| 0x00 50CD | | CLK_HSI TRIMR | HSI clock calibration trimming register | 0x00 |
| 0x00 50CE | | CLK_HSI UNLCKR | HSI unlock register | 0x00 |
| 0x00 50CF | | CLK_REGCSR | Main regulator control status register | 0bxx11100x |

Table 8. General hardware register map (continued)

| Address | Block | Register label | Register name | Reset status |
|------------------------------|--------------------------|-------------------------|--------------------------------|--------------|
| 0x00 50D0 to 0x00 50D2 | Reserved area (3 bytes) | | | |
| 0x00 50D3 | WWDG | WWDG_CR | WWDG control register | 0x7F |
| 0x00 50D4 | | WWDG_WR | WWDG window register | 0x7F |
| 0x00 50D5 to 00 50DF | Reserved area (11 bytes) | | | |
| 0x00 50E0 | IWDG | IWDG_KR | IWDG key register | 0x |
| 0x00 50E1 | | IWDG_PR | IWDG prescaler register | 0x00 |
| 0x00 50E2 | | IWDG_RLR | IWDG reload register | 0xFF |
| 0x00 50E3 to 0x00 50EF | Reserved area (13 bytes) | | | |
| 0x00 50F0 | BEEP | BEEP_CSR1 | BEEP control/status register 1 | 0x00 |
| 0x00 50F1 0x00 50F2 | | Reserved area (2 bytes) | | |
| 0x00 50F3 | | BEEP_CSR2 | BEEP control/status register 2 | 0x1F |
| 0x00 50F4 to 0x00 513F | Reserved area (76 bytes) | | | |

Table 8. General hardware register map (continued)

| Address | Block | Register label | Register name | Reset status | |
|---------------------------|-------|---------------------------|--------------------------------------|--------------|--|
| 0x00 5140 | RTC | RTC_TR1 | Time register 1 | 0x00 | |
| 0x00 5141 | | RTC_TR2 | Time register 2 | 0x00 | |
| 0x00 5142 | | RTC_TR3 | Time register 3 | 0x00 | |
| 0x00 5143 | | Reserved area (1 byte) | | | |
| 0x00 5144 | | RTC_DR1 | Date register 1 | 0x00 | |
| 0x00 5145 | | RTC_DR2 | Date register 2 | 0x00 | |
| 0x00 5146 | | RTC_DR3 | Date register 3 | 0x00 | |
| 0x00 5147 | | Reserved area (1 byte) | | | |
| 0x00 5148 | | RTC_CR1 | Control register 1 | 0x00 | |
| 0x00 5149 | | RTC_CR2 | Control register 2 | 0x00 | |
| 0x00 514A | | RTC_CR3 | Control register 3 | 0x00 | |
| 0x00 514B | | Reserved area (1 byte) | | | |
| 0x00 514C | | RTC_ISR1 | Initialization and status register 1 | 0x00 | |
| 0x00 514D | | RTC_ISR2 | Initialization and Status register 2 | 0x00 | |
| 0x00 514E 0x00 514F | | Reserved area (2 bytes) | | | |
| 0x00 5150 | | RTC_SPRERH | Synchronous prescaler register high | - | |
| 0x00 5151 | | RTC_SPRERL | Synchronous prescaler register low | - | |
| 0x00 5152 | | RTC_APRER | Asynchronous prescaler register | - | |
| 0x00 5153 | | Reserved area (1 byte) | | | |
| 0x00 5154 | | RTC_WUTRH | Wakeup timer register high | - | |
| 0x00 5155 | | RTC_WUTRL | Wakeup timer register low | - | |
| 0x00 5156 to 0x00 5158 | | Reserved area (3 bytes) | | | |
| 0x00 5159 | | RTC_WPR | Write protection register | 0x00 | |
| 0x00 515A 0x00 515B | | Reserved area (2 bytes) | | | |
| 0x00 515C | | RTC_ALRMAR1 | Alarm A register 1 | 0x00 | |
| 0x00 515D | | RTC_ALRMAR2 | Alarm A register 2 | 0x00 | |
| 0x00 515E | | RTC_ALRMAR3 | Alarm A register 3 | 0x00 | |
| 0x00 515F | | RTC_ALRMAR4 | Alarm A register 4 | 0x00 | |
| 0x00 5160 to 0x00 51FF | | Reserved area (160 bytes) | | | |

Table 8. General hardware register map (continued)

| Address | Block | Register label | Register name | Reset status | |
|------------------------------|-------------------------|--------------------------|-------------------------------------|--------------|--|
| 0x00 5200 | SPI1 | SPI1_CR1 | SPI1 control register 1 | 0x00 | |
| 0x00 5201 | | SPI1_CR2 | SPI1 control register 2 | 0x00 | |
| 0x00 5202 | | SPI1_ICR | SPI1 interrupt control register | 0x00 | |
| 0x00 5203 | | SPI1_SR | SPI1 status register | 0x02 | |
| 0x00 5204 | | SPI1_DR | SPI1 data register | 0x00 | |
| 0x00 5205 | | SPI1_CRCPR | SPI1 CRC polynomial register | 0x07 | |
| 0x00 5206 | | SPI1_RXCR | SPI1 Rx CRC register | 0x00 | |
| 0x00 5207 | | SPI1_TXCR | SPI1 Tx CRC register | 0x00 | |
| 0x00 5208 to 0x00 520F | Reserved area (8 bytes) | | | | |
| 0x00 5210 | I2C1 | I2C1_CR1 | I2C1 control register 1 | 0x00 | |
| 0x00 5211 | | I2C1_CR2 | I2C1 control register 2 | 0x00 | |
| 0x00 5212 | | I2C1_FREQR | I2C1 frequency register | 0x00 | |
| 0x00 5213 | | I2C1_OARL | I2C1 own address register low | 0x00 | |
| 0x00 5214 | | I2C1_OARH | I2C1 own address register high | 0x00 | |
| 0x00 5215 | | Reserved (1 byte) | | | |
| 0x00 5216 | | I2C1_DR | I2C1 data register | 0x00 | |
| 0x00 5217 | | I2C1_SR1 | I2C1 status register 1 | 0x00 | |
| 0x00 5218 | | I2C1_SR2 | I2C1 status register 2 | 0x00 | |
| 0x00 5219 | | I2C1_SR3 | I2C1 status register 3 | 0x0x | |
| 0x00 521A | | I2C1_ITR | I2C1 interrupt control register | 0x00 | |
| 0x00 521B | | I2C1_CCRL | I2C1 clock control register low | 0x00 | |
| 0x00 521C | | I2C1_CCRH | I2C1 clock control register high | 0x00 | |
| 0x00 521D | | I2C1_TRISER | I2C1 TRISE register | 0x02 | |
| 0x00 521E | | I2C1_PECR | I2C1 packet error checking register | 0x00 | |
| 0x00 521F to 0x00 522F | | Reserved area (17 bytes) | | | |

Table 8. General hardware register map (continued)

| Address | Block | Register label | Register name | Reset status |
|------------------------------|--------|--------------------------|-----------------------------|--------------|
| 0x00 5230 | USART1 | USART1_SR | USART1 status register | 0xC0 |
| 0x00 5231 | | USART1_DR | USART1 data register | undefined |
| 0x00 5232 | | USART1_BRR1 | USART1 baud rate register 1 | 0x00 |
| 0x00 5233 | | USART1_BRR2 | USART1 baud rate register 2 | 0x00 |
| 0x00 5234 | | USART1_CR1 | USART1 control register 1 | 0x00 |
| 0x00 5235 | | USART1_CR2 | USART1 control register 2 | 0x00 |
| 0x00 5236 | | USART1_CR3 | USART1 control register 3 | 0x00 |
| 0x00 5237 | | USART1_CR4 | USART1 control register 4 | 0x00 |
| 0x00 5238 | | USART1_CR5 | USART1 control register 5 | 0x00 |
| 0x00 5239 | | USART1_GTR | USART1 guard time register | 0x00 |
| 0x00 523A | | USART1_PSCR | USART1 prescaler register | 0x00 |
| 0x00 523B to 0x00 524F | | Reserved area (21 bytes) | | |

Table 8. General hardware register map (continued)

| Address | Block | Register label | Register name | Reset status |
|---------------------------|--------------------------|----------------|--|--------------|
| 0x00 5250 | TIM2 | TIM2_CR1 | TIM2 control register 1 | 0x00 |
| 0x00 5251 | | TIM2_CR2 | TIM2 control register 2 | 0x00 |
| 0x00 5252 | | TIM2_SMCR | TIM2 Slave mode control register | 0x00 |
| 0x00 5253 | | TIM2_ETR | TIM2 external trigger register | 0x00 |
| 0x00 5254 | | TIM2_DER | TIM2 DMA1 request enable register | 0x00 |
| 0x00 5255 | | TIM2_IER | TIM2 interrupt enable register | 0x00 |
| 0x00 5256 | | TIM2_SR1 | TIM2 status register 1 | 0x00 |
| 0x00 5257 | | TIM2_SR2 | TIM2 status register 2 | 0x00 |
| 0x00 5258 | | TIM2_EGR | TIM2 event generation register | 0x00 |
| 0x00 5259 | | TIM2_CCMR1 | TIM2 capture/compare mode register 1 | 0x00 |
| 0x00 525A | | TIM2_CCMR2 | TIM2 capture/compare mode register 2 | 0x00 |
| 0x00 525B | | TIM2_CCER1 | TIM2 capture/compare enable register 1 | 0x00 |
| 0x00 525C | | TIM2_CNTRH | TIM2 counter high | 0x00 |
| 0x00 525D | | TIM2_CNTRL | TIM2 counter low | 0x00 |
| 0x00 525E | | TIM2_PSCR | TIM2 prescaler register | 0x00 |
| 0x00 525F | | TIM2_ARRH | TIM2 auto-reload register high | 0xFF |
| 0x00 5260 | | TIM2_ARRL | TIM2 auto-reload register low | 0xFF |
| 0x00 5261 | | TIM2_CCR1H | TIM2 capture/compare register 1 high | 0x00 |
| 0x00 5262 | | TIM2_CCR1L | TIM2 capture/compare register 1 low | 0x00 |
| 0x00 5263 | | TIM2_CCR2H | TIM2 capture/compare register 2 high | 0x00 |
| 0x00 5264 | | TIM2_CCR2L | TIM2 capture/compare register 2 low | 0x00 |
| 0x00 5265 | | TIM2_BKR | TIM2 break register | 0x00 |
| 0x00 5266 | | TIM2_OISR | TIM2 output idle state register | 0x00 |
| 0x00 5267 to 0x00 527F | Reserved area (25 bytes) | | | |

Table 8. General hardware register map (continued)

| Address | Block | Register label | Register name | Reset status |
|---------------------------|--------------------------|----------------|--|--------------|
| 0x00 5280 | TIM3 | TIM3_CR1 | TIM3 control register 1 | 0x00 |
| 0x00 5281 | | TIM3_CR2 | TIM3 control register 2 | 0x00 |
| 0x00 5282 | | TIM3_SMCR | TIM3 Slave mode control register | 0x00 |
| 0x00 5283 | | TIM3_ETR | TIM3 external trigger register | 0x00 |
| 0x00 5284 | | TIM3_DER | TIM3 DMA1 request enable register | 0x00 |
| 0x00 5285 | | TIM3_IER | TIM3 interrupt enable register | 0x00 |
| 0x00 5286 | | TIM3_SR1 | TIM3 status register 1 | 0x00 |
| 0x00 5287 | | TIM3_SR2 | TIM3 status register 2 | 0x00 |
| 0x00 5288 | | TIM3_EGR | TIM3 event generation register | 0x00 |
| 0x00 5289 | | TIM3_CCMR1 | TIM3 Capture/Compare mode register 1 | 0x00 |
| 0x00 528A | | TIM3_CCMR2 | TIM3 Capture/Compare mode register 2 | 0x00 |
| 0x00 528B | | TIM3_CCER1 | TIM3 Capture/Compare enable register 1 | 0x00 |
| 0x00 528C | | TIM3_CNTRH | TIM3 counter high | 0x00 |
| 0x00 528D | | TIM3_CNTRL | TIM3 counter low | 0x00 |
| 0x00 528E | | TIM3_PSCR | TIM3 prescaler register | 0x00 |
| 0x00 528F | | TIM3_ARRH | TIM3 Auto-reload register high | 0xFF |
| 0x00 5290 | | TIM3_ARRL | TIM3 Auto-reload register low | 0xFF |
| 0x00 5291 | | TIM3_CCR1H | TIM3 Capture/Compare register 1 high | 0x00 |
| 0x00 5292 | | TIM3_CCR1L | TIM3 Capture/Compare register 1 low | 0x00 |
| 0x00 5293 | | TIM3_CCR2H | TIM3 Capture/Compare register 2 high | 0x00 |
| 0x00 5294 | | TIM3_CCR2L | TIM3 Capture/Compare register 2 low | 0x00 |
| 0x00 5295 | | TIM3_BKR | TIM3 break register | 0x00 |
| 0x00 5296 | | TIM3_OISR | TIM3 output idle state register | 0x00 |
| 0x00 5297 to 0x00 52AF | Reserved area (25 bytes) | | | |

Table 8. General hardware register map (continued)

| Address | Block | Register label | Register name | Reset status |
|-----------|-------|----------------|--|--------------|
| 0x00 52B0 | TIM1 | TIM1_CR1 | TIM1 control register 1 | 0x00 |
| 0x00 52B1 | | TIM1_CR2 | TIM1 control register 2 | 0x00 |
| 0x00 52B2 | | TIM1_SMCR | TIM1 Slave mode control register | 0x00 |
| 0x00 52B3 | | TIM1_ETR | TIM1 external trigger register | 0x00 |
| 0x00 52B4 | | TIM1_DER | TIM1 DMA1 request enable register | 0x00 |
| 0x00 52B5 | | TIM1_IER | TIM1 Interrupt enable register | 0x00 |
| 0x00 52B6 | | TIM1_SR1 | TIM1 status register 1 | 0x00 |
| 0x00 52B7 | | TIM1_SR2 | TIM1 status register 2 | 0x00 |
| 0x00 52B8 | | TIM1_EGR | TIM1 event generation register | 0x00 |
| 0x00 52B9 | | TIM1_CCMR1 | TIM1 Capture/Compare mode register 1 | 0x00 |
| 0x00 52BA | | TIM1_CCMR2 | TIM1 Capture/Compare mode register 2 | 0x00 |
| 0x00 52BB | | TIM1_CCMR3 | TIM1 Capture/Compare mode register 3 | 0x00 |
| 0x00 52BC | | TIM1_CCMR4 | TIM1 Capture/Compare mode register 4 | 0x00 |
| 0x00 52BD | | TIM1_CCER1 | TIM1 Capture/Compare enable register 1 | 0x00 |
| 0x00 52BE | | TIM1_CCER2 | TIM1 Capture/Compare enable register 2 | 0x00 |
| 0x00 52BF | | TIM1_CNTRH | TIM1 counter high | 0x00 |
| 0x00 52C0 | | TIM1_CNTRL | TIM1 counter low | 0x00 |
| 0x00 52C1 | | TIM1_PSCRH | TIM1 prescaler register high | 0x00 |
| 0x00 52C2 | | TIM1_PSCRL | TIM1 prescaler register low | 0x00 |
| 0x00 52C3 | | TIM1_ARRH | TIM1 Auto-reload register high | 0xFF |
| 0x00 52C4 | | TIM1_ARRL | TIM1 Auto-reload register low | 0xFF |
| 0x00 52C5 | | TIM1_RCR | TIM1 Repetition counter register | 0x00 |
| 0x00 52C6 | | TIM1_CCR1H | TIM1 Capture/Compare register 1 high | 0x00 |
| 0x00 52C7 | | TIM1_CCR1L | TIM1 Capture/Compare register 1 low | 0x00 |
| 0x00 52C8 | | TIM1_CCR2H | TIM1 Capture/Compare register 2 high | 0x00 |
| 0x00 52C9 | | TIM1_CCR2L | TIM1 Capture/Compare register 2 low | 0x00 |
| 0x00 52CA | | TIM1_CCR3H | TIM1 Capture/Compare register 3 high | 0x00 |
| 0x00 52CB | | TIM1_CCR3L | TIM1 Capture/Compare register 3 low | 0x00 |
| 0x00 52CC | | TIM1_CCR4H | TIM1 Capture/Compare register 4 high | 0x00 |
| 0x00 52CD | | TIM1_CCR4L | TIM1 Capture/Compare register 4 low | 0x00 |
| 0x00 52CE | | TIM1_BKR | TIM1 break register | 0x00 |
| 0x00 52CF | | TIM1_DTR | TIM1 dead-time register | 0x00 |
| 0x00 52D0 | | TIM1_OISR | TIM1 output idle state register | 0x00 |
| 0x00 52D1 | | TIM1_DCR1 | DMA1 control register 1 | |

Table 8. General hardware register map (continued)

| Address | Block | Register label | Register name | Reset status |
|------------------------------|--------------------------|--------------------------|-----------------------------------|--------------|
| 0x00 52D2 | | TIM1_DCR2 | TIM1 DMA1 control register 2 | 0x00 |
| 0x00 52D3 | | TIM1_DMA1R | TIM1 DMA1 address for burst mode | 0x00 |
| 0x00 52D4 to 0x00 52DF | Reserved area (12 bytes) | | | |
| 0x00 52E0 | TIM4 | TIM4_CR1 | TIM4 control register 1 | 0x00 |
| 0x00 52E1 | | TIM4_CR2 | TIM4 control register 2 | 0x00 |
| 0x00 52E2 | | TIM4_SMCR | TIM4 Slave mode control register | 0x00 |
| 0x00 52E3 | | TIM4_DER | TIM4 DMA1 request enable register | 0x00 |
| 0x00 52E4 | | TIM4_IER | TIM4 Interrupt enable register | 0x00 |
| 0x00 52E5 | | TIM4_SR1 | TIM4 status register 1 | 0x00 |
| 0x00 52E6 | | TIM4_EGR | TIM4 Event generation register | 0x00 |
| 0x00 52E7 | | TIM4_CNTR | TIM4 counter | 0x00 |
| 0x00 52E8 | | TIM4_PSCR | TIM4 prescaler register | 0x00 |
| 0x00 52E9 | | TIM4_ARR | TIM4 Auto-reload register | 0x00 |
| 0x00 52EA to 0x00 52FE | | Reserved area (21 bytes) | | |
| 0x00 52FF | IRTIM | IR_CR | Infrared control register | 0x00 |
| 0x00 5300 to 0x00 533F | Reserved area (64 bytes) | | | |
| 0x00 5340 | ADC1 | ADC1_CR1 | ADC1 configuration register 1 | 0x00 |
| 0x00 5341 | | ADC1_CR2 | ADC1 configuration register 2 | 0x00 |
| 0x00 5342 | | ADC1_CR3 | ADC1 configuration register 3 | 0x1F |
| 0x00 5343 | | ADC1_SR | ADC1 status register | 0x00 |
| 0x00 5344 | | ADC1_DRH | ADC1 data register high | 0x00 |
| 0x00 5345 | | ADC1_DRL | ADC1 data register low | 0x00 |
| 0x00 5346 | | ADC1_HTRH | ADC1 high threshold register high | 0x0F |
| 0x00 5347 | | ADC1_HTRL | ADC1 high threshold register low | 0xFF |
| 0x00 5348 | | ADC1_LTRH | ADC1 low threshold register high | 0x00 |
| 0x00 5349 | | ADC1_LTRL | ADC1 low threshold register low | 0x00 |
| 0x00 534A | | ADC1_SQR1 | ADC1 channel sequence 1 register | 0x00 |
| 0x00 534B | | ADC1_SQR2 | ADC1 channel sequence 2 register | 0x00 |
| 0x00 534C | | ADC1_SQR3 | ADC1 channel sequence 3 register | 0x00 |
| 0x00 534D | | ADC1_SQR4 | ADC1 channel sequence 4 register | 0x00 |

Table 8. General hardware register map (continued)

| Address | Block | Register label | Register name | Reset status | |
|---------------------------|--------------------------|--------------------------|--|--------------|--|
| 0x00 534E | ADC1 | ADC1_TRIGR1 | ADC1 trigger disable 1 | 0x00 | |
| 0x00 534F | | ADC1_TRIGR2 | ADC1 trigger disable 2 | 0x00 | |
| 0x00 5350 | | ADC1_TRIGR3 | ADC1 trigger disable 3 | 0x00 | |
| 0x00 5351 | | ADC1_TRIGR4 | ADC1 trigger disable 4 | 0x00 | |
| 0x00 5352 to 0x00 537F | Reserved area (46 bytes) | | | | |
| 0x00 5380 | DAC | DAC_CR1 | DAC control register 1 | 0x00 | |
| 0x00 5381 | | DAC_CR2 | DAC control register 2 | 0x00 | |
| 0x00 5382 to 0x00 5383 | | Reserved area (2 bytes) | | | |
| 0x00 5384 | | DAC_SWTRIGR | DAC software trigger register | 0x00 | |
| 0x00 5385 | | DAC_SR | DAC status register | 0x00 | |
| 0x00 5386 to 0x00 5387 | | Reserved area (2 bytes) | | | |
| 0x00 5388 | | DAC_RDHRH | DAC right aligned data holding register high | 0x00 | |
| 0x00 5389 | | DAC_RDHRL | DAC right aligned data holding register low | 0x00 | |
| 0x00 538A to 0x00 538B | | Reserved area (2 bytes) | | | |
| 0x00 538C | | DAC_LDHRH | DAC left aligned data holding register high | 0x00 | |
| 0x00 538D | | DAC_LDHRL | DAC left aligned data holding register low | 0x00 | |
| 0x00 538E to 0x00 538F | | Reserved area (2 bytes) | | | |
| 0x00 5390 | | DAC_DHR8 | DAC 8-bit data holding register | 0x00 | |
| 0x00 5391 to 0x00 53AB | | Reserved area (27 bytes) | | | |
| 0x00 53AC | | DAC_DORH | DAC data output register high | 0x00 | |
| 0x00 53AD | | DAC_DORL | DAC data output register low | 0x00 | |
| 0x00 53AE to 0x00 53FF | | Reserved area (82 bytes) | | | |

Table 8. General hardware register map (continued)

| Address | Block | Register label | Register name | Reset status |
|---------------------------|--------------------------|-------------------------|----------------------------------|--------------|
| 0x00 5400 | LCD | LCD_CR1 | LCD control register 1 | 0x00 |
| 0x00 5401 | | LCD_CR2 | LCD control register 2 | 0x00 |
| 0x00 5402 | | LCD_CR3 | LCD control register 3 | 0x00 |
| 0x00 5403 | | LCD_FRQ | LCD frequency selection register | 0x00 |
| 0x00 5404 | | LCD_PM0 | LCD Port mask register 0 | 0x00 |
| 0x00 5405 | | LCD_PM1 | LCD Port mask register 1 | 0x00 |
| 0x00 5406 | | LCD_PM2 | LCD Port mask register 2 | 0x00 |
| 0x00 5407 | | LCD_PM3 | LCD Port mask register 3 | 0x00 |
| 0x00 5408 to 0x00 540B | LCD | Reserved area (4 bytes) | | |
| 0x00 540C | | LCD_RAM0 | LCD display memory 0 | 0x00 |
| 0x00 540D | | LCD_RAM1 | LCD display memory 1 | 0x00 |
| 0x00 540E | | LCD_RAM2 | LCD display memory 2 | 0x00 |
| 0x00 540F | | LCD_RAM3 | LCD display memory 3 | 0x00 |
| 0x00 5410 | | LCD_RAM4 | LCD display memory 4 | 0x00 |
| 0x00 5411 | | LCD_RAM5 | LCD display memory 5 | 0x00 |
| 0x00 5412 | | LCD_RAM6 | LCD display memory 6 | 0x00 |
| 0x00 5413 | | LCD_RAM7 | LCD display memory 7 | 0x00 |
| 0x00 5414 | | LCD_RAM8 | LCD display memory 8 | 0x00 |
| 0x00 5415 | | LCD_RAM9 | LCD display memory 9 | 0x00 |
| 0x00 5416 | | LCD_RAM10 | LCD display memory 10 | 0x00 |
| 0x00 5417 | | LCD_RAM11 | LCD display memory 11 | 0x00 |
| 0x00 5418 | | LCD_RAM12 | LCD display memory 12 | 0x00 |
| 0x00 5419 | LCD_RAM13 | LCD display memory 13 | 0x00 | |
| 0x00 541A to 0x00 542F | Reserved area (22 bytes) | | | |

Table 8. General hardware register map (continued)

| Address | Block | Register label | Register name | Reset status |
|-----------|-----------|------------------------|--|--|
| 0x00 5430 | RI | Reserved area (1 byte) | | 0x00 |
| 0x00 5431 | | RI_ICR1 | Timer input capture routing register 1 | 0x00 |
| 0x00 5432 | | RI_ICR2 | Timer input capture routing register 2 | 0x00 |
| 0x00 5433 | | RI_IOIR1 | I/O input register 1 | undefined |
| 0x00 5434 | | RI_IOIR2 | I/O input register 2 | undefined |
| 0x00 5435 | | RI_IOIR3 | I/O input register 3 | undefined |
| 0x00 5436 | | RI_IOCMR1 | I/O control mode register 1 | 0x00 |
| 0x00 5437 | | RI_IOCMR2 | I/O control mode register 2 | 0x00 |
| 0x00 5438 | | RI_IOCMR3 | I/O control mode register 3 | 0x00 |
| 0x00 5439 | | RI_IOSR1 | I/O switch register 1 | 0x00 |
| 0x00 543A | | RI_IOSR2 | I/O switch register 2 | 0x00 |
| 0x00 543B | | RI_IOSR3 | I/O switch register 3 | 0x00 |
| 0x00 543C | | RI_IJGCR | I/O group control register | 0x3F |
| 0x00 543D | | RI_ASCR1 | Analog switch register 1 | 0x00 |
| 0x00 543E | | RI_ASCR2 | Analog switch register 2 | 0x00 |
| 0x00 543F | | RI_RCR | Resistor control register 1 | 0x00 |
| 0x00 5440 | | COMP | COMP_CSR1 | Comparator control and status register 1 |
| 0x00 5441 | COMP_CSR2 | | Comparator control and status register 2 | 0x00 |
| 0x00 5442 | COMP_CSR3 | | Comparator control and status register 3 | 0x00 |
| 0x00 5443 | COMP_CSR4 | | Comparator control and status register 4 | 0x00 |
| 0x00 5444 | COMP_CSR5 | | Comparator control and status register 5 | 0x00 |

Table 9. CPU/SWIM/debug module/interrupt controller registers

| Address | Block | Register Label | Register Name | Reset Status |
|------------------------------|--------------------------|----------------|--|--------------|
| 0x00 7F00 | CPU ⁽¹⁾ | A | Accumulator | 0x00 |
| 0x00 7F01 | | PCE | Program counter extended | 0x00 |
| 0x00 7F02 | | PCH | Program counter high | 0x00 |
| 0x00 7F03 | | PCL | Program counter low | 0x00 |
| 0x00 7F04 | | XH | X index register high | 0x00 |
| 0x00 7F05 | | XL | X index register low | 0x00 |
| 0x00 7F06 | | YH | Y index register high | 0x00 |
| 0x00 7F07 | | YL | Y index register low | 0x00 |
| 0x00 7F08 | | SPH | Stack pointer high | 0x03 |
| 0x00 7F09 | | SPL | Stack pointer low | 0xFF |
| 0x00 7F0A | | CCR | Condition code register | 0x28 |
| 0x00 7F0B to 0x00 7F5F | | CPU | Reserved area (85 bytes) | |
| 0x00 7F60 | CFG_GCR | | Global configuration register | 0x00 |
| 0x00 7F70 | ITC-SPR | ITC_SPR1 | Interrupt Software priority register 1 | 0xFF |
| 0x00 7F71 | | ITC_SPR2 | Interrupt Software priority register 2 | 0xFF |
| 0x00 7F72 | | ITC_SPR3 | Interrupt Software priority register 3 | 0xFF |
| 0x00 7F73 | | ITC_SPR4 | Interrupt Software priority register 4 | 0xFF |
| 0x00 7F74 | | ITC_SPR5 | Interrupt Software priority register 5 | 0xFF |
| 0x00 7F75 | | ITC_SPR6 | Interrupt Software priority register 6 | 0xFF |
| 0x00 7F76 | | ITC_SPR7 | Interrupt Software priority register 7 | 0xFF |
| 0x00 7F77 | | ITC_SPR8 | Interrupt Software priority register 8 | 0xFF |
| 0x00 7F78 to 0x00 7F79 | Reserved area (2 bytes) | | | |
| 0x00 7F80 | SWIM | SWIM_CSR | SWIM control status register | 0x00 |
| 0x00 7F81 to 0x00 7F8F | Reserved area (15 bytes) | | | |

Table 9. CPU/SWIM/debug module/interrupt controller registers (continued)

| Address | Block | Register Label | Register Name | Reset Status | |
|------------------------------|-------|-------------------------|---|--------------|--|
| 0x00 7F90 | DM | DM_BK1RE | DM breakpoint 1 register extended byte | 0xFF | |
| 0x00 7F91 | | DM_BK1RH | DM breakpoint 1 register high byte | 0xFF | |
| 0x00 7F92 | | DM_BK1RL | DM breakpoint 1 register low byte | 0xFF | |
| 0x00 7F93 | | DM_BK2RE | DM breakpoint 2 register extended byte | 0xFF | |
| 0x00 7F94 | | DM_BK2RH | DM breakpoint 2 register high byte | 0xFF | |
| 0x00 7F95 | | DM_BK2RL | DM breakpoint 2 register low byte | 0xFF | |
| 0x00 7F96 | | DM_CR1 | DM Debug module control register 1 | 0x00 | |
| 0x00 7F97 | | DM_CR2 | DM Debug module control register 2 | 0x00 | |
| 0x00 7F98 | | DM_CSR1 | DM Debug module control/status register 1 | 0x10 | |
| 0x00 7F99 | | DM_CSR2 | DM Debug module control/status register 2 | 0x00 | |
| 0x00 7F9A | | DM_ENFCTR | DM enable function register | 0xFF | |
| 0x00 7F9B to 0x00 7F9F | | Reserved area (5 bytes) | | | |

1. Accessible by debug module only

6 Interrupt vector mapping

Table 10. Interrupt mapping

| IRQ No. | Source block | Description | Wakeup from Halt mode | Wakeup from Active-halt mode | Wakeup from Wait (WFI mode) | Wakeup from Wait (WFE mode) ⁽¹⁾ | Vector address |
|---------|-----------------------------|--|-----------------------|------------------------------|-----------------------------|--|----------------|
| | RESET | Reset | Yes | Yes | Yes | Yes | 0x00 8000 |
| | TRAP | Software interrupt | - | - | - | - | 0x00 8004 |
| 0 | Reserved | | | | | | 0x00 8008 |
| 1 | FLASH | EOP/WR_PG_DIS | - | - | Yes | Yes ⁽²⁾ | 0x00 800C |
| 2 | DMA1 0/1 | DMA1 channels 0/1 | - | - | Yes | Yes ⁽²⁾ | 0x00 8010 |
| 3 | DMA1 2/3 | DMA1 channels 2/3 | - | - | Yes | Yes ⁽²⁾ | 0x00 8014 |
| 4 | RTC | RTC alarm interrupt | Yes | Yes | Yes | Yes | 0x00 8018 |
| 5 | EXTI E/F/PVD ⁽³⁾ | PortE/F interrupt/PVD interrupt | Yes | Yes | Yes | Yes ⁽²⁾ | 0x00 801C |
| 6 | EXTIB | External interrupt port B | Yes | Yes | Yes | Yes ⁽²⁾ | 0x00 8020 |
| 7 | EXTID | External interrupt port D | Yes | Yes | Yes | Yes ⁽²⁾ | 0x00 8024 |
| 8 | EXTI0 | External interrupt 0 | Yes | Yes | Yes | Yes ⁽²⁾ | 0x00 8028 |
| 9 | EXTI1 | External interrupt 1 | Yes | Yes | Yes | Yes ⁽²⁾ | 0x00 802C |
| 10 | EXTI2 | External interrupt 2 | Yes | Yes | Yes | Yes ⁽²⁾ | 0x00 8030 |
| 11 | EXTI3 | External interrupt 3 | Yes | Yes | Yes | Yes ⁽²⁾ | 0x00 8034 |
| 12 | EXTI4 | External interrupt 4 | Yes | Yes | Yes | Yes ⁽²⁾ | 0x00 8038 |
| 13 | EXTI5 | External interrupt 5 | Yes | Yes | Yes | Yes ⁽²⁾ | 0x00 803C |
| 14 | EXTI6 | External interrupt 6 | Yes | Yes | Yes | Yes ⁽²⁾ | 0x00 8040 |
| 15 | EXTI7 | External interrupt 7 | Yes | Yes | Yes | Yes ⁽²⁾ | 0x00 8044 |
| 16 | LCD | LCD interrupt | - | - | Yes | Yes | 0x00 8048 |
| 17 | CLK/TIM1/DAC | System clock switch/CSS interrupt/TIM1 Break/DAC | - | - | Yes | Yes | 0x00 804C |
| 18 | COMP/ADC1 | Comparator interrupt/ADC1 | Yes | Yes | Yes | Yes ⁽²⁾ | 0x00 8050 |
| 19 | TIM2 | Update /Overflow/Trigger/Break | - | - | Yes | Yes ⁽²⁾ | 0x00 8054 |
| 20 | TIM2 | Capture/Compare | - | - | Yes | Yes ⁽²⁾ | 0x00 8058 |
| 21 | TIM3 | Update /Overflow/Trigger/Break | - | - | Yes | Yes ⁽²⁾ | 0x00 805C |
| 22 | TIM3 | Capture/Compare | - | - | Yes | Yes ⁽²⁾ | 0x00 8060 |
| 23 | TIM1 | Update /Overflow/Trigger/COM | - | - | - | Yes ⁽²⁾ | 0x00 8064 |

Table 10. Interrupt mapping (continued)

| IRQ No. | Source block | Description | Wakeup from Halt mode | Wakeup from Active-halt mode | Wakeup from Wait (WFI mode) | Wakeup from Wait (WFE mode) ⁽¹⁾ | Vector address |
|---------|-------------------|--|-----------------------|------------------------------|-----------------------------|--|----------------|
| 24 | TIM1 | Capture/Compare | - | - | - | Yes ⁽²⁾ | 0x00 8068 |
| 25 | TIM4 | Update/overflow/trigger | - | - | Yes | Yes ⁽²⁾ | 0x00 806C |
| 26 | SPI1 | End of Transfer | Yes | Yes | Yes | Yes ⁽²⁾ | 0x00 8070 |
| 27 | USART 1 | Transmission complete/transmit data register empty | - | - | Yes | Yes ⁽²⁾ | 0x00 8074 |
| 28 | USART 1 | Receive Register Data full/overrun/idle line detected/parity error | - | - | Yes | Yes ⁽²⁾ | 0x00 8078 |
| 29 | I ² C1 | I ² C1 interrupt ⁽⁴⁾ | Yes | Yes | Yes | Yes ⁽²⁾ | 0x00 807C |

1. The Low power wait mode is entered when executing a WFE instruction in Low power run mode.
2. In WFE mode, this interrupt is served if it has been previously enabled. After processing the interrupt, the processor goes back to WFE mode. When this interrupt is configured as a wakeup event, the CPU wakes up and resumes processing.
3. The interrupt from PVD is logically OR-ed with Port E and F interrupts. Register EXTI_CONF allows to select between Port E and Port F interrupt (see [External interrupt port select register \(EXTI_CONF\)](#) in the RM0031).
4. The device is woken up from Halt or Active-halt mode only when the address received matches the interface address.

7 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated memory block.

All option bytes can be modified in ICP mode (with SWIM) by accessing the EEPROM address. See [Table 11](#) for details on option byte addresses.

The option bytes can also be modified 'on the fly' by the application in IAP mode, except for the ROP and UBC values which can only be taken into account when they are modified in ICP mode (with the SWIM).

Refer to the STM8L15x Flash programming manual (PM0051) and STM8 SWIM and Debug Manual (UM0320) for information on SWIM programming procedures.

Table 11. Option byte addresses

| Addr. | Option name | Option byte No. | Option bits | | | | | | | | Factory default setting |
|---------|--|-----------------|-------------|---|---|---|-------------|----------|-------------|----------|-------------------------|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 00 4800 | Read-out protection (ROP) | OPT0 | ROP[7:0] | | | | | | | | 0x00 |
| 00 4802 | UBC (User Boot code size) | OPT1 | UBC[7:0] | | | | | | | | 0x00 |
| 00 4807 | Reserved | | | | | | | | 0x00 | | |
| 00 4808 | Independent watchdog option | OPT3 [3:0] | Reserved | | | | WWDG _HALT | WWDG _HW | IWDG _HALT | IWDG _HW | 0x00 |
| 00 4809 | Number of stabilization clock cycles for HSE and LSE oscillators | OPT4 | Reserved | | | | LSECNT[1:0] | | HSECNT[1:0] | | 0x00 |
| 00 480A | Brownout reset (BOR) | OPT5 [3:0] | Reserved | | | | BOR_TH | | BOR_ON | 0x01 | |
| 00 480B | Bootloader option bytes (OPTBL) | OPTBL [15:0] | OPTBL[15:0] | | | | | | | | 0x00 |
| 00 480C | | | | | | | | | | | 0x00 |

Table 12. Option byte description

| Option byte No. | Option description |
|-----------------|--|
| OPT0 | ROP[7:0] Memory readout protection (ROP) 0xAA: Disable readout protection (write access via SWIM protocol) Refer to Readout protection section in the STM8L15x reference manual (RM0031). |
| OPT1 | UBC[7:0] Size of the user boot code area 0x00: no UBC 0x01: the UBC contains only the interrupt vectors. 0x02: Page 0 and 1 reserved for the UBC and read/write protected. Page 0 contains only the interrupt vectors. 0x03 - Page 0 to 2 reserved for UBC, memory write-protected ≥ 0xFE - Page 0 to 254 reserved for UBC, memory write-protected Refer to User boot code section in the STM8L15x reference manual (RM0031). |
| OPT2 | Reserved |
| OPT3 | IWDG_HW : Independent watchdog 0: Independent watchdog activated by software 1: Independent watchdog activated by hardware |
| | IWDG_HALT : Independent window watchdog reset on Halt/Active-halt 0: Independent watchdog continues running in Halt/Active-halt mode 1: Independent watchdog stopped in Halt/Active-halt mode |
| | WWDG_HW : Window watchdog 0: Window watchdog activated by software 1: Window watchdog activated by hardware |
| | WWDG_HALT : Window window watchdog reset on Halt/Active-halt 0: Window watchdog stopped in Halt mode 1: Window watchdog generates a reset when MCU enters Halt mode |
| OPT4 | HSECNT : Number of HSE oscillator stabilization clock cycles 0x00 - 1 clock cycle 0x01 - 16 clock cycles 0x10 - 512 clock cycles 0x11 - 4096 clock cycles |
| | LSECNT : Number of LSE oscillator stabilization clock cycles 0x00 - 1 clock cycle 0x01 - 16 clock cycles 0x10 - 512 clock cycles 0x11 - 4096 clock cycles |

Table 12. Option byte description (continued)

| Option byte No. | Option description |
|-----------------|--|
| OPT5 | BOR_ON: 0: Brownout reset off 1: Brownout reset on |
| | BOR_TH[3:1]: Brownout reset thresholds. Refer to Table 18 for details on the thresholds according to the value of BOR_TH bits. |
| OPTBL | OPTBL[15:0]: This option is checked by the boot ROM code after reset. Depending on content of addresses 00 480B, 00 480C and 0x8000 (reset vector) the CPU jumps to the bootloader or to the reset vector. Refer to the UM0560 bootloader user manual for more details. |

8 Unique ID

devices feature a 96-bit unique device identifier which provides a reference number that is unique for any device and in any context. The 96 bits of the identifier can never be altered by the user.

The unique device identifier can be read in single bytes and may then be concatenated using a custom algorithm.

The unique device identifier is ideally suited:

- For use as serial numbers
- For use as security keys to increase the code security in the program memory while using and combining this unique ID with software cryptographic primitives and protocols before programming the internal memory.
- To activate secure boot processes

Table 13. Unique ID registers (96 bits)

| Address | Content description | Unique ID bits | | | | | | | |
|---------|----------------------------|----------------|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x4926 | X co-ordinate on the wafer | U_ID[7:0] | | | | | | | |
| 0x4927 | | U_ID[15:8] | | | | | | | |
| 0x4928 | Y co-ordinate on the wafer | U_ID[23:16] | | | | | | | |
| 0x4929 | | U_ID[31:24] | | | | | | | |
| 0x492A | Wafer number | U_ID[39:32] | | | | | | | |
| 0x492B | Lot number | U_ID[47:40] | | | | | | | |
| 0x492C | | U_ID[55:48] | | | | | | | |
| 0x492D | | U_ID[63:56] | | | | | | | |
| 0x492E | | U_ID[71:64] | | | | | | | |
| 0x492F | | U_ID[79:72] | | | | | | | |
| 0x4930 | | U_ID[87:80] | | | | | | | |
| 0x4931 | | U_ID[95:88] | | | | | | | |

9 Electrical parameters

9.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS} .

9.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25\text{ }^\circ\text{C}$ and $T_A = T_A \text{ max}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation ($\text{mean} \pm 3\Sigma$).

9.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A = 25\text{ }^\circ\text{C}$, $V_{DD} = 3\text{ V}$. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated ($\text{mean} \pm 2\Sigma$).

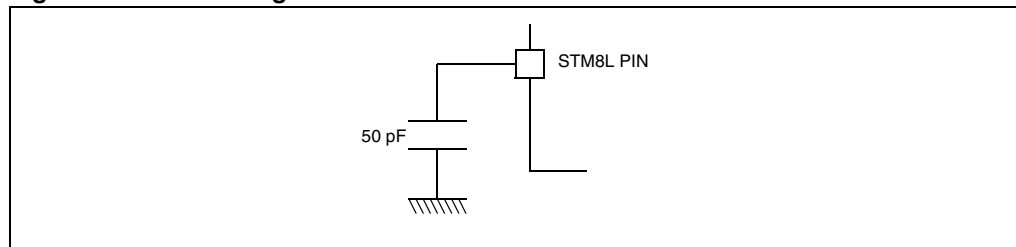
9.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

9.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 10](#).

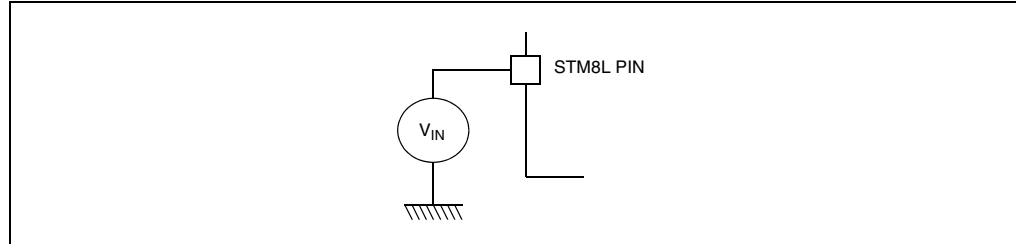
Figure 10. Pin loading conditions



9.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 11](#).

Figure 11. Pin input voltage



9.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 14. Voltage characteristics

| Symbol | Ratings | Min | Max | Unit |
|-------------------|---|---|----------------|------|
| $V_{DD} - V_{SS}$ | External supply voltage (including V_{DDA} and V_{DD2}) ⁽¹⁾ | - 0.3 | 4.0 | V |
| V_{IN} | Input voltage on true open-drain pins (PC0 and PC1) ⁽²⁾ | $V_{SS} - 0.3$ | $V_{DD} + 4.0$ | |
| | Input voltage on FT pins (PA7 and PE0) ⁽²⁾ | $V_{SS} - 0.3$ | $V_{DD} + 4.0$ | |
| | Input voltage on any other pin ⁽³⁾ | $V_{SS} - 0.3$ | 4.0 | |
| V_{ESD} | Electrostatic discharge voltage | see Absolute maximum ratings (electrical sensitivity) on page 108 | | |

1. All power (V_{DD1} , V_{DD2} , V_{DDA}) and ground (V_{SS1} , V_{SS2} , V_{SSA}) pins must always be connected to the external power supply.
2. Positive injection is not possible on these I/Os. V_{IN} maximum must always be respected. $I_{INJ(PIN)}$ must never be exceeded. A negative injection is induced by $V_{IN} < V_{SS}$.
3. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$.

Table 15. Current characteristics

| Symbol | Ratings | Max. | Unit |
|-----------------------|--|------|------|
| I_{VDD} | Total current into V_{DD} power line (source) | 80 | mA |
| I_{VSS} | Total current out of V_{SS} ground line (sink) | 80 | |
| I_{IO} | Output current sunk by IR_TIM pin (with high sink LED driver capability) | 80 | |
| | Output current sunk by any other I/O and control pin | 25 | |
| | Output current sourced by any I/Os and control pin | - 25 | |
| $I_{INJ(PIN)}$ | Injected current on true open-drain pins (PC0 and PC1) ⁽¹⁾ | - 5 | |
| | Injected current on FT pins (PA7 and PE0) ⁽¹⁾ | - 5 | |
| | Injected current on any other pin ⁽²⁾ | ± 5 | |
| $\Sigma I_{INJ(PIN)}$ | Total injected current (sum of all I/O and control pins) ⁽³⁾ | ± 25 | |

1. Positive injection is not possible on these I/Os. V_{IN} maximum must always be respected. $I_{INJ(PIN)}$ must never be exceeded. A negative injection is induced by $V_{IN} < V_{SS}$.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$.
3. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 16. Thermal characteristics

| Symbol | Ratings | Min | Unit |
|-----------|------------------------------|-------------|------|
| T_{STG} | Storage temperature range | -65 to +150 | °C |
| T_J | Maximum junction temperature | 150 | |

9.3 Operating conditions

Subject to general operating conditions for V_{DD} and T_A .

9.3.1 General operating conditions

Table 17. General operating conditions

| Symbol | Parameter | Conditions | Min | Max | Unit | |
|--------------------|---|---|---|---------------------|------|---|
| $f_{SYSCLK}^{(1)}$ | System clock frequency | $1.65\text{ V} \leq V_{DD} < 3.6\text{ V}$ | 0 | 16 | MHz | |
| V_{DD} | Standard operating voltage | | 1.65 ⁽²⁾ | 3.6 | V | |
| V_{DDA} | Analog operating voltage | ADC not used | Must be at the same potential as V_{DD} | 1.65 ⁽²⁾ | 3.6 | V |
| | | ADC used | | 1.8 | 3.6 | V |
| $P_D^{(3)}$ | Power dissipation at $T_A = 85\text{ °C}$ for suffix 6 devices | UFQFPN48 | | 288 | mW | |
| | | LQFP48 | | 288 | | |
| | | UFQFPN32 | | 288 | | |
| | | LQFP32 | | 288 | | |
| | | UFQFPN28 | | 282 | | |
| | | WLCSP28 | | 286 | | |
| | Power dissipation at $T_A = 125\text{ °C}$ for suffix 3 devices | UFQFPN48 | | 288 | | |
| | | LQFP48 | | 77 | | |
| | | UFQFPN32 | | 227 | | |
| | | LQFP32 | | 85 | | |
| | | UFQFPN28 | | 70 | | |
| | | WLCSP28 | | 71 | | |
| T_A | Temperature range | $1.65\text{ V} \leq V_{DD} < 3.6\text{ V}$ (6 suffix version) | -40 | 85 | °C | |
| | | $1.65\text{ V} \leq V_{DD} < 3.6\text{ V}$ (3 suffix version) | -40 | 125 | | |
| T_J | Junction temperature range | $-40\text{ °C} \leq T_A < 85\text{ °C}$ (6 suffix version) | -40 | 105 | °C | |
| | | $-40\text{ °C} \leq T_A < 125\text{ °C}$ (3 suffix version) | -40 | 130 | | |

1. $f_{SYSCLK} = f_{CPU}$

2. 1.8 V at power-up, 1.65 V at power-down if BOR is disabled

3. To calculate $P_{Dmax}(T_A)$, use the formula $P_{Dmax} = (T_{Jmax} - T_A) / \Theta_{JA}$ with T_{Jmax} in this table and Θ_{JA} in "Thermal characteristics" table.

9.3.2 Power-up / power-down operating conditions

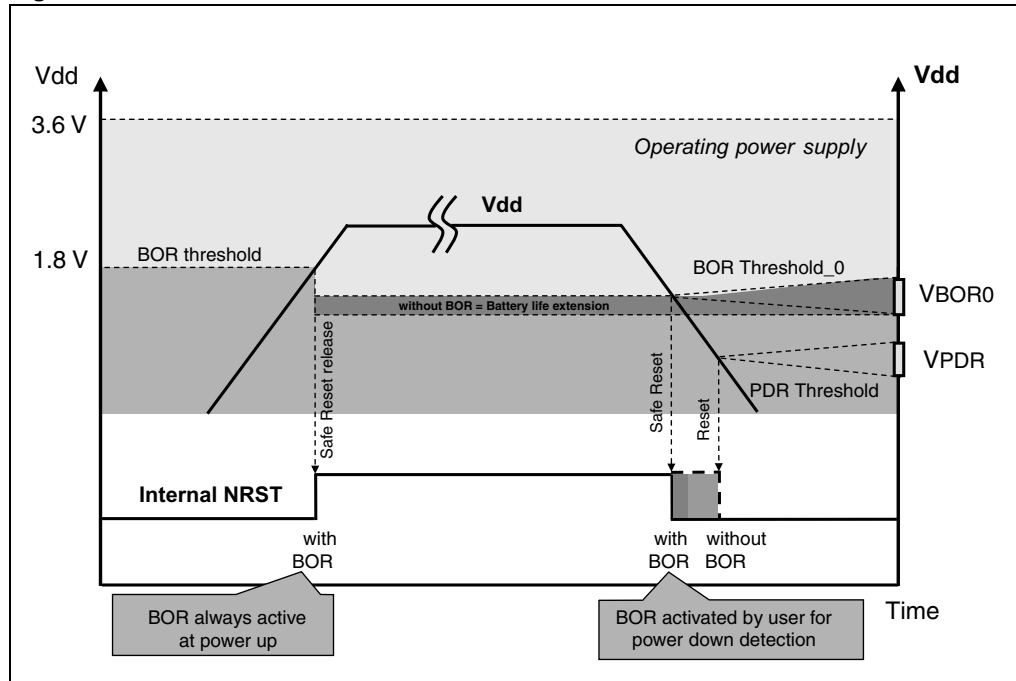
Table 18. Operating conditions at power-up / power-down

| Symbol ⁽¹⁾ | Parameter ⁽¹⁾ | Conditions ⁽¹⁾ | Min | Typ | Max | Unit |
|-----------------------|---|---------------------------|------------------|------|------|------|
| t _{VDD} | V _{DD} rise time rate | | 0 ⁽²⁾ | | ∞ | μs/V |
| | V _{DD} fall time rate | | 0 ⁽²⁾ | | ∞ | |
| t _{TEMP} | Reset release delay | V _{DD} rising | | 3 | | ms |
| V _{PDR} | Power-down reset threshold | Falling edge | 1.46 | 1.5 | 1.54 | V |
| V _{BOR0} | Brown-out reset threshold 0 (BOR_TH[2:0]=000) | Falling edge | 1.67 | 1.7 | 1.74 | |
| | | Rising edge | 1.69 | 1.75 | 1.80 | |
| V _{BOR1} | Brown-out reset threshold 1 (BOR_TH[2:0]=001) | Falling edge | 1.87 | 1.93 | 1.97 | |
| | | Rising edge | 1.96 | 2.04 | 2.07 | |
| V _{BOR2} | Brown-out reset threshold 2 (BOR_TH[2:0]=010) | Falling edge | 2.22 | 2.3 | 2.35 | |
| | | Rising edge | 2.31 | 2.41 | 2.44 | |
| V _{BOR3} | Brown-out reset threshold 3 (BOR_TH[2:0]=011) | Falling edge | 2.45 | 2.55 | 2.60 | |
| | | Rising edge | 2.54 | 2.66 | 2.7 | |
| V _{BOR4} | Brown-out reset threshold 4 (BOR_TH[2:0]=100) | Falling edge | 2.68 | 2.80 | 2.85 | |
| | | Rising edge | 2.78 | 2.90 | 2.95 | |
| V _{PVD0} | PVD threshold 0 | Falling edge | 1.80 | 1.84 | 1.88 | |
| | | Rising edge | 1.88 | 1.94 | 1.99 | |
| V _{PVD1} | PVD threshold 1 | Falling edge | 1.98 | 2.04 | 2.09 | |
| | | Rising edge | 2.08 | 2.14 | 2.18 | |
| V _{PVD2} | PVD threshold 2 | Falling edge | 2.2 | 2.24 | 2.28 | |
| | | Rising edge | 2.28 | 2.34 | 2.38 | |
| V _{PVD3} | PVD threshold 3 | Falling edge | 2.39 | 2.44 | 2.48 | |
| | | Rising edge | 2.47 | 2.54 | 2.58 | |
| V _{PVD4} | PVD threshold 4 | Falling edge | 2.57 | 2.64 | 2.69 | |
| | | Rising edge | 2.68 | 2.74 | 2.79 | |
| V _{PVD5} | PVD threshold 5 | Falling edge | 2.77 | 2.83 | 2.88 | |
| | | Rising edge | 2.87 | 2.94 | 2.99 | |
| V _{PVD6} | PVD threshold 6 | Falling edge | 2.97 | 3.05 | 3.09 | |
| | | Rising edge | 3.08 | 3.15 | 3.20 | |

1. Based on characterization results, unless otherwise specified.

2. Guaranteed by design, not tested in production.

Figure 12. POR/BOR thresholds



9.3.3 Supply current characteristics

Total current consumption

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if explicitly mentioned.

Subject to general operating conditions for V_{DD} and T_A .

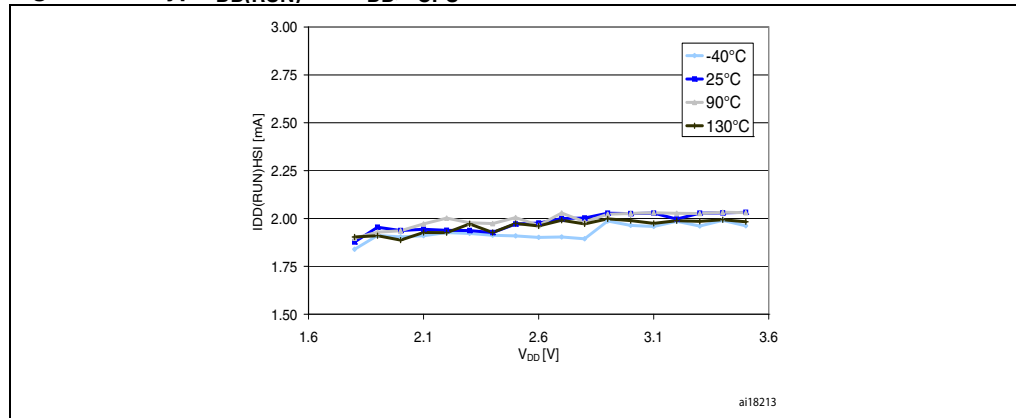
Table 19. Total current consumption in Run mode

| Symbol | Parameter (1) | Conditions ⁽¹⁾⁽²⁾ | | Typ | Max | | | | Unit | |
|---------------|--------------------------------|--|---|---------------------|---------------------------------|---------------------|------------|------------|----------------------|----|
| | | | | | 55°C | 85 °C (3) | 105 °C (4) | 125 °C (4) | | |
| $I_{DD(RUN)}$ | Supply current in run mode (5) | All peripherals OFF, code executed from RAM, V_{DD} from 1.65 V to 3.6 V | HSI RC osc. (16 MHz) ⁽⁶⁾ | $f_{CPU} = 125$ kHz | 0.39 | 0.47 | 0.49 | 0.52 | 0.55 | mA |
| | | | | $f_{CPU} = 1$ MHz | 0.48 | 0.56 | 0.58 | 0.61 | 0.65 | |
| | | | | $f_{CPU} = 4$ MHz | 0.75 | 0.84 | 0.86 | 0.91 | 0.99 | |
| | | | | $f_{CPU} = 8$ MHz | 1.10 | 1.20 | 1.25 | 1.31 | 1.40 | |
| | | | | $f_{CPU} = 16$ MHz | 1.85 | 1.93 | 2.12 | 2.29 | 2.36 | |
| | | | HSE external clock ($f_{CPU}=f_{HSE}$) ⁽⁷⁾ | $f_{CPU} = 125$ kHz | 0.05 | 0.06 | 0.09 | 0.11 | 0.12 | |
| | | | | $f_{CPU} = 1$ MHz | 0.18 | 0.19 | 0.20 | 0.22 | 0.23 | |
| | | | | $f_{CPU} = 4$ MHz | 0.55 | 0.62 | 0.64 | 0.71 | 0.77 | |
| | | | | $f_{CPU} = 8$ MHz | 0.99 | 1.20 | 1.21 | 1.22 | 1.24 | |
| | | | LSI RC osc. (typ. 38 kHz) | $f_{CPU} = f_{LSI}$ | 0.040 | 0.045 | 0.046 | 0.048 | 0.050 | |
| | | | | | LSE external clock (32.768 kHz) | $f_{CPU} = f_{LSE}$ | 0.035 | 0.040 | 0.048 ⁽⁸⁾ | |

Table 19. Total current consumption in Run mode (continued)

| Symbol | Parameter (1) | Conditions ⁽¹⁾⁽²⁾ | | | Typ | Max | | | | Unit |
|----------------------|----------------------------|---|---|---|-------------------------------------|-------|-----------|------------|------------|------|
| | | | | | | 55 °C | 85 °C (3) | 105 °C (4) | 125 °C (4) | |
| I _{DD(RUN)} | Supply current in Run mode | All peripherals OFF, code executed from Flash, V _{DD} from 1.65 V to 3.6 V | HSI RC osc. ⁽⁹⁾ | f _{CPU} = 125 kHz | 0.43 | 0.55 | 0.56 | 0.58 | 0.62 | mA |
| | | | | f _{CPU} = 1 MHz | 0.60 | 0.77 | 0.80 | 0.82 | 0.87 | |
| | | | | f _{CPU} = 4 MHz | 1.11 | 1.34 | 1.37 | 1.39 | 1.43 | |
| | | | | f _{CPU} = 8 MHz | 1.90 | 2.20 | 2.23 | 2.31 | 2.40 | |
| | | | | f _{CPU} = 16 MHz | 3.8 | 4.60 | 4.75 | 4.87 | 4.88 | |
| | | | HSE external clock (f _{CPU} =f _{HSE}) ⁽⁷⁾ | f _{CPU} = 125 kHz | 0.30 | 0.36 | 0.39 | 0.44 | 0.47 | |
| | | | | f _{CPU} = 1 MHz | 0.40 | 0.50 | 0.52 | 0.55 | 0.56 | |
| | | | | f _{CPU} = 4 MHz | 1.15 | 1.31 | 1.40 | 1.45 | 1.48 | |
| | | | | f _{CPU} = 8 MHz | 2.17 | 2.33 | 2.44 | 2.56 | 2.77 | |
| | | | LSI RC osc. | f _{CPU} = f _{LSI} | 0.110 | 0.123 | 0.130 | 0.140 | 0.150 | |
| | | | | LSE external clock (32.768 kHz) ⁽¹⁰⁾ | f _{CPU} = f _{LSE} | 0.100 | 0.101 | 0.104 | 0.119 | |

- Based on characterization results, unless otherwise specified
- All peripherals OFF, V_{DD} from 1.65 V to 3.6 V, HSI internal RC osc. , f_{CPU}=f_{SYSCLK}
- For devices with suffix 6
- For devices with suffix 3
- CPU executing typical data processing
- The run from RAM consumption can be approximated with the linear formula:
I_{DD(run_from_RAM)} = Freq * 90 μA/MHz + 380 μA
- Oscillator bypassed (HSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the HSE consumption (I_{DD HSE}) must be added. Refer to [Table 30](#).
- Data guaranteed, each individual device tested in production.
- The run from Flash consumption can be approximated with the linear formula:
I_{DD(run_from_Flash)} = Freq * 195 μA/MHz + 440 μA
- Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption (I_{DD LSE}) must be added. Refer to [Table 31](#)

Figure 13. Typ. $I_{DD(RUN)}$ vs. V_{DD} , $f_{CPU} = 16$ MHz

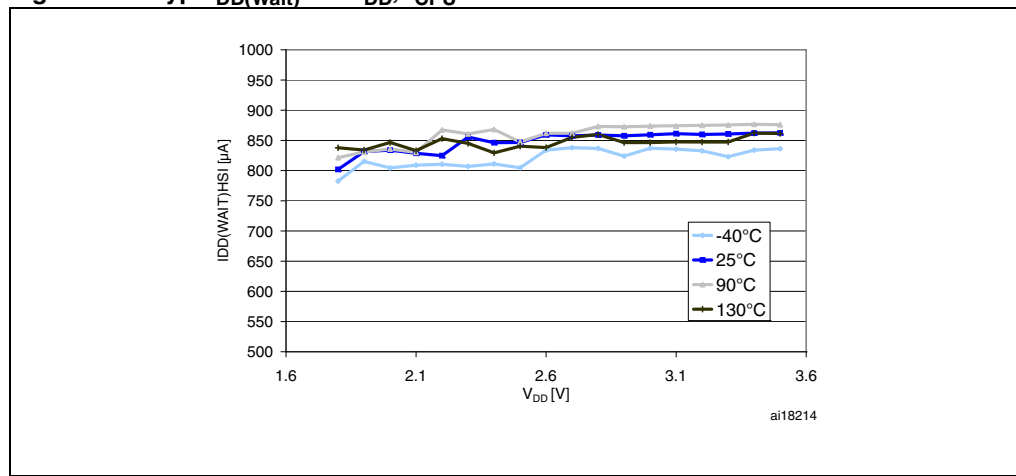
1. Typical current consumption measured with code executed from RAM

Table 20. Total current consumption in Wait mode⁽¹⁾

| Symbol | Parameter | Conditions ⁽²⁾ | Typ | Max | | | | Unit | | |
|--|-------------------------------------|---|---|-------------------------------------|--------------|---------------|---------------|-------|-------|----|
| | | | | 55°C | 85 °C (3) | 105 °C (4) | 125 °C (4) | | | |
| I _{DD(Wait)} | Supply current in Wait mode | CPU not clocked, all peripherals OFF, code executed from RAM with Flash in I _{DDQ} mode, ⁽⁵⁾ V _{DD} from 1.65 V to 3.6 V | HSI | f _{CPU} = 125 kHz | 0.33 | 0.39 | 0.41 | 0.43 | 0.45 | mA |
| | | | | f _{CPU} = 1 MHz | 0.35 | 0.41 | 0.44 | 0.45 | 0.48 | |
| | | | | f _{CPU} = 4 MHz | 0.42 | 0.51 | 0.52 | 0.54 | 0.58 | |
| | | | | f _{CPU} = 8 MHz | 0.52 | 0.57 | 0.58 | 0.59 | 0.62 | |
| | | | | f _{CPU} = 16 MHz | 0.68 | 0.76 | 0.79 | 0.82 | 0.85 | |
| | | | HSE external clock (f _{CPU} =f _{HSE}) ⁽⁶⁾ | f _{CPU} = 125 kHz | 0.032 | 0.056 | 0.068 | 0.072 | 0.093 | |
| | | | | f _{CPU} = 1 MHz | 0.078 | 0.121 | 0.144 | 0.163 | 0.197 | |
| | | | | f _{CPU} = 4 MHz | 0.218 | 0.26 | 0.30 | 0.36 | 0.40 | |
| | | | | f _{CPU} = 8 MHz | 0.40 | 0.52 | 0.57 | 0.62 | 0.66 | |
| | | | LSI | f _{CPU} = f _{LSI} | 0.035 | 0.044 | 0.046 | 0.049 | 0.054 | |
| LSE ⁽⁷⁾ external clock (32.768 kHz) | f _{CPU} = f _{LSE} | 0.032 | | 0.036 | 0.038 | 0.044 | 0.051 | | | |
| I _{DD(Wait)} | Supply current in Wait mode | CPU not clocked, all peripherals OFF, code executed from Flash, V _{DD} from 1.65 V to 3.6 V | HSI | f _{CPU} = 125 kHz | 0.38 | 0.48 | 0.49 | 0.50 | 0.56 | mA |
| | | | | f _{CPU} = 1 MHz | 0.41 | 0.49 | 0.51 | 0.53 | 0.59 | |
| | | | | f _{CPU} = 4 MHz | 0.50 | 0.57 | 0.58 | 0.62 | 0.66 | |
| | | | | f _{CPU} = 8 MHz | 0.60 | 0.66 | 0.68 | 0.72 | 0.74 | |
| | | | | f _{CPU} = 16 MHz | 0.79 | 0.84 | 0.86 | 0.87 | 0.90 | |
| | | | HSE ⁽⁶⁾ external clock (f _{CPU} =HSE) | f _{CPU} = 125 kHz | 0.06 | 0.08 | 0.09 | 0.10 | 0.12 | |
| | | | | f _{CPU} = 1 MHz | 0.10 | 0.17 | 0.18 | 0.19 | 0.22 | |
| | | | | f _{CPU} = 4 MHz | 0.24 | 0.36 | 0.39 | 0.41 | 0.44 | |
| | | | | f _{CPU} = 8 MHz | 0.50 | 0.58 | 0.61 | 0.62 | 0.64 | |
| | | | LSI | f _{CPU} = f _{LSI} | 0.055 | 0.058 | 0.065 | 0.073 | 0.080 | |
| LSE ⁽⁷⁾ external clock (32.768 kHz) | f _{CPU} = f _{LSE} | 0.051 | | 0.056 | 0.060 | 0.065 | 0.073 | | | |

1. Based on characterization results, unless specified
2. All peripherals OFF, V_{DD} from 1.65 V to 3.6 V, HSI internal RC osc. , $f_{CPU} = f_{SYSCLK}$
3. For temperature range 6.
4. For temperature range 3.
5. Flash is configured in I_{DDQ} mode in Wait mode by setting the EPM or WAITM bit in the Flash_CR1 register.
6. Oscillator bypassed (HSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the HSE consumption ($I_{DD\ HSE}$) must be added. Refer to [Table 30](#).
7. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ HSE}$) must be added. Refer to [Table 31](#)

Figure 14. Typ. $I_{DD(Wait)}$ vs. V_{DD} , $f_{CPU} = 16\text{ MHz}$ ¹⁾



1. Typical current consumption measured with code executed from Flash

Table 21. Total current consumption and timing in Low power run mode at $V_{DD} = 1.65$ V to 3.6 V

| Symbol | Parameter ⁽¹⁾ | Conditions ⁽²⁾ | | | Typ ⁽¹⁾ | Max ⁽¹⁾ | Unit |
|-----------------------------------|--|--|---------------------------------|--|--------------------|--------------------|---------------|
| $I_{DD(LPR)}$ | Supply current in Low power run mode | LSI RC osc. (at 38 kHz) | all peripherals OFF | $T_A = -40\text{ }^\circ\text{C}$ to $25\text{ }^\circ\text{C}$ | 5.1 | 5.4 | μA |
| | | | | $T_A = 55\text{ }^\circ\text{C}$ | 5.7 | 6 | |
| | | | | $T_A = 85\text{ }^\circ\text{C}$ | 6.8 | 7.5 | |
| | | | | $T_A = 105\text{ }^\circ\text{C}$ | 9.2 | 10.4 | |
| | | | | $T_A = 125\text{ }^\circ\text{C}$ | 13.4 | 16.6 | |
| | | | with TIM2 active ⁽³⁾ | $T_A = -40\text{ }^\circ\text{C}$ to $25\text{ }^\circ\text{C}$ | 5.4 | 5.7 | |
| | | | | $T_A = 55\text{ }^\circ\text{C}$ | 6.0 | 6.3 | |
| | | | | $T_A = 85\text{ }^\circ\text{C}$ | 7.2 | 7.8 | |
| | | | | $T_A = 105\text{ }^\circ\text{C}$ | 9.4 | 10.7 | |
| | | | | $T_A = 125\text{ }^\circ\text{C}$ | 13.8 | 17 | |
| | | LSE ⁽⁴⁾ external clock (32.768 kHz) | all peripherals OFF | $T_A = -40\text{ }^\circ\text{C}$ to $25\text{ }^\circ\text{C}$ | 5.25 | 5.6 | |
| | | | | $T_A = 55\text{ }^\circ\text{C}$ | 5.67 | 6.1 | |
| | | | | $T_A = 85\text{ }^\circ\text{C}$ | 5.85 | 6.3 | |
| | | | | $T_A = 105\text{ }^\circ\text{C}$ | 7.11 | 7.6 | |
| with TIM2 active ⁽³⁾ | $T_A = 125\text{ }^\circ\text{C}$ | | 9.84 | 12 | | | |
| | $T_A = -40\text{ }^\circ\text{C}$ to $25\text{ }^\circ\text{C}$ | | 5.59 | 6 | | | |
| | $T_A = 55\text{ }^\circ\text{C}$ | | 6.10 | 6.4 | | | |
| | $T_A = 85\text{ }^\circ\text{C}$ | | 6.30 | 7 | | | |
| $T_A = 105\text{ }^\circ\text{C}$ | 7.55 | 8.4 | | | | | |
| $T_A = 125\text{ }^\circ\text{C}$ | 10.1 | 15 | | | | | |

1. Based on characterization results, unless otherwise specified
2. No floating I/Os
3. Timer 2 clock enabled and counter running
4. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to [Table 31](#)

Figure 15. Typ. $I_{DD(LPR)}$ vs. V_{DD} (LSI clock source)

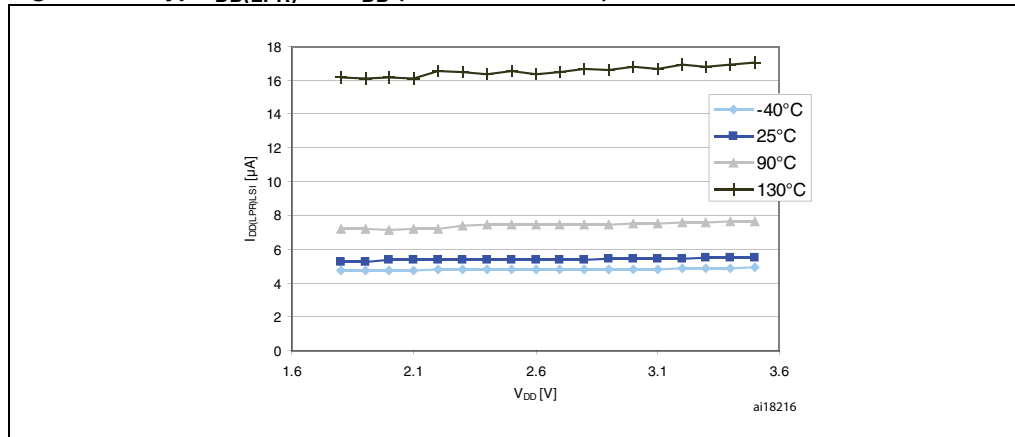


Table 22. Total current consumption in Low power wait mode at $V_{DD} = 1.65 \text{ V}$ to 3.6 V

| Symbol | Parameter ⁽¹⁾⁽²⁾ | Conditions | | Typ (1)(2) | Max (1)(2) | Unit | |
|------------------------------------|---------------------------------------|--|---------------------------------|---|---------------|------|---------------|
| $I_{DD(LPW)}$ | Supply current in Low power wait mode | LSI RC osc. (at 38 kHz) | all peripherals OFF | $T_A = -40 \text{ }^\circ\text{C}$ to $25 \text{ }^\circ\text{C}$ | 3 | 3.3 | μA |
| | | | | $T_A = 55 \text{ }^\circ\text{C}$ | 3.3 | 3.6 | |
| | | | | $T_A = 85 \text{ }^\circ\text{C}$ | 4.4 | 5 | |
| | | | | $T_A = 105 \text{ }^\circ\text{C}$ | 6.7 | 8 | |
| | | | | $T_A = 125 \text{ }^\circ\text{C}$ | 11 | 14 | |
| | | | with TIM2 active ⁽³⁾ | $T_A = -40 \text{ }^\circ\text{C}$ to $25 \text{ }^\circ\text{C}$ | 3.4 | 3.7 | |
| | | | | $T_A = 55 \text{ }^\circ\text{C}$ | 3.7 | 4 | |
| | | | | $T_A = 85 \text{ }^\circ\text{C}$ | 4.8 | 5.4 | |
| | | | | $T_A = 105 \text{ }^\circ\text{C}$ | 7 | 8.3 | |
| | | | | $T_A = 125 \text{ }^\circ\text{C}$ | 11.3 | 14.5 | |
| | | LSE external clock ⁽⁴⁾ (32.768 kHz) | all peripherals OFF | $T_A = -40 \text{ }^\circ\text{C}$ to $25 \text{ }^\circ\text{C}$ | 2.35 | 2.7 | |
| | | | | $T_A = 55 \text{ }^\circ\text{C}$ | 2.42 | 2.82 | |
| | | | | $T_A = 85 \text{ }^\circ\text{C}$ | 3.10 | 3.71 | |
| | | | | $T_A = 105 \text{ }^\circ\text{C}$ | 4.36 | 5.7 | |
| | | | | $T_A = 125 \text{ }^\circ\text{C}$ | 7.20 | 11 | |
| | | | with TIM2 active ⁽³⁾ | $T_A = -40 \text{ }^\circ\text{C}$ to $25 \text{ }^\circ\text{C}$ | 2.46 | 2.75 | |
| | | | | $T_A = 55 \text{ }^\circ\text{C}$ | 2.50 | 2.81 | |
| | | | | $T_A = 85 \text{ }^\circ\text{C}$ | 3.16 | 3.82 | |
| $T_A = 105 \text{ }^\circ\text{C}$ | 4.51 | | | 5.9 | | | |
| $T_A = 125 \text{ }^\circ\text{C}$ | 7.28 | | | 11 | | | |

1. No floating I/Os.
2. Based on characterization results, unless otherwise specified.
3. Timer 2 clock enabled and counter is running.
4. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD LSE}$) must be added. Refer to [Table 31](#).

Figure 16. Typ. $I_{DD(LPW)}$ vs. V_{DD} (LSI clock source)

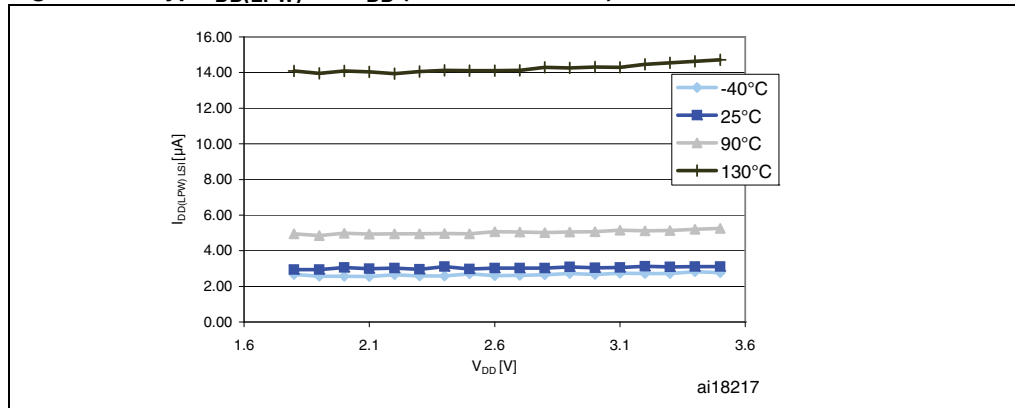


Table 23. Total current consumption and timing in Active-halt mode at $V_{DD} = 1.65\text{ V}$ to 3.6 V

| Symbol | Parameter ⁽¹⁾⁽²⁾ | Conditions | | Typ (1)(2) | Max | Unit | | | |
|--------------|------------------------------------|-----------------------|---|---|------------|-----------------------|-----|------|---------------|
| $I_{DD(AH)}$ | Supply current in Active-halt mode | LSI RC (at 38 kHz) | LCD OFF ⁽³⁾ | $T_A = -40\text{ °C}$ to 25 °C | 0.9 (4) | 2.1 | | | |
| | | | | $T_A = 55\text{ °C}$ | 1.2 | 3 | | | |
| | | | | $T_A = 85\text{ °C}$ | 1.5 | 3.4 | | | |
| | | | | $T_A = 105\text{ °C}$ | 2.6 | 6.6 | | | |
| | | | | $T_A = 125\text{ °C}$ | 5.1 | 12 | | | |
| | | | LCD ON (static duty/ external V_{LCD}) ⁽⁵⁾ | $T_A = -40\text{ °C}$ to 25 °C | 1.4 | 3.1 | | | |
| | | | | $T_A = 55\text{ °C}$ | 1.5 | 3.3 | | | |
| | | | | $T_A = 85\text{ °C}$ | 1.9 | 4.3 | | | |
| | | | | $T_A = 105\text{ °C}$ | 2.9 | 6.8 | | | |
| | | | | $T_A = 125\text{ °C}$ | 5.5 | 13 | | | |
| | | | LCD ON (1/4 duty/ external V_{LCD}) ⁽⁶⁾ | $T_A = -40\text{ °C}$ to 25 °C | 1.9 | 4.3 | | | |
| | | | | $T_A = 55\text{ °C}$ | 1.95 | 4.4 | | | |
| | | | | $T_A = 85\text{ °C}$ | 2.4 | 5.4 | | | |
| | | | | $T_A = 105\text{ °C}$ | 3.4 | 7.6 | | | |
| | | | LCD ON (1/4 duty/ internal V_{LCD}) ⁽⁷⁾ | $T_A = -40\text{ °C}$ to 25 °C | 3.9 | 8.75 | | | |
| | | | | $T_A = 55\text{ °C}$ | 4.15 | 9.3 | | | |
| | | | | $T_A = 85\text{ °C}$ | 4.5 | 10.2 | | | |
| | | | | $T_A = 105\text{ °C}$ | 5.6 | 13.5 | | | |
| | | | | | | $T_A = 125\text{ °C}$ | 6.8 | 16.3 | μA |

Table 23. Total current consumption and timing in Active-halt mode at $V_{DD} = 1.65\text{ V}$ to 3.6 V (continued)

| Symbol | Parameter ⁽¹⁾⁽²⁾ | Conditions | | | Typ (1)(2) | Max | Unit |
|---|---|--|--|---|---------------|------|---------------|
| $I_{DD(AH)}$ | Supply current in Active-halt mode | LSE external clock (32.768 kHz) (8) | LCD OFF ⁽⁹⁾ | $T_A = -40\text{ °C}$ to 25 °C | 0.5 | 1.2 | μA |
| | | | | $T_A = 55\text{ °C}$ | 0.62 | 1.4 | |
| | | | | $T_A = 85\text{ °C}$ | 0.88 | 2.1 | |
| | | | | $T_A = 105\text{ °C}$ | 2.1 | 4.85 | |
| | | | | $T_A = 125\text{ °C}$ | 4.8 | 11 | |
| | | | LCD ON (static duty) (5) | $T_A = -40\text{ °C}$ to 25 °C | 0.85 | 1.9 | |
| | | | | $T_A = 55\text{ °C}$ | 0.95 | 2.2 | |
| | | | | $T_A = 85\text{ °C}$ | 1.3 | 3.2 | |
| | | | | $T_A = 105\text{ °C}$ | 2.3 | 5.3 | |
| | | | | $T_A = 125\text{ °C}$ | 5.0 | 12 | |
| | | | LCD ON (1/4 duty) ⁽⁶⁾ | $T_A = -40\text{ °C}$ to 25 °C | 1.5 | 2.5 | |
| | | | | $T_A = 55\text{ °C}$ | 1.6 | 3.8 | |
| | | | | $T_A = 85\text{ °C}$ | 1.8 | 4.2 | |
| | | | | $T_A = 105\text{ °C}$ | 2.9 | 7.0 | |
| | | | | $T_A = 125\text{ °C}$ | 5.7 | 14 | |
| | | | LCD ON (1/4 duty/ internal V_{LCD}) ⁽⁷⁾ | $T_A = -40\text{ °C}$ to 25 °C | 3.4 | 7.6 | |
| | | | | $T_A = 55\text{ °C}$ | 3.7 | 8.3 | |
| | | | | $T_A = 85\text{ °C}$ | 3.9 | 9.2 | |
| | | | | $T_A = 105\text{ °C}$ | 5.0 | 14.5 | |
| | | | | $T_A = 125\text{ °C}$ | 6.3 | 15.2 | |
| $I_{DD(WUFAH)}$ | Supply current during wakeup time from Active-halt mode (using HSI) | | | | 2.4 | | mA |
| $t_{WU_HSI(AH)}$ ⁽¹⁰⁾ (11) | Wakeup time from Active-halt mode to Run mode (using HSI) | | | | 4.7 | 6.2 | μs |
| $t_{WU_LSI(AH)}$ ⁽¹⁰⁾ (11) | Wakeup time from Active-halt mode to Run mode (using LSI) | | | | 150 | | μs |

1. No floating I/O, unless otherwise specified.
2. Based on characterization results, unless otherwise specified.
3. RTC enabled. Clock source = LSI
4. Based on Design estimation.
5. RTC enabled, LCD enabled with external $V_{LCD} = 3\text{ V}$, static duty, division ratio = 256, all pixels active, no LCD connected.
6. RTC enabled, LCD enabled with external V_{LCD} , 1/4 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.

7. LCD enabled with internal LCD booster $V_{LCD} = 3\text{ V}$, 1/4 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
8. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to [Table 31](#)
9. RTC enabled. Clock source = LSE
10. Wakeup time until start of interrupt vector fetch.
The first word of interrupt routine is fetched 4 CPU cycles after t_{WU} .
11. ULP=0 or ULP=1 and FWU=1 in the PWR_CSR2 register.

Table 24. Typical current consumption in Active-halt mode, RTC clocked by LSE external crystal

| Symbol | Parameter | Condition | Typ | Unit | |
|--------------------|------------------------------------|-------------------------|-----------------------|------|---------------|
| $I_{DD(AH)}^{(1)}$ | Supply current in Active-halt mode | $V_{DD} = 1.8\text{ V}$ | LSE | 1.15 | μA |
| | | | LSE/32 ⁽²⁾ | 1.05 | |
| | | $V_{DD} = 3\text{ V}$ | LSE | 1.30 | |
| | | | LSE/32 ⁽²⁾ | 1.20 | |
| | | $V_{DD} = 3.6\text{ V}$ | LSE | 1.45 | |
| | | | LSE/32 ⁽²⁾ | 1.35 | |

1. Based on measurements on bench with 32.768 kHz external crystal oscillator.
2. RTC clock is LSE divided by 32.

Table 25. Total current consumption and timing in Halt mode at $V_{DD} = 2\text{ V}$

| Symbol | Parameter ⁽¹⁾⁽²⁾ | Condition | Typ ⁽¹⁾⁽²⁾ | Max ⁽¹⁾⁽²⁾ | Unit |
|------------------------------|---|---------------------------------------|-----------------------|-----------------------|---------------|
| $I_{DD(Halt)}$ | Supply current in Halt mode (Ultra low power ULP bit =1 in the PWR_CSR2 register) | $T_A = -40\text{ °C to }25\text{ °C}$ | 350 | 1400 | nA |
| | | $T_A = 55\text{ °C}$ | 580 | 2000 | |
| | | $T_A = 85\text{ °C}$ | 1160 | 2800 | |
| | | $T_A = 105\text{ °C}$ | 2560 | 6700 | |
| $I_{DD(WUHalt)}$ | Supply current during wakeup time from Halt mode (using HSI) | | 2.4 | | mA |
| $t_{WU_HSI(Halt)}^{(3)(4)}$ | Wakeup time from Halt to Run mode (using HSI) | | 4.7 | 6.2 | μs |
| $t_{WU_LSI(Halt)}^{(3)(4)}$ | Wakeup time from Halt mode to Run mode (using LSI) | | 150 | | μs |

1. $T_A = -40\text{ to }125\text{ °C}$, no floating I/O, unless otherwise specified
2. Based on characterization results, unless otherwise specified
3. ULP=0 or ULP=1 and FWU=1 in the PWR_CSR2 register
4. Wakeup time until start of interrupt vector fetch.
The first word of interrupt routine is fetched 4 CPU cycles after t_{WU}

Current consumption of on-chip peripherals

Table 26. Peripheral current consumption

| Symbol | Parameter | Typ. $V_{DD} = 3.0\text{ V}$ | Unit | |
|-------------------|--|---------------------------------|--------------------------|---|
| $I_{DD}(TIM1)$ | TIM1 supply current ⁽¹⁾ | 13 | $\mu\text{A}/\text{MHz}$ | |
| $I_{DD}(TIM2)$ | TIM2 supply current ⁽¹⁾ | 8 | | |
| $I_{DD}(TIM3)$ | TIM3 supply current ⁽¹⁾ | 8 | | |
| $I_{DD}(TIM4)$ | TIM4 timer supply current ⁽¹⁾ | 3 | | |
| $I_{DD}(USART1)$ | USART1 supply current ⁽²⁾ | 6 | | |
| $I_{DD}(SPI1)$ | SPI1 supply current ⁽²⁾ | 3 | | |
| $I_{DD}(I2C1)$ | I ² C1 supply current ⁽²⁾ | 5 | | |
| $I_{DD}(DMA1)$ | DMA1 supply current | 3 | | |
| $I_{DD}(WWDG)$ | WWDG supply current | 2 | | |
| $I_{DD}(ALL)$ | Peripherals ON ⁽³⁾ | 44 | $\mu\text{A}/\text{MHz}$ | |
| $I_{DD}(ADC1)$ | ADC1 supply current ⁽⁴⁾ | 1500 | μA | |
| $I_{DD}(DAC)$ | DAC supply current ⁽⁵⁾ | 370 | | |
| $I_{DD}(COMP1)$ | Comparator 1 supply current ⁽⁶⁾ | 0.160 | | |
| $I_{DD}(COMP2)$ | Comparator 2 supply current ⁽⁶⁾ | Slow mode | | 2 |
| | | Fast mode | | 5 |
| $I_{DD}(PVD/BOR)$ | Power voltage detector and brownout Reset unit supply current ⁽⁷⁾ | 2.6 | | |
| $I_{DD}(BOR)$ | Brownout Reset unit supply current ⁽⁷⁾ | 2.4 | | |
| $I_{DD}(IDWDG)$ | Independent watchdog supply current | including LSI supply current | 0.45 | |
| | | excluding LSI supply current | 0.05 | |

1. Data based on a differential I_{DD} measurement between all peripherals OFF and a timer counter running at 16 MHz. The CPU is in Wait mode in both cases. No IC/OC programmed, no I/O pins toggling. Not tested in production.
2. Data based on a differential I_{DD} measurement between the on-chip peripheral in reset configuration and not clocked and the on-chip peripheral when clocked and not kept under reset. The CPU is in Wait mode in both cases. No I/O pins toggling. Not tested in production.
3. Peripherals listed above the $I_{DD}(ALL)$ parameter ON: TIM1, TIM2, TIM3, TIM4, USART1, SPI1, I2C1, DMA1, WWDG.
4. Data based on a differential I_{DD} measurement between ADC in reset configuration and continuous ADC conversion.
5. Data based on a differential I_{DD} measurement between DAC in reset configuration and continuous DAC conversion of $V_{DD}/2$. Floating DAC output.
6. Data based on a differential I_{DD} measurement between COMP1 or COMP2 in reset configuration and COMP1 or COMP2 enabled with static inputs. Supply current of internal reference voltage excluded.
7. Including supply current of internal reference voltage.

Table 27. Current consumption under external reset

| Symbol | Parameter | Conditions | Typ | Unit | |
|---------------|--|--|-------------------------|------|---------------|
| $I_{DD(RST)}$ | Supply current under external reset ⁽¹⁾ | All pins are externally tied to V_{DD} | $V_{DD} = 1.8\text{ V}$ | 48 | μA |
| | | | $V_{DD} = 3\text{ V}$ | 76 | |
| | | | $V_{DD} = 3.6\text{ V}$ | 91 | |

1. All pins except PA0, PB0 and PB4 are floating under reset. PA0, PB0 and PB4 are configured with pull-up under reset.

9.3.4 Clock and timing characteristics

HSE external clock (HSEBYP = 1 in CLK_ECKCR)

Subject to general operating conditions for V_{DD} and T_A .

Table 28. HSE external clock characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|--|----------------------------|---------------------|-----|---------------------|---------------|
| f_{HSE_ext} | External clock source frequency ⁽¹⁾ | | 1 | | 16 | MHz |
| $V_{HSEH}^{(2)}$ | OSC_IN input pin high level voltage | | $0.7 \times V_{DD}$ | | V_{DD} | V |
| $V_{HSEL}^{(2)}$ | OSC_IN input pin low level voltage | | V_{SS} | | $0.3 \times V_{DD}$ | |
| $C_{in(HSE)}$ | OSC_IN input capacitance ⁽¹⁾ | | | 2.6 | | pF |
| I_{LEAK_HSE} | OSC_IN input leakage current | $V_{SS} < V_{IN} < V_{DD}$ | | | ± 1 | μA |

1. Guaranteed by design, not tested in production.

2. Data based on characterization results, not tested in production.

LSE external clock (LSEBYP=1 in CLK_ECKCR)

Subject to general operating conditions for V_{DD} and T_A .

Table 29. LSE external clock characteristics

| Symbol | Parameter | Min | Typ | Max | Unit |
|------------------|--|---------------------|--------|---------------------|---------------|
| f_{LSE_ext} | External clock source frequency ⁽¹⁾ | | 32.768 | | kHz |
| $V_{LSEH}^{(2)}$ | OSC32_IN input pin high level voltage | $0.7 \times V_{DD}$ | | V_{DD} | V |
| $V_{LSEL}^{(2)}$ | OSC32_IN input pin low level voltage | V_{SS} | | $0.3 \times V_{DD}$ | |
| $C_{in(LSE)}$ | OSC32_IN input capacitance ⁽¹⁾ | | 0.6 | | pF |
| I_{LEAK_LSE} | OSC32_IN input leakage current | | | ± 1 | μA |

1. Guaranteed by design, not tested in production.

2. Data based on characterization results, not tested in production.

HSE crystal/ceramic resonator oscillator

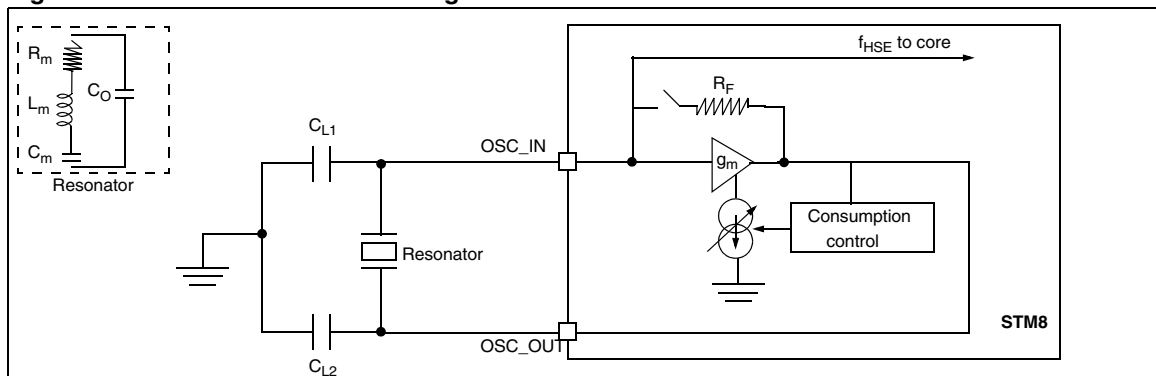
The HSE clock can be supplied with a 1 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 30. HSE oscillator characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|---|------------------------------------|-----|-----|---|------------|
| f_{HSE} | High speed external oscillator frequency | | 1 | | 16 | MHz |
| R_F | Feedback resistor | | | 200 | | k Ω |
| $C^{(1)}$ | Recommended load capacitance ⁽²⁾ | | | 20 | | pF |
| $I_{DD(HSE)}$ | HSE oscillator power consumption | $C = 20$ pF, $f_{OSC} = 16$ MHz | | | 2.5 (startup) 0.7 (stabilized) ⁽³⁾ | mA |
| | | $C = 10$ pF, $f_{OSC} = 16$ MHz | | | 2.5 (startup) 0.46 (stabilized) ⁽³⁾ | |
| g_m | Oscillator transconductance | | 3.5 | | | mA/V |
| $t_{SU(HSE)}^{(4)}$ | Startup time | V_{DD} is stabilized | | 1 | | ms |

- $C=C_{L1}=C_{L2}$ is approximately equivalent to $2 \times$ crystal C_{LOAD} .
- The oscillator selection can be optimized in terms of supply current using a high quality resonator with small R_m value. Refer to crystal manufacturer for more details
- Guaranteed by design. Not tested in production.
- $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 16 MHz oscillation. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 17. HSE oscillator circuit diagram



HSE oscillator critical g_m formula

$$g_{m\text{crit}} = (2 \times \pi \times f_{HSE})^2 \times R_m (2C_o + C)^2$$

R_m : Motional resistance (see crystal specification), L_m : Motional inductance (see crystal specification),
 C_m : Motional capacitance (see crystal specification), C_o : Shunt capacitance (see crystal specification),
 $C_{L1}=C_{L2}=C$: Grounded external capacitance
 $g_m \gg g_{m\text{crit}}$

LSE crystal/ceramic resonator oscillator

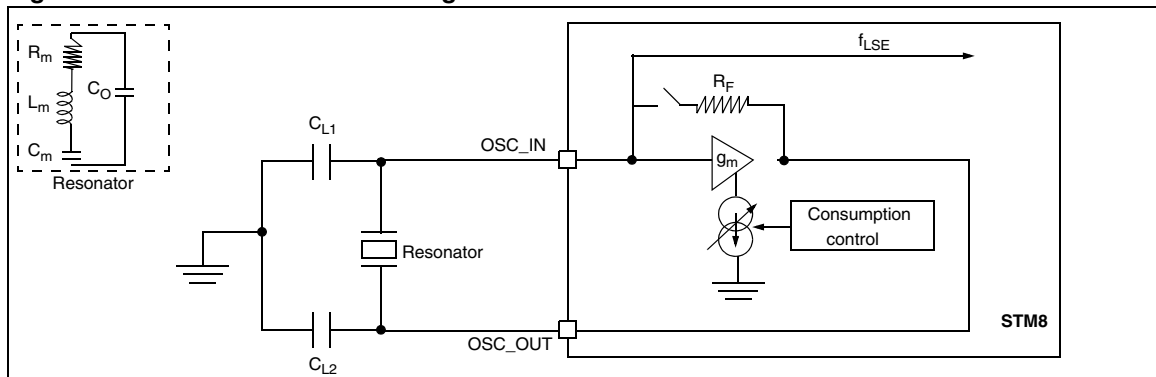
The LSE clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 31. LSE oscillator characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|---|-----------------------------|-----|--------|--------------------|-----------------|
| f_{LSE} | Low speed external oscillator frequency | | | 32.768 | | kHz |
| R_F | Feedback resistor | $\Delta V = 200 \text{ mV}$ | | 1.2 | | $M\Omega$ |
| $C^{(1)}$ | Recommended load capacitance ⁽²⁾ | | | 8 | | pF |
| $I_{DD(LSE)}$ | LSE oscillator power consumption | | | | 1.4 ⁽³⁾ | μA |
| | | $V_{DD} = 1.8 \text{ V}$ | | 450 | | nA |
| | | $V_{DD} = 3 \text{ V}$ | | 600 | | |
| | $V_{DD} = 3.6 \text{ V}$ | | 750 | | | |
| g_m | Oscillator transconductance | | 3 | | | $\mu\text{A/V}$ |
| $t_{SU(LSE)}^{(4)}$ | Startup time | V_{DD} is stabilized | | 1 | | s |

1. $C=C_{L1}=C_{L2}$ is approximately equivalent to 2 x crystal C_{LOAD} .
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with a small R_m value. Refer to crystal manufacturer for more details.
3. Guaranteed by design. Not tested in production.
4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 18. LSE oscillator circuit diagram



Internal clock sources

Subject to general operating conditions for V_{DD} , and T_A .

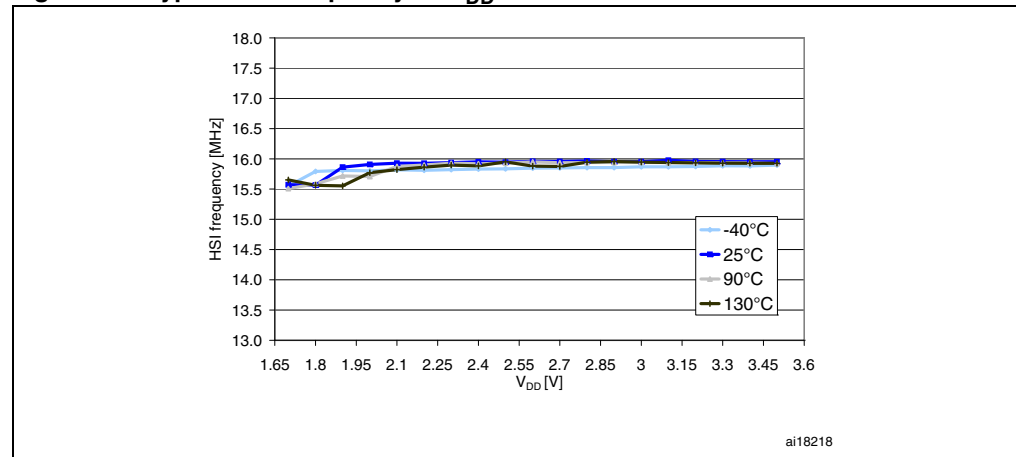
High speed internal RC oscillator (HSI)

Table 32. HSI oscillator characteristics

| Symbol | Parameter (1) | Conditions(1) | Min | Typ | Max | Unit |
|---------------|---|--|----------|---------------|---------------|---------------|
| f_{HSI} | Frequency | $V_{DD} = 3.0\text{ V}$ | | 16 | | MHz |
| ACC_{HSI} | Accuracy of HSI oscillator (factory calibrated) | $V_{DD} = 3.0\text{ V}, T_A = 25\text{ }^\circ\text{C}$ | -1 (2) | | 1 (2) | % |
| | | $V_{DD} = 3.0\text{ V}, 0\text{ }^\circ\text{C} \leq T_A \leq 55\text{ }^\circ\text{C}$ | -1.5 (2) | | 1.5 (2) | % |
| | | $V_{DD} = 3.0\text{ V}, -10\text{ }^\circ\text{C} \leq T_A \leq 70\text{ }^\circ\text{C}$ | -2 (2) | | 2 (2) | % |
| | | $V_{DD} = 3.0\text{ V}, -10\text{ }^\circ\text{C} \leq T_A \leq 85\text{ }^\circ\text{C}$ | -2.5 (2) | | 2 (2) | % |
| | | $V_{DD} = 3.0\text{ V}, -10\text{ }^\circ\text{C} \leq T_A \leq 125\text{ }^\circ\text{C}$ | -4.5 (2) | | 2 (2) | % |
| | | $1.65\text{ V} \leq V_{DD} \leq 3.6\text{ V}, -40\text{ }^\circ\text{C} \leq T_A \leq 125\text{ }^\circ\text{C}$ | -4.5 | | 3 | % |
| TRIM | HSI user trim resolution | $1.65\text{ V} \leq V_{DD} \leq 3.6\text{ V}, -40\text{ }^\circ\text{C} \leq T_A \leq 125\text{ }^\circ\text{C}$ | | ± 0.4 (2) | ± 0.5 (2) | % |
| $t_{su(HSI)}$ | HSI oscillator setup time (wakeup time) | | | 3.7 | 7.4 (2) | μs |
| $I_{DD(HSI)}$ | HSI oscillator power consumption | | | 100 | 140 (2) | μA |

- $V_{DD} = 3.0\text{ V}, T_A = -40\text{ to }125\text{ }^\circ\text{C}$ unless otherwise specified.
- Data based on characterization results, not tested in production.

Figure 19. Typical HSI frequency vs V_{DD}



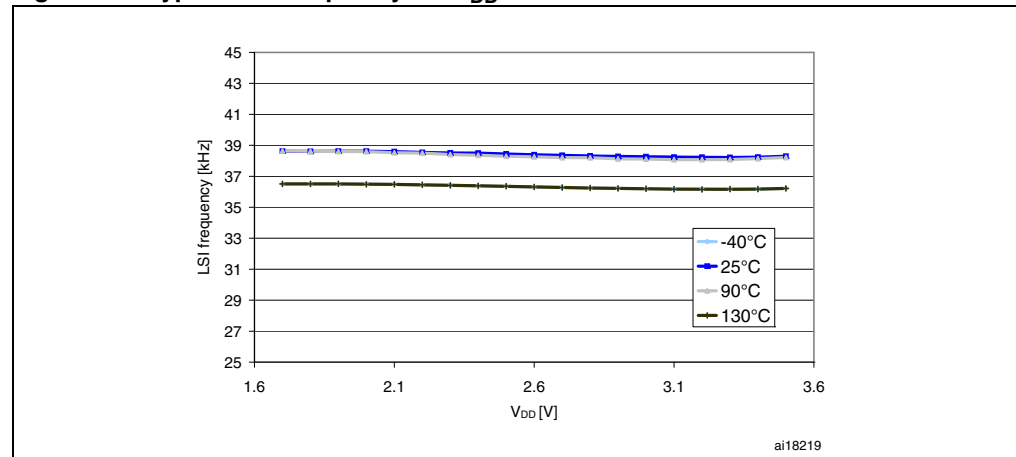
Low speed internal RC oscillator (LSI)

Table 33. LSI oscillator characteristics

| Symbol | Parameter (1) | Conditions(1) | Min | Typ | Max | Unit |
|---------------|-----------------------------------|--|-----|-----|--------|---------|
| f_{LSI} | Frequency | | 26 | 38 | 56 | kHz |
| $t_{su(LSI)}$ | LSI oscillator wakeup time | | | | 200(2) | μ s |
| $I_{DD(LSI)}$ | LSI oscillator frequency drift(3) | $0\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ | -10 | | 4 | % |

- $V_{DD} = 1.8\text{ V to }3.0\text{ V}$, $T_A = -40\text{ to }125\text{ }^{\circ}\text{C}$ unless otherwise specified.
- Data based on characterization results, not tested in production.
- This is a deviation for an individual part, once the initial frequency has been measured.

Figure 20. Typical LSI frequency vs. V_{DD}



9.3.5 Memory characteristics

$T_A = -40$ to 125 °C unless otherwise specified.

Table 34. RAM and hardware registers

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|------------------------------------|----------------------|-----|-----|-----|------|
| V_{RM} | Data retention mode ⁽¹⁾ | Halt mode (or Reset) | 1.4 | | | V |

1. Minimum supply voltage without losing data stored in RAM (in Halt mode or under Reset) or in hardware registers (only in Halt mode). Guaranteed by characterization, not tested in production.

Flash memory

Table 35. Flash program and data EEPROM memory

| Symbol | Parameter | Conditions | Min | Typ | Max (1) | Unit |
|------------|--|----------------------------------|---------------------------|-----|------------|---------|
| V_{DD} | Operating voltage (all modes, read/write/erase) | $f_{SYSCLK} = 16$ MHz | 1.65 | | 3.6 | V |
| t_{prog} | Programming time for 1 or 128 bytes (block) erase/write cycles (on programmed byte) | | | 6 | | ms |
| | Programming time for 1 to 128 bytes (block) write cycles (on erased byte) | | | 3 | | ms |
| I_{prog} | Programming/ erasing consumption | $T_A = +25$ °C, $V_{DD} = 3.0$ V | | 0.7 | | mA |
| | | $T_A = +25$ °C, $V_{DD} = 1.8$ V | | | | |
| t_{RET} | Data retention (program memory) after 10000 erase/write cycles at $T_A = +85$ °C | $T_{RET} = +55$ °C | 20 ⁽¹⁾ | | | years |
| | Data retention (data memory) after 10000 erase/write cycles at $T_A = +85$ °C | $T_{RET} = +55$ °C | 20 ⁽¹⁾ | | | |
| | Data retention (data memory) after 10000 erase/write cycles at $T_A = +85$ °C | $T_{RET} = +85$ °C | 1 ⁽¹⁾ | | | |
| N_{RW} | Erase/write cycles (program memory) | See notes ⁽¹⁾⁽²⁾ | 10 ⁽¹⁾ | | | kcycles |
| | Erase/write cycles (data memory) | See notes ⁽¹⁾⁽³⁾ | 300 ⁽¹⁾ (4) | | | |

1. Data based on characterization results, not tested in production.

2. Retention guaranteed after cycling is 10 years @ 55 °C.

3. Retention guaranteed after cycling is 1 year @ 55 °C.

4. Data based on characterization performed on the whole data memory.

9.3.6 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 36. I/O static characteristics

| Symbol | Parameter ⁽¹⁾ | Conditions ⁽¹⁾ | Min | Typ | Max | Unit |
|-------------------------|---|---|----------------------|-----|---------------------|------------|
| V_{IL} | Input low level voltage ⁽²⁾ | Input voltage on true open-drain pins (PC0 and PC1) | $V_{SS} - 0.3$ | | $0.3 \times V_{DD}$ | V |
| | | Input voltage on FT pins (PA7 and PE0) | $V_{SS} - 0.3$ | | $0.3 \times V_{DD}$ | |
| | | Input voltage on any other pin | $V_{SS} - 0.3$ | | $0.3 \times V_{DD}$ | |
| V_{IH} | Input high level voltage ⁽²⁾ | Input voltage on true open-drain pins (PC0 and PC1) with $V_{DD} < 2\text{ V}$ | $0.70 \times V_{DD}$ | | 5.2 | V |
| | | Input voltage on true open-drain pins (PC0 and PC1) with $V_{DD} \geq 2\text{ V}$ | | | 5.5 | |
| | | Input voltage on FT pins (PA7 and PE0) with $V_{DD} < 2\text{ V}$ | $0.70 \times V_{DD}$ | | 5.2 | |
| | | Input voltage on FT pins (PA7 and PE0) with $V_{DD} \geq 2\text{ V}$ | | | 5.5 | |
| | | Input voltage on any other pin | $0.70 \times V_{DD}$ | | $V_{DD} + 0.3$ | |
| V_{hys} | Schmitt trigger voltage hysteresis ⁽³⁾ | Standard I/Os | | 200 | | mV |
| | | True open drain I/Os | | 200 | | |
| I_{IKG} | Input leakage current ⁽⁴⁾ | $V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os | - | - | 50 ⁽⁵⁾ | nA |
| | | $V_{SS} \leq V_{IN} \leq V_{DD}$ True open drain I/Os | - | - | 200 ⁽⁵⁾ | |
| | | $V_{SS} \leq V_{IN} \leq V_{DD}$ PA0 with high sink LED driver capability | - | - | 200 ⁽⁵⁾ | |
| R_{PU} | Weak pull-up equivalent resistor ⁽⁶⁾ | $V_{IN} = V_{SS}$ | 30 | 45 | 60 | k Ω |
| C_{IO} ⁽⁷⁾ | I/O pin capacitance | | | 5 | | pF |

1. $V_{DD} = 3.0\text{ V}$, $T_A = -40$ to $125\text{ }^\circ\text{C}$ unless otherwise specified.

2. Data based on characterization results, not tested in production.
3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
4. The max. value may be exceeded if negative current is injected on adjacent pins.
5. Not tested in production.
6. R_{PU} pull-up equivalent resistor based on a resistive transistor (corresponding I_{PU} current characteristics described in [Figure 24](#)).
7. Data guaranteed by Design, not tested in production.

Figure 21. Typical V_{IL} and V_{IH} vs V_{DD} (standard I/Os)

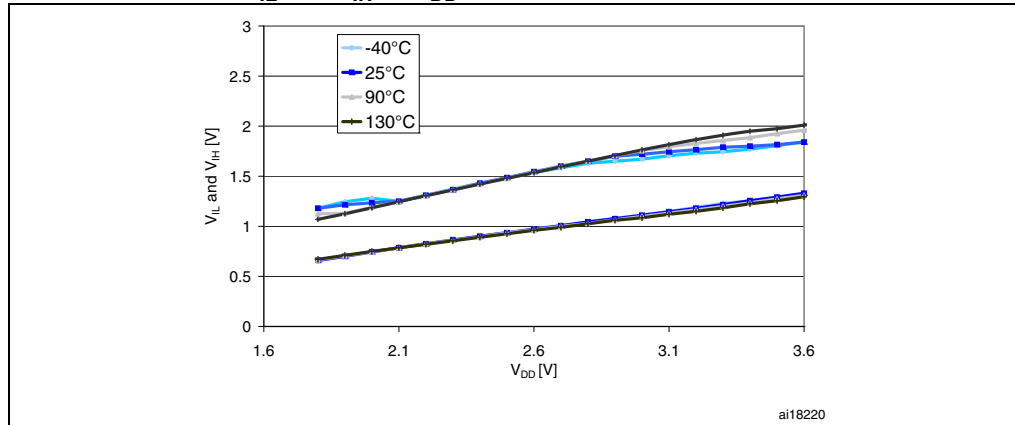


Figure 22. Typical V_{IL} and V_{IH} vs V_{DD} (true open drain I/Os)

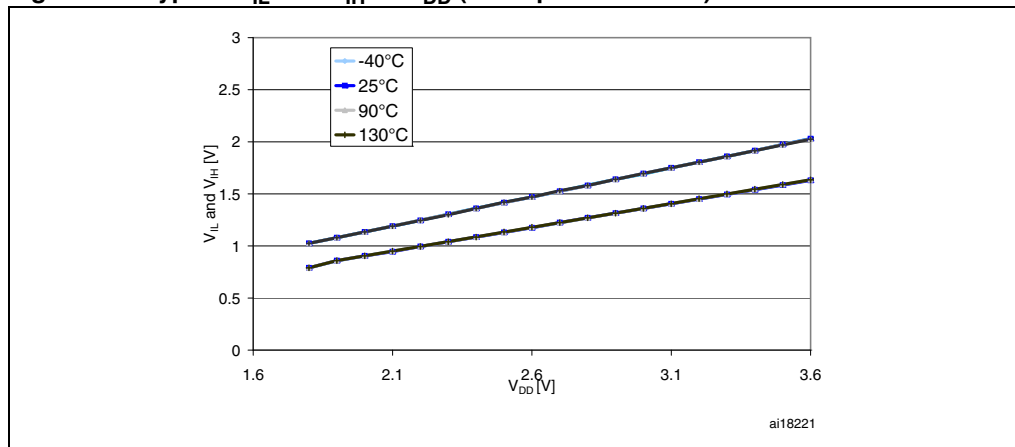


Figure 23. Typical pull-up resistance R_{PU} vs V_{DD} with $V_{IN}=V_{SS}$

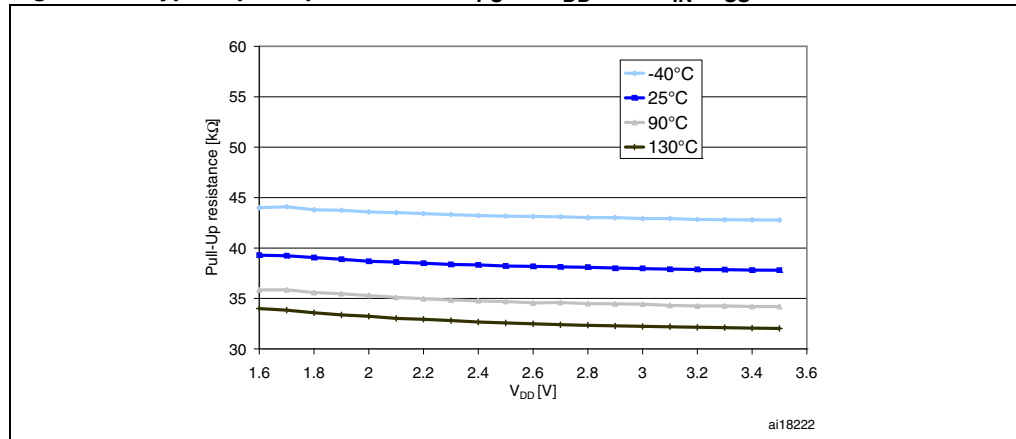
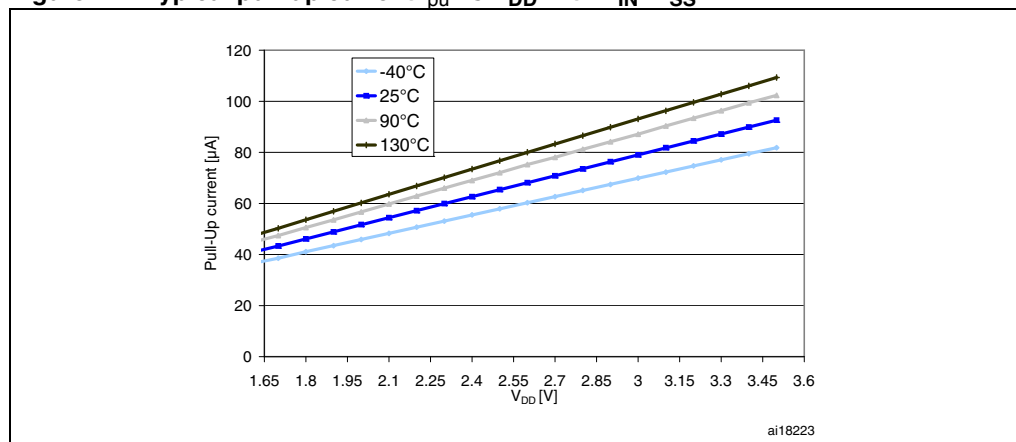


Figure 24. Typical pull-up current I_{PU} vs V_{DD} with $V_{IN}=V_{SS}$



Output driving current

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 37. Output driving current (standard ports)

| I/O Type | Symbol | Parameter | Conditions | Min | Max | Unit |
|----------|----------------|--|---|---------------|------|------|
| Standard | $V_{OL}^{(1)}$ | Output low level voltage for an I/O pin | $I_{IO} = +2 \text{ mA}$, $V_{DD} = 3.0 \text{ V}$ | | 0.45 | V |
| | | | $I_{IO} = +2 \text{ mA}$, $V_{DD} = 1.8 \text{ V}$ | | 0.45 | V |
| | | | $I_{IO} = +10 \text{ mA}$, $V_{DD} = 3.0 \text{ V}$ | | 0.7 | V |
| | $V_{OH}^{(2)}$ | Output high level voltage for an I/O pin | $I_{IO} = -2 \text{ mA}$, $V_{DD} = 3.0 \text{ V}$ | $V_{DD}-0.45$ | | V |
| | | | $I_{IO} = -1 \text{ mA}$, $V_{DD} = 1.8 \text{ V}$ | $V_{DD}-0.45$ | | V |
| | | | $I_{IO} = -10 \text{ mA}$, $V_{DD} = 3.0 \text{ V}$ | $V_{DD}-0.7$ | | V |

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in [Table 15](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in [Table 15](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD} .

Table 38. Output driving current (true open drain ports)

| I/O Type | Symbol | Parameter | Conditions | Min | Max | Unit |
|------------|----------------|---|--|-----|------|------|
| Open drain | $V_{OL}^{(1)}$ | Output low level voltage for an I/O pin | $I_{IO} = +3 \text{ mA}$, $V_{DD} = 3.0 \text{ V}$ | | 0.45 | V |
| | | | $I_{IO} = +1 \text{ mA}$, $V_{DD} = 1.8 \text{ V}$ | | 0.45 | |

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in [Table 15](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .

Table 39. Output driving current (PA0 with high sink LED driver capability)

| I/O Type | Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------------|----------------|---|---|-----|------|------|
| $\overline{\text{PE}}$ | $V_{OL}^{(1)}$ | Output low level voltage for an I/O pin | $I_{IO} = +20 \text{ mA}$, $V_{DD} = 2.0 \text{ V}$ | | 0.45 | V |

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in [Table 15](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .

Figure 25. Typ. V_{OL} @ $V_{DD} = 3.0$ V (standard ports)

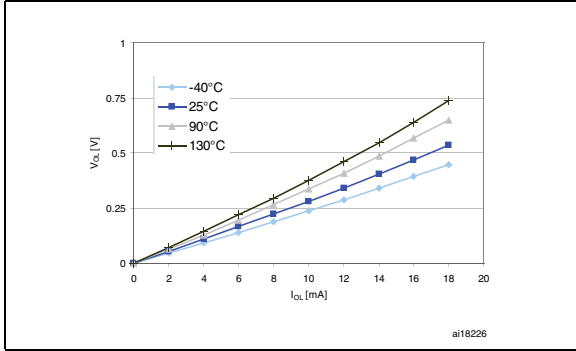


Figure 26. Typ. V_{OL} @ $V_{DD} = 1.8$ V (standard ports)

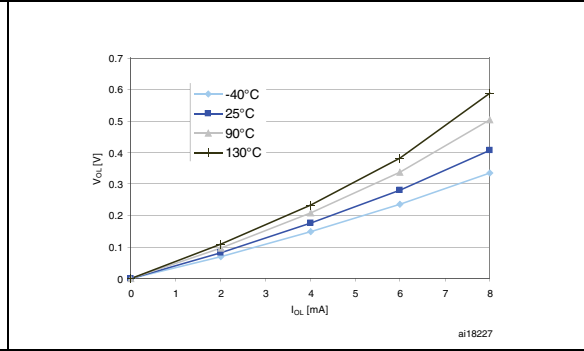


Figure 27. Typ. V_{OL} @ $V_{DD} = 3.0$ V (true open drain ports)

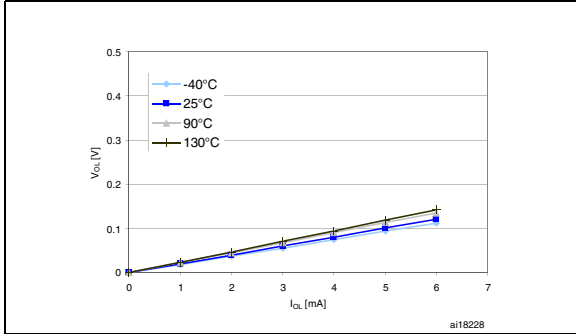


Figure 28. Typ. V_{OL} @ $V_{DD} = 1.8$ V (true open drain ports)

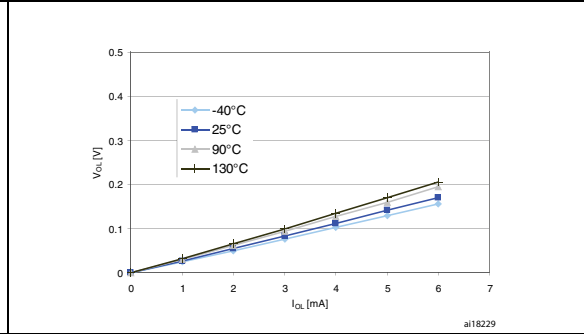


Figure 29. Typ. $V_{DD} - V_{OH}$ @ $V_{DD} = 3.0$ V (standard ports)

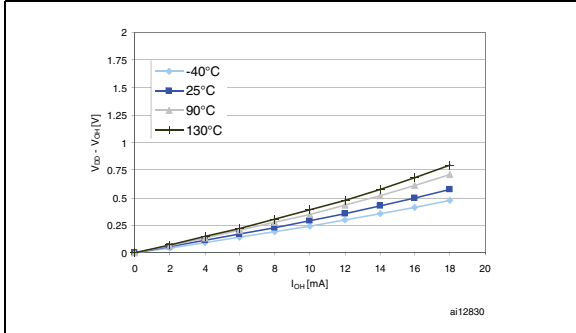
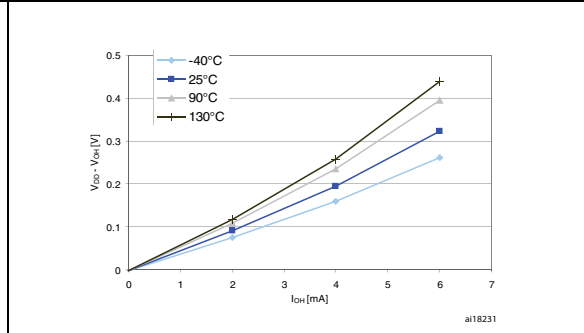


Figure 30. Typ. $V_{DD} - V_{OH}$ @ $V_{DD} = 1.8$ V (standard ports)



NRST pin

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 40. NRST pin characteristics

| Symbol | Parameter | Conditions | Min | Typ ⁽¹⁾ | Max | Unit |
|----------------|--|--|---------------------|--------------------|----------|------------|
| $V_{IL(NRST)}$ | NRST input low level voltage ⁽¹⁾ | | V_{SS} | | 0.8 | V |
| $V_{IH(NRST)}$ | NRST input high level voltage ⁽¹⁾ | | 1.4 | | V_{DD} | |
| $V_{OL(NRST)}$ | NRST output low level voltage | $I_{OL} = 2 \text{ mA}$ for $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$ $I_{OL} = 1.5 \text{ mA}$ for $V_{DD} < 2.7 \text{ V}$ | | | 0.4 | |
| V_{HYST} | NRST input hysteresis ⁽³⁾ | | $10\%V_{DD}$ (2) | | | mV |
| $R_{PU(NRST)}$ | NRST pull-up equivalent resistor | | 30 | 45 | 60 | k Ω |
| $V_{F(NRST)}$ | NRST input filtered pulse ⁽³⁾ | | | | 50 | ns |
| $V_{NF(NRST)}$ | NRST input not filtered pulse ⁽³⁾ | | 300 | | | |

1. Data based on characterization results, not tested in production.

2. 200 mV min.

3. Data guaranteed by design, not tested in production.

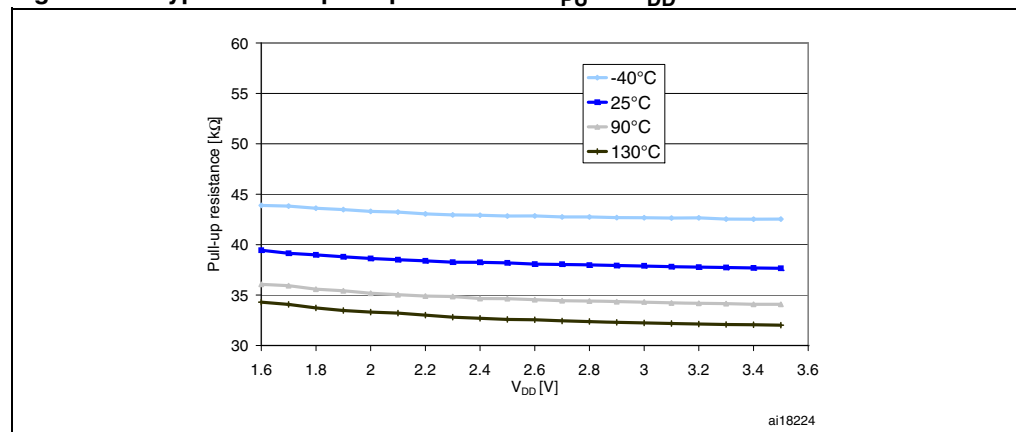
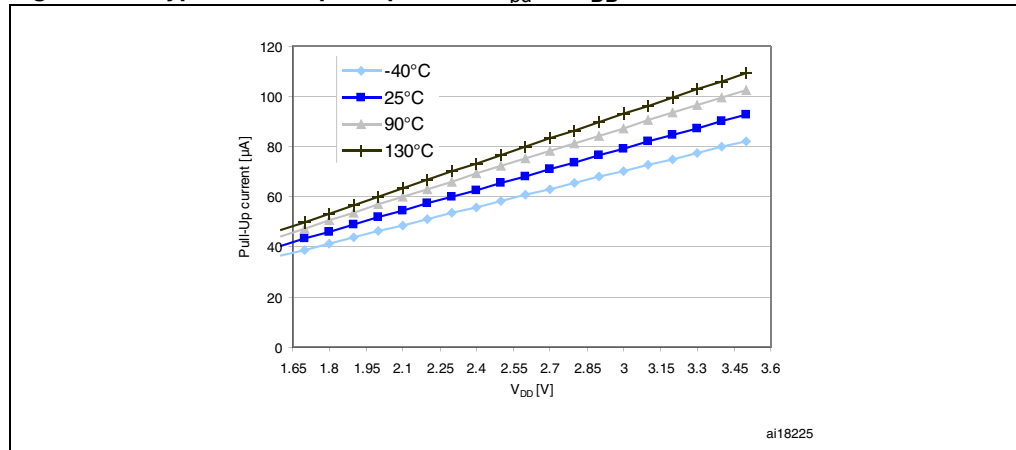
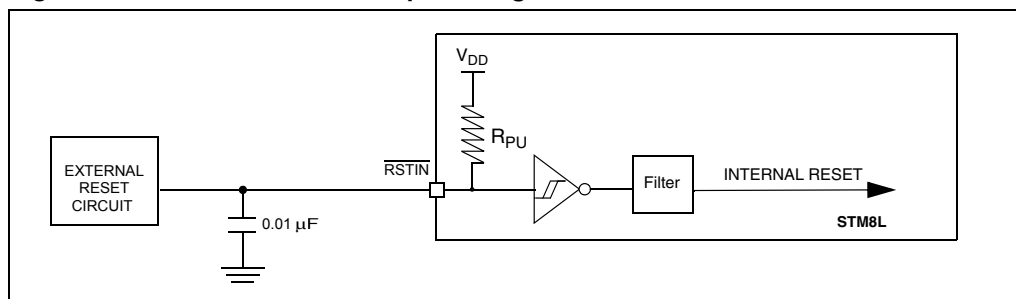
Figure 31. Typical NRST pull-up resistance R_{PU} vs V_{DD} 

Figure 32. Typical NRST pull-up current I_{DU} vs V_{DD}



The reset network shown in [Figure 33](#) protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below the V_{IL} max. level specified in [Table 40](#). Otherwise the reset is not taken into account internally.

Figure 33. Recommended NRST pin configuration



9.3.7 Communication interfaces

SPI1 - Serial peripheral interface

Unless otherwise specified, the parameters given in [Table 41](#) are derived from tests performed under ambient temperature, f_{SYSCLK} frequency and V_{DD} supply voltage conditions summarized in [Section 9.3.1](#). Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 41. SPI1 characteristics

| Symbol | Parameter | Conditions ⁽¹⁾ | Min | Max | Unit |
|--|-------------------------------|--|--------------------------------|--------------------------------|------|
| f_{SCK} $1/t_{\text{c(SCK)}}$ | SPI1 clock frequency | Master mode | 0 | 8 | MHz |
| | | Slave mode | 0 | 8 | |
| $t_{\text{r(SCK)}}$ $t_{\text{f(SCK)}}$ | SPI1 clock rise and fall time | Capacitive load: C = 30 pF | - | 30 | ns |
| $t_{\text{su(NSS)}}^{(2)}$ | NSS setup time | Slave mode | $4 \times 1/f_{\text{SYSCLK}}$ | - | |
| $t_{\text{h(NSS)}}^{(2)}$ | NSS hold time | Slave mode | 80 | - | |
| $t_{\text{w(SCKH)}}^{(2)}$ $t_{\text{w(SCKL)}}^{(2)}$ | SCK high and low time | Master mode, $f_{\text{MASTER}} = 8 \text{ MHz}$, $f_{\text{SCK}} = 4 \text{ MHz}$ | 105 | 145 | |
| $t_{\text{su(MI)}}^{(2)}$ $t_{\text{su(SI)}}^{(2)}$ | Data input setup time | Master mode | 30 | - | |
| | | Slave mode | 3 | - | |
| $t_{\text{h(MI)}}^{(2)}$ $t_{\text{h(SI)}}^{(2)}$ | Data input hold time | Master mode | 15 | - | |
| | | Slave mode | 0 | - | |
| $t_{\text{a(SO)}}^{(2)(3)}$ | Data output access time | Slave mode | - | $3 \times 1/f_{\text{SYSCLK}}$ | |
| $t_{\text{dis(SO)}}^{(2)(4)}$ | Data output disable time | Slave mode | 30 | - | |
| $t_{\text{v(SO)}}^{(2)}$ | Data output valid time | Slave mode (after enable edge) | - | 60 | |
| $t_{\text{v(MO)}}^{(2)}$ | Data output valid time | Master mode (after enable edge) | - | 20 | |
| $t_{\text{h(SO)}}^{(2)}$ $t_{\text{h(MO)}}^{(2)}$ | Data output hold time | Slave mode (after enable edge) | 15 | - | |
| | | Master mode (after enable edge) | 1 | - | |

- Parameters are given by selecting 10 MHz I/O output frequency.
- Values based on design simulation and/or characterization results, and not tested in production.
- Min time is for the minimum time to drive the output and max time is for the maximum time to validate the data.
- Min time is for the minimum time to invalidate the output and max time is for the maximum time to put the data in Hi-Z.

Figure 34. SPI1 timing diagram - slave mode and CPHA=0

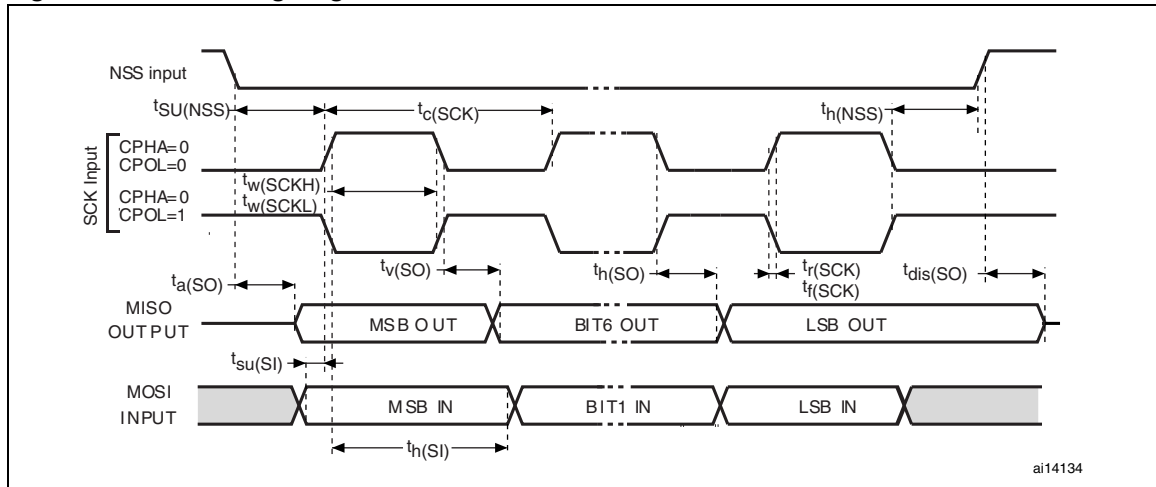
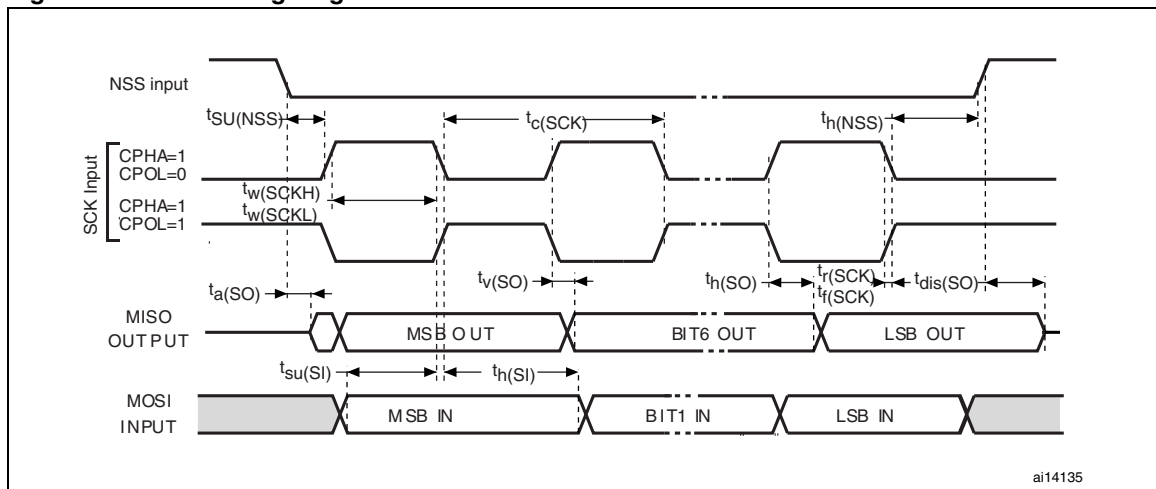
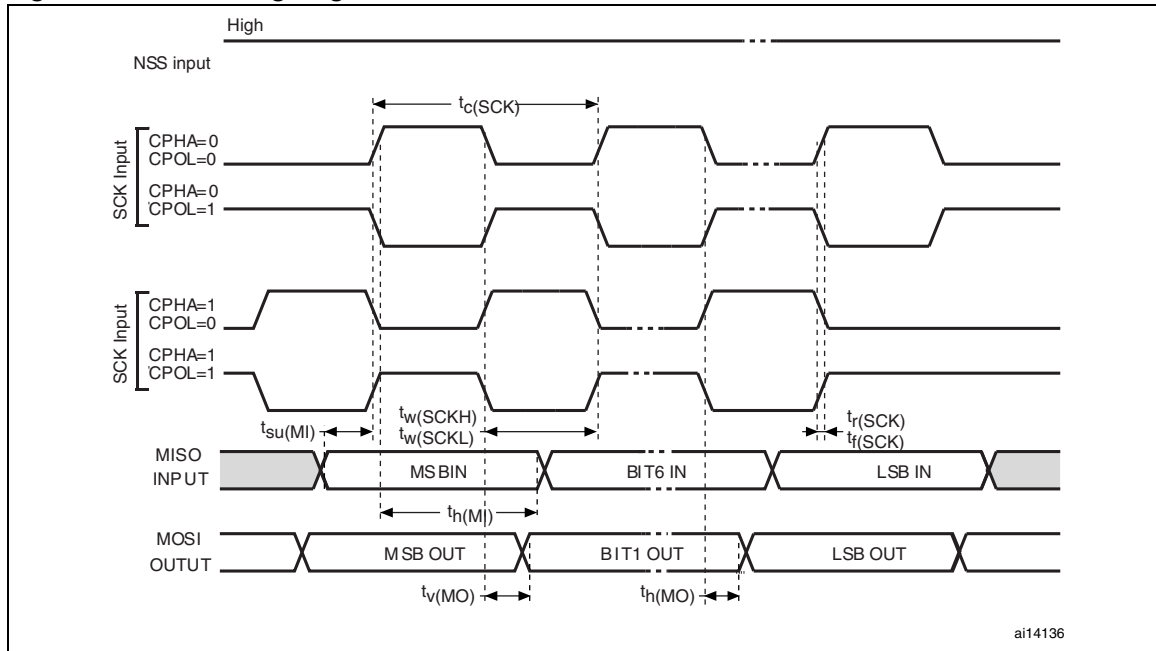


Figure 35. SPI1 timing diagram - slave mode and CPHA=1⁽¹⁾



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 36. SPI1 timing diagram - master mode⁽¹⁾



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

I²C - Inter IC control interface

Subject to general operating conditions for V_{DD} , f_{SYSCLK} , and T_A unless otherwise specified.

The STM8L I²C interface (I2C1) meets the requirements of the Standard I²C communication protocol described in the following table with the restriction mentioned below:

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (SDA and SCL).

Table 42. I2C characteristics

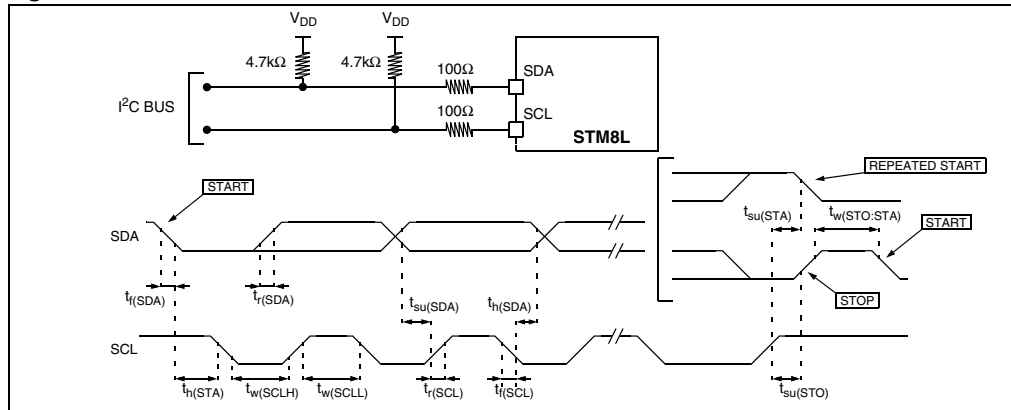
| Symbol | Parameter | Standard mode I ² C | | Fast mode I ² C ⁽¹⁾ | | Unit |
|--------------------------|---|--------------------------------|--------------------|---|--------------------|---------|
| | | Min ⁽²⁾ | Max ⁽²⁾ | Min ⁽²⁾ | Max ⁽²⁾ | |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | | 1.3 | | μ s |
| $t_{w(SCLH)}$ | SCL clock high time | 4.0 | | 0.6 | | |
| $t_{su(SDA)}$ | SDA setup time | 250 | | 100 | | ns |
| $t_h(SDA)$ | SDA data hold time | 0 | | 0 | 900 | |
| $t_r(SDA)$ $t_r(SCL)$ | SDA and SCL rise time | | 1000 | | 300 | |
| $t_f(SDA)$ $t_f(SCL)$ | SDA and SCL fall time | | 300 | | 300 | |
| $t_h(STA)$ | START condition hold time | 4.0 | | 0.6 | | μ s |
| $t_{su(STA)}$ | Repeated START condition setup time | 4.7 | | 0.6 | | |
| $t_{su(STO)}$ | STOP condition setup time | 4.0 | | 0.6 | | μ s |
| $t_w(STO:STA)$ | STOP to START condition time (bus free) | 4.7 | | 1.3 | | μ s |
| C_b | Capacitive load for each bus line | | 400 | | 400 | pF |

1. f_{SYSCLK} must be at least equal to 8 MHz to achieve max fast I²C speed (400 kHz).

2. Data based on standard I²C protocol requirement, not tested in production.

Note: *For speeds around 200 kHz, the achieved speed can have a $\pm 5\%$ tolerance
For other speed ranges, the achieved speed can have a $\pm 2\%$ tolerance
The above variations depend on the accuracy of the external components used.*

Figure 37. Typical application with I²C bus and timing diagram ¹⁾



1. Measurement points are done at CMOS levels: $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$

9.3.8 LCD controller (STM8L152xx only)

Table 43. LCD characteristics⁽¹⁾

| Symbol | Parameter | Min | Typ | Max. | Unit |
|----------------------------------|---|-----|---------------|------------|------------|
| V_{LCD} | LCD external voltage | | | 3.6 | V |
| V_{LCD0} | LCD internal reference voltage 0 | | 2.6 | | V |
| V_{LCD1} | LCD internal reference voltage 1 | | 2.7 | | V |
| V_{LCD2} | LCD internal reference voltage 2 | | 2.8 | | V |
| V_{LCD3} | LCD internal reference voltage 3 | | 2.9 | | V |
| V_{LCD4} | LCD internal reference voltage 4 | | 3.0 | | V |
| V_{LCD5} | LCD internal reference voltage 5 | | 3.1 | | V |
| V_{LCD6} | LCD internal reference voltage 6 | | 3.2 | | V |
| V_{LCD7} | LCD internal reference voltage 7 | | 3.3 | | V |
| C_{EXT} | V_{LCD} external capacitance | 0.1 | | 2 | μF |
| I_{DD} | Supply current ⁽²⁾ at $V_{DD} = 1.8$ V | | 3 | | μA |
| | Supply current ⁽²⁾ at $V_{DD} = 3$ V | | 3 | | μA |
| $R_{HN}^{(3)}$ (= 3 X R_H) | Low drive resistive network | | 6.6 | | M Ω |
| $R_{LN}^{(4)}$ (= 3 X R_L) | High drive resistive network | | 360 | | k Ω |
| V_{33} | Segment/Common higher level voltage | | | V_{LCDx} | V |
| V_{23} | Segment/Common 2/3 level voltage | | $2/3V_{LCDx}$ | | V |
| V_{12} | Segment/Common 1/2 level voltage | | $1/2V_{LCDx}$ | | V |
| V_{13} | Segment/Common 1/3 level voltage | | $1/3V_{LCDx}$ | | V |
| V_0 | Segment/Common lowest level voltage | 0 | | | V |

1. Data guaranteed by Design, not tested in production.
2. LCD enabled with 3 V internal booster (LCD_CR1 = 0x08), 1/4 duty, 1/3 bias, division ratio= 64, all pixels active, no LCD connected.
3. R_{HN} is the total resistive network value. The bridge is made of 3 R_H serial resistors.
4. R_{LN} is the total resistive network value. The bridge is made of 3 R_L serial resistors.

VLCD external capacitor (STM8L152xx only)

The application can achieve a stabilized LCD reference voltage by connecting an external capacitor C_{EXT} to the V_{LCD} pin. C_{EXT} is specified in [Table 43](#).

9.3.9 Embedded reference voltage

Based on characterization results, unless otherwise specified.

Table 44. Reference voltage characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max. | Unit |
|--------------------|--|---|-------|-------|---------|-------------------------|
| I_{REFINT} | Internal reference voltage consumption | | | 1.4 | | μA |
| $T_{S_VREFINT}$ | ADC sampling time when reading the internal reference voltage ⁽¹⁾ | | | 5 | 10 | μs |
| I_{BUF} | Internal reference voltage buffer consumption (used for ADC) | | | 13.5 | 25 | μA |
| V_{REFINT_out} | Reference voltage output | | 1.202 | 1.224 | 1.242 | V |
| V_{REFINT_DIV1} | 1/4 reference voltage | | | 25 | | % V_{REFINT_COMP} |
| V_{REFINT_DIV2} | 1/2 reference voltage | | | 50 | | |
| V_{REFINT_DIV3} | 3/4 reference voltage | | | 75 | | |
| I_{LPBUF} | Internal reference voltage low power buffer consumption (used for comparators or output) | | | 730 | 1200 | nA |
| I_{REFOUT} | Buffer output current ⁽²⁾ | | | | 1 | μA |
| C_{REFOUT} | Reference voltage output load | | | | 50 | pF |
| $t_{VREFINT}$ | Internal reference voltage startup time | | | 2 | 3 | ms |
| t_{BUFEN} | Internal reference voltage buffer startup time once enabled ⁽¹⁾ | | | | 10 | μs |
| $ACC_{VREFINT}$ | Accuracy of V_{REFINT} stored in the $V_{REFINT_Factory_CONV}$ byte ⁽³⁾ | | | | ± 5 | mV |
| $STAB_{VREFINT}$ | Stability of V_{REFINT} over temperature | $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$ | | 20 | 50 | ppm/ $^{\circ}\text{C}$ |
| | Stability of V_{REFINT} over temperature | $0\text{ }^{\circ}\text{C} \leq T_A \leq 50\text{ }^{\circ}\text{C}$ | | | 20 | ppm/ $^{\circ}\text{C}$ |
| $STAB_{VREFINT}$ | Stability of V_{REFINT} after 1000 hours | | | | TBD | ppm |

1. Defined when ADC output reaches its final value $\pm 1/2\text{LSB}$

2. To guaranty less than 1% V_{REFOUT} deviation

3. Measured at $V_{DD} = 3\text{ V} \pm 10\text{ mV}$. This value takes into account V_{DD} accuracy and ADC conversion accuracy.

9.3.10 Temperature sensor

Based on characterization results, unless otherwise specified.

Table 45. TS characteristics

| Symbol | Parameter | Min | Typ | Max. | Unit |
|------------------------------|---|-------|---------|---------|------------------------------|
| V_{90} | Sensor reference voltage at $90^{\circ}\text{C} \pm 5^{\circ}\text{C}$, (1) | 0.580 | 0.597 | 0.614 | V |
| T_L | V_{SENSOR} linearity with temperature | | ± 1 | ± 2 | $^{\circ}\text{C}$ |
| Avg_slope | Average slope ⁽²⁾ | 1.59 | 1.62 | 1.65 | $\text{mV}/^{\circ}\text{C}$ |
| $\text{IDD}_{(\text{TEMP})}$ | Consumption | | 3.4 | 6 | μA |
| $T_{\text{START}}^{(2)}$ | Temperature sensor startup time ⁽³⁾ | | | 10 | μs |
| $T_{\text{S_TEMP}}^{(2)}$ | ADC sampling time when reading the temperature sensor | | 5 | 10 | μs |

1. Measured at $V_{\text{DD}} = 3\text{ V} \pm 10\text{ mV}$. The 8 LSB of the V_{90} ADC conversion result are stored in the TS_Factory_CONV_V90 byte.

2. Guaranteed by Design, not tested in production.

3. Defined for ADC output reaching its final value $\pm 1/2\text{LSB}$.

9.3.11 Comparator characteristics

Data guaranteed by design, not tested in production.

Table 46. Comparator 1 characteristics

| Symbol | Parameter | Min | Typ | Max | Unit |
|---------------------|---|-------|-------|------------------|--------------------|
| V_{DDA} | Analog supply voltage | 1.65 | | 3.6 | V |
| T_A | Temperature range | -40 | | 125 | $^{\circ}\text{C}$ |
| R_{400} | R_{400} value | 300 | 400 | 500 | $\text{k}\Omega$ |
| R_{10} | R_{10} value | 7.5 | 10 | 12.5 | $\text{k}\Omega$ |
| V_{IN} | Comparator input voltage range | 0.6 | | V_{DDA} | V |
| V_{REFINT} | Internal reference voltage ⁽¹⁾ | 1.202 | 1.225 | 1.242 | V |
| t_{START} | Startup time after enable | | 7 | 10 | μs |
| t_d | Propagation delay ⁽²⁾ | | 3 | 10 | μs |
| V_{offset} | Comparator offset error | | | ± 10 | mV |
| I_{CMP1} | Consumption ⁽³⁾ | | 160 | 260 | nA |

1. Based on characterization results.

2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.

3. Comparator consumption only. Internal reference voltage not included.

Data guaranteed by design, not tested in production.

Table 47. Comparator 2 characteristics

| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------------|---|------|-----|-----------|------|
| V_{DDA} | Analog supply voltage | 1.65 | | 3.6 | V |
| T_A | Temperature range | -40 | | 125 | °C |
| V_{IN} | Comparator input voltage range | 0 | | V_{DDA} | V |
| t_{START} | Startup time after enable in fast mode | | | 20 | μs |
| | Startup time after enable in slow mode | | | 30 | μs |
| t_{df} | Propagation delay in fast mode ⁽¹⁾ | | | 2.5 | μs |
| t_{ds} | Propagation delay in slow mode ⁽¹⁾ | | | 6 | μs |
| V_{offset} | Comparator offset error | | | ±10 | mV |
| $I_{DD(CMP2F)}$ | Consumption in fast mode | | | 5 | μA |
| $I_{DD(CMP2S)}$ | Consumption in slow mode | | | 2 | μA |

1. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.

9.3.12 12-bit DAC characteristics

Data guaranteed by design, not tested in production.

Table 48. DAC characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|--|--|-----|-----|----------------------------|------|
| V_{DDA} | Analog supply voltage | | 1.8 | | 3.6 | V |
| T_A | Temperature range | | -40 | | 125 | °C |
| $I_{DD(DAC)}^{(1)}$ | DAC supply current | Middle code | | 370 | 550 | μA |
| | | Worst code | | 500 | 700 | |
| I_{VREF+} | Current on V_{REF+} supply | | | 140 | 360 | μA |
| R_L | Resistive load ^{(2) (3)} | DACOUT buffer ON | 5 | | | kΩ |
| R_O | Output impedance | DACOUT buffer OFF | | 8 | 10 | kΩ |
| C_L | Capacitive load ⁽⁴⁾ | | | | 50 | pF |
| DAC_OUT | DAC_OUT voltage ⁽⁵⁾ | DACOUT buffer ON | 0.2 | | $V_{REF+}-0.2$ | V |
| | | DACOUT buffer OFF | 0 | | $V_{REF+} - 1 \text{ LSB}$ | V |
| $t_{settling}$ | Settling time (full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches the final value ±1LSB) | $R_L \geq 5 \text{ k}\Omega, C_L \leq 50 \text{ pF}$ | | 7 | 12 | μs |
| Update rate | Max frequency for a correct DAC_OUT (@95%) change when small variation of the input code (from code i to i+1LSB). | $R_L \geq 5 \text{ k}\Omega, C_L \leq 50 \text{ pF}$ | | | 1 | MspS |

Table 48. DAC characteristics (continued)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------|---|---|-----|-----|-----|---------------|
| t_{WAKEUP} | Wakeup time from OFF state. Input code between lowest and highest possible codes. | $R_L \geq 5 \text{ k}\Omega$, $C_L \leq 50 \text{ pF}$ | | 9 | 15 | μs |
| PSRR+ | Power supply rejection ratio (to V_{DDA}) (static DC measurement) | $R_L \geq 5 \text{ k}\Omega$, $C_L \leq 50 \text{ pF}$ | | -60 | -35 | dB |

1. Includes supply current on V_{DDA} and V_{REF+}
2. Resistive load between DACOUT and GNDA
3. Output on PF0 (48-pin package only)
4. Capacitive load at DACOUT pin
5. It gives the output excursion of the DAC

Data based on characterization results, not tested in production.

Table 49. DAC accuracy

| Symbol | Parameter | Conditions | Typ | Max | Unit |
|------------|---|--|-----------|-----------|---------------|
| DNL | Differential non linearity ⁽¹⁾ | $R_L \geq 5 \text{ k}\Omega$, $C_L \leq 50 \text{ pF}$ DACOUT buffer ON ⁽²⁾ | 1.5 | 3 | 12-bit LSB |
| | | No load DACOUT buffer OFF | 1.5 | 3 | |
| INL | Integral non linearity ⁽³⁾ | $R_L \geq 5 \text{ k}\Omega$, $C_L \leq 50 \text{ pF}$ DACOUT buffer ON ⁽²⁾ | 2 | 4 | |
| | | No load DACOUT buffer OFF | 2 | 4 | |
| Offset | Offset error ⁽⁴⁾ | $R_L \geq 5 \text{ k}\Omega$, $C_L \leq 50 \text{ pF}$ DACOUT buffer ON ⁽²⁾ | ± 10 | ± 25 | |
| | | No load DACOUT buffer OFF | ± 5 | ± 8 | |
| Offset1 | Offset error at Code 1 ⁽⁵⁾ | DACOUT buffer OFF | ± 1.5 | ± 5 | |
| Gain error | Gain error | $R_L \geq 5 \text{ k}\Omega$, $C_L \leq 50 \text{ pF}$ DACOUT buffer ON ⁽²⁾ | ± 0.2 | ± 0.5 | % |
| | | No load DACOUT buffer OFF | ± 0.3 | ± 0.5 | |
| TUE | Total unadjusted error | $R_L \geq 5 \text{ k}\Omega$, $C_L \leq 50 \text{ pF}$ DACOUT buffer ON ⁽²⁾ | 12 | 30 | 12-bit LSB |
| | | No load DACOUT buffer OFF | 8 | 12 | |

1. Difference between two consecutive codes - 1 LSB.
2. For 48-pin packages only. For 28-pin and 32-pin packages, DAC output buffer must be kept off and no load must be applied.
3. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023.
4. Difference between measured value and ideal value = $V_{REF}/2$.

5. Difference between measured value and ideal value Code 1.

Table 50. DAC output on PB4-PB5-PB6⁽¹⁾

| Symbol | Parameter | Conditions | Max | Unit |
|-----------|---|--|-----|------------|
| R_{int} | Internal resistance between DAC output and PB4-PB5-PB6 output | $2.7\text{ V} < V_{DD} < 3.6\text{ V}$ | 1.4 | k Ω |
| | | $2.4\text{ V} < V_{DD} < 3.6\text{ V}$ | 1.6 | |
| | | $2.0\text{ V} < V_{DD} < 3.6\text{ V}$ | 3.2 | |
| | | $1.8\text{ V} < V_{DD} < 3.6\text{ V}$ | 8.2 | |

1. 32 or 28-pin packages only. The DAC channel can be routed either on PB4, PB5 or PB6 using the routing interface I/O switch registers.

12-bit ADC1 characteristics

Table 51. ADC1 characteristics

| Symbol | Parameter ⁽¹⁾ | Conditions | Min ⁽¹⁾ | Typ ⁽¹⁾ | Max ⁽¹⁾ | Unit |
|-------------|-------------------------------------|---|--------------------|--------------------|------------------------------|--------------------|
| V_{DDA} | Analog supply voltage | | 1.8 | | 3.6 | V |
| V_{REF+} | Reference supply voltage | $2.4\text{ V} \leq V_{DDA} \leq 3.6\text{ V}$ | 2.4 | | V_{DDA} | V |
| | | $1.8\text{ V} \leq V_{DDA} \leq 2.4\text{ V}$ | | | V_{DDA} | V |
| V_{REF-} | Lower reference voltage | | | | V_{SSA} | V |
| I_{VDDA} | Current on the V_{DDA} input pin | | | 1000 | 1450 | μA |
| I_{VREF+} | Current on the V_{REF+} input pin | | | 400 | 700 (peak) ⁽²⁾ | μA |
| | | | | | 450 (average) ⁽²⁾ | μA |
| V_{AIN} | Conversion voltage range | | 0 ⁽³⁾ | | V_{REF+} | |
| T_A | Temperature range | | -40 | | 125 | $^{\circ}\text{C}$ |
| R_{AIN} | External resistance on V_{AIN} | on PF0 fast channel | | | 50 ⁽⁴⁾ | k Ω |
| | | on all other channels | | | | |
| C_{ADC} | Internal sample and hold capacitor | on PF0 fast channel | | 16 | | pF |
| | | on all other channels | | | | |
| f_{ADC} | ADC sampling clock frequency | $2.4\text{ V} \leq V_{DDA} \leq 3.6\text{ V}$ without zooming | 0.320 | | 16 | MHz |
| | | $1.8\text{ V} \leq V_{DDA} \leq 2.4\text{ V}$ with zooming | 0.320 | | 8 | MHz |

Table 51. ADC1 characteristics (continued)

| Symbol | Parameter ⁽¹⁾ | Conditions | Min ⁽¹⁾ | Typ ⁽¹⁾ | Max ⁽¹⁾ | Unit |
|----------------------------------|---|--|------------------------|--------------------|-----------------------------------|-----------------------|
| f _{CONV} | 12-bit conversion rate | V _{AIN} on PF0 fast channel | | | 1 ⁽⁴⁾⁽⁵⁾ | MHz |
| | | V _{AIN} on all other channels | | | 760 ⁽⁴⁾⁽⁵⁾ | kHz |
| f _{TRIG} | External trigger frequency | | | | t _{conv} | 1/f _{ADC} |
| t _{LAT} | External trigger latency | | | | 3.5 | 1/f _{SYSCLK} |
| t _S | Sampling time | V _{AIN} on PF0 fast channel V _{DDA} < 2.4 V | 0.43 ⁽⁴⁾⁽⁵⁾ | | | μs |
| | | V _{AIN} on PF0 fast channel 2.4 V ≤ V _{DDA} ≤ 3.6 V | 0.22 ⁽⁴⁾⁽⁵⁾ | | | μs |
| | | V _{AIN} on slow channels V _{DDA} < 2.4 V | 0.86 ⁽⁴⁾⁽⁵⁾ | | | μs |
| | | V _{AIN} on slow channels 2.4 V ≤ V _{DDA} ≤ 3.6 V | 0.41 ⁽⁴⁾⁽⁵⁾ | | | μs |
| t _{conv} | 12-bit conversion time | | | | 12 + t _S | 1/f _{ADC} |
| | | 16 MHz | | | 1 ⁽⁴⁾ | μs |
| t _{WKUP} | Wakeup time from OFF state | | | | 3 | μs |
| t _{IDLE} ⁽⁶⁾ | Time before a new conversion | T _A = +25 °C | | | 1 | s |
| | | T _A = +70 °C | | | 20 | ms |
| | | T _A = +125 °C | | | 2 | ms |
| t _{VREFINT} | Internal reference voltage startup time | | | | refer to Table 44 | ms |

1. Data guaranteed by design, not tested in production.
2. The current consumption through V_{REF} is composed of two parameters:
 - one constant (max 300 μA)
 - one variable (max 400 μA), only during sampling time + 2 first conversion pulses.
 So, peak consumption is 300+400 = 700 μA and average consumption is 300 + [(4 sampling + 2) / 16] x 400 = 450 μA at 1Msps
3. V_{REF} or V_{DDA} must be tied to ground.
4. Minimum sampling and conversion time is reached for maximum R_{ext} = 0.5 kΩ.
5. Value obtained for continuous conversion on fast channel.
6. The time between 2 conversions, or between ADC ON and the first conversion must be lower than t_{IDLE}.

Table 52. ADC1 accuracy with $V_{DDA} = 3.3\text{ V to }2.5\text{ V}$

| Symbol | Parameter | Conditions | Typ | Max ⁽¹⁾ | Unit |
|--------|----------------------------|----------------------------------|-----|--------------------|------|
| DNL | Differential non linearity | $f_{\text{ADC}} = 16\text{ MHz}$ | 1 | 1.6 | LSB |
| | | $f_{\text{ADC}} = 8\text{ MHz}$ | 1 | 1.6 | |
| | | $f_{\text{ADC}} = 4\text{ MHz}$ | 1 | 1.5 | |
| INL | Integral non linearity | $f_{\text{ADC}} = 16\text{ MHz}$ | 1.2 | 2 | |
| | | $f_{\text{ADC}} = 8\text{ MHz}$ | 1.2 | 1.8 | |
| | | $f_{\text{ADC}} = 4\text{ MHz}$ | 1.2 | 1.7 | |
| TUE | Total unadjusted error | $f_{\text{ADC}} = 16\text{ MHz}$ | 2.2 | 3.0 | |
| | | $f_{\text{ADC}} = 8\text{ MHz}$ | 1.8 | 2.5 | |
| | | $f_{\text{ADC}} = 4\text{ MHz}$ | 1.8 | 2.3 | |
| Offset | Offset error | $f_{\text{ADC}} = 16\text{ MHz}$ | 1.5 | 2 | LSB |
| | | $f_{\text{ADC}} = 8\text{ MHz}$ | 1 | 1.5 | |
| | | $f_{\text{ADC}} = 4\text{ MHz}$ | 0.7 | 1.2 | |
| Gain | Gain error | $f_{\text{ADC}} = 16\text{ MHz}$ | 1 | 1.5 | |
| | | $f_{\text{ADC}} = 8\text{ MHz}$ | | | |
| | | $f_{\text{ADC}} = 4\text{ MHz}$ | | | |

1. Data based on characterization, not tested in production.

Table 53. ADC1 accuracy with $V_{DDA} = 2.4\text{ V to }3.6\text{ V}$

| Symbol | Parameter | Typ | Max ⁽¹⁾ | Unit |
|--------|----------------------------|-----|--------------------|------|
| DNL | Differential non linearity | 1 | 2 | LSB |
| INL | Integral non linearity | 1.7 | 3 | LSB |
| TUE | Total unadjusted error | 2 | 4 | LSB |
| Offset | Offset error | 1 | 2 | LSB |
| Gain | Gain error | 1.5 | 3 | LSB |

1. Data based on characterization, not tested in production.

Table 54. ADC1 accuracy with $V_{DDA} = V_{\text{REF}}^+ = 1.8\text{ V to }2.4\text{ V}$

| Symbol | Parameter | Typ | Max ⁽¹⁾ | Unit |
|--------|----------------------------|-----|--------------------|------|
| DNL | Differential non linearity | 1 | 2 | LSB |
| INL | Integral non linearity | 2 | 3 | LSB |
| TUE | Total unadjusted error | 3 | 5 | LSB |
| Offset | Offset error | 2 | 3 | LSB |
| Gain | Gain error | 2 | 3 | LSB |

1. Data based on characterization, not tested in production.

Figure 38. ADC1 accuracy characteristics

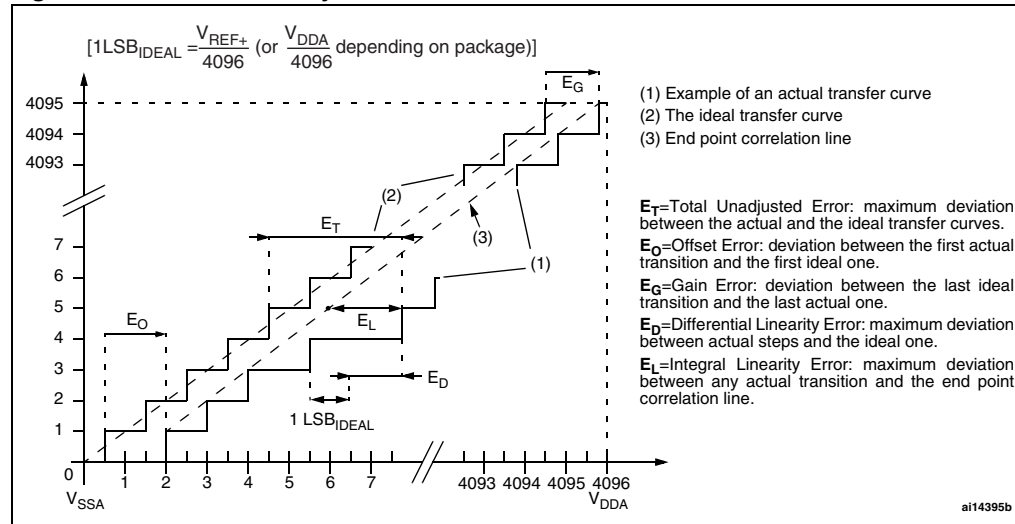
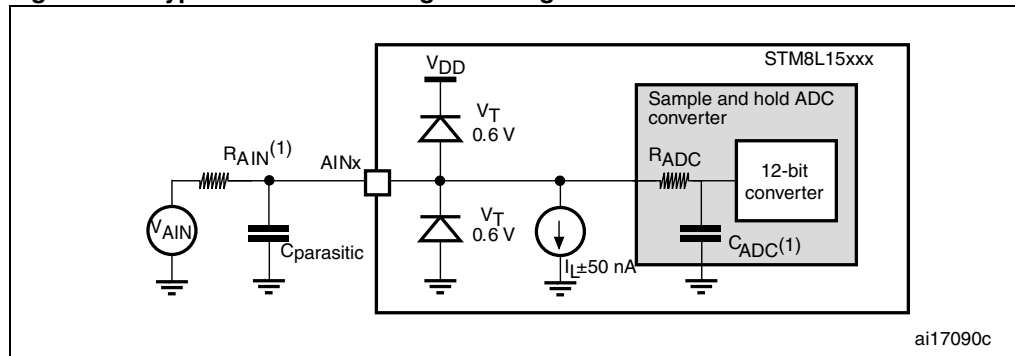


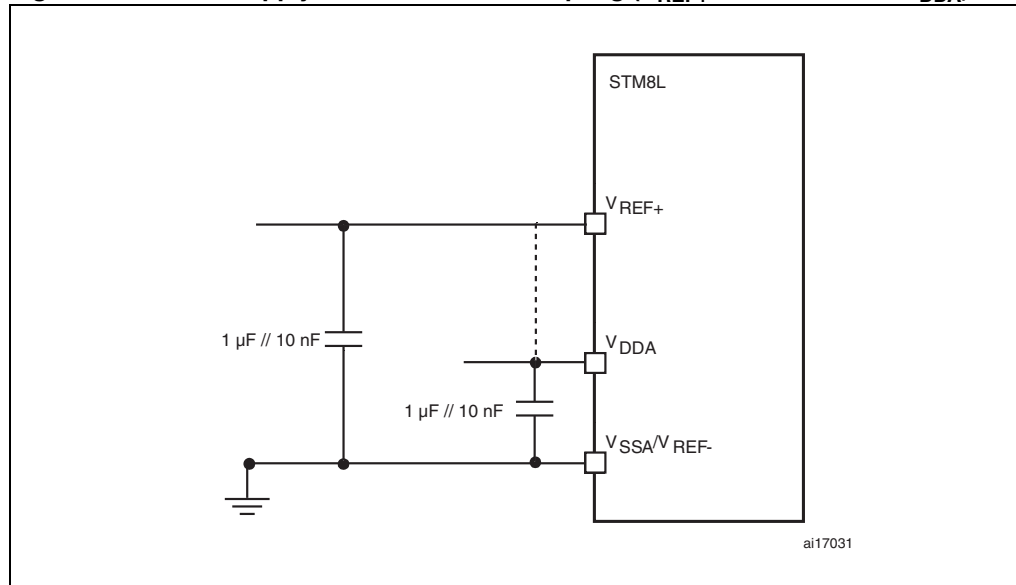
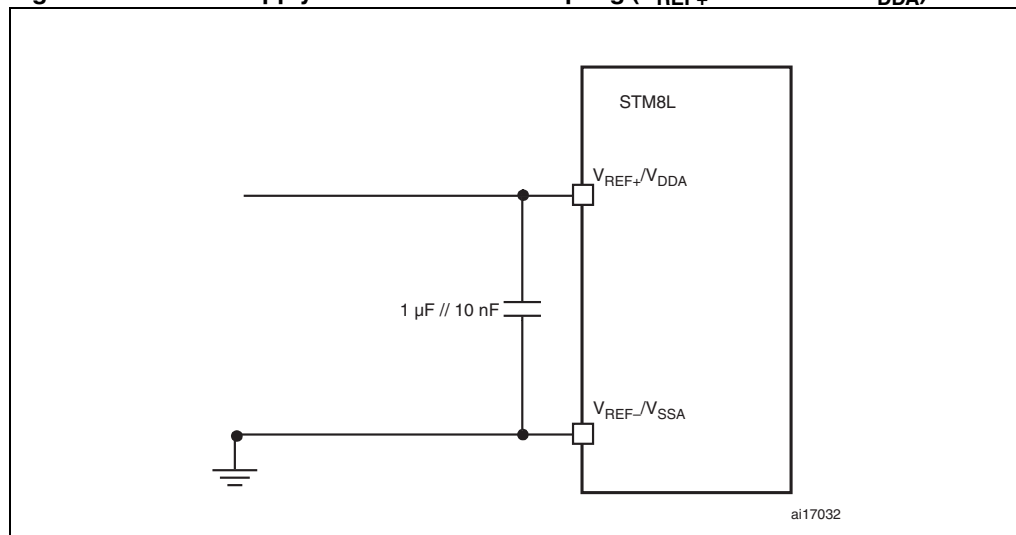
Figure 39. Typical connection diagram using the ADC



1. Refer to [Table 51](#) for the values of R_{AIN} and C_{ADC} .
2. $C_{\text{parasitic}}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{\text{parasitic}}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in [Figure 40](#) or [Figure 41](#), depending on whether $V_{\text{REF}+}$ is connected to V_{DDA} or not. Good quality ceramic 10 nF capacitors should be used. They should be placed as close as possible to the chip.

Figure 40. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})Figure 41. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})

9.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD:** Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000 standard.
- **FTB:** A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 55. EMS data

| Symbol | Parameter | Conditions | Level/Class | |
|------------|---|---|-------------|----|
| V_{FESD} | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD} = 3.3\text{ V}$, $T_A = +25\text{ °C}$, $f_{CPU} = 16\text{ MHz}$, conforms to IEC 61000 | 3B | |
| V_{EFTB} | Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance | $V_{DD} = 3.3\text{ V}$, $T_A = +25\text{ °C}$, $f_{CPU} = 16\text{ MHz}$, conforms to IEC 61000 | Using HSI | 4A |
| | | | Using HSE | 2B |

Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm IEC61967-2 which specifies the board and the loading of each pin.

Table 56. EMI data ⁽¹⁾

| Symbol | Parameter | Conditions | Monitored frequency band | Max vs. | Unit |
|------------------|------------|---|--------------------------|---------|------------|
| | | | | 16 MHz | |
| S _{EMI} | Peak level | V _{DD} = 3.6 V, T _A = +25 °C, LQFP32 conforming to IEC61967-2 | 0.1 MHz to 30 MHz | -3 | dB μ V |
| | | | 30 MHz to 130 MHz | -9 | |
| | | | 130 MHz to 1 GHz | 4 | |
| | | | SAE EMI Level | 2 | - |

1. Not tested in production.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models can be simulated: human body model and charge device model. This test conforms to the JESD22-A114A/A115A standard.

Table 57. ESD absolute maximum ratings

| Symbol | Ratings | Conditions | Maximum value ⁽¹⁾ | Unit |
|-----------------------|---|-------------------------|------------------------------|------|
| V _{ESD(HBM)} | Electrostatic discharge voltage (human body model) | T _A = +25 °C | 2000 | V |
| V _{ESD(CDM)} | Electrostatic discharge voltage (charge device model) | | 500 | |

1. Data based on characterization results, not tested in production.

Static latch-up

- **LU:** 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 58. Electrical sensitivities

| Symbol | Parameter | Class |
|--------|-----------------------|-------|
| LU | Static latch-up class | II |

9.4 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in [Table 17: General operating conditions on page 63](#).

The maximum chip-junction temperature, T_{Jmax} , in degree Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in °C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins

Where:

$$P_{I/Omax} = \Sigma (V_{OL} * I_{OL}) + \Sigma ((V_{DD} - V_{OH}) * I_{OH}),$$

taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 59. Thermal characteristics⁽¹⁾

| Symbol | Parameter | Value | Unit |
|---------------|---|-------|------|
| Θ_{JA} | Thermal resistance junction-ambient UFQFPN28 - 4 x 4 mm | 118 | °C/W |
| Θ_{JA} | Thermal resistance junction-ambient WLCSP28 | 70 | °C/W |
| Θ_{JA} | Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm | 59 | °C/W |
| Θ_{JA} | Thermal resistance junction-ambient UFQFPN 32 - 5 x 5 mm | 38 | °C/W |
| Θ_{JA} | Thermal resistance junction-ambient LQFP 48- 7 x 7 mm | 65 | °C/W |
| Θ_{JA} | Thermal resistance junction-ambient UFQFPN 48- 7 x 7mm | 32 | °C/W |

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

10 Package characteristics

10.1 ECOPACK

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

10.2 Package mechanical data

Figure 42. UFQFPN28 – 28-lead very very thin fine pitch quad flat no-lead package outline (4 x 4)⁽¹⁾

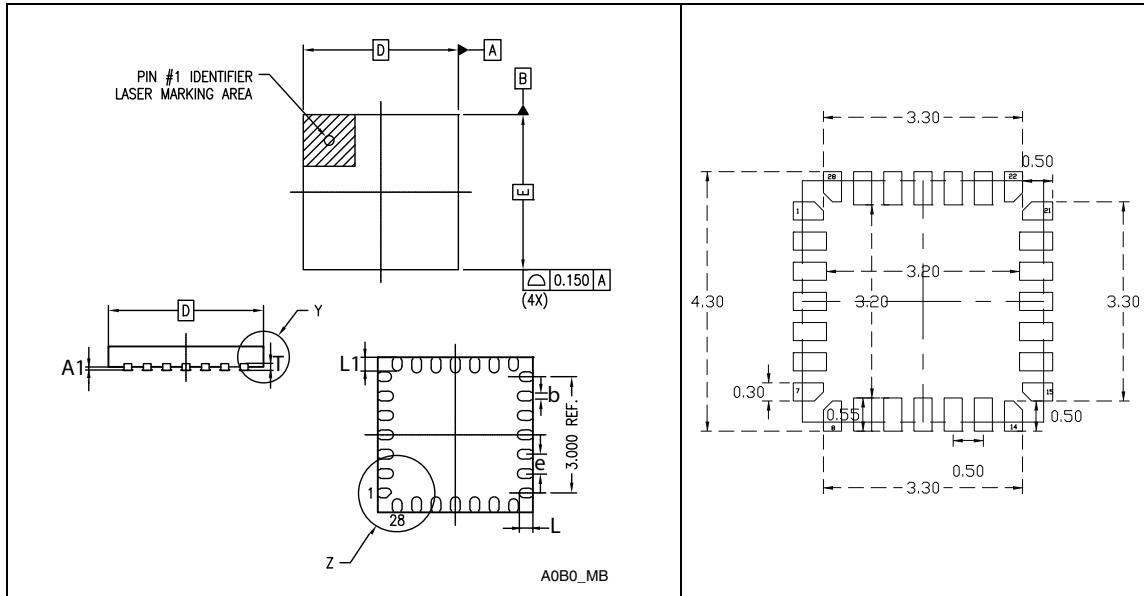
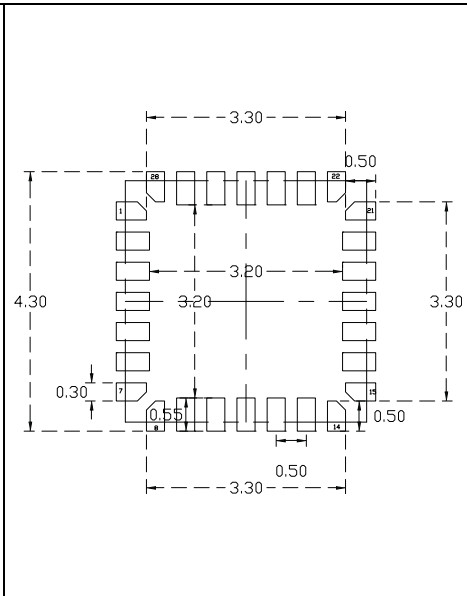


Figure 43. Recommended footprint (dimensions in mm)⁽¹⁾



1. Drawing is not to scale.

Table 60. UFQFPN28 – 28-lead ultra thin fine pitch quad flat no-lead package (4 x 4), package mechanical data

| Dim. | mm | | | inches ⁽¹⁾ | | |
|------|----------------|-------|-------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.500 | 0.550 | 0.600 | 0.0197 | 0.0217 | 0.0236 |
| A1 | 0 | 0 | 0.050 | 0 | 0 | 0.002 |
| D | 3.900 | 4.000 | 4.100 | 0.1535 | 0.1575 | 0.1614 |
| E | 3.900 | 4.000 | 4.100 | 0.1535 | 0.1575 | 0.1614 |
| L | 0.300 | 0.400 | 0.500 | 0.0118 | 0.0157 | 0.0197 |
| L1 | 0.250 | 0.350 | 0.450 | 0.0098 | 0.0138 | 0.0177 |
| T | | 0.152 | | | 0.0060 | |
| b | 0.200 | 0.250 | 0.300 | 0.0079 | 0.0098 | 0.0118 |
| e | | 0.500 | | | 0.0197 | |
| | Number of pins | | | | | |
| N | 28 | | | | | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 44. WLCSP28 – 28-pin wafer level chip scale package, package outline

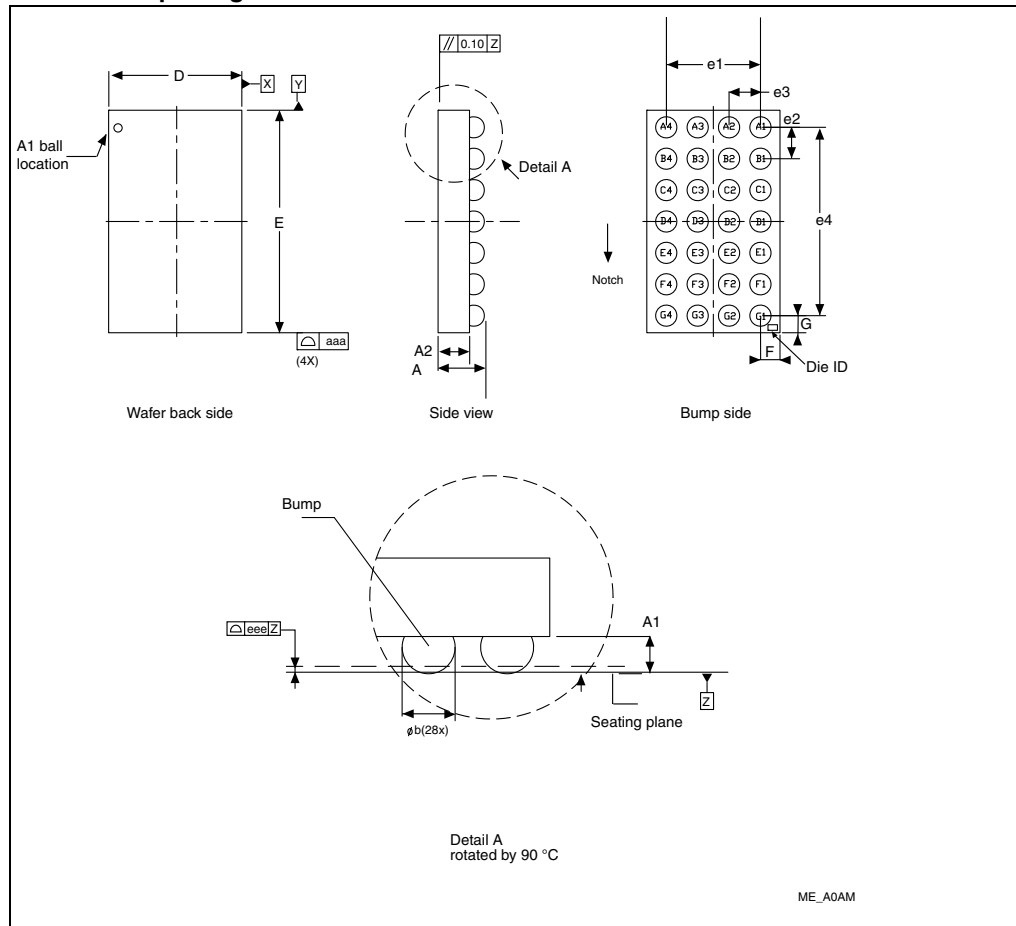


Table 61. WLCSP28 – 28-pin wafer level chip scale package, package mechanical data

| Dim. | mm | | | inches ⁽¹⁾ | | |
|------|-------|-------|-------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.440 | 0.590 | 0.640 | 0.0173 | 0.0232 | 0.0252 |
| A1 | 0.165 | 0.190 | 0.215 | 0.0065 | 0.0075 | 0.0085 |
| A2 | 0.375 | 0.400 | 0.425 | 0.0148 | 0.0157 | 0.0167 |
| b | 0.265 | 0.270 | 0.275 | 0.0104 | 0.0106 | 0.0108 |
| D | 1.677 | 1.697 | 1.717 | 0.0660 | 0.0668 | 0.0676 |
| E | 2.815 | 2.835 | 2.855 | 0.1108 | 0.1116 | 0.1124 |
| e1 | 1.190 | 1.200 | 1.210 | 0.0469 | 0.0472 | 0.0476 |
| e2 | 0.390 | 0.400 | 0.410 | 0.0154 | 0.0157 | 0.0161 |
| e3 | 0.390 | 0.400 | 0.410 | 0.0154 | 0.0157 | 0.0161 |

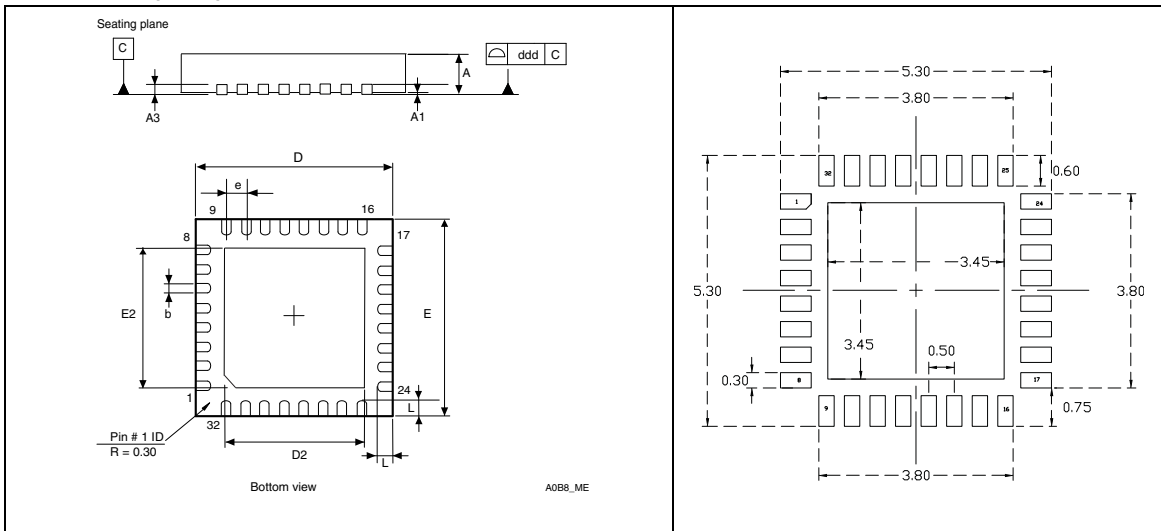
Table 61. WLCSP28 – 28-pin wafer level chip scale package, package mechanical data (continued)

| Dim. | mm | | | inches ⁽¹⁾ | | |
|------|----------------|-------|-------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| e4 | 2.390 | 2.400 | 2.410 | 0.0941 | 0.0945 | 0.0949 |
| F | 0.239 | 0.249 | 0.259 | 0.0094 | 0.0098 | 0.0102 |
| G | 0.208 | 0.218 | 0.228 | 0.0082 | 0.0086 | 0.0090 |
| eee | | 0.050 | | | 0.0020 | |
| | Number of pins | | | | | |
| N | 28 | | | | | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 45. UFQFPN32 - 32-lead ultra thin fine pitch quad flat no-lead package outline (5 x 5)⁽¹⁾⁽²⁾⁽³⁾

Figure 46. UFQFPN32 recommended footprint⁽¹⁾⁽⁴⁾



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.
4. Dimensions are in millimeters.

Table 62. UFQFPN32 - 32-lead ultra thin fine pitch quad flat no-lead package (5 x 5), package mechanical data

| Dim. | mm | | | inches ⁽¹⁾ | | |
|------|----------------|-------|------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.5 | 0.55 | 0.6 | 0.0197 | 0.0217 | 0.0236 |
| A1 | 0.00 | 0.02 | 0.05 | 0 | 0.0008 | 0.0020 |
| A3 | | 0.152 | | | 0.006 | |
| b | 0.18 | 0.23 | 0.28 | 0.0071 | 0.0091 | 0.0110 |
| D | 4.90 | 5.00 | 5.10 | 0.1929 | 0.1969 | 0.2008 |
| D2 | | 3.50 | | | 0.1378 | |
| E | 4.90 | 5.00 | 5.10 | 0.1929 | 0.1969 | 0.2008 |
| E2 | 3.40 | 3.50 | 3.60 | 0.1339 | 0.1378 | 0.1417 |
| e | | 0.500 | | | 0.0197 | |
| L | 0.30 | 0.40 | 0.50 | 0.0118 | 0.0157 | 0.0197 |
| ddd | 0.08 | | | 0.0031 | | |
| | Number of pins | | | | | |
| N | 32 | | | | | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 47. LQFP32 – 32-pin low profile quad flat package outline

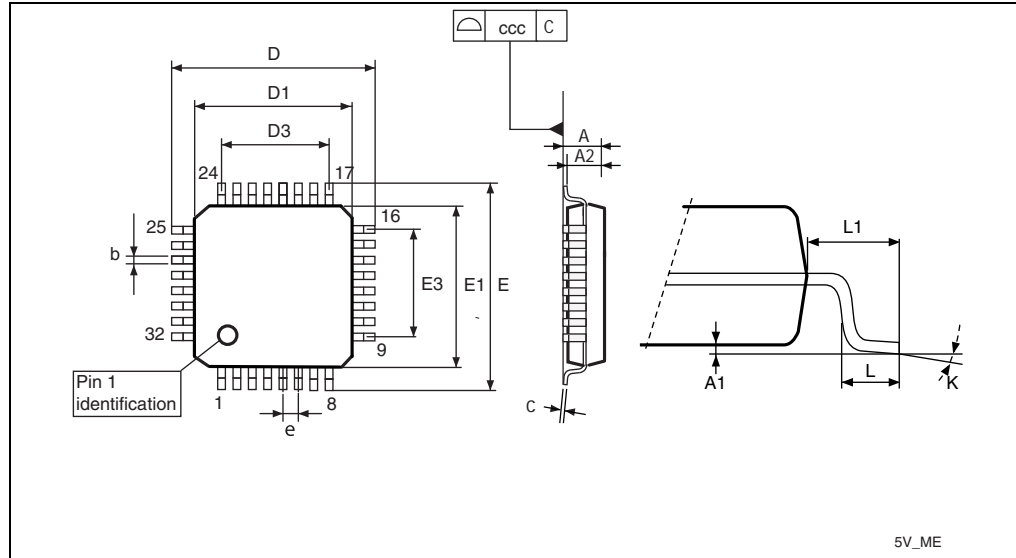
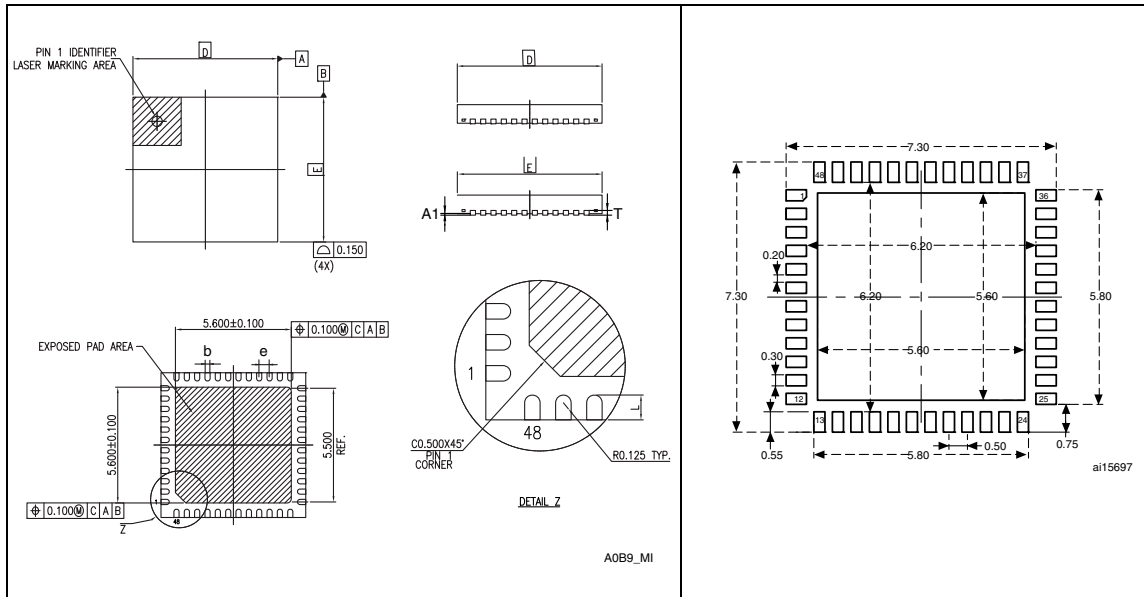


Table 63. LQFP32 – 32-pin low profile quad flat package, package mechanical data

| Dim. | mm | | | inches ⁽¹⁾ | | |
|------|----------------|-------|-------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.6 | | | 0.063 |
| A1 | 0.05 | | 0.15 | 0.0020 | | 0.0059 |
| A2 | 1.35 | 1.4 | 1.45 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.3 | 0.37 | 0.45 | 0.0118 | 0.0146 | 0.0177 |
| c | 0.09 | | 0.2 | 0.0035 | | 0.0079 |
| D | 8.8 | 9 | 9.2 | 0.3465 | 0.3543 | 0.3622 |
| D1 | 6.8 | 7 | 7.2 | 0.2677 | 0.2756 | 0.2835 |
| D3 | | 5.6 | | | 0.2205 | |
| E | 8.8 | 9 | 9.2 | 0.3465 | 0.3543 | 0.3622 |
| E1 | 6.8 | 7 | 7.2 | 0.2677 | 0.2756 | 0.2835 |
| E3 | | 5.6 | | | 0.2205 | |
| e | | 0.8 | | | 0.0315 | |
| L | 0.45 | 0.6 | 0.75 | 0.0177 | 0.0236 | 0.0295 |
| L1 | | 1 | | | 0.0394 | |
| k | 0.0 ° | 3.5 ° | 7.0 ° | 0.0 ° | 3.5 ° | 7.0 ° |
| ccc | 0.1 | | | 0.0039 | | |
| | Number of pins | | | | | |
| N | 32 | | | | | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 48. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package **Figure 49. Recommended footprint outline⁽¹⁾**



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Table 64. UFQFPN48 – ultra thin fine pitch quad flat pack no-lead 7 × 7 mm, 0.5 mm pitch package mechanical data

| Symbol | millimeters | | | inches ⁽¹⁾ | | |
|--------|-------------|-------|-------|-----------------------|--------|--------|
| | Typ | Min | Max | Typ | Min | Max |
| A | 0.500 | 0.550 | 0.600 | 0.0197 | 0.0217 | 0.0236 |
| A1 | 0.000 | 0.020 | 0.050 | 0.0000 | 0.0008 | 0.0020 |
| D | 6.900 | 7.000 | 7.100 | 0.2717 | 0.2756 | 0.2795 |
| E | 6.900 | 7.000 | 7.100 | 0.2717 | 0.2756 | 0.2795 |
| L | 0.300 | 0.400 | 0.500 | 0.0118 | 0.0157 | 0.0197 |
| T | | 0.152 | | | 0.0060 | |
| b | 0.200 | 0.250 | 0.300 | 0.0079 | 0.0098 | 0.0118 |
| e | | 0.500 | | | 0.0197 | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 50. LQFP48 – 48-pin low profile quad flat package outline (7x7)

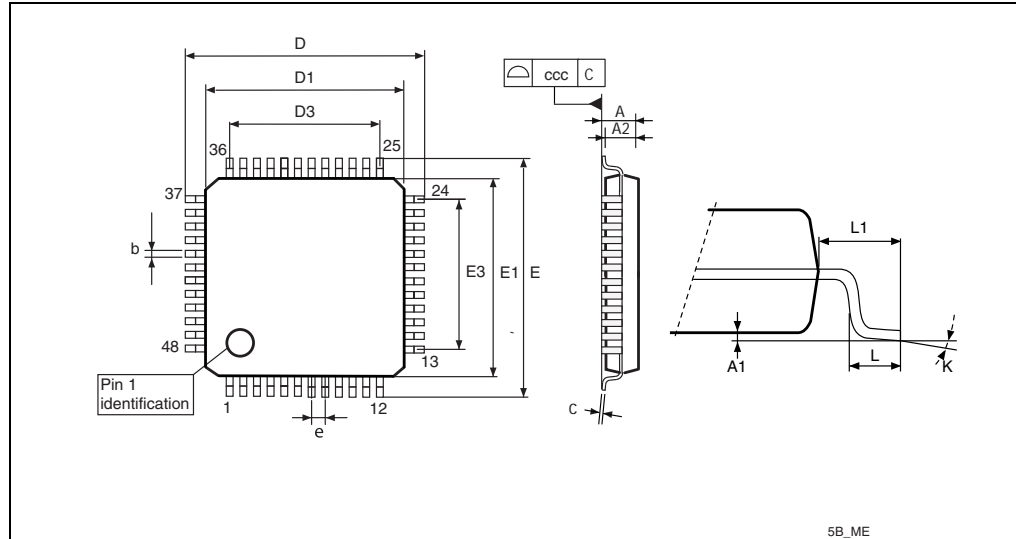


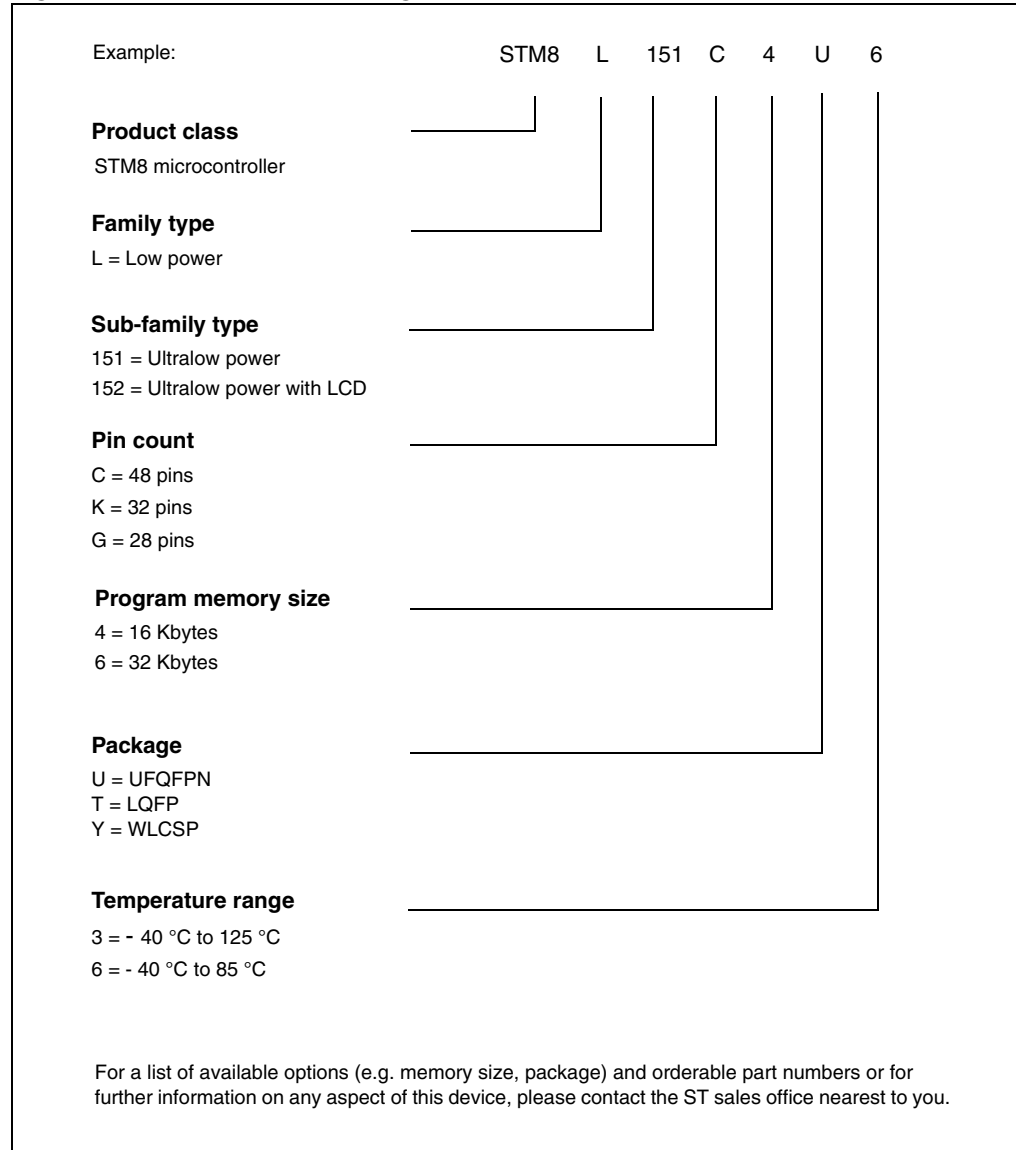
Table 65. LQFP48 – 48-pin low profile quad flat package (7x7), package mechanical data

| Dim. | mm | | | inches ⁽¹⁾ | | |
|------|----------------|------|------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.6 | | | 0.063 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.0059 |
| A2 | 1.35 | 1.4 | 1.45 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.17 | 0.22 | 0.27 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.09 | | 0.2 | 0.0035 | | 0.0079 |
| D | 8.8 | 9 | 9.2 | 0.3465 | 0.3543 | 0.3622 |
| D1 | 6.8 | 7 | 7.2 | 0.2677 | 0.2756 | 0.2835 |
| D3 | | 5.5 | | | 0.2165 | |
| E | 8.8 | 9 | 9.2 | 0.3465 | 0.3543 | 0.3622 |
| E1 | 6.8 | 7 | 7.2 | 0.2677 | 0.2756 | 0.2835 |
| E3 | | 5.5 | | | 0.2165 | |
| e | | 0.5 | | | 0.0197 | |
| L | 0.45 | 0.6 | 0.75 | 0.0177 | 0.0236 | 0.0295 |
| L1 | | 1 | | | 0.0394 | |
| k | 0.0° | 3.5° | 7.0° | 0.0° | 3.5° | 7.0° |
| ccc | | | 0.08 | | | 0.0031 |
| | Number of pins | | | | | |
| N | 48 | | | | | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

11 Device ordering information

Figure 51. STM8L15xxx ordering information scheme



12 Revision history

Table 66. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 06-Aug-2009 | 1 | Initial release |
| 10-Sep-2009 | 2 | Updated peripheral naming throughout document. Added Figure 7: STM8L151Cx 48-pin pinout (without LCD) on page 25 Added capacitive sensing channels in Features on page 1 Updated PA7, PC0 and PC1 in Table 5: STM8L15x pin description Changed CLK and REMAP register names in Table 8 Changed description of WDGHALT in Table 12 Added typical power consumption values in Table 18 to Table 26 Correct VIH max in Table 36 |
| 11-Dec-2009 | 3 | Added WLCSP28 package Modified Figure 9: Memory map on page 35 and added 2 notes. Modified Low power run mode in Section 3.1: Low power modes on page 14 Added Section 8: Unique ID on page 59 Modified Table 10: Interrupt mapping on page 54 (added reserved area at address 0x00 8008) Modified OPT4 option bits in Table 11: Option byte addresses on page 56 Table 12: Option byte description on page 57 : modified OPT0 description (“disable” instead of “enable”) and OPT1 description Added OPTBL option bytes Modified Section 9: Electrical parameters on page 60 |
| 02-Apr-2010 | 4 | Changed title of the document (STM8L151x4, STM8L151x6, STM8L152x4, STM8L152x6) Changed pinout (V _{SS1} , V _{DD1} , V _{SS2} , V _{DD 2} instead of V _{SS} , V _{DD} , V _{SSIO} , V _{DDIO}) Changed packages Changed first page Modified note 1 in Table 5: STM8L15x pin description on page 27 Added note to PA7, PC0, PC1 and PE0 in Table 5: STM8L15x pin description on page 27 Modified Figure 9: Memory map on page 35 Modified Table 61: WLCSP28 – 28-pin wafer level chip scale package, package mechanical data on page 113 (min and max columns swapped) Modified Figure 44: WLCSP28 – 28-pin wafer level chip scale package, package outline on page 113 (A1 ball location) Section : on page 79 : renamed Rm, Lm and Cm EXTI_CONF replaced with EXTI_CONF1 in Table 8: General hardware register map on page 37 Updated Section 9: Electrical parameters on page 60 |

Table 66. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 23-Jul-2010 | 5 | <p>Modified Introduction and Description</p> <p>Modified Table 4: Legend/abbreviation for table 5 on page 27 and Table 5: STM8L15x pin description on page 27 (for PA0, PA1, PB0 and PB4 and for reset states in the floating input column)</p> <p>Modified Figure 1: STM8L15xxx device block diagram on page 13 and Figure 2: STM8L15x clock tree diagram on page 18</p> <p>Modified Figure 3.1: Low power modes on page 14 and Figure 3.5: Low power real-time clock on page 18</p> <p>Modified CLK_PCKENR2 and CLK_HSICALR reset values in Table 8: General hardware register map on page 37</p> <p>Modified notes below Figure 9: Memory map on page 35</p> <p>Modified PA_CR1 reset value in Table 7 on page 36</p> <p>Modified reset values for Px_IDR registers in Table 7 on page 36</p> <p>Modified Table 14: Voltage characteristics on page 61, Table 15: Current characteristics on page 62</p> <p>Modified V_{IH} in Table 36: I/O static characteristics on page 85</p> <p>Modified Table 20: Total current consumption in Wait mode on page 69</p> <p>Modified Figure 37: Typical application with I2C bus and timing diagram 1) on page 96</p> <p>Modified I_L value in Figure 39: Typical connection diagram using the ADC on page 105</p> <p>Modified R_H and R_L in Table 43: LCD characteristics on page 97</p> <p>Added graphs in Section 9: Electrical parameters on page 60</p> <p>Modified note 3 below Table 44: Reference voltage characteristics on page 98</p> <p>Added notes to</p> <p>Modified note 1 below Table 45: TS characteristics on page 99</p> <p>Changed $V_{ESD(CDM)}$ value in Table 57 on page 108</p> <p>Modified notes or added notes below UFQFPN32 and UFQFPN48 packages</p> |

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