Output Voltage Clamping Using the LM5069 Hot Swap Controller

National Semiconductor
Application Note 2040
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March 15, 2010

The Issue

One of the many benefits of using the LM5069 Hot Swap Controller, besides inrush current limiting and fault monitoring, is that the controller supplies a voltage to the load that is between defined limits. This feature prevents the load from receiving a voltage less than what it is rated for (which could result in erratic behavior), and prevents it from receiving a voltage higher than what it is rated for, which could result in overheating and/or damage. The voltage limits to the load are set by the UVLO (Under-Voltage Lock Out) and OVLO (Over-Voltage Lock Out) thresholds, which are set with external resistors (R1-R3 in Figure 1).

While the OVLO function can be used to keep excessive voltages at V_{IN} from reaching the load at V_{OUT}, a potential drawback to this method of over-voltage protection is that the voltage at V_{OUT} is shut off for the duration of the over-voltage condition. This can (and likely will) result in a shutdown of the load circuitry, followed by a restart – an event which may interrupt the normal operation of other associated circuitry.

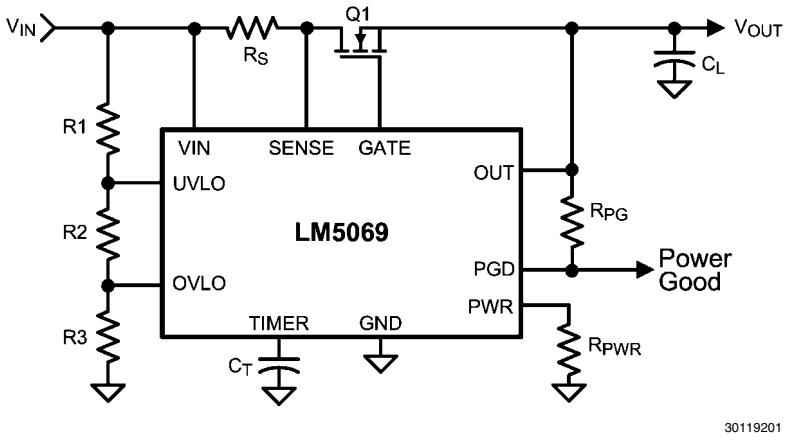


FIGURE 1. LM5069 Basic Application Circuit

The Solution

The solution presented here is to limit the voltage at V_{OUT} to a maximum value, rather than shut it off, when an over-voltage condition appears at V_{IN}. This is accomplished by adding a zener diode at the GATE pin of the LM5069, as shown in Figure 2.

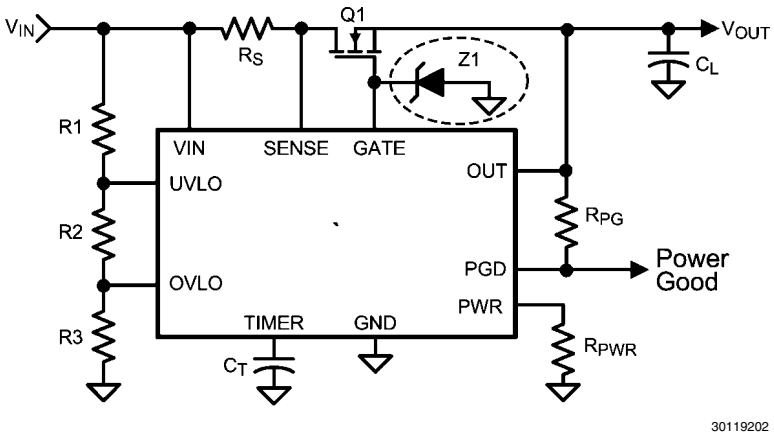


FIGURE 2. Zener Clamp Added to the Gate

In normal operation (when the over-voltage condition is not present) the GATE pin of the LM5069 is approximately 12V above the voltage at V_{OUT}. As the voltage at V_{IN} increases above the normal operating range, Q1's gate voltage is clamped by Z1. As V_{IN} continues to increase, the voltage at V_{OUT} is clamped when Q1's gate-to-source voltage (V_{GS}) reduces to a level where Q1 limits the current to the load. Any additional increase in V_{IN} is absorbed by Q1 as there is no additional increase in the voltage at V_{OUT}.

The choice of zener voltage for Z1 depends not only on the voltage at which V_{OUT} is to be clamped, but also on the specific MOSFET chosen for Q1 – more specifically, its V_{GS} characteristics. Typically Z1 should have a zener voltage approximately 2V to 5V above the desired clamping voltage at V_{OUT}. Using the Transfer Characteristics information in the MOSFET's datasheet can provide an initial value for the difference between Z1's voltage and the desired clamping voltage at V_{OUT}. The final selection for Z1 should be determined experimentally.

Test Results

Two LM5069 circuits were tested with different value zener diodes for Z1. In both tests the pertinent external components were:

- R_S = 20 mohms
- R_{PWR} = 12.5 kohms
- Power Limit = 5 Watts
- Q1 = Vishay SUM40N15-38

A) In the first test, a 20V zener diode was used for Z1. The circuit's load resistance was 40 ohms, resistive. The result, shown in Figure 3, is that the GATE pin was clamped at approximately 20V for V_{IN} >11V, and the output voltage was clamped at between 15.6V and 17V as V_{IN} was increased from 16V to 27V. In this test circuit, increasing V_{IN} above 27V activated the power limiting feature of the LM5069, and Q1 was shut off after the fault timeout period.

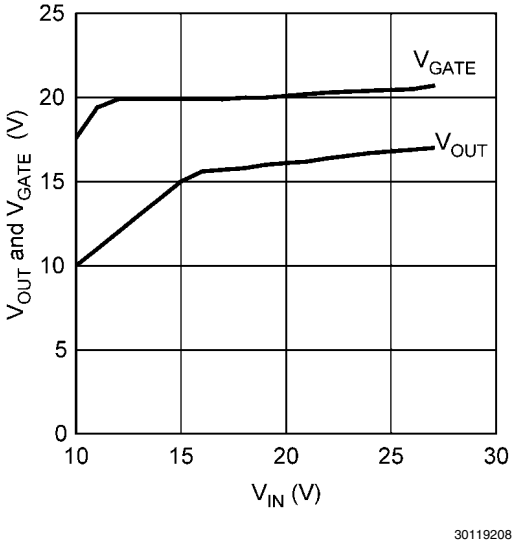
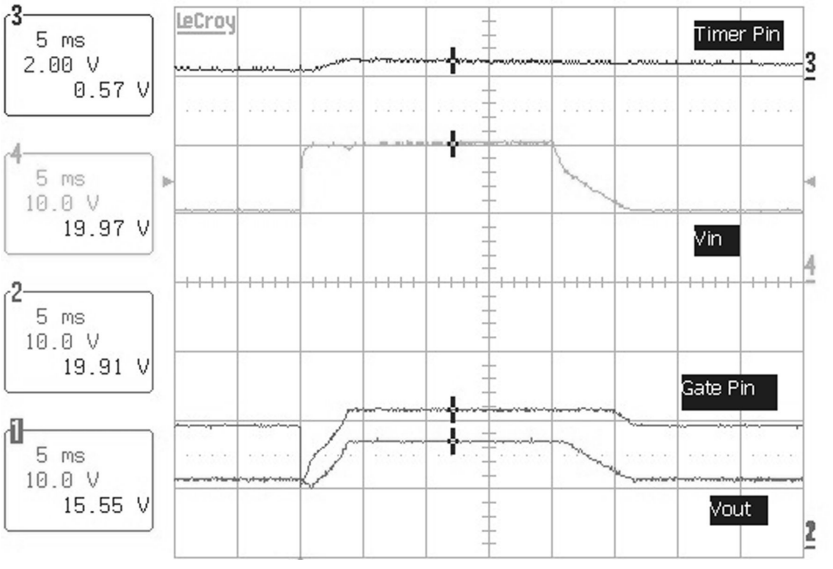


FIGURE 3. Z1 = 20V

Transient testing was performed by quickly increasing V_{IN} from 10V to 20V for 20 milliseconds, and then returning V_{IN} to 10V. The scope photo in Figure 4 shows the results:



Trace 1: V_{OUT} (10V/div)
Trace 2: GATE pin (10/V/div)
Trace 3: TIMER pin (2V/div)
Trace 4: V_{IN} (10V/div)

FIGURE 4. Transient Testing with Z1 = 20V

Referring to Figure 4, initially V_{IN} and V_{OUT} are at 10V, and the GATE pin is at approximately 17.6V. The voltage at the TIMER pin is at zero since the load current is below the current limit threshold. When V_{IN} increases quickly from 10V to 20V, there is a momentary current surge through R_S and Q1 to the capacitor at V_{OUT} (C_L). The current surge amplitude reached the Circuit Breaker limit of the LM5069, which triggered the strong pull-down at the GATE pin.* This is why the GATE pin voltage quickly dropped almost 10V when V_{IN} increased, and the voltage at V_{OUT} dropped a small amount as the load current was momentarily reduced. Immediately after that, the circuit breaker function is shut off (due to the reduced current level), and the current limit feature of the LM5069 then limits the current through R_S and Q1. During this time of current limiting (approximately 3 ms in Figure 4) the voltage at the TIMER pin increases since current limiting is a fault condition.

As the voltage at V_{OUT} increases the voltage at the GATE pin increases with it until it reaches the clamp voltage set by Z1 (19.91V in Figure 4). At this point the voltage at V_{OUT} is clamped at 15.55V, and remains at that level for the remaining time that V_{IN} is at 20V. During the time that V_{OUT} is clamped, the load current (0.389A) is below the current limit threshold, and the power dissipated in Q1 (1.73W) is below the power limit threshold. The TIMER pin voltage is decreasing back towards zero volts. When the voltage at V_{IN} drops back to 10V, the voltage levels at the GATE pin and at V_{OUT} reduce back to their original levels.

*The current surge amplitude was verified with a current probe in series with R_S.

B) In the second test, a 56V zener diode was used for Z1. The circuit's load resistance was 140 ohms, resistive. The result, shown in Figure 5, is that the GATE pin was clamped at approximately 56V for V_{IN} >44V, and the output voltage was clamped at between 51V and 51.5V as V_{IN} was increased from 52V to 62V. In this test circuit, increasing V_{IN} above 62V activated the power limiting feature of the LM5069, and Q1 was shut off after the fault timeout period.

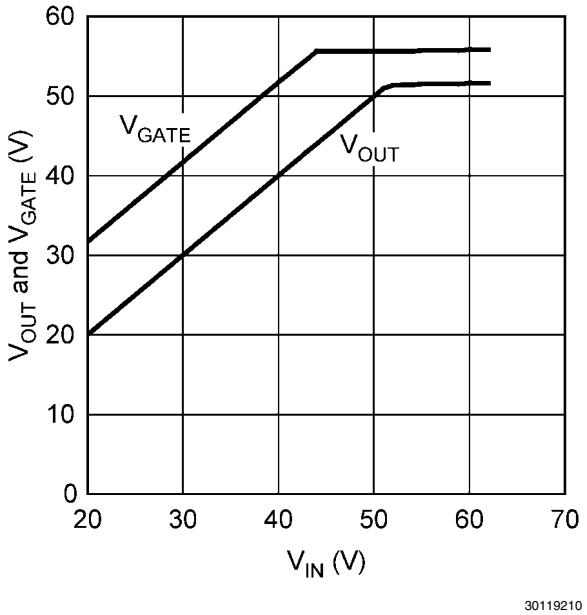
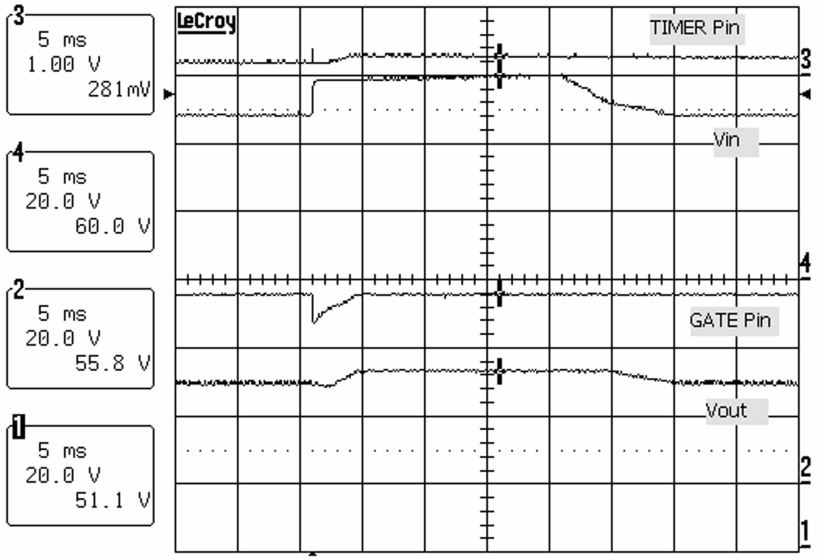


FIGURE 5. Z1 = 56V

Transient testing was performed by quickly increasing V_{IN} from 48V to 60V for 20 milliseconds, and then returning V_{IN} to 48V. The load was 240 ohms, resistive, for this test. The scope photo in Figure 6 shows the results:



Trace 1: V_{OUT} (20V/div)
Trace 2: GATE pin (20V/div)
Trace 3: TIMER pin (1V/div)
Trace 4: V_{IN} (20V/div)

FIGURE 6. Transient Testing with Z1 = 56V

Referring to Figure 6, initially V_{IN} and V_{OUT} are at 48V. The GATE pin, which would normally be at 60V if Z1 were not present, is at approximately 55.8V due to Z1. But the gate-to-source voltage is sufficient to fully enhance Q1's gate so that V_{OUT} is not clamped, and is equal to V_{IN}. The voltage at the TIMER pin is at zero since the load current is below the current limit threshold. When V_{IN} increases quickly from 48V to 60V, there is a momentary current surge through R_S and Q1 to the capacitor at V_{OUT} (C_L). The current surge amplitude reached the Circuit Breaker limit of the LM5069, which triggered the strong pull-down at the GATE pin.* This is why the GATE pin voltage quickly dropped 10V when V_{IN} increased, and the voltage at V_{OUT} dropped a small amount as the load current was momentarily reduced. Immediately after that, the circuit breaker function is shut off (due to the reduced current level), and the current limit feature of the LM5069 then limits the current through R_S and Q1. During this time of current limiting (approximately 2 ms in Figure 6) the voltage at the TIMER pin increases since current limiting is a fault condition.

As the voltage at V_{OUT} increases the voltage at the GATE pin increases with it until it reaches the clamp voltage set by Z1 (55.8V in Figure 6). At this point the voltage at V_{OUT} is clamped at 51.1V, and remains at that level for the remaining time that V_{IN} is at 60V. During the time that V_{OUT} is clamped, the load current (0.213A) is below the current limit threshold, and the power dissipated in Q1 (1.9W) is below the power limit threshold. The TIMER pin voltage is decreasing back towards zero volts. When the voltage at V_{IN} reduces back to 48V, the voltage at V_{OUT} reduces back to 48V. The GATE pin voltage remains at 55.8V since V_{IN} is above 44V.

*The current surge amplitude was verified with a current probe in series with R_S.

Transient Testing and Fault Timeout

In the above two transient tests, the simulated transients were repetitive with V_{IN} held at its higher level for 20 ms, and at the lower level for 80 ms. The LM5069 did not produce a fault timeout since the TIMER pin voltage, which increased during the brief current limiting period, was able to reduce to zero before the next transient arrived. However, a fault timeout, with the accompanying shutdown of Q1, would occur if any of the following test changes were made:

- The upper voltage level at V_{IN} was increased, or
- The load current was increased by reducing the load resistance, or
- The time interval between transients was decreased.

If any of these changes were made, the TIMER pin voltage would not be able to decrease to zero during each transient cycle, causing the pin's voltage to repetitively increase with the arrival of each transient. When the voltage at the TIMER pin reached 4 volts, Q1 was shut off.

In an actual application, if transients are known to be very frequent, the TIMER pin should be monitored on a scope during testing of this proposed solution to see if the voltage stays near zero, or if it drifts up a significant amount with the arrival of each transient. If the TIMER pin voltage reaches 4V at any time Q1 is shut off. The conditions required to cause a fault timeout and a shutdown of Q1 are different for each application.

Power Dissipation in Q1

Implementing this voltage clamp requires re-evaluating the possible power dissipation in Q1. During an over-voltage condition where V_{OUT} is clamped, the power dissipated by Q1 is due to the voltage difference across Q1 ($V_{IN} - V_{OUT}$), and the load current. The different scenarios which can result are:

- If the power dissipation in Q1 is less than the maximum power limit allowed by the LM5069 (set by R_{PWR} and R_S), and/or the duration of the over-voltage condition is known to be less than the fault timeout set by C_T, a fault timeout does not occur. The appropriate limit line in the MOSFET's SOA chart can be used to determine the maximum power limit setting.

- In the case where the duration of the over-voltage condition is extended (possibly lasting several seconds) rather than brief, and the power dissipation in Q1 is less than the maximum power limit allowed by the LM5069, a fault timeout does not occur. However, in this case Q1 can dissipate significant power for the extended time. The DC limit line of the MOSFET's SOA chart must be checked, and the heat sink provided for Q1 must be reviewed.

- If the power dissipation in Q1 reaches the maximum power limit allowed by the LM5069, the fault timer is activated. If the duration of the over-voltage condition is less than the LM5069's fault timeout period (set by C_T), the circuit returns to normal operation ($V_{OUT} = V_{IN}$) when the over-voltage condition subsides. But if the duration of the over-voltage condition is longer than the fault timeout period, Q1 is shut off at the end of the fault timeout period.

Diode Selection

As mentioned above, the selection of a diode for Z1 should be determined experimentally. The voltage at which V_{OUT} is clamped during an over-voltage condition depends not only on Z1 and its tolerances, but also on Q1's V_{GS} characteristics, the load current, and Q1's junction temperature. As for the power rating required for Z1, the current which flows through Z1 is the current supplied from the GATE pin of the LM5069, which is nominally 16 µA. This current flows through Z1 only when it is actively clamping the LM5069's GATE pin.

Change the OVLO Threshold

When implementing this output voltage clamp, the OVLO threshold must either be disabled, or set higher than the maximum voltage expected at V_{IN} during the transient or over-voltage condition. Otherwise, Q1 is shut off anytime the voltage at V_{IN} exceeds the OVLO threshold. To disable the OVLO function connect the OVLO pin to Ground. To change the OVLO threshold, see the LM5069 datasheet for the procedure to calculate new values for the external resistors.

PGD Output

When V_{OUT} is clamped during an over-voltage condition, a voltage difference exists across Q1 ($V_{IN} - V_{OUT}$). If that voltage difference exceeds 2.5V the PGD output switches low. When the over-voltage condition subsides, and the voltage across Q1 decreases below 1.25V, Q1 switches high.

Notes

Notes

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