6A Integrated FET Regulator with 5V LDO

Features

- Input voltage — 3V to 28V
- Internal power MOSFETs — 6A
- Integrated bootstrap switch
- Smart power-save protection
- Integrated 5V, 150mA LDO with bypass capability
- TC compensated $R_{DS(ON)}$ sensed current limit
- Pseudo-fixed frequency adaptive on-time control
- Designed for use with ceramic capacitors
- Programmable V_{IN} UVLO threshold
- Independent enable for switcher and LDO
- Selectable ultrasonic power-save (SC414)
- Selectable power-save (SC424)
- Internal soft-start and soft-shutdown at output
- Internal reference — 1% tolerance
- Over-voltage and under-voltage fault protection
- Power good output
- SmartDrive™
- Lead-free 4x4mm, 28 Pin MLPQ package
- Fully WEEE and RoHS compliant, and halogen free

Applications

- Notebook, desktop, tablet, and server computers
- Networking and telecommunication equipment
- Printers, DSL, and STB applications
- Embedded applications
- Power supply modules
- Point of load power supplies

Description

The SC414/SC424 is a stand-alone synchronous buck regulated power supply. It features integrated power MOSFETs, a bootstrap switch, and a 5V LDO in a space-saving MLPQ-4x4mm 28-pin package. The device is highly efficient and uses minimal PCB area. It uses pseudo-fixed frequency adaptive on-time operation to provide fast transient response.

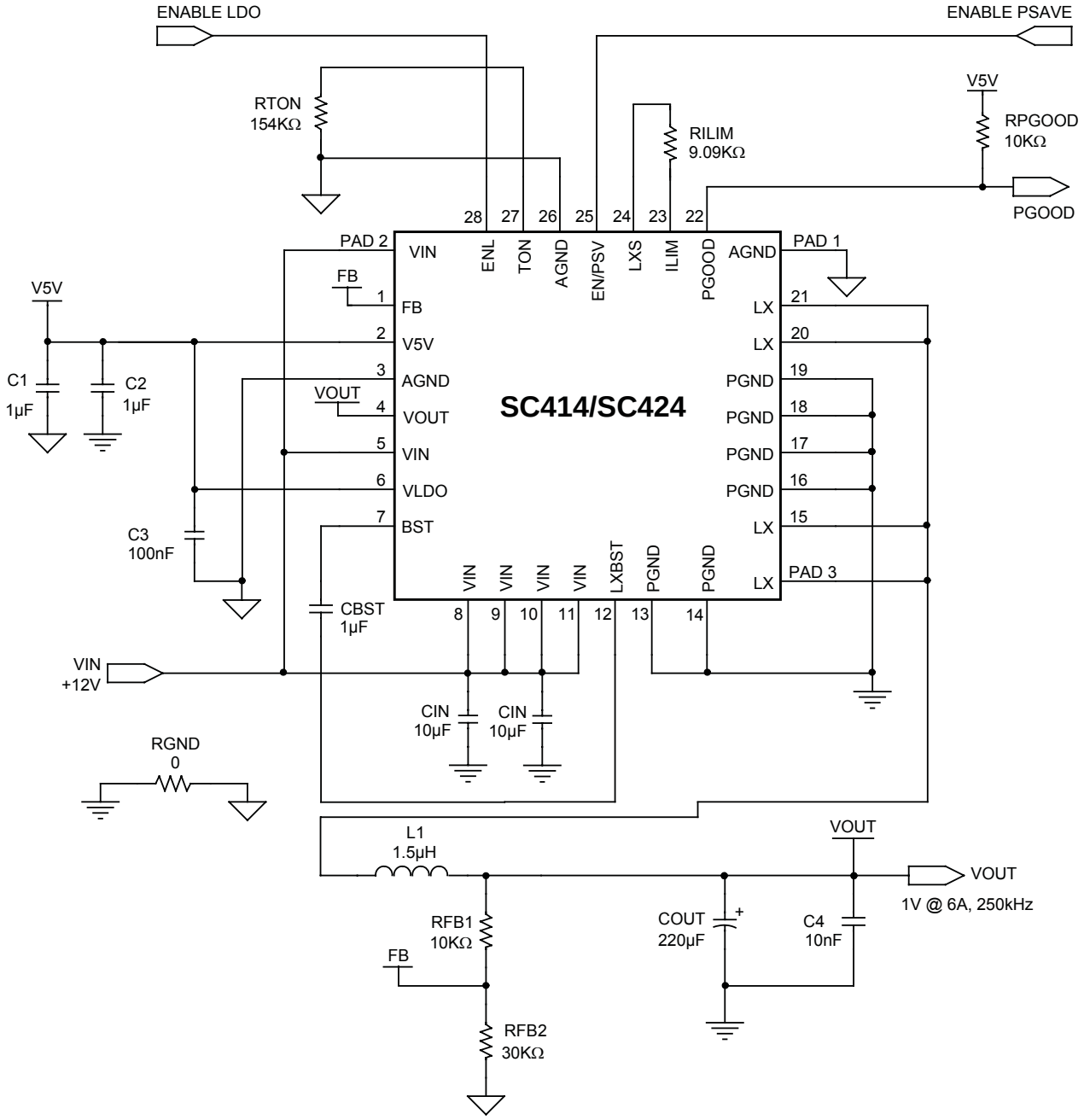
The SC414/SC424 supports using standard capacitor types such as electrolytic or special polymer, in addition to ceramic, at switching frequencies up to 1MHz. The programmable frequency, synchronous operation, and selectable power-save provide high efficiency operation over a wide load range.

Additional features include cycle-by-cycle current limit, soft-start, under and over-voltage protection, programmable over-current protection, soft shutdown, and selectable power-save. The device also provides separate enable inputs for the PWM controller and LDO as well as a power good output for the PWM controller.

The input voltage can range from 3V to 28V. The wide input voltage range, programmable frequency, and 5V LDO make the device extremely flexible and easy to use in a broad range of applications. It can be used for single cell or multi-cell battery systems in addition to traditional DC power supply applications.

The 5V LDO or an external 3.3V to 5V supply can be used to provide the bias voltage for the SC414/SC424. When the SC414/SC424 is used as a 5V output switching regulator, the 5V LDO can be used as an initial bias supply for the device. Once the switch regulator output is in the switch over range, the LDO will be bypassed by the switcher output for optimum efficiency.

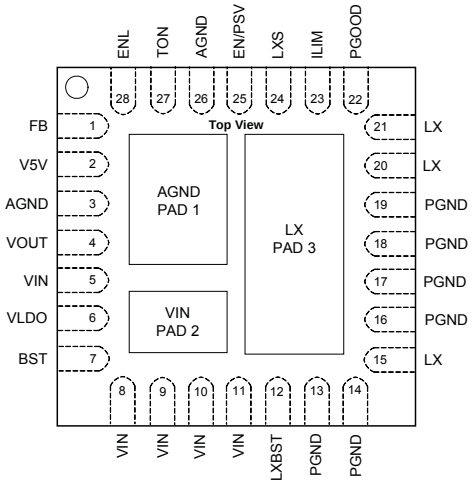
Typical Application Circuit



Key Components

Component	Value	Manufacturer	Part Number	Web
CIN	10µF/25V	Murata	GRM32DR71E106KA12L	www.murata.com
COUT	220µF/15mΩ/6.3V	Panasonic	EEFUE0J221R	www.panasonic.com
L1	1.5µH/9A	Vishay	IHLP2525CZER1R5M01	www.vishay.com
All other small signal components (resistors and capacitors) are standard SMT devices.				

Pin Configuration



SC414 and SC424
MLPQ-28; 4x4, 28 LEAD

Ordering Information

Device	Package
SC414MLTRT(1)(2)	MLPQ-28 4x4
SC424MLTRT(1)(2)	MLPQ-28 4x4
SC414EVB	Evaluation Board
SC424EVB	Evaluation Board

Notes:
1) Available in tape and reel only. A reel contains 3000 devices.
2) Lead-free packaging only. Device is WEEE and RoHS compliant, and halogen free.

Marking Information

yyww = Date Code
xxxxx = Semtech Lot Number

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xxxxx = Semtech Lot Number

SEMTECH

Absolute Maximum Ratings

LX to PGND (V) ..... -0.3 to +30
LX to PGND (V) (transient — 100ns max.) ..... -2 to +30
VIN to PGND (V) ..... -0.3 to +30
EN/PSV, PGOOD, ILIM, to GND (V) ..... -0.3 to +(V5V+0.3)
VOUT, VLDO, FB, to GND (V) ..... -0.3 to +(V5V+0.3)
V5V to PGND (V) ..... -0.3 to +6
TON to PGND (V) ..... -0.3 to +(V5V - 1.5)
ENL (V) ..... -0.3 to V_{IN}
BST to LX (V) ..... -0.3 to +6.0
BST to PGND (V) ..... -0.3 to +35
AGND to PGND (V) ..... -0.3 to +0.3
ESD Protection Level[1] (kV) 2

Recommended Operating Conditions

Input Voltage (V) ..... 3.0 to 28
V5V to PGND (V) ..... 3.0 to 5.5
VOUT to PGND (V) ..... 0.75 to 5.5

Thermal Information

Storage Temperature (°C) ..... -60 to +150
Maximum Junction Temperature (°C) 150
Operating Junction Temperature (°C) ..... -40 to +125
Thermal resistance, junction to ambient [2] (°C/W)
- High-side MOSFET 53
- Low-side MOSFET 42
- PWM controller and LDO thermal resistance 40

Peak IR Reflow Temperature (°C) 260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) Tested according to JEDEC standard JESD22-A114.
(2) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless specified: V_{IN} =12V, T_A = +25°C for Typical, -40 to +85 °C for Min. and Max., T_J < 125°C, V5V = +5V, Typical Application Circuit

Parameter	Conditions	Min	Typ	Max	Units
Input Supplies					
VIN UVLO Threshold[1] (not available for V5V < 4.5V)	Sensed at ENL pin, rising edge	2.40	2.60	2.95	V
	Sensed at ENL pin, falling edge	2.235	2.40	2.565	
VIN UVLO Hysteresis	EN/PSV = High		0.2		V
V5V UVLO Threshold	Measured at V5V pin, rising edge	2.50	2.9	3.0	V
	Measured at V5V pin, falling edge	2.40	2.7	2.90	
V5V UVLO Hysteresis			0.2		V
VIN Supply Current	ENL, EN/PSV = 0V, V_{IN} = 28V		8.5	20	µA
	Standby mode; ENL=V5V, EN/PSV = 0V		130		

Electrical Characteristics (continued)

Parameter	Conditions	Min	Typ	Max	Units
Input Supplies (continued)					
V5V Supply Current	ENL, EN/PSV = 0V , V5V = 5V		3	7	µA
	ENL, EN/PSV = 0V , V5V = 3V		2		
	SC414, EN/PSV = V5V, no load (f_{SW} = 25kHz), V_{FB} > 750mV[2]		1		mA
	SC424, EN/PSV = V5V, no load, V_{FB} > 750mV[2]		0.4		
	V5V = 5V, f_{SW} = 250kHz, EN/PSV = floating, no load[2]		4		
	V5V = 3V, f_{SW} = 250kHz, EN/PSV = floating, no load[2]		2.5		
FB Comparator Threshold	Static V_{IN} and load, 0 to +85 °C, V5V = 3V or 5V	0.744	0.750	0.756	V
	Static V_{IN} and load, -40 to +85 °C, V5V = 3V or 5V	0.7425		0.7575	V
Frequency Range	Continuous mode operation			1000	kHz
	Minimum f_{SW}, (SC414 only), EN/PSV = V5V, no load		25		
Bootstrap Switch Resistance			10		Ω
Timing					
On-Time	Continuous mode operation, V_{IN} = 15V, V_{OUT} = 3V, R_{TON} = 300kΩ	1350	1500	1650	ns
	V5V < 4.5V[3]				
Minimum On-Time [2]			80		ns
Minimum Off-Time [2]	V5V = 5V		320		ns
	V5V = 3V		390		
Soft-Start					
Soft-Start Ramp Time [2]			1.7		ms
Analog Inputs/Outputs					
VOUT Input Resistance			500		kΩ
Current Sense					
Zero-Crossing Detector Threshold	LX - PGND, V5V = 3V or 5V	-3	0	+3	mV

Electrical Characteristics (continued)

Parameter	Conditions	Min	Typ	Max	Units
Power Good					
Power Good Threshold	Upper limit, V_{FB} > internal 750mV reference		+20		%
	Lower limit, V_{FB} < internal 750mV reference		-10		%
Start-Up Delay Time (Time between EN going high and PGOOD going high)	V5V = 3V		2		ms
	V5V = 5V		4		
Fault (noise immunity) Delay Time[2]			5		µs
Leakage				1	µA
Power Good On-Resistance			10		Ω
Fault Protection					
Valley Current Limit	V5V = 5V, R_{ILIM} = 5k Ω	3	4	5	A
Valley Current Limit	V5V = 3V, R_{ILIM} = 5k Ω		3.4		A
I_{LIM} Source Current			8		µA
I_{LIM} Comparator Offset	With respect to AGND	-8	0	+8	mV
Output Under-Voltage Fault	V_{FB} with respect to internal 750mV reference, 8 consecutive clock cycles		-25		%
Smart Power-save Protection Threshold [2]	V_{FB} with respect to internal 750mV reference		+10		%
Over-Voltage Protection Threshold	V_{FB} with respect to internal 750mV reference		+20		%
Over-Voltage Fault Delay[2]			5		µs
Over-Temperature Shutdown[2]	10°C hysteresis		150		°C
Logic Inputs/Outputs					
Logic Input High Voltage	ENL	1			V
Logic Input Low Voltage	ENL			0.4	V
EN/PSV Input for PSAVE Operation [2]	% of V5V	45		100	%
EN/PSV Input for Forced Continuous Operation [2]	% of V5V	1V		42	%
EN/PSV Input for Disabling Switcher [2]		0		0.4	V
EN/PSV Input Bias Current	EN/PSV= V5V or AGND	-10		+10	µA
ENL Input Bias Current	V_{IN} = 28V		11	18	µA
FB Input Bias Current	FB = V5V or AGND	-1		+1	µA

Electrical Characteristics (continued)

Parameter	Conditions	Min	Typ	Max	Units
Linear Regulator — LDO (not available for V5V < 5V)					
VLDO Accuracy	VLDO load = 10mA	4.9	5.0	5.1	V
LDO Current Limit	Start-up and foldback, V_{IN} = 12V		85		mA
	Operating current limit, V_{IN} = 12V	135	200		
VLDO to VOUT Switch-over Threshold (4)		-140		+140	mV
VLDO to VOUT Non-switch-over Threshold (4)		-450		+450	mV
VLDO to VOUT Switch-over Resistance	V_{OUT} = +5V		2		Ω
LDO Drop Out Voltage (5)	From V_{IN} to V_{VLDO}, V_{VLDO} = +5V, I_{VLDO} = 100mA		1.2		V

Notes:

(1) V_{IN} UVLO is programmable using a resistor divider from VIN to ENL to AGND. The ENL voltage is compared to an internal reference.

(2) Guaranteed by design.

(3) For V5V less than 4.5V, the On-Time may be limited by the V5V supply voltage and by V_{IN}. See the TON Limitations and V5V Supply Voltage section in the applications Information.

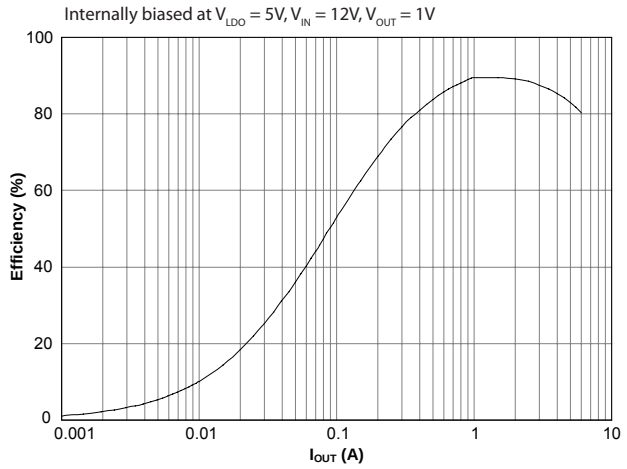
(4) The switch-over threshold is the maximum voltage differential between the VLDO and VOUT pins which ensures that VLDO will internally switch-over to V_{OUT}. The non-switch-over threshold is the minimum voltage differential between the VLDO and VOUT pins which ensures that VLDO will not switch-over to V_{OUT}.

(5) The LDO drop out voltage is the voltage at which the LDO output drops 2% below the nominal regulation point. Thermal resistance, junction to ambient — guaranteed by design (°C/W)

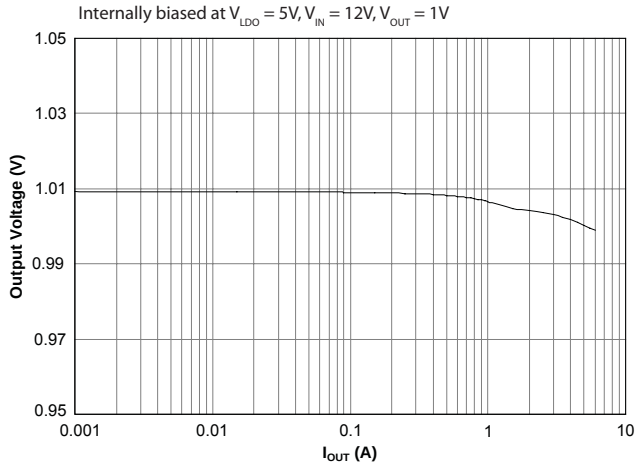
Typical Characteristics

Characteristics in this section are based on using the Typical Application Circuit on page 2 (SC414/SC424).

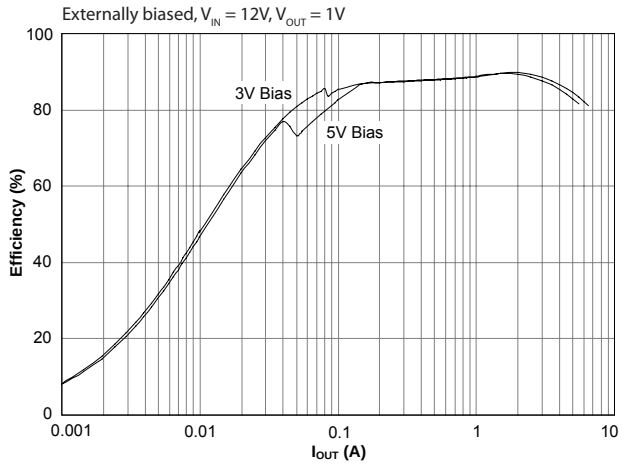
Efficiency vs. Load — Forced Continuous Mode



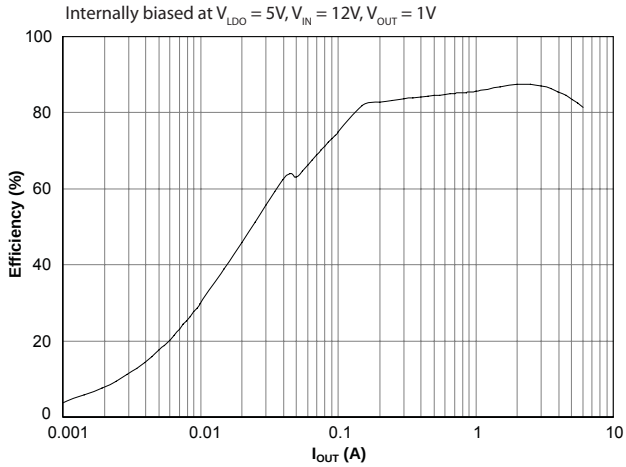
V_{OUT} vs. Load — Forced Continuous Mode



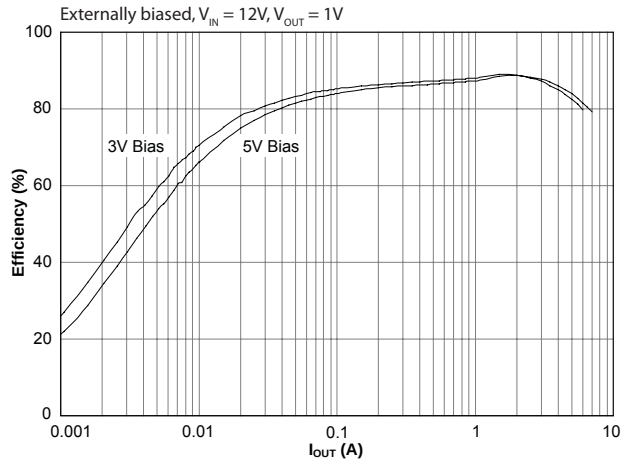
Efficiency vs. Load — Powersave Mode (SC414)



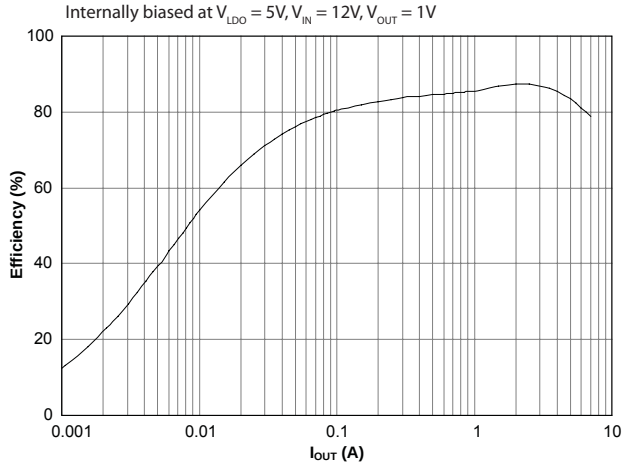
Efficiency vs. Load — Powersave Mode (SC414)



Efficiency vs. Load — Powersave Mode (SC424)



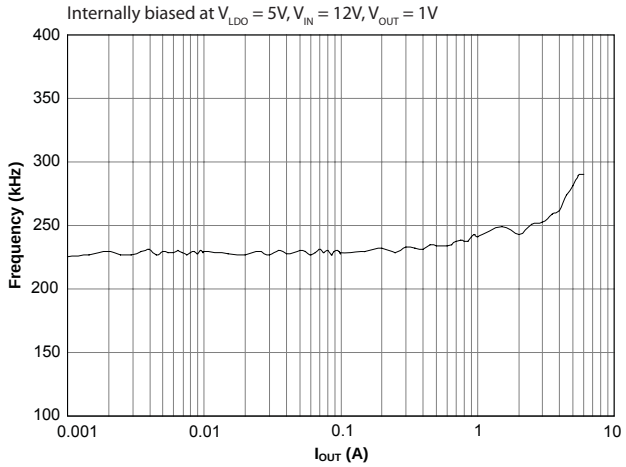
Efficiency vs. Load — Powersave Mode (SC424)



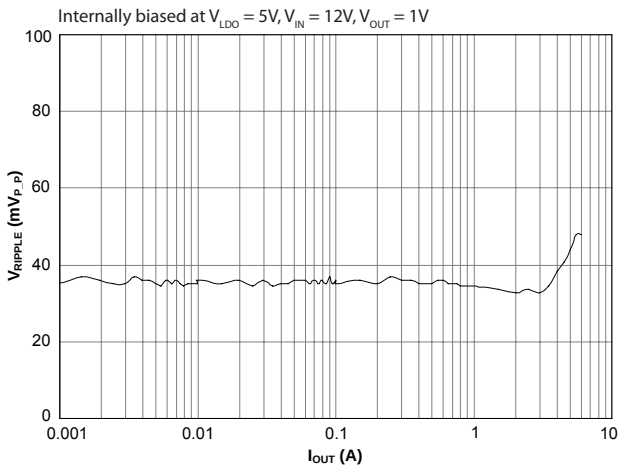
Typical Characteristics (continued)

Characteristics in this section are based on using the Typical Application Circuit on page 2 (SC414/SC424).

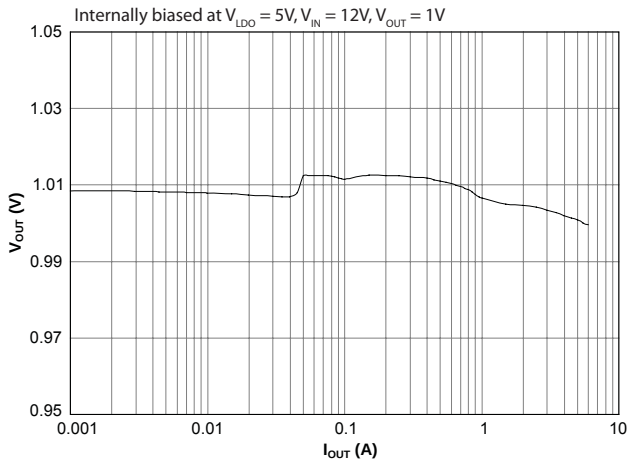
Frequency vs. Load — Forced Continuous Mode



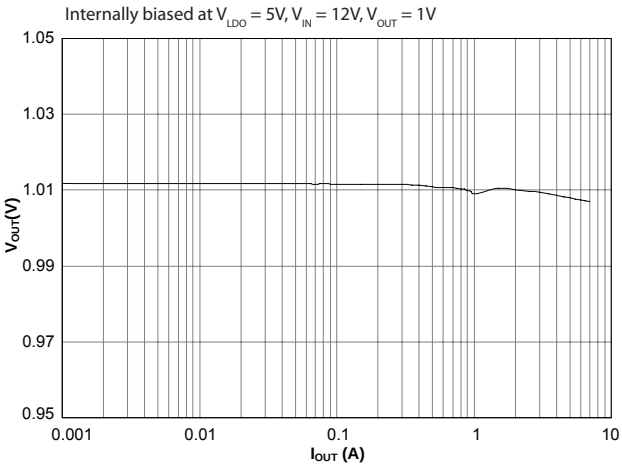
V_{RIPPLE} vs. Load — Forced Continuous Mode



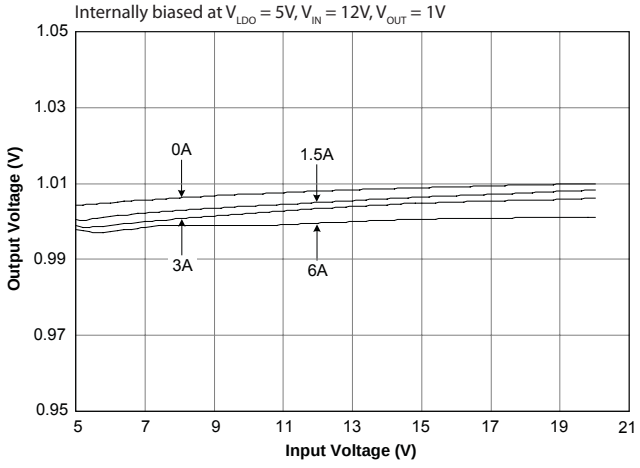
V_{OUT} vs. Load — Powersave Mode (SC414)



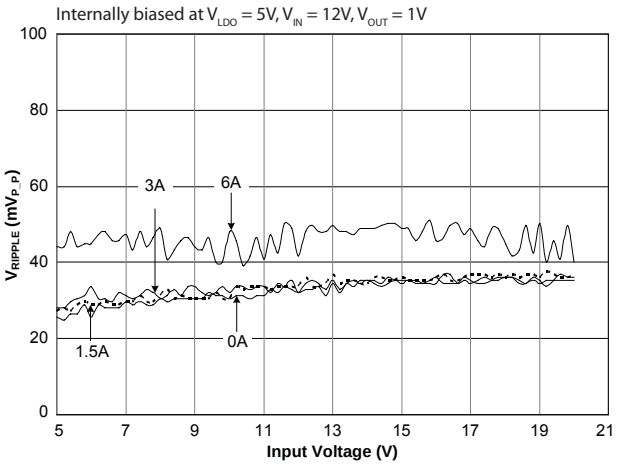
V_{OUT} vs. Load — Powersave Mode (SC424)



V_{OUT} vs. Line — Forced Continuous Mode



V_{OUT} vs. Line — Forced Continuous Mode

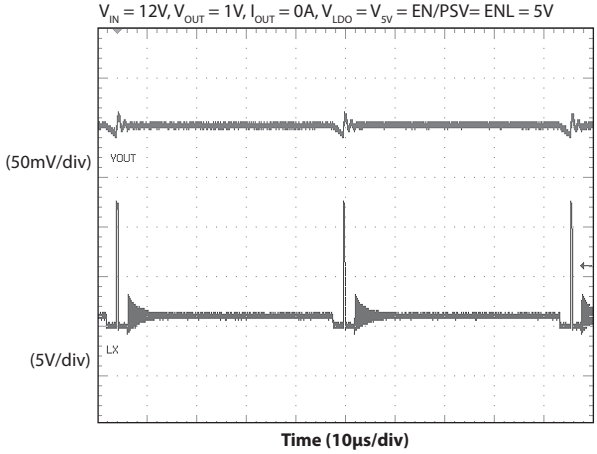


Typical Characteristics (continued)

Characteristics in this section are based on using the Typical Application Circuit on page 2 (SC414/SC424).

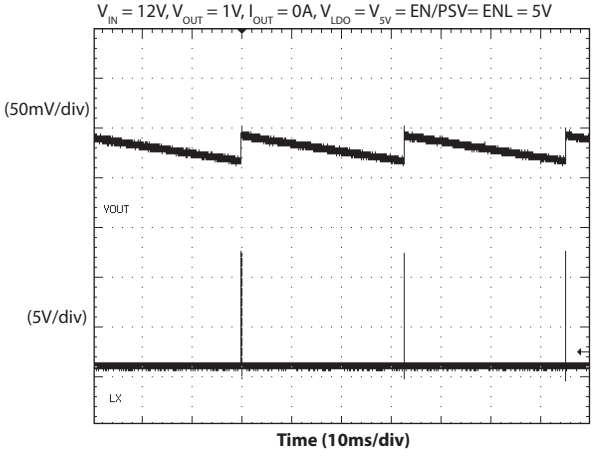
Ultrasonic Powersave Mode — No Load (SC414)

V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 0A, V_{LDO} = V_{5V} = EN/PSV= ENL = 5V



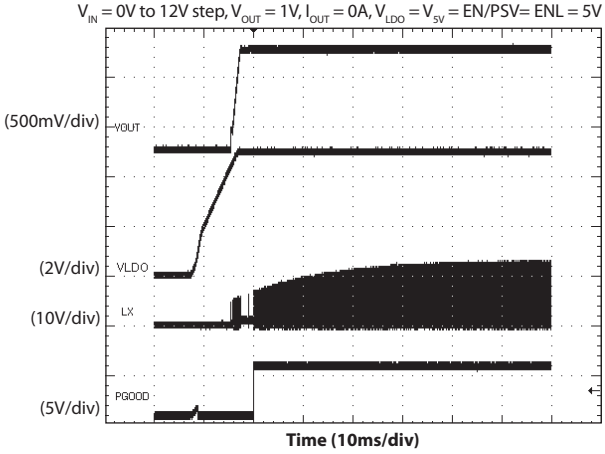
Powersave Mode — No Load (SC424)

V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 0A, V_{LDO} = V_{5V} = EN/PSV= ENL = 5V



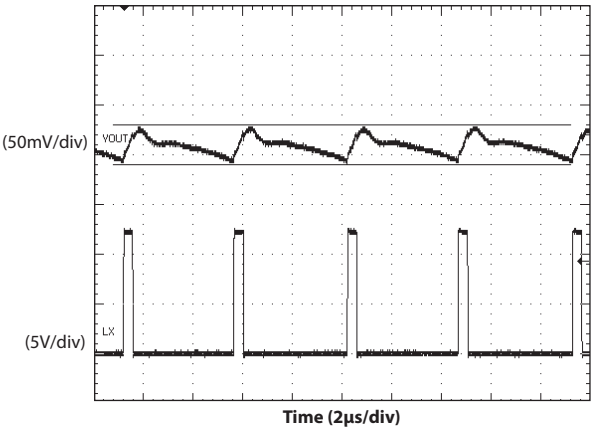
Self-Biased Start-Up — Power Good True

V_{IN} = 0V to 12V step, V_{OUT} = 1V, I_{OUT} = 0A, V_{LDO} = V_{5V} = EN/PSV= ENL = 5V



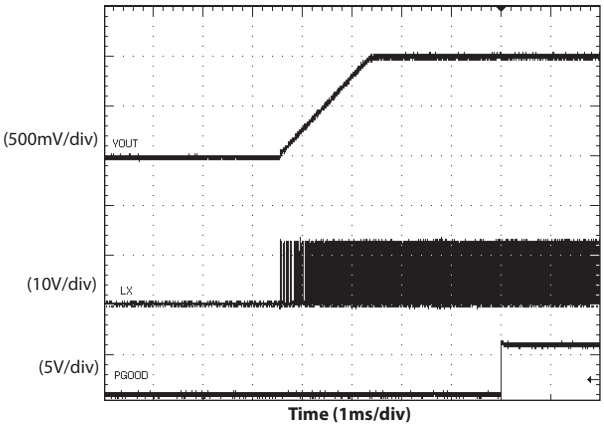
Forced Continuous Mode — No Load

V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 0A, V_{LDO} = V_{5V} = ENL = 5V, EN/PSV= float



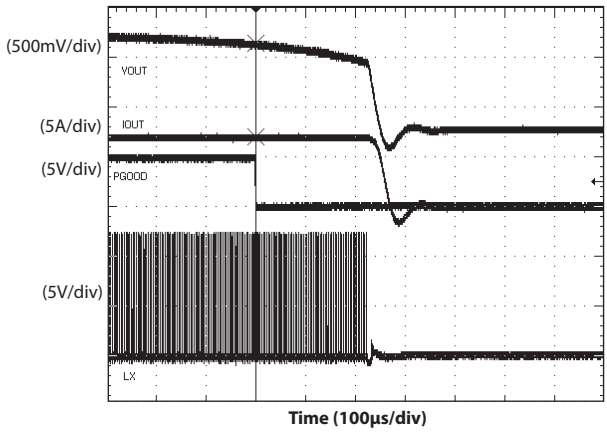
Enabled Loaded Output — Power Good True

V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 1A, V_{LDO} = V_{5V} = ENL = 5V. EN/PSV= 5V



Output Over-current Response — Normal Operation

V_{IN} = 12V, V_{OUT} = 1V, V_{LDO} = V_{5V} = ENL = 5V, EN/PSV= floating; I_{OUT} ramped to trip point

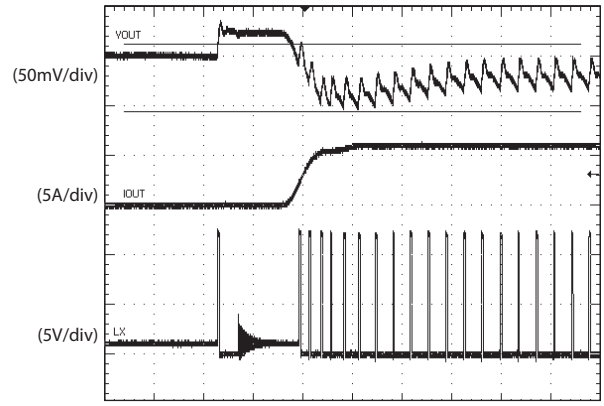


Typical Characteristics (continued)

Characteristics in this section are based on using the Typical Application Circuit on page 2 (SC414/SC424).

Transient Response — Load Rising (SC414)

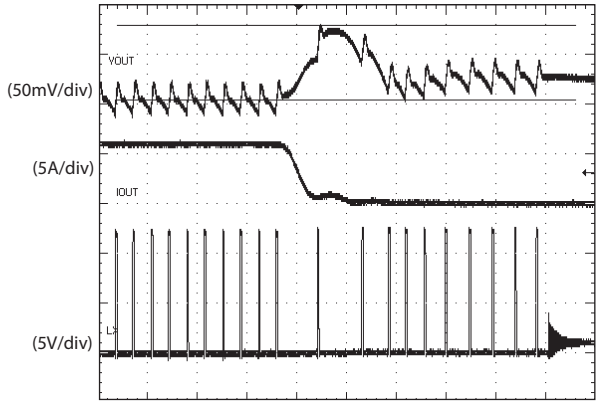
V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 200mA to 6A, V_{LDO} = V_{5V} = EN/PSV= ENL = 5V



Time (10µs/div)

Transient Response — Load Falling (SC414)

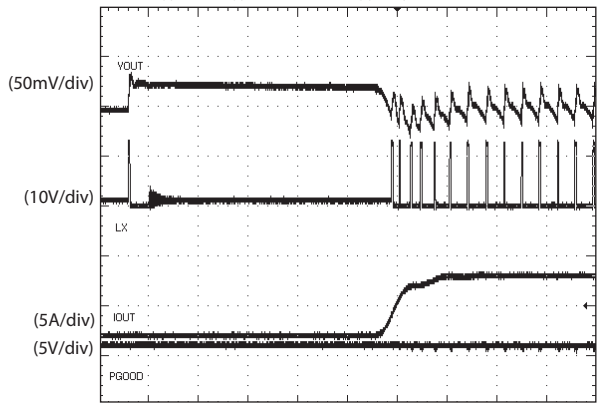
V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 6A to 0A, V_{LDO} = V_{5V} = EN/PSV= ENL = 5V



Time (10µs/div)

Transient Response — Load Rising (SC424)

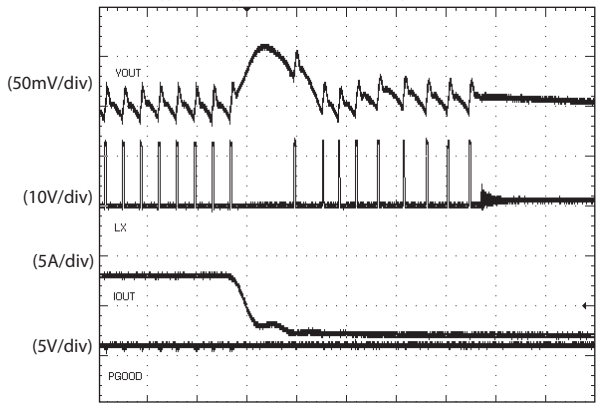
V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 0A to 6A, V_{LDO} = V_{5V} = EN/PSV= ENL = 5V



Time (10µs/div)

Transient Response — Load Falling (SC424)

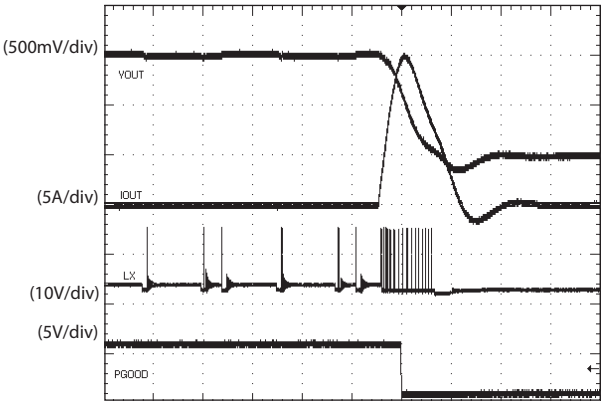
V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 6A to 0A, V_{LDO} = V_{5V} = EN/PSV= ENL = 5V



Time (10µs/div)

Shorted Output Response — Normal Operation

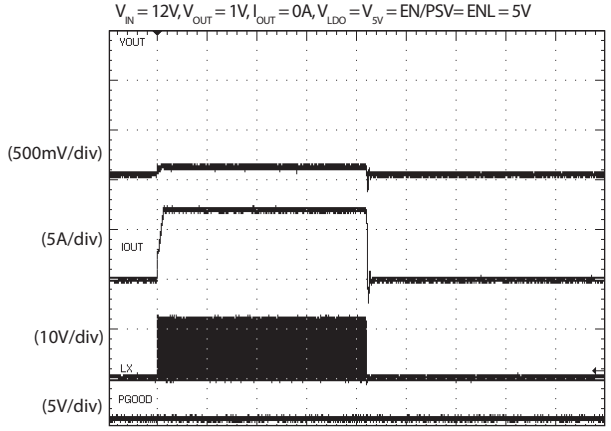
V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 0A, V_{LDO} = V_{5V} = EN/PSV= ENL = 5V



Time (40µs/div)

Shorted Output Response — Power-UP Operation

V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 0A, V_{LDO} = V_{5V} = EN/PSV= ENL = 5V

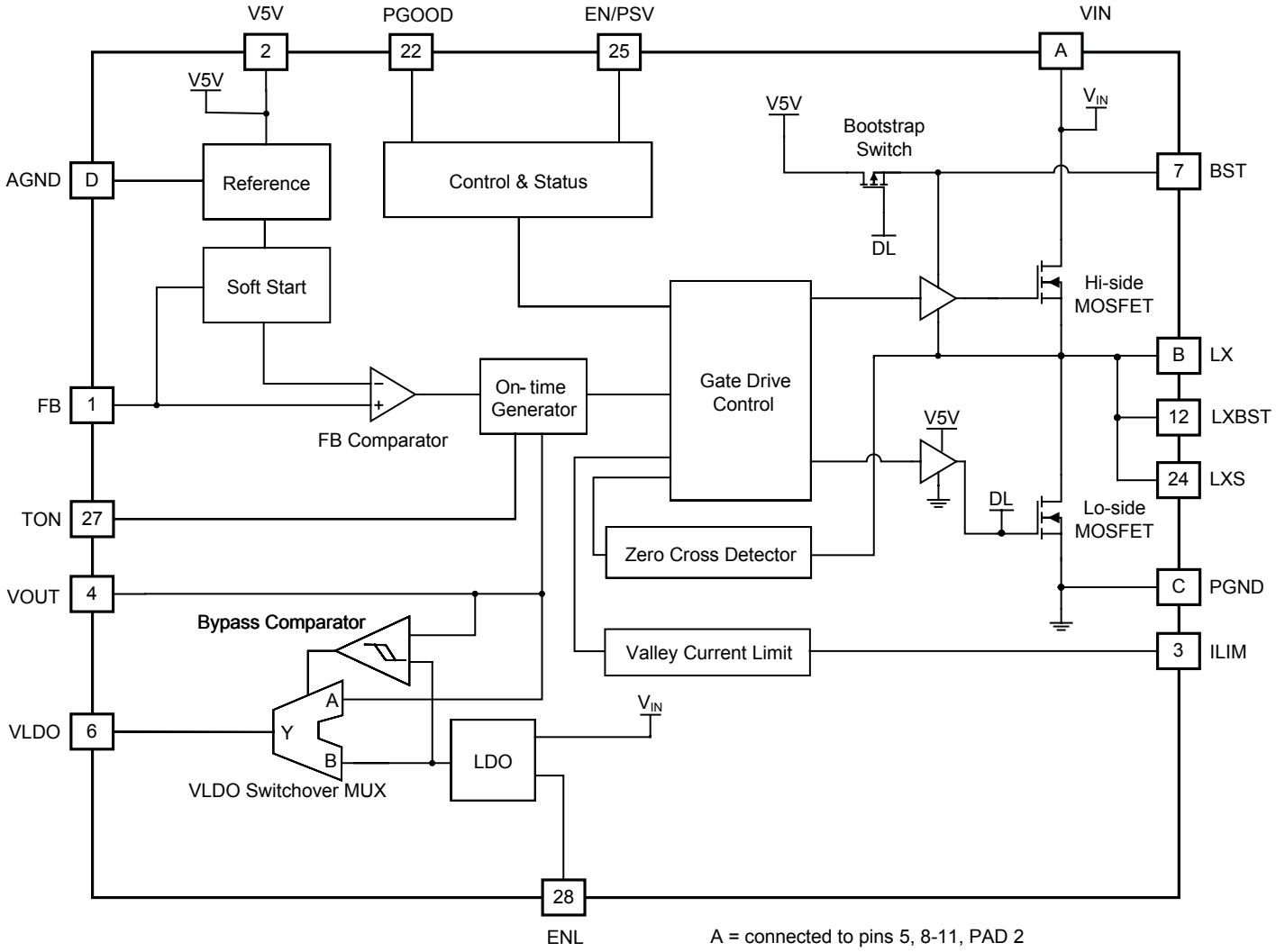


Time (1ms/div)

Pin Descriptions

Pin #	Pin Name	Pin Function
1	FB	Feedback input for switching regulator used to program the output voltage — connect to an external resistor divider from VOUT to AGND.
2	V5V	Bias input for internal analog circuits and gate drives — connect to external 3V or 5V supply or bias connection to VLDO.
3, 26, PAD 1	AGND	Analog ground
4	VOUT	Switcher output voltage sense pin, and also the input to the internal switch-over between VOUT and VLDO.
5, 8-11 PAD 2	VIN	Input supply voltage
6	VLDO	5V LDO output
7	BST	Bootstrap pin — connect a capacitor from BST to LXBST to develop the floating supply for the high-side gate drive.
12	LXBST	LX Boost — connect to the BST capacitor.
15,20, 21, PAD 3	LX	Switching (phase) node
13, 14, 16-19	PGND	Power ground
22	PGOOD	Open-drain power good indicator — high impedance indicates power is good. An external pull-up resistor is required.
23	ILIM	Current limit sense pin — used to program the current limit by connecting a resistor from ILIM to LXS.
24	LXS	LX sense — connects to RILIM resistor
25	EN/PSV	Enable/power save input for the switching regulator — connect to AGND to disable the switching regulator. Float to operate in forced continuous mode (power save disabled). For SC414, connect to V5V to operate with ultrasonic power save mode enabled. For SC424, connect to V5V to operate with power save mode enabled with no minimum frequency.
27	TON	On-time programming input — set the on-time by connecting through a resistor to AGND
28	ENL	Enable input for the LDO — connect ENL to AGND to disable the LDO. Drive with logic to +3V for logic control, or program the VIN UVLO with a resistor divider between VIN, ENL, and AGND.

Block Diagram



A = connected to pins 5, 8-11, PAD 2
B = connected to pins 15, 20, 21, PAD 3
C = connected to pins 13, 14, 16-19
D = connect to pins 3, 26, PAD 1

Applications Information

Synchronous Buck Converter

The SC414/SC424 is a step down synchronous DC-DC buck converter with integrated power MOSFETs and a 5V LDO. The device is capable of 6A operation at very high efficiency. A space saving 4x4 (mm) 28-pin package is used. The programmable operating frequency range of 200kHz to 1MHz enables optimizing the configuration for PCB area and efficiency.

The buck controller uses a pseudo-fixed frequency adaptive on-time control. This control method allows fast transient response which permits the use of smaller output capacitors.

Input Voltage Requirements

The SC414/SC424 requires two input supplies for normal operation: V_{IN} and V5V. V_{IN} operates over the wide range from 3V to 28V. V5V requires a 3.3 or 5V supply input that can be an external source or the internal LDO configured to supply 5V. If the LDO is enabled, V5V voltage must be $\geq$ 5V.

Psuedo-fixed Frequency Adaptive On-time Control

The PWM control method used by the SC414/SC424 is pseudo-fixed frequency, adaptive on-time, as shown in Figure 1. The ripple voltage generated at the output capacitor (ESR) is used as a PWM ramp signal. This ripple is used to trigger the on-time of the controller.

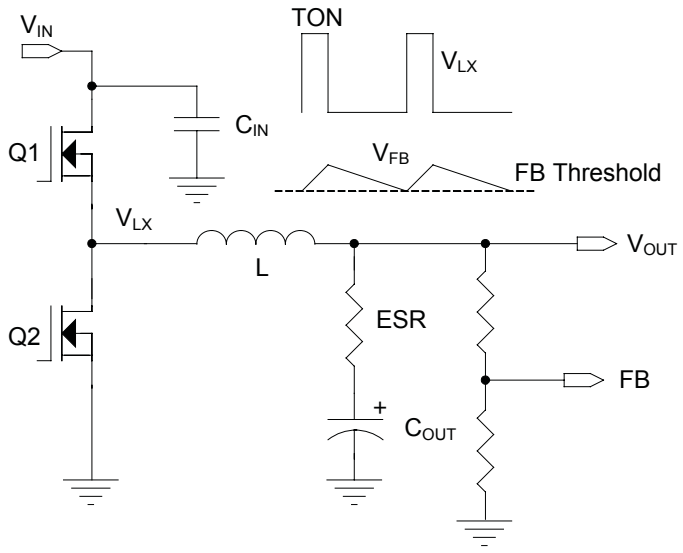


Figure 1 — PWM Control Method, V_{OUT} Ripple

The adaptive on-time is determined by an internal one-shot timer. When the one-shot is triggered by the output ripple, the device sends a single on-time pulse to the high-side MOSFET. The pulse period is determined by V_{OUT} and V_{IN}. The period is proportional to output voltage and inversely proportional to input voltage. With this adaptive on-time configuration, the device automatically anticipates the on-time needed to regulate V_{OUT} for the present V_{IN} condition and at the selected frequency.

The advantages of adaptive on-time control are:

- Predictable operating frequency compared to other variable frequency methods.
- Reduced component count by eliminating the error amplifier and compensation components.
- Reduced component count by removing the need to sense and control inductor current.
- Fast transient response — the response time is controlled by a fast comparator instead of a typically slow error amplifier.
- Reduced output capacitance due to fast transient response

One-Shot Timer and Operating Frequency

One-shot timer operation is shown in Figure 2. The FB Comparator output goes high when V_{FB} is less than the internal 750mV reference. This feeds into the gate drive and turns on the high-side MOSFET, and starts the one-shot timer. The one-shot timer uses an internal comparator and a capacitor. One comparator input is connected to V_{OUT}, the other input is connected to the capacitor. When the on-time begins, the internal capacitor charges from zero volts through a current which is proportional to V_{IN}. When the capacitor voltage reaches V_{OUT}, the on-time is completed and the high-side MOSFET turns off.

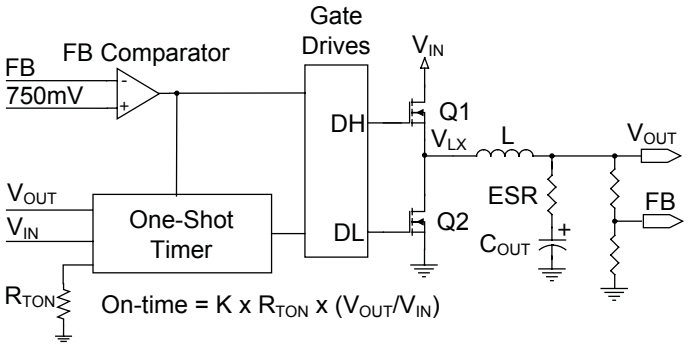


Figure 2 — On-Time Generation

Applications Information (continued)

This method automatically produces an on-time that is proportional to V_{OUT} and inversely proportional to V_{IN}. Under steady-state conditions, the switching frequency can be determined from the on-time by the following equation.

$$f_{SW} = \frac{V_{OUT}}{T_{ON} \times V_{IN}}$$

The SC414/SC424 uses an external resistor to set the on-time which indirectly sets the frequency. The on-time can be programmed to provide an operating frequency from 200kHz to 1MHz using a resistor between the TON pin and ground. The resistor value is selected by the following equation.

$$R_{TON} = \frac{1}{25pF \times f_{SW}} - 400\Omega \times \frac{V_{IN}}{V_{OUT}}$$

The maximum R_{TON} value allowed is shown by the following equation.

$$R_{TON\_MAX} = \frac{V_{IN\_MIN}}{10 \times 1.5\mu A}$$

Immediately after the on-time, the DL (drive signal for the low side FET) output drives high to turn on the low-side MOSFET. DL has a minimum high time of ~320ns, after which DL continues to stay high until one of the following occurs:

- VFB falls below the 750mV reference
- The Zero Cross Detector senses that the voltage on the LX node is below ground. Power Save is activated when a zero crossing is detected.

TON limitations and V5V Supply Voltage

For V5V below 4.5V, the TON accuracy may be limited by the input voltage.

The original RTON equation is accurate if V_{IN} satisfies the below relation over the entire V_{IN} range:

$$V_{IN} < (V5V - 1.6V) \times 10$$

If V_{IN} exceeds (V5V - 1.6V) x 10, for all or part of the V_{IN} range, the RTON equation is not accurate. In all cases where $V_{IN} >$ (V5V - 1.6V) x 10, the RTON equation must be modified as follows.

$$R_{TON} = \frac{1}{25pF \times f_{SW}} - 400\Omega \times \frac{(V5V - 1.6V) \times 10}{V_{OUT}}$$

Note that when $V_{IN} >$ (V5V - 1.6V) x 10 , the actual on-time is fixed and does not vary with V_{IN}. When operating in this condition, the switching frequency will vary inversely with V_{IN} rather than approximating a fixed frequency.

V_{OUT} Voltage Selection

The switcher output voltage is regulated by comparing V_{OUT} as seen through a resistor divider at the FB pin to the internal 750mV reference voltage (see Figure 3).

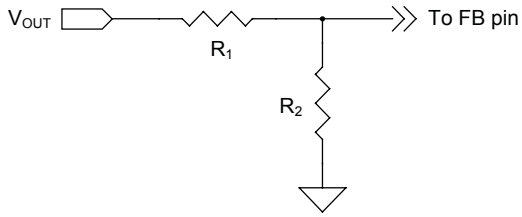


Figure 3 — Output Voltage Selection

Note that this control method regulates the valley of the output ripple voltage, not the DC value. The DC output voltage V_{OUT} is offset by the output ripple according to the following equation.

$$V_{OUT} = 0.75 \times \left(1 + \frac{R_1}{R_2}\right) + \left(\frac{V_{RIPPLE}}{2}\right)$$

When a large capacitor is placed in parallel with R1 (C_{TOP}) V_{OUT} is shown by the following equation.

$$V_{OUT} = 0.75 \times \left(1 + \frac{R_1}{R_2}\right) + \left(\frac{V_{RIPPLE}}{2}\right) \times \sqrt{\frac{1 + (R_1 \omega C_{TOP})^2}{1 + \left(\frac{R_2 \times R_1}{R_2 + R_1} \omega C_{TOP}\right)^2}}$$

Where ω is the angular switching frequency.

Enable and Power-save Inputs

The EN/PSV and ENL inputs are used to enable or disable the switching regulator and the LDO. When EN/PSV is low (grounded), the switching regulator is off and in its lowest power state. When off, the output of the switching regulator soft-discharges the output into a 10Ω internal resistor via the VOUT pin. When EN/PSV is allowed to float, the pin voltage will float to 33% of the voltage at V5V. The switching regulator turns on with power-save disabled and all switching is in forced continuous mode. For V5V < 4.5V, it

Applications Information (continued)

is recommended to force 33% of the V5V voltage on the EN/PSV pin to operate in forced continuous mode.

When EN/PSV is high (above 45% of the voltage at V5V) for SC414, the switching regulator turns on with ultrasonic power-save enabled. The SC414 ultrasonic power-save operation maintains a minimum switching frequency of 25kHz, for applications with stringent audio requirements.

When EN/PSV is high (above 45% of the voltage at V5V) for SC424, the switching regulator turns on with power-save enabled. The SC424 power-save operation is designed to maximize efficiency at light loads with no minimum frequency limits. This makes the SC424 an excellent choice for portable and battery-operated systems.

The ENL input is used to control the internal LDO. This input provides a second function by acting as a V_{IN} ULVO sensor for the switching regulator. When ENL is low (grounded), the LDO is off. When ENL is a logic high but below the V_{IN} UVLO threshold (2.6V typical), then the LDO is on and the switcher is off. When ENL is above the V_{IN} UVLO threshold, the LDO is enabled and the switcher is also enabled if the EN/PSV pin is not grounded.

Forced Continuous Mode Operation

The SC414/SC424 operates the switcher in Forced Continuous Mode (FCM) by floating the EN/PSV pin (see Figure 4). In this mode of operation, the MOSFETs are turned on alternately to each other with a short dead time between them to avoid cross conduction. This feature results in uniform frequency across the full load range with the trade-off being poor efficiency at light loads due to the high-frequency switching of the MOSFETs.

For V5V < 4.5V, it is recommended to force 33% of the V5V voltage on the EN/PSV pin to operate in forced continuous mode.

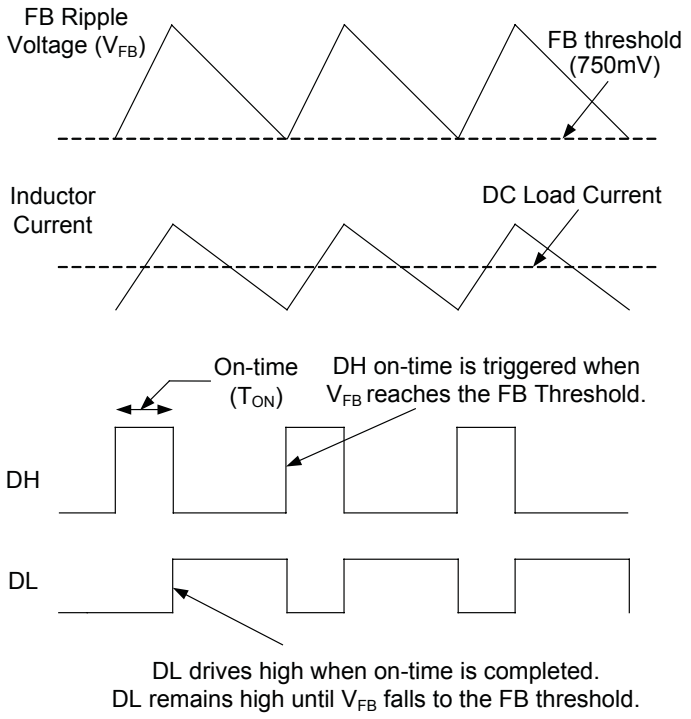


Figure 4 — Forced Continuous Mode Operation

Ultrasonic Power-save Operation (SC414)

The SC414 provides ultrasonic power-save operation at light loads, with the minimum operating frequency fixed at slightly under 25kHz. This is accomplished by using an internal timer that monitors the time between consecutive high-side gate pulses. If the time exceeds 40µs, DL drives high to turn the low-side MOSFET on. This draws current from V_{OUT} through the inductor, forcing both V_{OUT} and V_{FB} to fall. When V_{FB} drops to the 750mV threshold, the next DH (the drive signal for the high side FET) on-time is triggered. After the on-time is completed the high-side MOSFET is turned off and the low-side MOSFET turns on. The low-side MOSFET remains on until the inductor current ramps down to zero, at which point the low-side MOSFET is turned off.

Applications Information (continued)

Because the on-times are forced to occur at intervals no greater than 40µs, the frequency will not fall far below 25kHz. Figure 5 shows ultrasonic power-save operation.

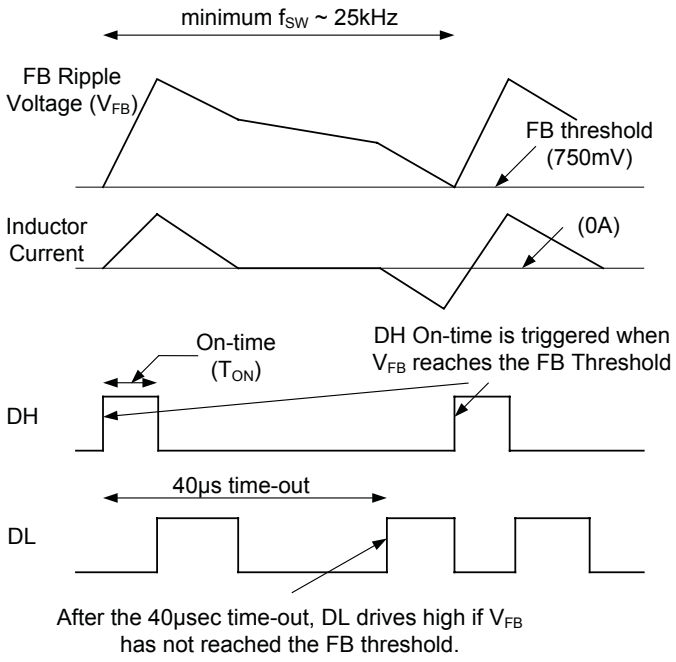


Figure 5 — Ultrasonic Power-save Operation

Power-save Mode Operation (SC424)

The SC424 provides power-save operation at light loads with no minimum operating frequency. With power-save enabled, the internal zero crossing comparator monitors the inductor current via the voltage across the low-side MOSFET during the off-time. If the inductor current falls to zero for 8 consecutive switching cycles, the controller enters power-save operation. It will turn off the low-side MOSFET on each subsequent cycle provided that the current crosses zero. At this time both MOSFETs remain off until V_{FB} drops to the 750mV threshold. Because the MOSFETs are off, the load is supplied by the output capacitor. If the inductor current does not reach zero on any switching cycle, the controller immediately exits power-save and returns to forced continuous mode. Figure 6 shows power-save operation at light loads.

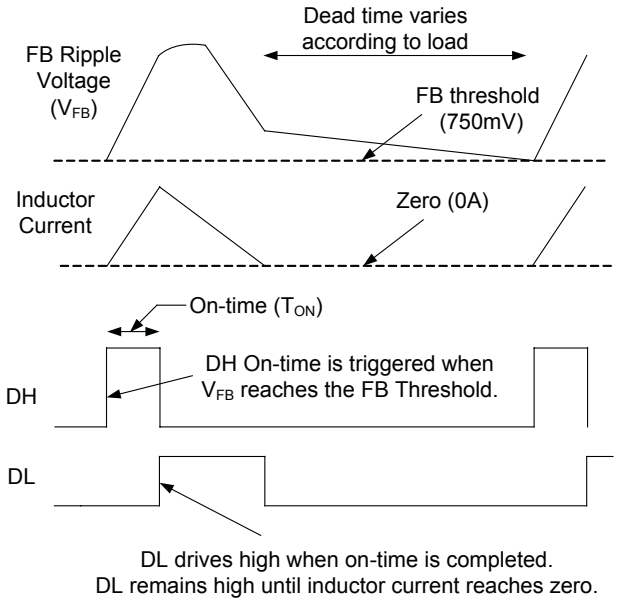


Figure 6 — Power-save Operation

Smart Power-save Protection

Active loads may leak current from a higher voltage into the switcher output. Under light load conditions with power-save enabled, this can force V_{OUT} to slowly rise and reach the over-voltage threshold, resulting in a hard shut-down. Smart power-save prevents this condition. When the FB voltage exceeds 10% above nominal (exceeds 825mV), the device immediately disables power-save, and DL drives high to turn on the low-side MOSFET. This draws current from V_{OUT} through the inductor and causes V_{OUT} to fall. When V_{FB} drops back to the 750mV trip point, a normal T_{ON} switching cycle begins. This method prevents a hard OVP shutdown and also cycles energy from V_{OUT} back to V_{IN}. It also minimizes operating power by avoiding forced conduction mode operation. Figure 7 shows typical waveforms for the Smart Power-save feature.

SmartDrive™

For each DH pulse, the DH driver initially turns on the high-side MOSFET at a slower speed, allowing a softer, smooth turn-off of the low-side diode. Once the DH node is high and the LX voltage has risen 1V above PGND, the SmartDrive circuit automatically drives the high-side MOSFET on at a rapid rate. This technique reduces ringing while maintaining high efficiency and also avoids the need for snubbers or series resistors in the gate drive.

Applications Information (continued)

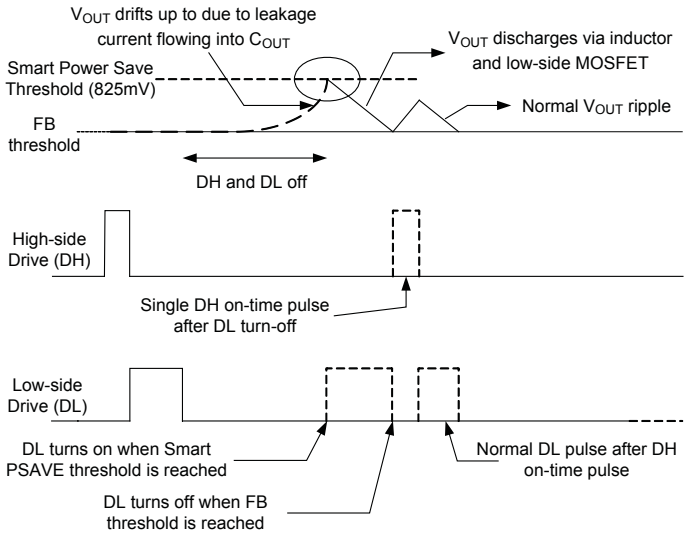


Figure 7 — Smart Power-save

Current Limit Protection

The device features programmable current limiting, which is accomplished by using the RDS_{ON} of the lower MOSFET for current sensing. The current limit is set by R_{ILIM} resistor. The R_{ILIM} resistor connects from the ILIM pin to the LXS pin which is also the drain of the low-side MOSFET. When the low-side MOSFET is on, an internal ~8µA current flows from the ILIM pin and through the R_{ILIM} resistor, creating a voltage drop across the resistor. While the low-side MOSFET is on, the inductor current flows through it and creates a voltage across the RDS_{ON}. The voltage across the MOSFET is negative with respect to ground. If this MOSFET voltage drop exceeds the voltage across R_{ILIM}, the voltage at the ILIM pin will be negative and current limit will activate. The current limit then keeps the low-side MOSFET on and will not allow another high-side on-time, until the current in the low-side MOSFET reduces enough to bring the ILIM voltage to zero. This method regulates the inductor valley current at the level shown by ILIM in Figure 8.

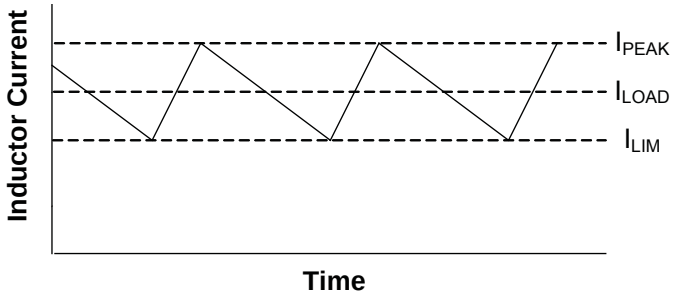


Figure 8 — Valley Current Limit

Setting the valley current limit to 6A results in a peak inductor current of 6A plus peak ripple current. In this situation, the average (load) current through the inductor is 6A plus one-half the peak-to-peak ripple current.

The internal 8µA current source is temperature compensated at 4100ppm in order to provide tracking with the RDS_{ON}.

The R_{ILIM} value is calculated by the following equation.

$$R_{ILIM} = 1250 \times I_{LIM} \times [0.088 \times (5V - V5V) + 1]$$

When selecting a value for R_{ILIM} do not exceed the absolute maximum voltage value for the ILIM pin. Note that because the low-side MOSFET with low RDS_{ON} is used for current sensing, the PCB layout, solder connections, and PCB connection to the LX node must be done carefully to obtain good results. R_{ILIM} should be connected directly to LXS (pin 24).

Soft-Start of PWM Regulator

Soft-start is achieved in the PWM regulator by using an internal voltage ramp as the reference for the FB comparator. The voltage ramp is generated using an internal charge pump which drives the reference from zero to 750mV in ~1.8mV increments, using an internal ~500kHz oscillator. When the ramp voltage reaches 750mV, the ramp is ignored and the FB comparator switches over to a fixed 750mV threshold. During soft-start the output voltage tracks the internal ramp, which limits the start-up inrush current and provides a controlled soft-start profile for a wide range of applications. Typical soft-start ramp time is 1.7ms.

Applications Information (continued)

During soft-start the regulator turns off the low-side MOSFET on any cycle if the inductor current falls to zero. This prevents negative inductor current, allowing the device to start into a pre-biased output. This soft start operation is implemented even if FCM is selected. FCM operation is allowed only after PGOOD is high.

Power Good Output

The power good (PGOOD) output is an open-drain output which requires a pull-up resistor. When the output voltage is 10% below the nominal voltage, PGOOD is pulled low. It is held low until the output voltage returns to the nominal voltage. PGOOD is held low during start-up and will not be allowed to transition high until soft-start is completed (when V_{FB} reaches 750mV) and typically 4ms has passed.

PGOOD will transition low if the V_{FB} pin exceeds +20% of nominal, which is also the over-voltage shutdown threshold (900mV). PGOOD also pulls low if the EN/PSV pin is low when V5V is present.

Output Over-Voltage Protection

Over-Voltage Protection (OVP) becomes active as soon as the device is enabled. The threshold is set at 750mV + 20% (900mV). When V_{FB} exceeds the OVP threshold, DL latches high and the low-side MOSFET is turned on. DL remains high and the controller remains off, until the EN/PSV input is toggled or V5V is cycled. There is a 5µs delay built into the OVP detector to prevent false transitions. PGOOD is also low after an OVP event.

Output Under-Voltage Protection

When V_{FB} falls to 75% of its nominal voltage (falls to 562.5mV) for eight consecutive clock cycles, the switcher is shut off and the DH and DL drives are pulled low to turn off the MOSFETs. The controller stays off until EN/PSV is toggled or V5V is cycled.

V5V UVLO, and POR

Under-Voltage Lock-Out (UVLO) circuitry inhibits switching and tri-states the DH/DL drivers until V5V rises above 2.9V. An internal Power-On Reset (POR) occurs when V5V exceeds 2.9V, which resets the fault latch and soft-start counter to begin the soft-start cycle. The SC414/SC424 then begins a soft-start cycle. The PWM will shut off if V5V falls below 2.7V.

LDO Regulator

The device features an integrated LDO regulator with a fixed output voltage of 5V. There is also an enable pin (ENL) for the LDO that provides independent control. The LDO voltage can also be used to provide the bias voltage for the switching regulator.

A minimum capacitance of 1µF referenced to AGND is normally required at the output of the LDO for stability. If the LDO is providing bias power to the device, then a minimum 0.1µF capacitor referenced to AGND is required, along with a minimum 1µF capacitor referenced to PGND to filter the gate drive pulses. Refer to the layout guidelines section.

LDO Start-up

Before start-up, the LDO checks the status of the following signals to ensure proper operation can be maintained.

1. ENL pin
2. VLDO output
3. V_{IN} input voltage

When the ENL pin is high, the LDO will begin start-up, see Figure 10. During the initial phase, when the LDO output voltage is near zero, the LDO initiates a current-limited start-up (typically 85mA) to charge the output capacitor. When V_{LDO} has reached 90% of the final value, the LDO current limit is increased to ~200mA and the LDO output is quickly driven to the nominal value by the internal LDO regulator.

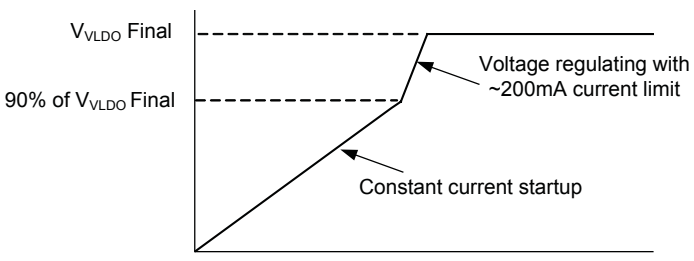


Figure 10 — LDO Start-Up

Applications Information (continued)

LDO Switch-Over Operation

The SC414/SC424 includes a switch-over function for the LDO. The switch-over function is designed to increase efficiency by using the more efficient DC-DC converter to power the LDO output, avoiding the less efficient LDO regulator when possible. The switch-over function connects the VLDO pin directly to the VOUT pin using an internal switch. When the switch-over is complete the LDO is turned off, which results in a power savings and maximizes efficiency. If the LDO output is used to bias the SC414/SC424, then after switch-over the device is self-powered from the switching regulator with the LDO turned off.

The switch-over logic waits for 32 switching cycles before it starts the switch-over. There are two methods that determine the switch-over of V_{LDO} to V_{OUT}.

In the first method, the LDO is already in regulation and the DC-DC converter is later enabled. As soon as the PGOOD output goes high, the 32 cycle counter is started. The voltages at the VLDO and VOUT pins are then compared; if the two voltages are within ±300mV (typically) of each other, within 32 cylces, the VLDO pin connects to the VOUT pin using an internal switch, and the LDO is turned off.

In the second method, the DC-DC converter is already running and the LDO is enabled. In this case the 32 cycles are started as soon as the LDO reaches 90% of its final value. At this time, the VLDO and VOUT pins are compared, and if within ±300mV (typically) the switch-over occurs and the LDO is turned off.

Switch-over Limitations on VOUT and VLDO

Because the internal switch-over circuit always compares the VOUT and VLDO pins at start-up, there are voltage limitations on permissible combinations of these pins. Consider the situation where V_{OUT} is programmed to 4.7V. After start-up, the device would connect VOUT to VLDO and disable the LDO, since the two voltage are within the ±300mV switch-over window. To avoid unwanted switch-over, the minimum difference between the voltages for V_{OUT} and V_{LDO} should be ±500mV.

Switch-over MOSFET Parasitic Diodes

The switch-over MOSFET contains parasitic diodes that are inherent to its construction, as shown in Figure 11.

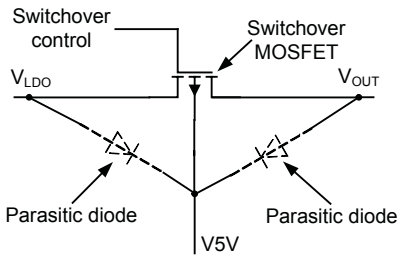


Figure 11— Switch-over MOSFET Parasitic Diodes

There are some important design rules that must be followed to prevent forward bias of these diodes. The following two conditions need to be satisfied in order for the parasitic diodes to stay off.

- $V5V \geq V_{LDO}$
- $V5V \geq V_{OUT}$

If either V_{LDO} or V_{OUT} is higher than V5V, then the respective diode will turn on and the SC414/SC424 operating current will flow through this diode. This has the potential of damaging the device.

ENL pin and V_{IN} UVLO

The ENL pin also acts as the switcher under-voltage lockout for the V_{IN} supply. The V_{IN} UVLO voltage is programmable via a resistor divider at the VIN, ENL, and AGND pins.

ENL is the enable/disable signal for the LDO. In order to implement the V_{IN} UVLO there is also a timing requirement that needs to be satisfied.

If the ENL pin transitions low within 2 switching cycles and is < 1V, then the LDO will turn off but the switcher remains on. If ENL goes below the V_{IN} UVLO threshold and stays above 1V, then the switcher will turn off but the LDO remains on.

The V_{IN} UVLO function has a typical threshold of 2.6V on the V_{IN} rising edge. The falling edge threshold is 2.4V.

Applications Information (continued)

Note that it is possible to operate the switcher with the LDO disabled, but the ENL pin must be below the logic low threshold (0.4V maximum). The table below summarizes the function of the ENL and EN pins, with respect to the rising edge of ENL.

EN	ENL	LDO status	Switcher status
low	low, < 0.4V	off	off
high	low, < 0.4V	off	on
low	high, < 2.6V	on	off
high	high, < 2.6V	on	off
low	high, > 2.6V	on	off
high	high, > 2.6V	on	on

Figure 12 below shows the ENL voltage thresholds and their effect on LDO and Switcher operation.

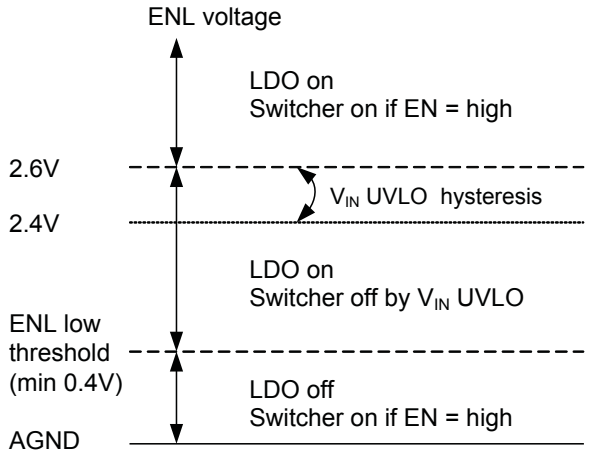


Figure 12 — ENL Thresholds

ENL Logic Control of PWM Operation

When the ENL input is driven above 2.6V, it is impossible to determine if the LDO output is going to be used to power the device or not. In self-powered operation where the LDO will power the device, it is necessary during the LDO start-up to hold the PWM switching off until the LDO has reached 90% of the final value. This prevents overloading the current-limited LDO output during the LDO start-up. However, if the switcher was previously operating (with EN/PSV high but ENL at ground, and V5V supplied externally), then it is undesirable to shut down the switcher. To prevent this, when the ENL input is above 2.6V (above the V_{IN} UVLO threshold), the internal logic checks the PGOOD signal. If PGOOD is high, then the switcher is already running and the LDO will run through the start-up cycle without affecting the switcher. If PGOOD is low, then the LDO will not allow any PWM switching until the LDO output has reached 90% of it's final value.

Using the On-chip LDO to Bias the SC414/SC424

The following steps must be followed when using the internal LDO to bias the device.

- Connect V5V to VLDO before enabling the LDO.
- Any external load on VLDO should not exceed 40mA until the LDO voltage has reached 90% of final value.
- Do not connect the EN pin directly to the V5V or any other supply voltage if Vout is greater than or equal to 4.5V

Many applications connect the EN pin to V5V and control the on/off of the LDO and PWM simultaneously with the ENL pin. This allows one signal to control both the bias and power output of the SC414. When V_{OUT} > 4.5V this configuration can cause problems due to the parasitic diodes in the LDO switchover circuitry. After the Vout > 4.5V PWM output is up and running the switchover diodes can hold up V5V > UVLO even if the ENL pin is grounded, turning off the LDO. Operating in this way can potentially damage the part.

Design Procedure

When designing a switch mode supply the input voltage range, load current, switching frequency, and inductor ripple current must be specified.

The maximum input voltage (V_{INMAX}) is the highest specified input voltage. The minimum input voltage (V_{INMIN}) is determined by the lowest input voltage after evaluating the voltage drops due to connectors, fuses, switches, and PCB traces.

The following parameters define the design.

- Nominal output voltage (V_{OUT})
- Static or DC output tolerance
- Transient response
- Maximum load current (I_{OUT})

Applications Information (continued)

There are two values of load current to evaluate — continuous load current and peak load current. Continuous load current relates to thermal stresses which drive the selection of the inductor and input capacitors. Peak load current determines instantaneous component stresses and filtering requirements such as inductor saturation, output capacitors, and design of the current limit circuit.

The following values are used in this design.

- V_{IN} = 12V ± 10%
- V_{OUT} = 1V ± 4%
- f_{SW} = 250kHz
- Load = 6A maximum

Frequency Selection

Selection of the switching frequency requires making a trade-off between the size and cost of the external filter components (inductor and output capacitor) and the power conversion efficiency.

The desired switching frequency is 250kHz which results from using components selected for optimum size and cost .

A resistor (R_{TON}) is used to program the on-time (indirectly setting the frequency) using the following equation.

$$R_{TON} = \frac{1}{25pF \times f_{SW}} - 400\Omega \times \frac{V_{IN}}{V_{OUT}}$$

To select R_{TON}, use the maximum value for V_{IN}, and for T_{ON} use the value associated with maximum V_{IN}.

$$T_{ON} = \frac{V_{OUT}}{V_{INMAX} \times f_{SW}}$$

T_{ON} = 303 ns at 13.2V_{IN}, 1V_{OUT}, 250kHz

Substituting for R_{TON} results in the following solution.

R_{TON} = 130.9kΩ, use R_{TON} = 130kΩ

Inductor Selection

In order to determine the inductance, the ripple current must first be defined. Low inductor values result in smaller size but create higher ripple current which can reduce efficiency. Higher inductor values will reduce the ripple current/voltage and for a given DC resistance are more efficient. However, larger inductance translates directly into larger packages and higher cost. Cost, size, output ripple, and efficiency are all used in the selection process.

The ripple current will also set the boundary for power-save operation. The switching will typically enter power-save mode when the load current decreases to 1/2 of the ripple current. For example, if ripple current is 4A then Power-save operation will typically start for loads less than 2A. If ripple current is set at 40% of maximum load current, then power-save will start for loads less than 20% of maximum current.

The inductor value is typically selected to provide a ripple current that is between 25% to 50% of the maximum load current. This provides an optimal trade-off between cost, efficiency, and transient performance.

During the DH on-time, voltage across the inductor is (V_{IN} - V_{OUT}). The equation for determining inductance is shown next.

$$L = \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{I_{RIPPLE}}$$

Example

In this example, the inductor ripple current is set equal to 50% of the maximum load current. Therefore ripple current will be 50% x 6A or 3A. To find the minimum inductance needed, use the V_{IN} and T_{ON} values that correspond to V_{INMAX}.

$$L = \frac{(13.2V - 1V) \times 318ns}{3A} = 1.26\mu H$$

A slightly larger value of 1.5µH is selected. This will decrease the maximum I_{RIPPLE} to 2.53A.

Note that the inductor must be rated for the maximum DC load current plus 1/2 of the ripple current.

The ripple current under minimum V_{IN} conditions is also checked using the following equations.

$$T_{ON\_VINMIN} = \frac{25pF \times R_{TON} \times V_{OUT}}{V_{INMIN}} + 10ns = 311ns$$

Applications Information (continued)

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{L}$$

$$I_{RIPPLE\_VINMIN} = \frac{(10.8 - 1V) \times 311ns}{1.5\mu H} = 2.03A$$

Capacitor Selection

The output capacitors are chosen based on required ESR and capacitance. The maximum ESR requirement is controlled by the output ripple requirement and the DC tolerance. The output voltage has a DC value that is equal to the valley of the output ripple plus 1/2 of the peak-to-peak ripple. Change in the output ripple voltage will lead to a change in DC voltage at the output.

The design goal is for the output voltage regulation to be ±4% under static conditions. The internal 750mV reference tolerance is 1%. Assuming a 1% tolerance from the FB resistor divider, this allows 2% tolerance due to V_{OUT} ripple. Since this 2% error comes from 1/2 of the ripple voltage, the allowable ripple is 4%, or 40mV for a 1V output.

The maximum ripple current of 2.53A creates a ripple voltage across the ESR. The maximum ESR value allowed is shown by the following equations.

$$ESR_{MAX} = \frac{V_{RIPPLE}}{I_{RIPPLEMAX}} = \frac{40mV}{2.53A}$$

$$ESR_{MAX} = 15.8\ m\Omega$$

The output capacitance is chosen to meet transient requirements. A worst-case load release, from maximum load to no load at the exact moment when inductor current is at the peak, determines the required capacitance. If the load release is instantaneous (load changes from maximum to zero in < 1µs), the output capacitor must absorb all the inductor's stored energy. This will cause a peak voltage on the capacitor according to the following equation.

$$COUT_{MIN} = \frac{L\left(I_{OUT} + \frac{1}{2} \times I_{RIPPLEMAX}\right)^2}{(V_{PEAK})^2 - (V_{OUT})^2}$$

Assuming a peak voltage V_{PEAK} of 1.150 (100mV rise upon load release), and a 6A load release, the required capacitance is shown by the next equation.

$$COUT_{MIN} = \frac{1.5\mu H\left(6A + \frac{1}{2} \times 2.53A\right)^2}{(1.05V)^2 - (1V)^2}$$

$$COUT_{MIN} = 772\mu F$$

If the load release is relatively slow, the output capacitance can be reduced. At heavy loads during normal switching, when the FB pin is above the 750mV reference, the DL output is high and the low-side MOSFET is on. During this time, the voltage across the inductor is approximately $-V_{OUT}$. This causes a down-slope or falling di/dt in the inductor. If the load di/dt is not much faster than the -di/dt in the inductor, then the inductor current will tend to track the falling load current. This will reduce the excess inductive energy that must be absorbed by the output capacitor, therefore a smaller capacitance can be used.

The following can be used to calculate the needed capacitance for a given dI_{LOAD}/dt. Peak inductor current is shown by the next equation.

$$I_{LPK} = I_{MAX} + 1/2 \times I_{RIPPLEMAX}$$

$$I_{LPK} = 6A + 1/2 \times 2.53A = 7.26A$$

$$\text{Rate of change of Load Current} = \frac{dI_{LOAD}}{dt}$$

I_{MAX} = maximum load release = 6A

$$C_{OUT} = I_{LPK} \times \frac{L \times \frac{I_{LPK}}{V_{OUT}} - \frac{I_{MAX}}{dI_{LOAD}} \times dt}{2(V_{PK} - V_{OUT})}$$

Example

$$\frac{dI_{LOAD}}{dt} = \frac{1.25A}{1\mu s}$$

Applications Information (continued)

This causes the output current to move from 6A to 0A in 4.8µs, giving the minimum output capacitance requirement shown in the following equation.

$$C_{OUT} = 7.26A \times \frac{1.5\mu H \times \frac{7.26A}{1V} - \frac{6A}{1.25A} \times 1\mu s}{2(1.05V - 1V)}$$

$$C_{OUT} = 443\mu F$$

Note that C_{OUT} is much smaller in this example, 443µF compared to 772µF based on a worst-case load release. To meet the two design criteria of minimum 443µF and maximum 15mΩ ESR, select two capacitors rated at 220µF and 15mΩ ESR or less.

It is recommended that an additional small capacitor be placed in parallel with C_{OUT} in order to filter high frequency switching noise.

Stability Considerations

Unstable operation is possible with adaptive on-time controllers, and usually takes the form of double-pulsing or ESR loop instability.

Double-pulsing occurs due to switching noise seen at the FB input or because the FB ripple voltage is too low. This causes the FB comparator to trigger prematurely after the minimum off-time has expired. In extreme cases the noise can cause three or more successive on-times. Double-pulsing will result in higher ripple voltage at the output, but in most applications it will not affect operation. This form of instability can usually be avoided by providing the FB pin with a smooth, clean ripple signal that is at least 10mVp-p, which may dictate the need to increase the ESR of the output capacitors. It is also imperative to provide a proper PCB layout as discussed in the Layout Guidelines section.

Another way to eliminate doubling-pulsing is to add a small (~ 10pF) capacitor across the upper feedback resistor, as shown in Figure 13. This capacitor should be left unpopulated unless it can be confirmed that double-pulsing exists. Adding the C_{TOP} capacitor will couple more ripple into FB to help eliminate the problem. An optional connection on the PCB should be available for this capacitor.

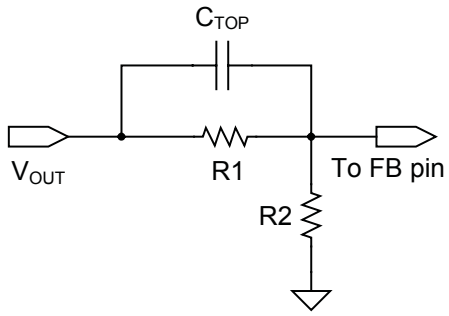


Figure 13 — Capacitor Coupling to FB Pin

ESR loop instability is caused by insufficient ESR. The details of this stability issue are discussed in the ESR Requirements section. The best method for checking stability is to apply a zero-to-full load transient and observe the output voltage ripple envelope for overshoot and ringing. Ringing for more than one cycle after the initial step is an indication that the ESR should be increased.

One simple way to solve this problem is to add trace resistance in the high current output path. A side effect of adding trace resistance is a decrease in load regulation.

ESR Requirements

A minimum ESR is required for two reasons. One reason is to generate enough output ripple voltage to provide 10mVp-p at the FB pin (after the resistor divider) to avoid double-pulsing.

The second reason is to prevent instability due to insufficient ESR. The on-time control regulates the valley of the output ripple voltage. This ripple voltage is the sum of the two voltages. One is the ripple generated by the ESR, the other is the ripple due to capacitive charging and discharging during the switching cycle. For most applications, the total output ripple voltage is dominated by the output capacitors, typically SP or POSCAP devices. For stability the ESR zero of the output capacitor should be lower than approximately one-third the switching frequency. The formula for minimum ESR is shown by the following equation.

$$ESR_{MIN} = \frac{3}{2 \times \pi \times C_{OUT} \times f_{sw}}$$

Applications Information (continued)

Using Ceramic Output Capacitors

When applications use ceramic output capacitors, the ESR is normally too small to meet the previously stated ESR criteria. In these applications it is necessary to add a small virtual ESR network composed of two capacitors and one resistor, as shown in Figure 14. This network creates a ramp voltage across C_L, analogous to the ramp voltage generated across the ESR of a standard capacitor. This ramp is then capacitively coupled into the FB pin via capacitor C_C.

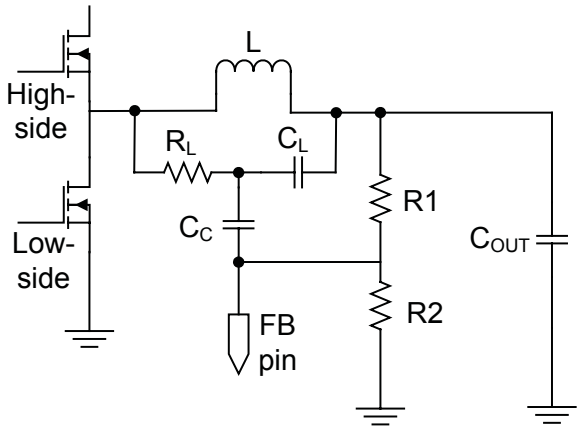


Figure 14 — Virtual ESR Ramp Current

Output Voltage Dropout

The output voltage adjustable range for continuous-conduction operation is limited by the fixed 320ns (typical) minimum off-time. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on and off times.

The duty-factor limitation is shown by the next equation.

$$DUTY = \frac{T_{ON(MIN)}}{T_{ON(MIN)} + T_{OFF(MIN)}}$$

The inductor resistance and MOSFET on-state voltage drops must be included when performing worst-case dropout duty-factor calculations.

System DC Accuracy — V_{OUT} Controller

Three factors affect V_{OUT} accuracy: the trip point of the FB error comparator, the ripple voltage variation with line and load, and the external resistor tolerance. The error comparator offset is trimmed so that under static conditions it trips when the feedback pin is 750mV, 1%.

The on-time pulse from the SC414/SC424 in the design example is calculated to give a pseudo-fixed frequency of 250kHz. Some frequency variation with line and load is expected. This variation changes the output ripple voltage. Because constant on-time converters regulate to the valley of the output ripple, ½ of the output ripple appears as a DC regulation error. For example, if the output ripple is 50mV with V_{IN} = 6 volts, then the measured DC output will be 25mV above the comparator trip point. If the ripple increases to 80mV with V_{IN} = 25V, then the measured DC output will be 40mV above the comparator trip. The best way to minimize this effect is to minimize the output ripple.

To compensate for valley regulation, it may be desirable to use passive droop. Take the feedback directly from the output side of the inductor and place a small amount of trace resistance between the inductor and output capacitor. This trace resistance should be optimized so that at full load the output droops to near the lower regulation limit. Passive droop minimizes the required output capacitance because the voltage excursions due to load steps are reduced as seen at the load.

The use of 1% feedback resistors may result in up to an additional 1% error. If tighter DC accuracy is required, resistors with lower tolerances should be used.

The output inductor value may change with current. This will change the output ripple and therefore will have a minor effect on the DC output voltage. The output ESR also affects the output ripple and thus has a minor effect on the DC output voltage.

Switching Frequency Variations

The switching frequency will vary depending on line and load conditions. The line variations are a result of fixed propagation delays in the on-time one-shot, as well as unavoidable delays in the external MOSFET switching. As V_{IN} increases, these factors make the actual DH on-time slightly longer than the ideal on-time. The net effect is that frequency tends to falls slightly with increasing input voltage.

Applications Information (continued)

The switching frequency also varies with load current as a result of the power losses in the MOSFETs and the inductor. For a conventional PWM constant-frequency converter, as load increases the duty cycle also increases slightly to compensate for IR and switching losses in the MOSFETs and inductor. A constant on-time converter must also compensate for the same losses by increasing the effective duty cycle (more time is spent drawing energy from V_{IN} as losses increase). The on-time is essentially constant for a given V_{OUT} and V_{IN} combination, to offset the losses the off-time will tend to reduce slightly as load increases. The net effect is that switching frequency increases slightly with increasing load.

PCB Layout Guidelines

The optimum layout for the SC414/SC424 is shown in Figure 15. This layout shows an integrated FET buck regulator with a maximum current of 6A. The total PCB area is approximately 20 x 25 mm.

Critical Layout Guidelines

The following critical layout guidelines must be followed to ensure proper performance of the device.

- IC Decoupling capacitors
- PGND plane
- AGND island
- FB, VOUT, and other analog control signals
- BST, ILIM, and LX
- Capacitors and Current Loops

IC Decoupling Capacitors

- A 0.1 µF capacitor must be located as close as possible to the IC and directly connected to pins 2 (V5V) and 3 (AGND).

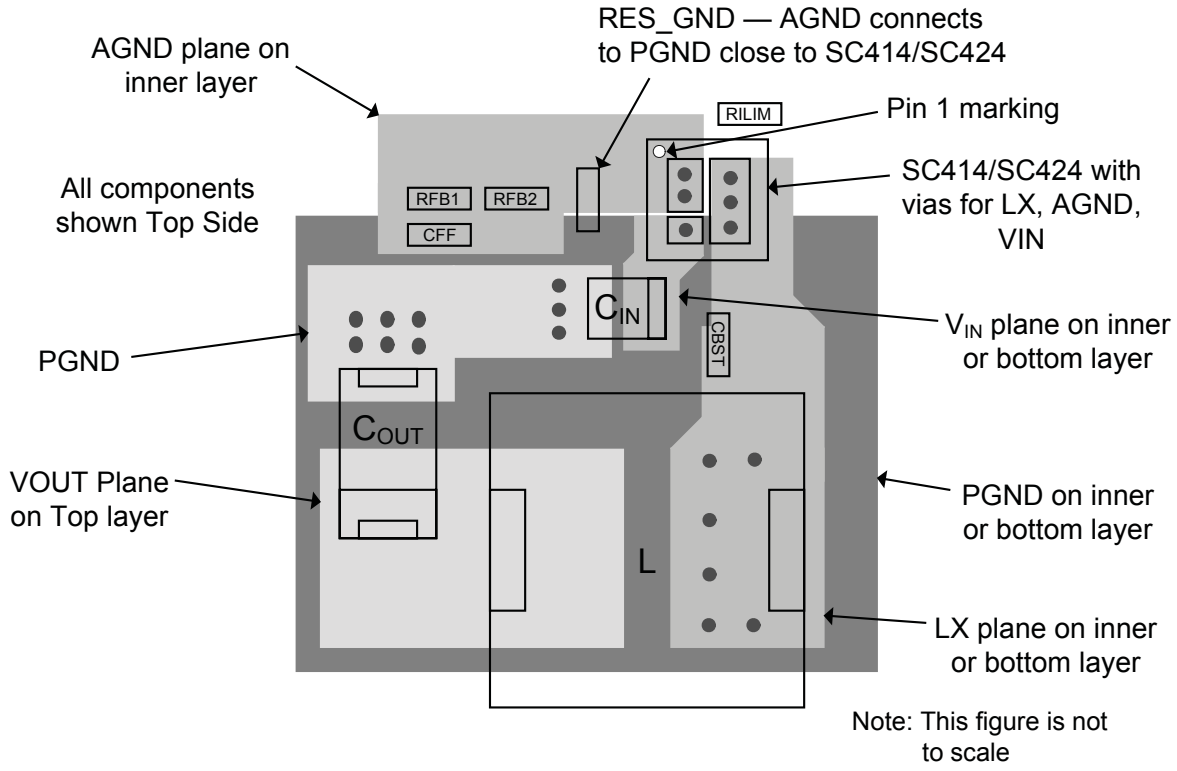


Figure 15 — PCB Layout

Applications Information (continued)

- All other decoupling capacitors must be located as close as possible to the IC.

PGND Plane

- PGND requires its own copper plane with no other signal traces routed on it.
- Copper planes, multiple vias, and wide traces are needed to connect PGND to input capacitors, output capacitors, and the PGND pins on the IC.
- The PGND copper area between the input capacitors, output capacitors, and PGND pins must be as small as and as compact as possible to reduce the area of the PCB that is exposed to noise due to current flow on this node.
- Connect PGND to AGND with a short trace or 0Ω resistor. This connection should be as close to the IC as possible.

AGND Island

- AGND should have its own island of copper with no other signal traces routed on this layer that connects the AGND pins and pad of the IC to the analog control components.
- All of the components for the analog control circuitry should be located so that the connections to AGND are done by wide copper traces or vias down to AGND.
- Connect PGND to AGND with a short trace or 0Ω resistor. This connection should be as close to the IC as possible.

FB, VOUT, and Other Analog Control Signals

- The connection from the V_{OUT} power to the analog control circuitry must be routed from the output capacitors and located on a quiet layer.
- The traces between VOUT and the analog control circuitry (VOUT, and FB pins) must be short and routed away from noise sources, such as BST, LX, VIN, and PGND between the input capacitors, output capacitors, and the IC.
- ILIM and TON nodes must be as short as possible to ensure the best accuracy in current limit and on time.
- R_{ILIM} should be close to the IC and connected to LXS with a Kelvin trace to pin 24 on the IC. This will be a sufficient connection and will prevent the need to connect the resistor further into the LX plane.
- The feedback components for the switcher need to be as close to the FB pin of the IC as possible to reduce the possibility of noise corrupting these analog signals.

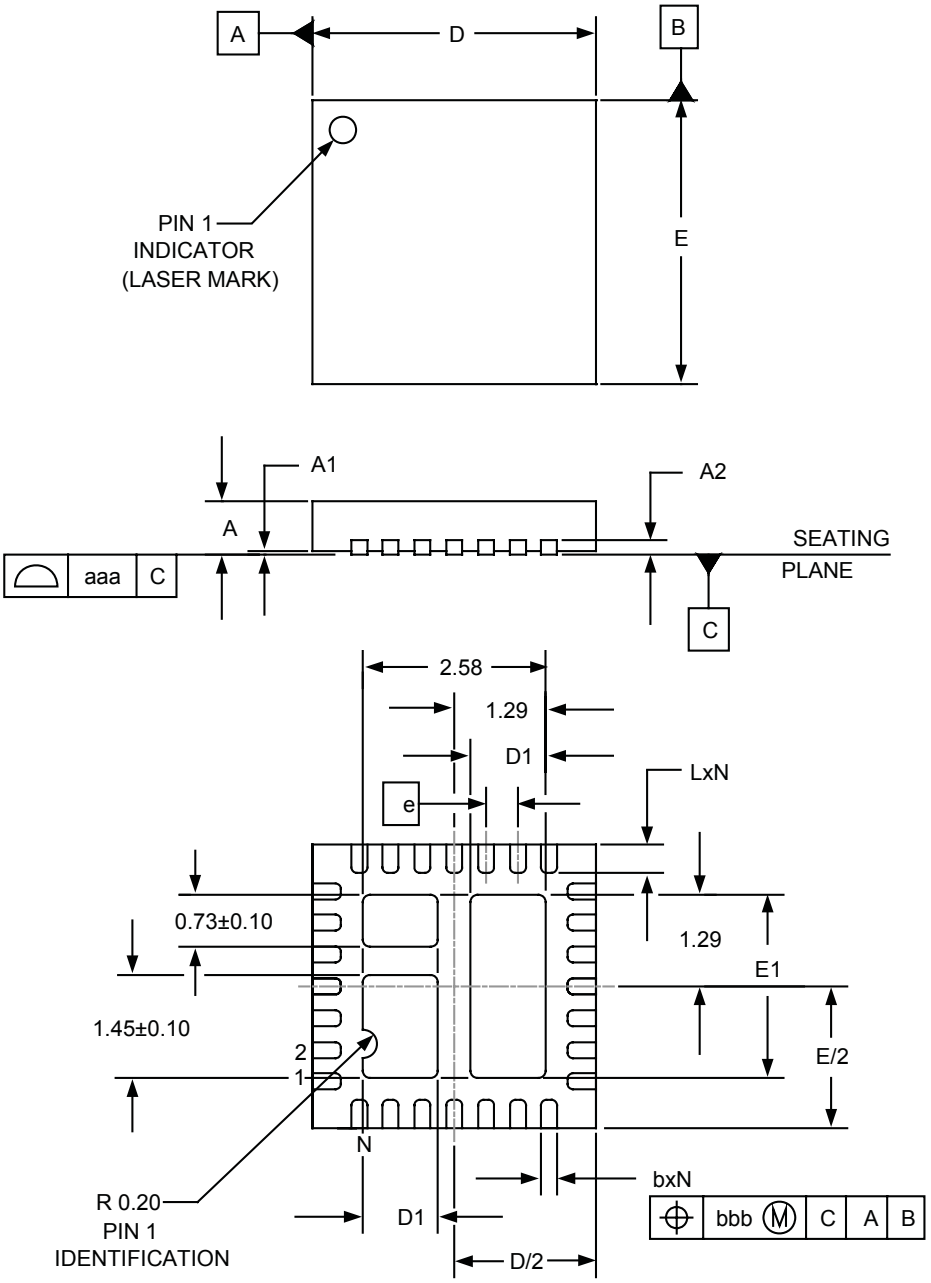
BST, ILIM and LX

- LX and BST are very noisy nodes and must be carefully routed to minimized the PCB area that is exposed to these signals.
- The connections for the boost capacitor between the IC and LX must be short and directly connected to the LXBST (pin 12).
- The connections for the current limit resistor between the ILIM pin and LX must be as short as possible and directly connected to pin 24 (LXS).
- The LX node between the IC and the inductor should be wide enough to handle the inductor current and short enough to eliminate the possibility of LX noise corrupting other signals.
- Multiple vias should be used to provide a good connection to LX between the IC and the inductor.

Capacitors and Current Loops

- The current loops between the input capacitors, the IC, the inductor, and the output capacitors must be as close as possible to each other to reduce IR drop across the copper.
- All bypass and output capacitors must be connected as close as possible to the respective pin on the IC.

Outline Drawing — MLPQ-4x4-28

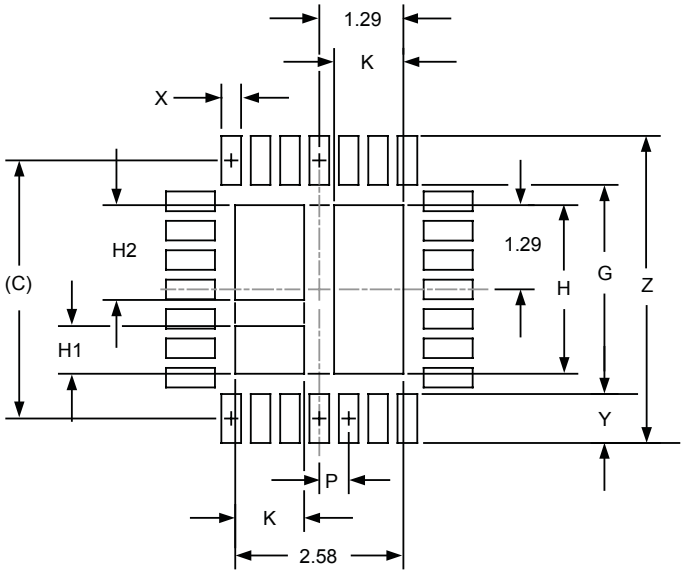


DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	-	1.00
A1	0.00	-	0.05
A2	-	(0.20)	-
b	0.17	0.23	0.29
D	3.90	4.00	4.10
D1	0.96	1.06	1.16
E	3.90	4.00	4.10
E1	2.48	2.58	2.68
e	0.45 BSC		
L	0.30	0.40	0.50
N	28		
aaa	0.08		
bbb	0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Land Pattern — MLPQ-4x4-28



DIMENSIONS	
DIM	MILLIMETERS
C	(3.95)
G	3.20
H	2.58
H1	0.73
H2	1.45
K	1.06
P	0.45
X	0.30
Y	0.75
Z	4.70

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. SQUARE PACKAGE-DIMENSIONS APPLY IN BOTH X AND Y DIRECTIONS.

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