Boot Capacitor Regulation in LM25007 Constant-On-Time (COT) Converter

National Semiconductor
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The Issue

LM25000 series of constant-on-time (COT) integrated regulators provide a simple, cost-effective way of implementing a step down buck regulator with nearly fixed frequency. Non-synchronous operation reduces switching frequency at very light load resulting in higher efficiency than a comparable fixed frequency converter. The non-synchronous operation, however, causes two problems related to boot capacitor regulation under certain operating conditions.

Bootstrap capacitor (C_{BST}) may have insufficient voltage during startup if a voltage is present at the output of the converter see *Figure 1*. This voltage is usually referred to as prebias. Since, at startup, there is no current in the inductor (L), the prebias voltage at the output appears at the switch node. If this prebias voltage is high such that the boot capacitor voltage (V_{BST}=V_{CC}-V_{SW}) is lower than the threshold voltage (V_{TH}) of high side gate, the high side switch fails to turn 'on' and the converter fails to startup see *Figure 2* . This condition persists until prebias is removed. A prebias is often caused by some leakage path in downstream circuits, e.g., a logic circuit or FPGA with a pin pulled high, or leftover charge from a previous power down.

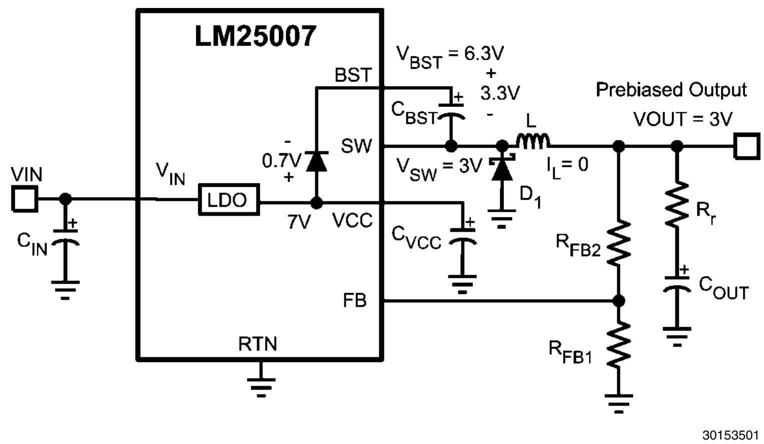

FIGURE 1. LM25007 Application with Prebiased Output

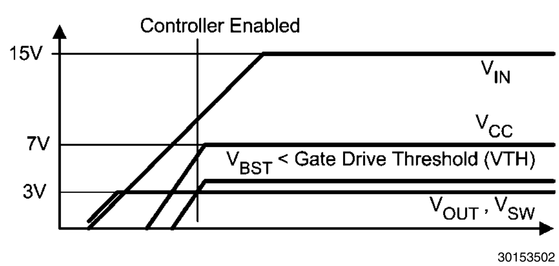

FIGURE 2. Startup with Prebiased Output

A similar situation may occur under light load or no load conditions see *Figure 3*. At light load/no load, the inductor current is discontinuous causing the diode (D1) to turn off for a relatively long off time. During this time the bootstrap capacitor (C_{BST}) may discharge to a level below the top side FET gate drive threshold (V_{TH}), which is normally around 5V. Under these conditions the top side FET fails to turn on and the output voltage is no longer regulated. Since there is no current in the inductor, this output voltage appears at the switch node (V_{SW}=V_{OUT}). As V_{OUT}, and therefore VSW, drops, the bootstrap capacitor voltage rises and is given by V_{BST} = V_{CC}-V_{OUT}. When V_{CC}-V_{OUT} > V_{TH}, the hi-side FET turns on again and the switching resumes bringing the VOUT to the target level. At that time, if the low load condition persists, the whole cycle will repeat itself, causing a hiccup mode operation in which V_{OUT} fall to V_{CC}-V_{TH} and rises back to the target level. This loss of regulation is undesirable in many applications.

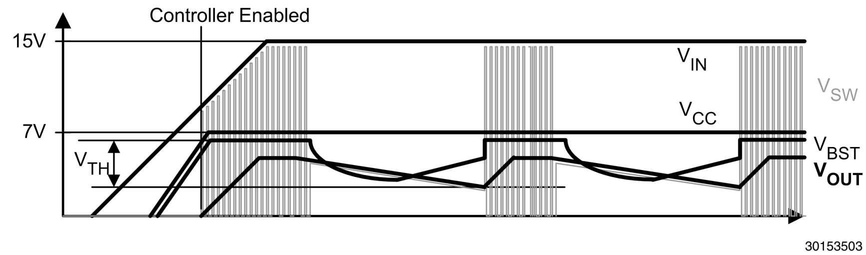

FIGURE 3. Hiccup Mode Operation at No Load

The Solution

For prebiased startup problem, the source of prebias should be removed if possible. If the prebias source is some leakage path in the downstream logic circuit, the system designer should consider the option of tying unused logic pin, which is the source of leakage, low. In some cases, this leakage path may be difficult to identify, or a necessary part of design. In other cases, the source of prebias may be a stiff source, e.g., a battery or super capacitor at the output of the converter. The system designer can choose from the techniques described below depending on the constraints of his design.

INCREASING BOOT CAPACITOR (CBST)

The designer can increase the boot capacitor value so that during no load boot capacitor is not discharged below the gate threshold of high side switch before V_{OUT}, and hence V_{FB}, falls below the reference. The hiccup free operation should be verified for whole input voltage (V_{IN}) range. The designer should not exceed the recommended boot capacitor value in the datasheet. This method does not help in case of prebiased output.

REDUCING FEEDBACK RESISTORS (RFB1, RFB2)

In no load condition, feedback Resistors, FB1 and FB2, constitute the total load at the output of the converter. These should be chosen so that V_{OUT} and hence V_{FB} fall below the reference level faster than V_{BST} falls below the gate threshold (V_{TH}). The hiccup free operation should be verified for whole input voltage (V_{IN}) range.

For prebiased outputs during startup, reducing the feedback resistors effectively pulls the V_{OUT} and V_{SW} closer to ground, thereby raising the boot capacitor (C_{BST}) voltage. The extent of this pull down however depends on the strength and voltage level of the prebias source. This method of counteracting prebias is limited to weak prebias sources or leftover charge on output capacitor (C_{OUT}) from previous power cycle.

RAISING VBST USING EXTERNAL CIRCUIT

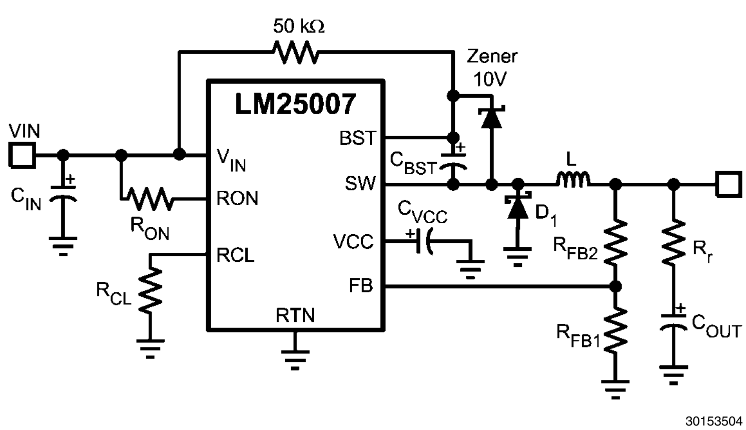

FIGURE 4. Raising Boot Capacitor Voltage Using External Circuit

If none of the simpler solutions presented above are sufficient, an external pull up circuit can be used to raise the boot capacitor voltage (V_{BST}) above gate threshold (V_{TH}) of high side switch. An example circuit is shown in *Figure 4*. The 50kΩ pull up resistor pulls BST pin up while limiting the current drawn from V_{IN}. The 10V zener prevents the boot capacitor voltage from exceeding the maximum voltage rating between BST and SW pins. This method is effective for no load as well as prebiased output conditions. The designer should select the pull up resistor to optimize the voltage drop across it and the power dissipation in the pull up resistor and the zener.

Notes

Notes

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