

### FEATURES

#### UHF High Performance Transceiver

- Frequency bands
  - 862 MHz to 928 MHz
  - 431 MHz to 464 MHz
- Data rates supported
  - 1 kbps to 300 kbps
- Receiver sensitivity (BER)
  - 107.5 dBm at 38.4 kbps, 2FSK
- Single ended and differential PA
- Fully automatic frequency control loop (AFC)
- Low External BOM
- Integrated PLL loop filter & antenna switch
- On-chip Hardware packet handling
  - Highly flexible for a wide range of packet formats
  - Automatic address filtering
  - Automatic CRC insertion / check

#### Power

- Supply Range: 1.8 V to 3.6 V
- Power Consumption:
  - 680 nA, in power down mode, non-retained state
  - 1.6  $\mu$ A, in power down mode, MCU memory and transceiver memory retained
  - 190  $\mu$ A / MHz, Cortex in Active mode
  - 12.8 mA transceiver in receive mode, Cortex in power down mode
  - 9 to 32 mA transceiver in transmit mode, Cortex in power down mode

#### Analog I/O

- Multi-Channel, 14-bit ADC
- Programmable data rate up to 500kSPS
- On-Chip Voltage Reference and Temperature Sensor
- Single ended and differential inputs

#### Microcontroller

- ARM Cortex™-M3 32-bit processor
- Serial Wire download and debug
- External Watch crystal for wakeup timer
- 16 MHz Oscillator with 8-way Programmable Divider

#### Memory

- 128k Bytes Flash/EE Memory, 16k Bytes SRAM
- 20000 cycle Flash/EE endurance
- 10 year Flash/EE retention
- In-circuit download via Serial Wire and UART

#### On-Chip Peripherals

- UART, I<sup>2</sup>C and SPI Serial I/O
- 29-Pin GPIO Port
- 2 General Purpose Timers
- Wake-up Timer
- Watchdog Timer
- 8-Channel PWM

#### Packages and Temperature Range

- 64 lead LFCSP (9mm x 9mm) package -40°C to 85°C

#### Tools

- Low-Cost Development System
- Third-Party Compiler and emulator tool Support

### FUNCTIONAL BLOCK DIAGRAM

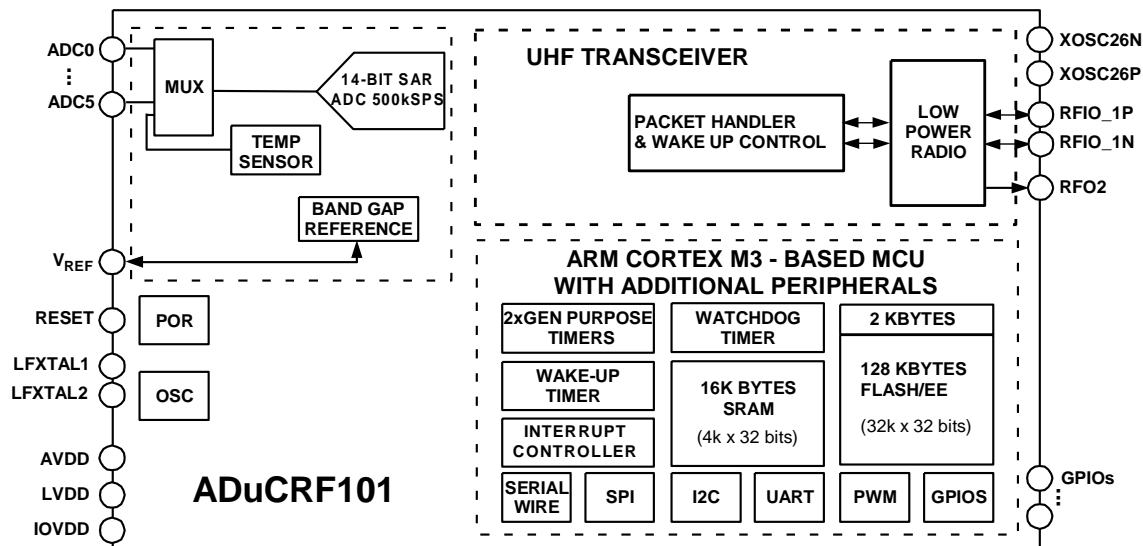


Figure 1.

#### Rev. PrD

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## GENERAL DESCRIPTION

The ADuCRF101 is a fully integrated System On Chip (SOC) solution designed for low power wireless applications. It includes 431-464 MHz and 862-928 MHz UHF transceiver, low power Cortex-M3 core from ARM and Flash/EE memory in a dual stacked die configuration, packaged in a 9 mm x 9 mm LFCSP.

The device operates directly from a 3.6V battery and is specifically designed for low power operation using an autonomous packet handler to minimise system current consumption during wireless communications.

The UHF transceiver is based on the ADF7023 device, a very low power, highly integrated 2FSK/GFSK/OOK transceiver designed for operation in the frequency bands, 861MHz to 928MHz and 431MHz to 464MHz, which cover the worldwide license-free ISM bands at 433 MHz, 868 MHz and 915 MHz. It is suitable for circuit applications that operate under the European ETSI EN300-220, the North American FCC (Part 15), the Chinese short range wireless regulatory standards or other similar regional standards. Data rates from 1kbps to 300kbps are supported.

The ADuCRF101 integrates a low power Cortex-M3 core from ARM. It is a 32-bit RISC machine, offering up to 1.25 DMIPS peak performance. The Cortex-M3 MCU also has a flexible 14-channel DMA controller. 128k Bytes of non-volatile Flash/EE and 16k Bytes of SRAM are also provided on-chip.

The device operates from an on-chip oscillator generating an internal 16MHz high-frequency clock. This clock is routed through a programmable clock divider from which the MCU core clock operating frequency is generated.

The SOC also integrates a range of on-chip peripherals which can be configured under microcontroller software control as required in the application. These peripherals include UART, I<sup>2</sup>C and SPI Serial I/O communication controllers, 6-Channel ADC, a 29-Pin GPIO Port, 8-Channel PWM, 2 General Purpose Timers, Wake-up Timer and System Watchdog Timer

The ADC consists of 6 single ended inputs used for ratio metric measurements on external sensors. These sensors can be powered temporarily from the internal LDO for the measurements. An internal battery monitor channel is also available.

The SOC is specifically designed to operate in battery powered applications where low power operation is critical. The SOC can be configured in normal operating mode consuming 190  $\mu$ A/MHz or different low power modes under direct program control, including hibernate mode (internal wake-up timer active) consuming 1.6  $\mu$ A. In hibernate mode, peripherals such as external interrupts, UHF transceiver and wake up timer can wake up the device. This allows the part to operate in an ultra-low power operating mode and still respond to active radio communication events, approximately 14 mA with UHF receiver on. A non-retain state mode is also provided, consuming as low 680 nA. In this mode, external interrupts can wake up the part.

On-chip factory firmware supports in-circuit serial download via UART interface. Non-intrusive emulation and in-circuit download is supported via the serial wire interface. These features are incorporated into a low-cost Development System supporting this Precision Analog Microcontroller family.

The part operates from 1.8 V to 3.6 V and are specified over an industrial temperature range of -40°C to 85°C.

## SPECIFICATIONS

### POWER SPECIFICATIONS

VBAT = IOVDD = 1.8 V to 3.6 V,  $V_{REF} = 1.25V$  internal reference,  $f_{CORE} = 16$  MHz, all specifications  $T_A = T_{MAX}$  to  $T_{MIN}$ , unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER CONSUMPTION					
Cortex in SHUTDOWN mode		680		nA	UHF transceiver in sleep mode, memory not retained
Cortex in HIBERNATE mode					Wake up timer running from external 32kHz crystal, 8kB of SRAM retained (8kB non-retained)
UHF transceiver in sleep mode, memory retained		1.6		μA	
UHF transceiver in sleep mode, memory not retained		1.38		μA	
UHF transceiver in receive mode		12.8		mA	
UHF transceiver in transmit mode		9 to 32		mA	
Cortex active, UHF transceiver active					UHF transceiver in PHY_ON or PHY_OFF state
Static current		1.8		mA	
Dynamic current		190		μA/MHz	
STARTUP TIME					
Cortex at Power On		40		ms	
From SLEEP mode		3 to 5		FCLK	FCLK is the Cortex-M3 clock or divided version of the 16MHz oscillator.
Cortex from HIBERNATE mode		12		μs	
Cortex from SHUTDOWN mode		40		ms	
UHF transceiver from sleep mode		225		μs	
POWER REQUIREMENTS					
Power Supply Voltage Range					
VBAT and IOVDD <sup>1</sup>	1.8		3.6V	V	

<sup>1</sup> These numbers are not production tested, but are guaranteed by design and/or characterization data at production release.

## MICROCONTROLLER ELECTRICAL SPECIFICATIONS

VBAT = IOVDD = 1.8 V to 3.6 V,  $V_{REF} = 1.25V$  internal reference,  $f_{CORE} = 16$  MHz, all specifications  $T_A = T_{MAX}$  to  $T_{MIN}$ , unless otherwise noted.

**Table 2.**

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
<b>ADC CHANNEL SPECIFICATIONS</b>					
ADC Power-up Time		5		μs	Eight acquisition clocks and $f_{ADC}/2$ Excludes reference power up time
DC Accuracy					
Resolution		14		Bits	
Integral Nonlinearity		±1		LSB	$V_{REF} = 1.25V$
		±2		LSB	$V_{REF} = 1.8V$ from LDO
Differential Nonlinearity		±1		LSB	
DC Code Distribution		2		LSB	ADC input is a DC voltage
<b>CALIBRATED ENDPOINT ERRORS<sup>1</sup></b>					
Offset Error		±2.5	TBD	LSB	
Offset Error Match		±1		LSB	
Gain Error		±5	TBD	LSB	
Gain Error Match		±1		LSB	
<b>DYNAMIC PERFORMANCE</b>					
Signal-to-Noise Ratio (SNR)		-80		dB	$f_{IN} = 10$ kHz sine wave, $f_{SAMPLE} = 500$ kSPS
Total Harmonic Distortion (THD)		TBD			
Peak Harmonic or Spurious Noise (PHSN)		TBD			
Channel-to-Channel Crosstalk		TBD			Measured on adjacent channels
<b>ANALOG INPUT</b>					
<b>Input Voltage Ranges<sup>2</sup></b>					
Single ended input	0		$V_{REF}$	V	
Differential input	0		$V_{CM} \pm V_{REF}/2$	V	
Leakage Current		100		nA	
Input Capacitance		20		pF	During ADC Acquisition
<b>ON-CHIP VOLTAGE REFERENCE</b>					
Output Voltage		1.25		V	
Accuracy		±5		mV	Measured at $T_A = 25^\circ C$
Reference Temperature Coefficient		±40		ppm/°C	
Power Supply Rejection Ratio		60		dB	
Output Impedance		2		Ω	
Internal $V_{REF}$ Power-On Time		5		ms	0.47μF external capacitor
<b>TEMPERATURE SENSOR<sup>2,3</sup></b>					
Voltage Output at 25°C		TBD		mV	
Voltage TC		TBD		mV/°C	
Accuracy		TBD		°C	MCU in low power mode
Thermal impedance		TBD			
<b>POWER SUPPLY MONITOR (PSM)</b>					
Trip Point voltage		TBD		V	
Trip Point accuracy		TBD		%	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER-ON-RESET		TBD		V	
Watchdog Timer (WDT) <sup>2</sup>					
Timeout Period	0		512	s	Programmable
Flash/EE MEMORY <sup>2</sup>					
Endurance <sup>4</sup>	20,000			Cycles	
Data Retention <sup>5</sup>	10			Years	T <sub>J</sub> = 85°C
Digital Inputs					All digital inputs including LFXCLK1 and LFXCLK2
Logic 1 Input Current (leakage current)		50		nA	V <sub>INH</sub> = IOVDD or V <sub>INH</sub> = 1.8V, pull up disabled.
Logic 0 Input Current (leakage current)		50		nA	V <sub>INL</sub> = 0V, pull up disabled.
Input Capacitance		10		pF	
Logic Inputs					All Logic inputs including LFXCLK1 and LFXCLK2
VINL, Input Low Voltage			0.2 x IOVDD	V	
VINH, Input High Voltage	0.7 x IOVDD			V	
Logic Outputs					
VOH, Output High Voltage	IOVDD – 0.4			V	I <sub>source</sub> = 1mA
VOL, Output Low Voltage			0.4	V	I <sub>sink</sub> = 1mA
CRYSTAL INPUTS LFX TAL1 and LFX TAL2					32.768 kHz crystal, for use with timers and/or UHF transceiver wake up controller, see Table 6.
LFX TAL1 Input Capacitance		2		pF	
LFX TAL2 Output Capacitance		2		pF	
MCU CLOCK RATE <sup>2</sup>			16	MHz	8 programmable core clock selections within this range.
INTERNAL HF OSCILLATOR		16		MHz	
Tolerance		±3		%	
INTERNAL LF OSCILLATOR		32.768		kHz	
Tolerance		±20		%	
EXTERNAL CLOCK INPUT (P0.5)					
Range <sup>2</sup>	32.768		16000	kHz	

<sup>1</sup> Measured using the factory-set default values in the ADC offset register (ADCOF) and gain coefficient register (ADCGN).

<sup>2</sup> These numbers are not production tested, but are guaranteed by design and/or characterization data at production release.

<sup>3</sup> Die temperature.

<sup>4</sup> Endurance is qualified to 20,000 cycles as per JEDEC Std. 22 Method A117 and measured at –40°C, +25°C, and +85°C. Typical endurance at 25°C is 170,000 cycles.

<sup>5</sup> Retention lifetime equivalent at a junction temperature (T<sub>J</sub>) of 85°C as per JEDEC Std. 22 Method A117. Retention lifetime derates with junction temperature.

**UHF ELECTRICAL SPECIFICATIONS**

$V_{DD} = 1.8V$  to  $3.6V$ ,  $GND = 0V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical specifications are at  $V_{DD} = 3V$ ,  $T_A = 25^\circ C$ . All measurements are performed using the reference design with PN9 data sequence, unless otherwise noted.

**Table 3. RF and Synthesizer specifications**

Parameter	Min	Typ	Max	Unit	Test Conditions / Comments
<b>RF CHARACTERISTICS</b>					
Frequency Ranges	862		928	MHz	
	431		464	MHz	
<b>PHASE-LOCKED LOOP</b>					
Channel Frequency Resolution		396.7	Hz		
Phase Noise (In-Band)		TBD		dBc/Hz	10 kHz offset, PA output power = 10 dBm, RF = 868 MHz
Phase Noise at Offset of					
1 MHz		TBD		dBc/Hz	PA output power = 10 dBm, RF = 868 MHz
2 MHz		TBD		dBc/Hz	PA output power = 10 dBm, RF = 868 MHz
10 MHz		TBD		dBc/Hz	PA output power = 10 dBm, RF = 868 MHz
VCO Calibration Time		142		$\mu s$	
Synthesizer Settling Time		56		$\mu s$	Frequency synthesizer settles to within $\pm 5$ ppm of the target frequency within this time following the VCO calibration, transmit, and receive, 2FSK/GFSK/MSK/GMSK
<b>CRYSTAL OSCILLATOR</b>					
Crystal frequency		26		MHz	Parallel load resonant crystal
Pin Capacitance		10		pF	
Maximum Crystal ESR		1800		$\Omega$	
Startup Time		384		$\mu s$	26 MHz with 10pF load capacitance
<b>SPURIOUS EMISSIONS</b>					
Integer Boundary Spurious					
910.1 MHz		TBD		dBc	Using 130 kHz synthesizer bandwidth, integer boundary spur at 910 MHz ( $26\text{ MHz} \times 35$ ), inside synthesizer loop bandwidth
911.0 MHz		TBD		dBc	Using 130 kHz synthesizer bandwidth, integer boundary spur at 910 MHz ( $26\text{ MHz} \times 35$ ), outside synthesizer loop bandwidth
Reference Spurious					
868 MHz/915 MHz		TBD		dBc	Using 130 kHz synthesizer bandwidth and using 92 kHz synthesizer bandwidth (default for PHY_RX)
Clock-Related Spur Level		TBD		dBc	Measured in a span of $\pm 350$ MHz for synthesizer bandwidth = 92 kHz, RF frequency = 868.95 MHz, PA output power = 10 dBm, $V_{DD} = 3.6V$ , single-ended PA used

Table 4. Transmitter specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DATA RATE					
2FSK	1		300	kbps	
OOK	2.4		19.2	kbps	Manchester Encoding enabled (Manchester chip rate = 2 x datarate)
Data rate resolution		100		bps	
MODULATION ERROR RATE (MER)					
10 kbps to 49.5 kbps		25.4		dB	RF frequency = 928 MHz, GFSK Modulation index = 1
49.6 kbps to 129.5 kbps		25.3		dB	Modulation index = 1
129.6 kbps to 179.1 kbps		23.9		dB	Modulation index = 0.5
179.2 kbps to 239.9 kbps		23.3		dB	Modulation index = 0.5
240 kbps to 300 kbps		23		dB	Modulation index = 0.5
MODULATION					
2FSK/GFSK Frequency Deviation	0.1		409.5	kHz	
Deviation Frequency Resolution		100		Hz	
Gaussian filter BT		0.5			Fixed
OOK					
PA Off Feedthrough		TBD		dBm	
VCO Frequency Pulling		TBD		kHz rms	Data rate = 19.2 kbps (38.4 kcps Manchester encoded), PA output = 10 dBm, PA ramp rate = 64 codes/bit
SINGLE-ENDED PA					
Maximum Power <sup>1</sup>		13.5		dBm	Programmable
Minimum Power		-20		dBm	
Transmit Power Variation vs. Temperature		±0.5		dB	From -40°C to +85°C, RF frequency = 868 MHz
Transmit Power Variation vs. V <sub>DD</sub>		±1		dB	From 1.8 V to 3.6 V, RF frequency = 868 MHz
Transmit Power Flatness		±1		dB	From 902 MHz to 928 MHz and 863 MHz to 870 MHz
Programmable Step Size					
-20 dBm to +13.5 dBm		0.5		dB	Programmable in 63 steps
DIFFERENTIAL PA					
Maximum Power <sup>1</sup>		10		dBm	Programmable
Minimum Power		-20		dBm	
Transmit Power Variation vs. Temperature		±1		dB	From -40°C to +85°C, RF frequency = 868 MHz
Transmit Power Variation vs. V <sub>DD</sub>		±2		dB	From 1.8 V to 3.6 V, RF frequency = 868 MHz
Transmit Power Flatness		±1		dB	From 863 MHz to 870 MHz
Programmable Step Size					
-20 dBm to +10 dBm		0.5		dB	Programmable in 63 steps
HARMONICS					
Single-Ended PA					
Second Harmonic		TBD		dBc	
Third Harmonic		TBD		dBc	
All Other Harmonics		TBD		dBc	



Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Differential PA					
Second Harmonic		TBD		dBc	
Third Harmonic		TBD		dBc	
All Other Harmonics		TBD		dBc	
OPTIMUM LOAD IMPEDANCE					
Single-Ended PA					
$f_{RF} = 915$ MHz		31.0+j11.3		$\Omega$	
$f_{RF} = 868$ MHz		24.3+j10.3		$\Omega$	
$f_{RF} = 434$ MHz		35.6+j3.7		$\Omega$	
Differential PA					Load impedance between RFIO_1P and RFIO_1N to ensure maximum output power
$f_{RF} = 915$ MHz		55.6+j54.8		$\Omega$	
$f_{RF} = 868$ MHz		42.2+j20.1		$\Omega$	
$f_{RF} = 433$ MHz		38.6+j20.6		$\Omega$	
PA INPUT IMPEDANCE					Single-Ended PA impedance, when transceiver in Receive Mode
$f_{RF} = 915$ MHz		-22.3-j2107		$\Omega$	
$f_{RF} = 868$ MHz		7.37-j143.7		$\Omega$	
$f_{RF} = 433$ MHz		7.7-j134.9		$\Omega$	

<sup>1</sup> Measured as the maximum unmodulated power.

Table 5. Receiver specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
2FSK/GFSK/MSK/GMSK INPUT SENSITIVITY, BIT ERROR RATE (BER)					At BER = $1E - 3$ , RF frequency = 868 MHz, 915 MHz
1.0 kbps		TBD		dBm	Frequency deviation = 4.8 kHz, IF filter bandwidth = 100 kHz
50 kbps		TBD		dBm	Frequency deviation = 12.5 kHz, IF filter bandwidth = 100 kHz
100 kbps		TBD		dBm	Frequency deviation = 25 kHz, IF filter bandwidth = 100 kHz
150 kbps		TBD		dBm	Frequency deviation = 37.5 kHz, IF filter bandwidth = 150 kHz
200 kbps		TBD		dBm	Frequency deviation = 50 kHz, IF filter bandwidth = 200 kHz
300 kbps		TBD		dBm	Frequency deviation = 75 kHz, IF filter bandwidth = 300 kHz
2FSK/GFSK/MSK/GMSK INPUT SENSITIVITY, PACKET ERROR RATE (PER)					At PER = 1%, RF frequency = 868 MHz, 915 MHz, packet length = 128 bits, packet mode
1.0 kbps		TBD		dBm	Frequency deviation = 4.8 kHz, IF filter bandwidth = 100 kHz
50 kbps		TBD		dBm	Frequency deviation = 12.5 kHz, IF filter bandwidth = 100 kHz
100 kbps		TBD		dBm	Frequency deviation = 25 kHz, IF filter bandwidth = 100 kHz
150 kbps		TBD		dBm	Frequency deviation = 37.5 kHz, IF filter bandwidth = 150 kHz
200 kbps		TBD		dBm	Frequency deviation = 50 kHz, IF filter bandwidth = 200 kHz
300 kbps		TBD		dBm	Frequency deviation = 75 kHz, IF filter bandwidth = 300 kHz
OOK INPUT SENSITIVITY, PACKET ERROR RATE (PER)					At PER = 1%, RF frequency = 868 MHz, 915 MHz, 433 MHz, packet length = 128 bits, packet mode, IF filter bandwidth = 100 kHz
19.2 kbps (38.4 kcps, Manchester Encoded)		TBD		dBm	
2.4 kbps (4.8 kcps, Manchester Encoded)		TBD		dBm	
LNA AND MIXER, INPUT IP3					Receiver LO frequency ( $f_{LO}$ ) = 914.8 MHz, $f_{SOURCE1} = f_{LO} + 0.4$ MHz, $f_{SOURCE2} = f_{LO} + 0.7$ MHz
Minimum LNA Gain		TBD		dBm	
Maximum LNA Gain		TBD		dBm	
LNA AND MIXER, INPUT IP2					Receiver LO frequency ( $f_{LO}$ ) = 920.8 MHz, $f_{SOURCE1} = f_{LO} + 1.1$ MHz, $f_{SOURCE2} = f_{LO} + 1.3$ MHz
Max LNA Gain, Max Mixer Gain		TBD		dBm	
Min LNA Gain, Min Mixer Gain		TBD		dBm	
LNA AND MIXER, 1 dB COMPRESSION POINT					RF frequency = 915 MHz
Max LNA Gain, Max Mixer Gain		TBD		dBm	
Min LNA Gain, Min Mixer Gain		TBD		dBm	
ADJACENT CHANNEL REJECTION					
CW Interferer					Wanted signal 3 dB above the input sensitivity level (BER = $10^{-3}$ ), CW interferer power level increased until BER = $10^{-3}$ , image calibrated

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
200 kHz Channel Spacing		TBD		dBm	IF BW = 100 kHz, wanted signal: $F_{DEV} = 12.5$ kHz, DR = 50 kbps
300 kHz Channel Spacing		TBD		dBm	IF BW = 100 kHz, wanted signal: $F_{DEV} = 25$ kHz, DR = 100 kbps
		TBD		dBm	IF BW = 150 kHz, wanted signal: $F_{DEV} = 37.5$ kHz, DR = 150 kbps
400 kHz Channel Spacing		TBD		dBm	IF BW = 200 kHz, wanted signal: $F_{DEV} = 50$ kHz, DR = 200 kbps
600 kHz Channel Spacing		TBD		dBm	IF BW = 300 kHz, wanted signal: $F_{DEV} = 75$ kHz, DR = 300 kbps
Modulated Interferer					Wanted signal 3 dB above the input sensitivity level ( $BER = 10^{-3}$ ), modulated interferer with the same modulation as the wanted signal; interferer power level increased until $BER = 10^{-3}$ , image calibrated
200 kHz Channel Spacing		TBD		dBm	IF BW = 100 kHz, wanted signal: $F_{DEV} = 12.5$ kHz, DR = 50 kbps
300 kHz Channel Spacing		TBD		dBm	IF BW = 100 kHz, wanted signal: $F_{DEV} = 25$ kHz, DR = 100 kbps
300 kHz Channel Spacing		TBD		dBm	IF BW = 150 kHz, wanted signal: $F_{DEV} = 37.5$ kHz, DR = 150 kbps
400 kHz Channel Spacing		TBD		dBm	IF BW = 200 kHz, wanted signal: $F_{DEV} = 50$ kHz, DR = 200 kbps
600 kHz Channel Spacing		TBD		dBm	IF BW = 300 kHz, wanted signal: $F_{DEV} = 75$ kHz, DR = 300 kbps
CO-CHANNEL REJECTION		TBD		dB	Desired signal 10 dB above the input sensitivity level ( $BER = 10^{-3}$ ), data rate = 38.4 kbps, frequency deviation = 20 kHz, RF frequency = 868 MHz
BLOCKING					Desired signal 3 dB above the input sensitivity level ( $BER = 10^{-3}$ ) of -107.5 dBm (data rate = 38.4 kbps), modulated interferer power level increased until $BER = 10^{-3}$
RF Frequency = 433 MHz					
±2 MHz		TBD		dB	
±10 MHz		TBD		dB	
RF Frequency = 868 MHz					
±2 MHz		TBD		dB	
±10 MHz		TBD		dB	
RF Frequency = 915 MHz					
±2 MHz		TBD		dB	
±10 MHz		TBD		dB	
BLOCKING, ETSI EN 300 220					Measurement procedure as per ETSI EN 300 220-1 V2.3.1; desired signal 3 dB above the ETSI EN 300 220 reference sensitivity level of -99 dBm, IF bandwidth = 100 kHz, data rate = 38.4 kbps, unmodulated interferer
±2 MHz		TBD		dBm	
±10 MHz		TBD		dBm	
WIDEBAND INTERFERENCE REJECTION		75		dB	RF frequency = 868 MHz, swept from 10 MHz to 100 MHz either side of the RF frequency

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
IMAGE CHANNEL ATTENUATION					Measured as image attenuation at the IF filter output, carrier wave interferer at 400 kHz below the channel frequency, 100 kHz IF filter bandwidth
868 MHz, 915 MHz <sup>1</sup>		36/45		dB	Uncalibrated/calibrated
433 MHz <sup>1</sup>		40/54		dB	Uncalibrated/calibrated
AFC					
Accuracy		1		kHz	
Maximum Pull-In Range					Achievable pull-in range dependent on discriminator bandwidth and modulation
300 kHz IF Filter Bandwidth		±150		kHz	
200 kHz IF Filter Bandwidth		±100		kHz	
150 kHz IF Filter Bandwidth		±75		kHz	
100 kHz IF Filter Bandwidth		±50		kHz	
PREAMBLE LENGTH					Minimum number of preamble bits to ensure the minimum packet error rate across the full input power range
AFC Off, AGC Lock on Sync Word Detection					
38.4 kbps		8		Bits	
300 kbps		24		Bits	
AFC On, AFC and AGC Lock on Preamble Detection					
9.6 kbps		44		Bits	
38.4 kbps		44		Bits	
50 kbps		50		Bits	
100 kbps		52		Bits	
150 kbps		54		Bits	
200 kbps		58		Bits	
300 kbps		64		Bits	
AFC On, AFC and AGC Lock on Sync Word Detection					
38.4 kbps		14		Bits	
300 kbps		32		Bits	
RSSI					
Range at Input		-97 to -26		dBm	
Linearity		±2		dB	
Absolute Accuracy		±3		dB	
SATURATION (MAXIMUM INPUT LEVEL)					
2FSK/GFSK/MSK/GMSK		12		dBm	
OOK		-13		dBm	OOK modulation depth = 20 dB
		10		dBm	OOK modulation depth = 60 dB
RX SPURIOUS EMISSIONS					
Maximum <1 GHz		-66		dBm	At antenna input, unfiltered conductive
Maximum >1 GHz		-62		dBm	At antenna input, unfiltered conductive
LNA INPUT IMPEDANCE					
Receive Mode					
$f_{RF} = 915 \text{ MHz}$		68.9-j36.1		$\Omega$	
$f_{RF} = 868 \text{ MHz}$		71.6-j35.0		$\Omega$	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
$f_{RF} = 433 \text{ MHz}$		99.2-j31.3		$\Omega$	
Transmit Mode					
$f_{RF} = 915 \text{ MHz}$		8.6+j21.1		$\Omega$	
$f_{RF} = 868 \text{ MHz}$		8.6+j20.4		$\Omega$	
$f_{RF} = 433 \text{ MHz}$		8.2+j11.4		$\Omega$	

<sup>1</sup> Measured with IMAGE\_REJECT\_CAL\_AMPLITUDE = 0 and IMAGE\_REJECT\_CAL\_PHASE = 14 at 433MHz and IMAGE\_REJECT\_CAL\_AMPLITUDE = 8 and IMAGE\_REJECT\_CAL\_PHASE = 55 at 868 MHz/915 MHz.

Table 6. UHF transceiver auxiliary block specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
<b>32 kHz RC OSCILLATOR</b>					
Frequency		32.768		kHz	After calibration
Frequency Accuracy		1.5		%	After calibration at 25°C
<b>Frequency Drift</b>					
Temperature Coefficient		0.14		%/°C	
Voltage Coefficient		4		%/V	
Calibration Time		1		ms	
<b>32 kHz XTAL OSCILLATOR</b>					
Frequency		32.768		kHz	
Start-Up Time		630		ms	32.768 kHz crystal with 7 pF load capacitance
<b>WAKE UP CONTROLLER (WUC)</b>					
<b>Hardware Timer</b>					
Wake-Up Period	$61 \times 10^{-6}$		$1.31 \times 10^5$	sec	
<b>Firmware Timer</b>					
Wake-Up Period	1		$2^{16}$	Hardware periods	Firmware counter counts of the number of hardware wake-ups, resolution of 16 bits
<b>ADC</b>					
Resolution		8		Bits	
DNL		$\pm 1$		LSB	From 1.8 V to 3.6 V, $T_A = 25^\circ\text{C}$
INL		$\pm 1$		LSB	From 1.8 V to 3.6 V, $T_A = 25^\circ\text{C}$
Conversion Time		1		$\mu\text{s}$	
Input Capacitance		12.4		pF	
<b>BATTERY MONITOR</b>					
Absolute Accuracy		$\pm 45$		mV	
Alarm Voltage Set Point	1.7		2.7	V	
Alarm Voltage Step Size		62		mV	5-bit resolution
Start-Up Time			100	$\mu\text{s}$	
Current Consumption		30		$\mu\text{A}$	When enabled
<b>TEMPERATURE SENSOR</b>					
Range	-40		+85	°C	
Resolution		0.3		°C	With averaging
Accuracy of Temperature Readback					With a temperature correction value (determined at a known temperature) applied, from -40°C to +85°C
Single Readback		$\pm 14$		°C	
Average of 10 Readbacks		$\pm 4.4$		°C	
Average of 50 Readbacks		$\pm 2$		°C	

**Table 7. General UHF transceiver specifications**

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TRANSMIT CURRENT CONSUMPTION					In the PHY_TX state, single-ended PA matched to 50 Ω, differential PA matched to 100 Ω, separate single-ended PA and LNA match, combined differential PA and LNA match
Single-Ended PA, 433 MHz					
–10 dBm		8.7		mA	
0 dBm		12.2		mA	
10 dBm		23.3		mA	
13.5 dBm		32.1		mA	
Differential PA, 433 MHz					
–10 dBm		7.9		mA	
0 dBm		11		mA	
5 dBm		15		mA	
10 dBm		22.6		mA	
Single-Ended PA, 868 MHz/915 MHz					
–10 dBm		10.3		mA	
0 dBm		13.3		mA	
10 dBm		24.1		mA	
13.5 dBm		32.1		mA	
Differential PA, 868 MHz/915 MHz					
–10 dBm		9.3		mA	
0 dBm		12		mA	
5 dBm		16.7		mA	
10 dBm		28		mA	
POWER MODES					
PHY_SLEEP (Deep Sleep Mode 2)		0.18		μA	Sleep mode, wake-up configuration values (BBRAM) not retained
PHY_SLEEP (Deep Sleep Mode 1)		0.33		μA	Sleep mode, wake-up configuration values (BBRAM) retained
PHY_SLEEP (RCO Wake Mode)		0.75		μA	WUC active, RC oscillator running, wake-up configuration values retained (BBRAM)
PHY_SLEEP (XTO Wake Mode)		1.28		μA	WUC active, 32 kHz crystal running, wake-up configuration values retained (BBRAM)
PHY_OFF		1		mA	Device in PHY_OFF state, 26 MHz oscillator running, digital and synthesizer regulators active, all register values retained
PHY_ON		1		mA	Device in PHY_ON state, 26 MHz oscillator running, digital, synthesizer, VCO, and RF regulators active, baseband filter calibration performed, all register values retained
PHY_RX		12.8		mA	Device in PHY_RX state

<b>Parameter</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Unit</b>	<b>Test Conditions/Comments</b>
SMART WAKE MODE					Average current consumption
		21.78		μA	Autonomous reception every 1 sec, with receive dwell time of 1.25 ms, using RC oscillator, data rate = 38.4 kbps
		11.75		μA	Autonomous reception every 1 sec, with receive dwell time of 0.5 ms, using RC oscillator, data rate = 300 kbps



**UHF TRANSCEIVER TIMING SPECIFICATIONS**

**Table 8. UHF transceiver Command Execution Times and State Transition Times That Are Not Related to PHY\_TX or PHY\_RX**

Command/Bit	Command Initiated By	Present State	Next State	Transition Time (µs), Typical	Condition
CMD_HW_RESET	Host	Any	PHY_SLEEP	1	
CMD_PHY_SLEEP	Host	PHY_OFF	PHY_SLEEP	22.3	
CMD_PHY_SLEEP	Host	PHY_ON	PHY_SLEEP	24.1	
CMD_PHY_OFF	Host	PHY_ON	PHY_OFF	19	
CMD_PHY_ON	Host	PHY_OFF	PHY_ON	248	Including IF filter calibration
CMD_GET_RSSI	Host	PHY_ON	PHY_ON	612.5	
CMD_CONFIG_DEV	Host	PHY_OFF	PHY_OFF	66.8	
CMD_CONFIG_DEV	Host	PHY_ON	PHY_ON	66.8	
CMD_BB_CAL	Host	PHY_ON	PHY_ON	211	
Wake-Up from PHY_SLEEP, (WUC Timeout)	Automatic	PHY_SLEEP	PHY_OFF	310 + 252.8	The 310 µs is for startup of the 26 MHz crystal (7 pF load capacitance, T <sub>A</sub> = 25°C).
Wake-Up from PHY_SLEEP, (CS Low)	Host	PHY_SLEEP	PHY_OFF	310 + 252.8	The 310 µs is for startup of the 26 MHz crystal (7 pF load capacitance, T <sub>A</sub> = 25°C)
Cold Start	Application of power	N/A	PHY_OFF	310 + 252.8	The 310 µs is for startup of the 26 MHz crystal (7 pF load capacitance, T <sub>A</sub> = 25°C)

**Table 9. UHF transceiver State Transition Times Related to PHY\_TX and PHY\_RX**

Mode	Command/Bit/ Automatic Transition	Present State	Next State	Transition Time (µs) <sup>1,2</sup> , Typical	Condition
Packet	CMD_PHY_ON	PHY_TX	PHY_ON	T <sub>EOP</sub> + 10.8 + T <sub>PARAMP_DOWN</sub> + 36	
Packet	CMD_PHY_ON	PHY_RX	PHY_ON	5 + T <sub>BYTE</sub> + 38.2	CMD_PHY_ON issued during search for preamble
				41.7	CMD_PHY_ON issued during preamble qualification
				41.2	CMD_PHY_ON issued during sync word qualification
				T <sub>EOP</sub> + 31.7	CMD_PHY_ON issued during Rx data (after a sync word)
Packet	CMD_PHY_TX	PHY_ON	PHY_TX	293 + T <sub>PARAMP_UP</sub> + 3	
Packet	CMD_PHY_TX	PHY_RX	PHY_TX	5 + T <sub>BYTE</sub> + 305.3 + T <sub>PARAMP_UP</sub> + 3	CMD_PHY_TX issued during search for preamble
				308.5 + T <sub>PARAMP_UP</sub> + 3	CMD_PHY_TX issued during preamble qualification
				308 + T <sub>PARAMP_UP</sub> + 3	CMD_PHY_TX issued during sync word qualification
				298.5 + T <sub>EOP</sub> + T <sub>PARAMP_UP</sub> + 3	CMD_PHY_TX issued during Rx data (after a sync word)
Packet	CMD_PHY_TX	PHY_TX	PHY_TX	T <sub>EOP</sub> + 10.8 + T <sub>PARAMP_DOWN</sub> + 297 + T <sub>PARAMP_UP</sub> + 3	CMD_PHY_TX issued during packet transmission
Packet	RX_TO_TX_AUTO_TURNAROUND	PHY_RX	PHY_TX	287.3 + T <sub>PARAMP_UP</sub> + 3	
Packet	CMD_PHY_RX	PHY_ON	PHY_RX	300	
Packet	CMD_PHY_RX	PHY_TX	PHY_RX	T <sub>EOP</sub> + 10.8 + T <sub>PARAMP_DOWN</sub> + 317	CMD_PHY_RX issued during packet transmission
Packet	TX_EOF	PHY_TX	PHY_ON	10.8 + T <sub>PARAMP_DOWN</sub> + 36	
Packet	RX_EOF	PHY_RX	PHY_ON	17.2	

Mode	Command/Bit/ Automatic Transition	Present State	Next State	Transition Time ( $\mu\text{s}$ ) <sup>1, 2</sup> , Typical	Condition
Packet	CMD_PHY_RX	PHY_RX	PHY_RX	$5 + T_{\text{BYTE}} + 305.2$	CMD_PHY_RX issued during search for preamble
				308.4	CMD_PHY_RX issued during preamble qualification
				307.9	CMD_PHY_RX issued during sync word qualification
				$T_{\text{EOP}} + 298.4$	CMD_PHY_RX issued during Rx data (after a sync word)
Packet	TX_TO_RX_AUTO_TURNAROUND	PHY_TX	PHY_RX	$10.8 + T_{\text{PARAMP\_DOWN}} + 306$	
Sport	CMD_PHY_ON	PHY_TX	PHY_ON	$10.8 + T_{\text{PARAMP\_DOWN}} + 36$	
Sport	CMD_PHY_ON	PHY_RX	PHY_ON	$5 + T_{\text{BYTE}} + 38.2$	CMD_PHY_ON issued during search for a preamble
				41.7	CMD_PHY_ON issued during preamble qualification
				41.2	CMD_PHY_ON issued during sync word qualification
				31.7	CMD_PHY_ON issued during Rx data (after a sync word)
Sport	CMD_PHY_TX	PHY_ON	PHY_TX	$293 + T_{\text{PARAMP\_UP}} + 3$	
Sport	CMD_PHY_TX	PHY_RX	PHY_TX	$5 + T_{\text{BYTE}} + 305.3 + T_{\text{PARAMP\_UP}} + 3$	CMD_PHY_TX issued during search for a preamble
				$308.5 + T_{\text{PARAMP\_UP}} + 3$	CMD_PHY_TX issued during preamble qualification
				$308 + T_{\text{PARAMP\_UP}} + 3$	CMD_PHY_TX issued during sync word qualification
				$298.5 + T_{\text{PARAMP\_UP}} + 3$	CMD_PHY_TX issued during Rx data (after a sync word)
Sport	CMD_PHY_TX	PHY_TX	PHY_TX	$10.8 + T_{\text{PARAMP\_DOWN}} + 297 + T_{\text{PARAMP\_UP}} + 3$	
Sport	RX_TO_TX_AUTO_TURNAROUND	PHY_RX	PHY_TX	$287.3 + T_{\text{PARAMP\_UP}} + 3$	
Sport	CMD_PHY_RX	PHY_ON	PHY_RX	300	
Sport	CMD_PHY_RX	PHY_TX	PHY_RX	$1.8 + T_{\text{PARAMP\_DOWN}} + 317$	
Sport	CMD_PHY_RX	PHY_RX	PHY_RX	$5 + T_{\text{BYTE}} + 305.2$	CMD_PHY_RX issued during search for a preamble
				308.4	CMD_PHY_RX issued during preamble qualification
				307.9	CMD_PHY_RX issued during sync word qualification
				298.4	CMD_PHY_RX issued during Rx data (after a sync word)
Sport	TX_TO_RX_AUTO_TURNAROUND	PHY_TX	PHY_RX	$10.8 + T_{\text{PARAMP\_DOWN}} + 306$	

<sup>1</sup>  $T_{\text{PARAMP\_UP}} = T_{\text{PARAMP\_DOWN}} = \frac{PA\_LEVEL\_MCR}{2 \times (9 - PA\_RAMP) \times DATA\_RATE \times 100}$ , where PA\_LEVEL\_MCR sets the maximum PA output power (PA\_LEVEL\_MCR register, Address 0x307),

PA\_RAMP sets the PA ramp rate (RADIO\_CFG\_8 register, Address 0x114), and DATA\_RATE sets the transmit data rate (RADIO\_CFG\_0 register, Address 0x10C and RADIO\_CFG\_1 register, Address 0x10D).

<sup>2</sup>  $T_{\text{BYTE}}$  = one byte period ( $\mu\text{s}$ ),  $T_{\text{EOP}}$  = time to end of packet ( $\mu\text{s}$ ).

**I<sup>2</sup>C TIMING DIAGRAMS**

Capacitive load for each of the I<sup>2</sup>C-bus line, C<sub>b</sub> = 400pF maximum as per I<sup>2</sup>C-bus specifications.

I<sup>2</sup>C timing is guaranteed by design and not production tested.

**Table 10 I<sup>2</sup>C Timing in Fast Mode (400 kHz)**

Parameter	Description	Min	Max	Unit
t <sub>L</sub>	Clock low pulse width	1300	-	ns
t <sub>H</sub>	Clock high pulse width	600	-	ns
t <sub>SHD</sub>	Start condition hold time	600	-	ns
t <sub>DSU</sub>	Data setup time	100	-	ns
t <sub>DHD</sub>	Data hold time	0	-	ns
t <sub>RSU</sub>	Setup time for repeated start	600	-	ns
t <sub>PSU</sub>	Stop condition setup time	600	-	ns
t <sub>BUF</sub>	Bus-free time between a stop condition and a start condition	1.3	-	μs
t <sub>R</sub>	Rise time for both clock and data	20 + 0.1 C <sub>b</sub>	300	ns
t <sub>F</sub>	Fall time for both clock and data	20 + 0.1 C <sub>b</sub>	300	ns
t <sub>SUP</sub>	Pulse width of spike suppressed	0	50	ns

**Table 11. I<sup>2</sup>C Timing in Standard Mode (100 kHz)**

Parameter	Description	Min	Max	Unit
t <sub>L</sub>	Clock low pulse width	4.7	-	μs
t <sub>H</sub>	Clock high pulse width	4.0	-	ns
t <sub>SHD</sub>	Start condition hold time	4.7	-	μs
t <sub>DSU</sub>	Data setup time	250	-	ns
t <sub>DHD</sub>	Data hold time	0	-	μs
t <sub>RSU</sub>	Setup time for repeated start	4.0	-	μs
t <sub>PSU</sub>	Stop condition setup time	4.0	-	μs
t <sub>BUF</sub>	Bus-free time between a stop condition and a start condition	4.7	-	μs
t <sub>R</sub>	Rise time for both clock and data	-	1	μs
t <sub>F</sub>	Fall time for both clock and data	-	300	ns

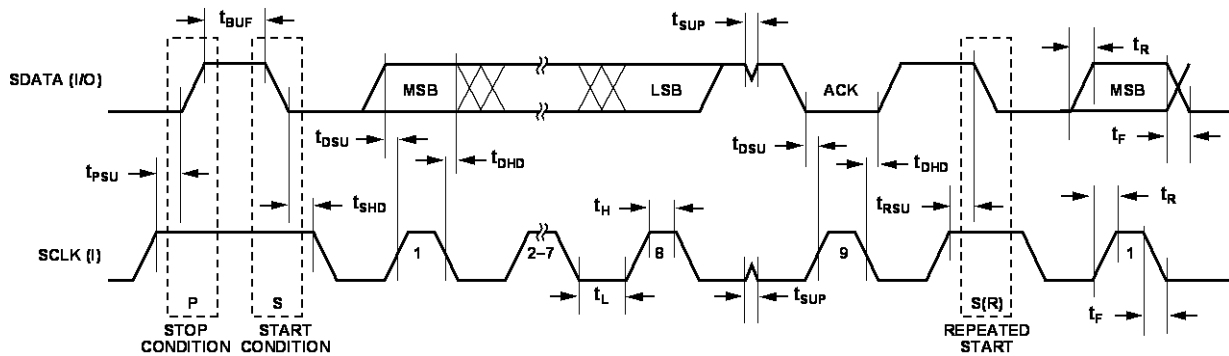


Figure 2. I<sup>2</sup>C Compatible Interface Timing

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## SPI TIMING DIAGRAMS

Table 12. SPI Master Mode Timing

Parameter	Description	Min	Typ	Max	Unit
$t_{SL}$	SCLOCK low pulse width <sup>1</sup>		$(SPIxDIV + 1) \times t_{UCLK}$		ns
$t_{SH}$	SCLOCK high pulse width <sup>1</sup>		$(SPIxDIV + 1) \times t_{UCLK}$		ns
$t_{DAV}$	Data output valid after SCLOCK edge		0	35.5	ns
$t_{DOSU}$	Data output setup before SCLOCK edge <sup>1</sup>	$(SPIxDIV + 1) \times t_{UCLK}$			ns
$t_{DSU}$	Data input setup time before SCLOCK edge	58.7			ns
$t_{DHD}$	Data input hold time after SCLOCK edge	16			ns
$t_{DF}$	Data output fall time		12	35.5	ns
$t_{DR}$	Data output rise time		12	35.5	ns
$t_{SR}$	SCLOCK rise time		12	35.5	ns
$t_{SF}$	SCLOCK fall time		12	35.5	ns

<sup>1</sup>  $t_{UCLK} = 62.5$  ns. It corresponds to the internal 16MHz clock before the clock divider.

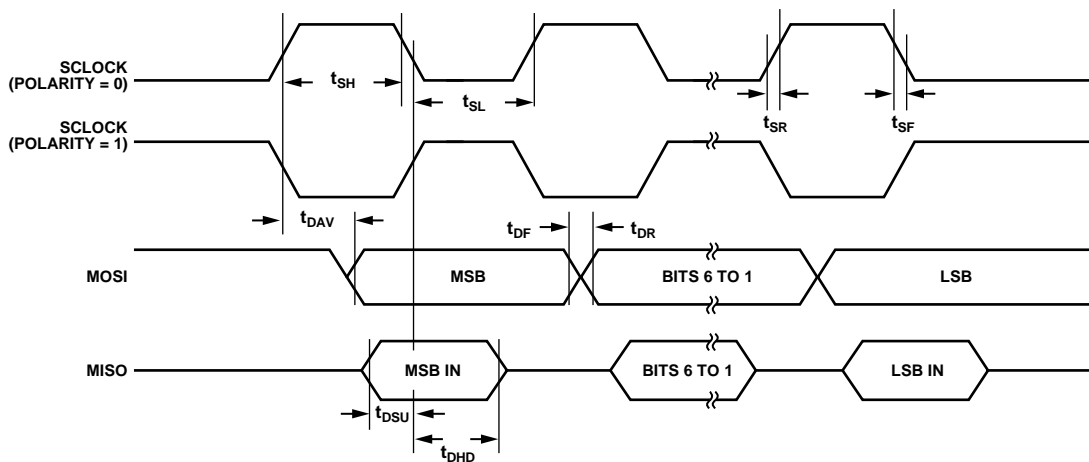


Figure 3. SPI Master Mode Timing (PHASE Mode = 1)

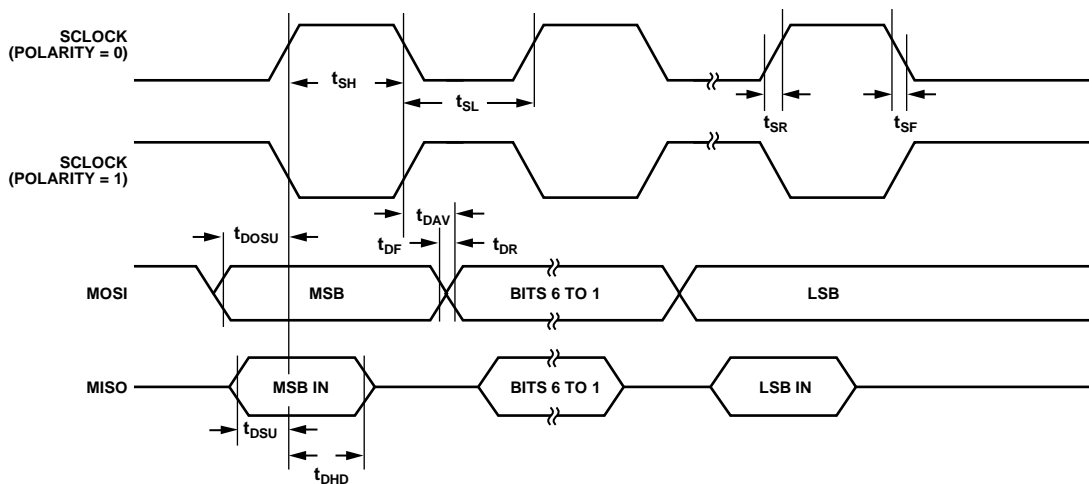


Figure 4. SPI Master Mode Timing (PHASE Mode = 0)

Table 13. SPI Slave Mode Timing

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{CS}}$	$\overline{CS}$ to SCLOCK edge	38			ns
$t_{SL}$	SCLOCK low pulse width <sup>1</sup>		$2 \times t_{UCLK}$		ns
$t_{SH}$	SCLOCK high pulse width <sup>1</sup>	62.5	$2 \times t_{UCLK}$		ns
$t_{DAV}$	Data output valid after SCLOCK edge			49.1	ns
$t_{DSU}$	Data input setup time before SCLOCK edge	20.2			ns
$t_{DHD}$	Data input hold time after SCLOCK edge	10.1			ns
$t_{DF}$	Data output fall time		12	35.5	ns
$t_{DR}$	Data output rise time		12	35.5	ns
$t_{SR}$	SCLOCK rise time		12	35.5	ns
$t_{SF}$	SCLOCK fall time		12	35.5	ns
$t_{DOCS}$	Data output valid after $\overline{CS}$ edge			25	ns
$t_{SFS}$	$\overline{CS}$ high after SCLOCK edge	0			ns

<sup>1</sup>  $t_{UCLK} = 62.5$  ns. It corresponds to the internal 16MHz clock before the clock divider.

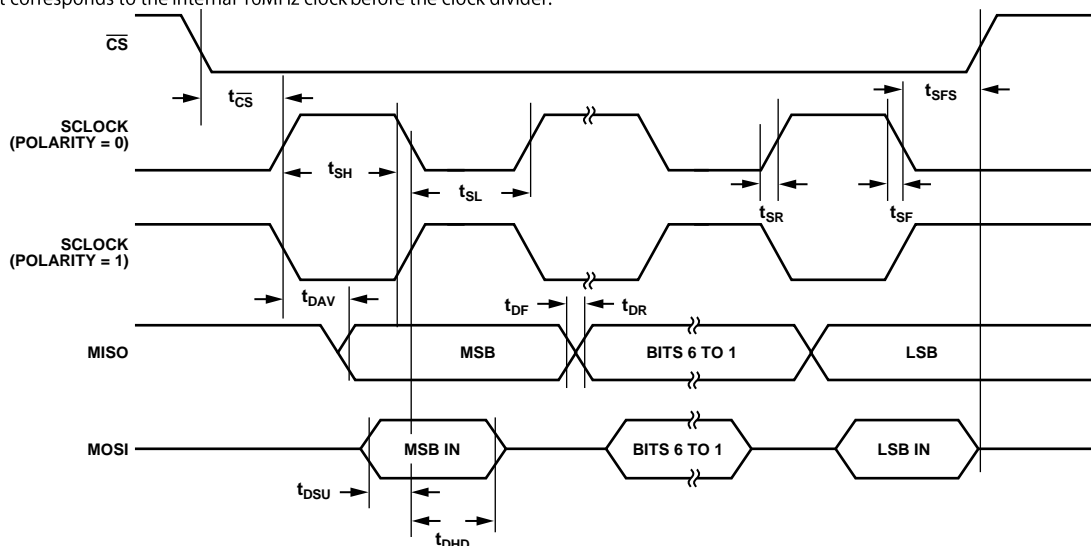


Figure 5. SPI Slave Mode Timing (PHASE Mode = 1)

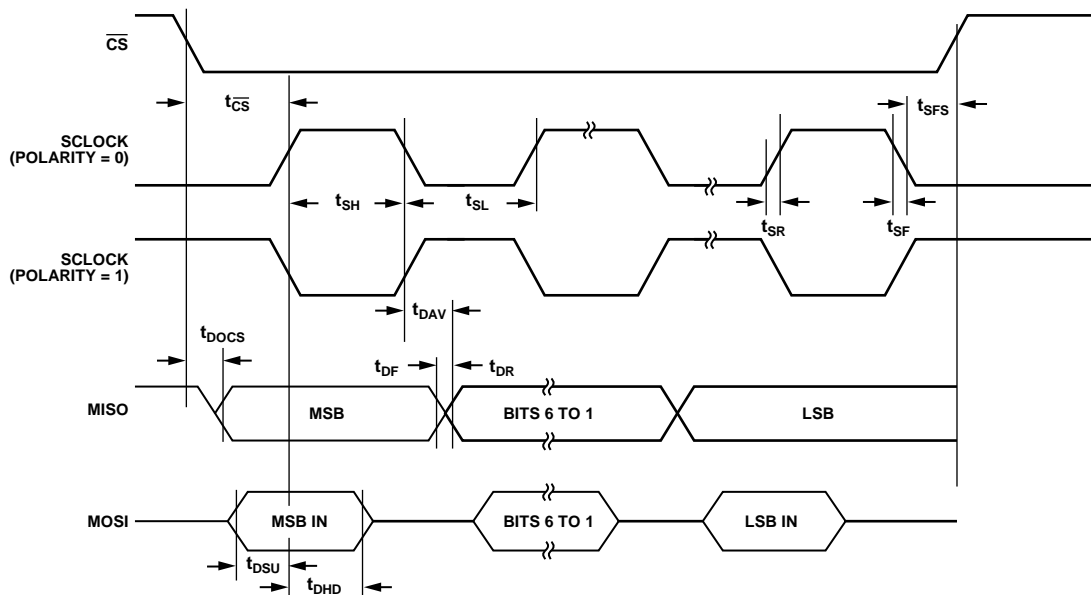


Figure 6. SPI Slave Mode Timing (PHASE Mode = 0)

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$  unless otherwise noted

Table 14.

Parameter	Rating
V <sub>BAT</sub> and I <sub>O</sub> V <sub>DD</sub> to GND	-0.3 V to 3.96V
Digital Input Voltage to GND	-0.3 V to 3.96V
Digital Output Voltage to GND	-0.3 V to 3.96V
V <sub>REF</sub> to GND	-0.3 V to 3.96V
Analog Inputs to AGND	-0.3 V to 2.1V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	105°C
$\theta_{JA}$ Thermal Impedance	
64-Pin LFCSP _VQ	25°C/W
Peak Solder Reflow Temperature	
Pb-Free Assemblies (30 s)	260°C

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

The exposed paddle of the LFCSP package should be connected to ground.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

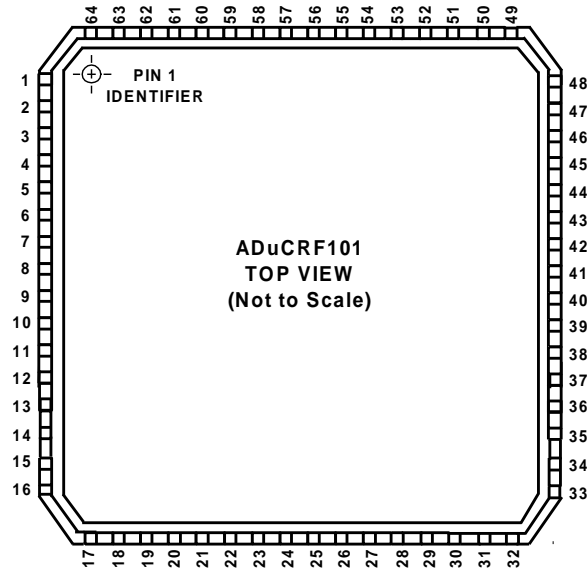


Figure 8. 64-Lead LFCSP\_VQ Pin Configuration

Table 15. Pin Function Descriptions

Pin No.	Mnemonic	Description
TBD	VDDRF1	Voltage Regulator output for RF block. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
TBD	RBIAS	External bias resistor. Optimum resistor is 36 kΩ with 5% tolerance.
TBD	VDDRF2	Voltage Regulator output for RF block. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
TBD	AVDD	Battery terminal, Analog Supply for ADC and ADC internal reference (VREF).
TBD	VREF	Internal 1.25V ADC reference. A 0.47uF capacitor between this pin and ground is required.
TBD	RFIO_1P	LNA Positive Input in Receive Mode. Differential PA Positive Output in Transmit Mode.
TBD	RFIO_1N	LNA Negative Input in Receive Mode. Differential PA Negative Output in Transmit Mode.
TBD	RF02	Single ended PA output.
TBD	VDD_VBAT2	Battery Terminal.
TBD	ADC0	ADC input channel 0
TBD	ADC1	ADC input channel 1
TBD	ADC2	ADC input channel 2
TBD	ADC3	ADC input channel 3
TBD	ADC4	ADC input channel 4
TBD	ADC5	ADC input channel 5
TBD	P1.6/IRQ7/PWM_SYNC	General Purpose Input and Output Port 1.6/External Interrupt 7/PWM synchronisation.
TBD	VDDVCO	Voltage Regulator output for VCO. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
TBD	SWDIO	Serial Wire debug data in-out
TBD	LVDD	On chip LDO decoupling output. Connect a 0.47uF capacitor to the 1.8V output to ensure core operating voltage is stable
TBD	GROUND	Ground. The exposed package paddle should be grounded.
TBD	IOVDD	General Purpose IO supply. Connect to the battery terminal
TBD	SWCLK	Serial Wire debug clock
TBD	VCOGUARD	Guard, screen for VCO.

Pin No.	Mnemonic	Description
TBD	VDDSYNTH	Voltage Regulator output for Synthesizer. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
TBD	CWAKE	External capacitor for wake up control. A 150 nF capacitor should be placed between this pin and ground.
TBD	XOSC26P	The 26MHz reference crystal should be connected between this pin and XOSC26N.
TBD	XOSC26N	The 26MHz reference crystal should be connected between this pin and XOSC26P.
TBD	DGUARD	Internal Guard, Screen for Digital Cells
TBD	VDD_DIG 1	Voltage Regulator output for Digital. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
TBD	P1.5/IRQ6/I2C0S DA/PWM7	General Purpose Input and Output Port 1.5/External Interrupt 6/I2C 0 Serial Data/PWM channel 7.
TBD	P1.4/IRQ5/I2C0S CL/PWM6	General Purpose Input and Output Port 1.4/External Interrupt 5/I2C 0 Serial Clock/PWM channel 6.
TBD	P1.3/PWM5	General Purpose Input and Output Port 1.3/PWM channel 5.
TBD	P1.2/PWM4	General Purpose Input and Output Port 1.2/PWM channel 4.
TBD	PORB/P1.1/TXD /PWM3	POR output/General Purpose Input and Output Port 1.1/UART TXD/ PWM channel 3.
TBD	P1.0/RXD/IRQ4/ MOSI /PWM2	General Purpose Input and Output Port 1.0/UART RXD/ External Interrupt 4/ SPI1 Master Out Slave In Pin (MOSI)/PWM channel 2.
TBD	P0.5/CS2/ECLKIN	General Purpose Input and Output Port 0.5/SPI1 Chip Select 2/External Clock Input
TBD	P0.4/IRQ0/CS1 /ECLKOUT	General Purpose Input and Output Port 0.4/External Interrupt 0/SPI1 Chip Select 1/External Clock Output.
TBD	P2.6/GP0	General Purpose Input and Output Port 2.6
TBD	P0.3/IRQ1/CS0/P WM1	General Purpose Input and Output Port 0.3/External Interrupt 1/SPI1 Chip Select 0/PWM channel 1.
TBD	P2.4/IRQ8	General Purpose Input and Output Port 2.4/ External Interrupt 8
TBD	P0.2/MOSI/PWM 0	General Purpose Input and Output Port 0.2/SPI1 Master Out Slave In Pin (MOSI)/PWM channel 0.
TBD	P0.1/SCLK	General Purpose Input and Output Port 0.1/SPI1 Serial Clock
TBD	P0.0/MISO	General Purpose Input and Output Port 0.0/SPI1 Master In Slave Out Pin (MISO)
TBD	IOVDD	General Purpose I/O supply. Connect to the battery terminal
TBD	P0.7/IRQ3/CS4 /CTS	General Purpose Input and Output Port 0.7/ External Interrupt 3 / SPI1 Chip Select 4/ UART hand shake.
TBD	P0.6/ IRQ2/CS3/ RTS/PWM0	General Purpose Input and Output Port 0.6 / External Interrupt 2/ SPI1 Chip Select 3 / UART hand shake/PWM channel 0.
TBD	RESET	Active Low. A low signal on this pin for 24 system clocks will cause the part to reset.
TBD	P4.0/PWM0	General Purpose Input and Output Port 4.0/PWM channel 0.
TBD	P4.1/PWM1	General Purpose Input and Output Port 4.1/PWM channel 1.
TBD	P4.2/PWM2	General Purpose Input and Output Port 4.2/PWM channel 2.
TBD	P4.3/PWM3	General Purpose Input and Output Port 4.3/PWM channel 3.
TBD	P4.4/PWM4	General Purpose Input and Output Port 4.4/PWM channel 4.
TBD	P4.5/PWM5	General Purpose Input and Output Port 4.5/PWM channel 5.
TBD	LFXTAL2	32.768kHz watch crystal output for WU timers.
TBD	LFXTAL1	32.768kHz watch crystal input for WU timers.
TBD	VDD_DIG2	Voltage Regulator output for Digital. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
TBD	VDDBAT	Battery Terminal, connected to the top die (UHF transceiver's LDOs) and to the LF receiver.
TBD	P4.6/PWM6	General Purpose Input and Output Port 4.6/PWM channel 6.
TBD	P4.7/PWM7	General Purpose Input and Output Port 4.7/PWM channel 7.
TBD	ADCREF	Top die ADC Reference Output. A 220 nF capacitor should be placed between this pin and ground for adequate noise rejection.
TBD	P3.2/PWM_SYNC	General Purpose Input and Output Port 3.2/PWM synchronisation.

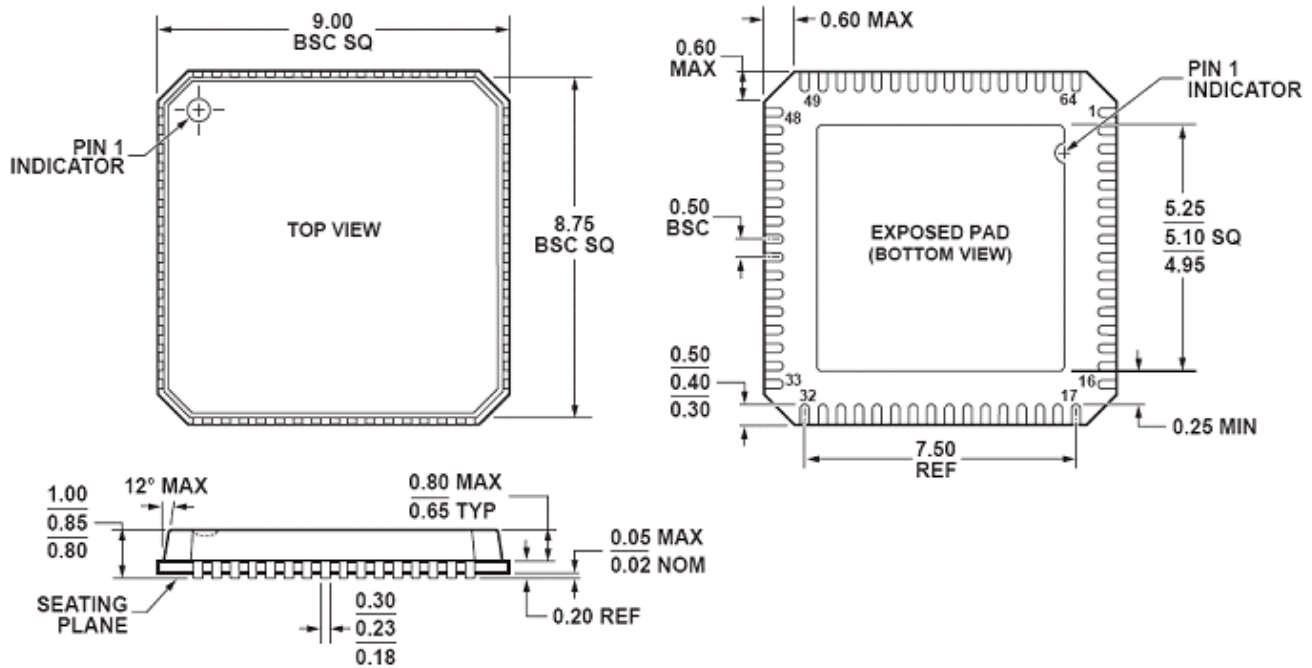


TBD	P3.3/PWM_TRIP	General Purpose Input and Output Port 3.3/PWM safety cut off.
TBD	P3.4	General Purpose Input and Output Port 3.4
TBD	P3.5	General Purpose Input and Output Port 3.5
TBD	PADDLE	Connected to the GROUND pin.

OUTLINE DIMENSIONS



64-Lead Lead Frame Chip Scale Package [LFCSP\_VQ]  
 9 x 9 mm Body, Very Thin Quad  
 (CP-64-5)  
 Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VMMD-4

073108-A

Figure 7. 64-Lead Frame Chip Scale Package [LFCSP\_VQ]  
 9 mm x 9 mm Body, Very Thin Quad  
 (CP-64-1)  
 Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option

I<sup>2</sup>C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).