

STANDARD CAPACITANCE TVS ARRAY

APPLICATIONS

- ✓ Ethernet - 10 Base T
- ✓ Cellular Phones
- ✓ Handheld Electronics
- ✓ FireWire & USB Interfaces
- ✓ Multiple I/O Ports or Power Supplies

IEC COMPATIBILITY (EN61000-4)

- ✓ 61000-4-2 (ESD): Air - 15kV, Contact - 8kV
- ✓ 61000-4-4 (EFT): 40A - 5/50ns
- ✓ 61000-4-5 (Surge): 12A, 8/20 μ s - Level 1(Line-Gnd) & Level 2(Line-Line)

FEATURES

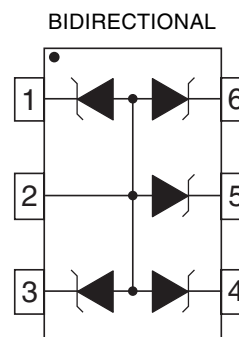
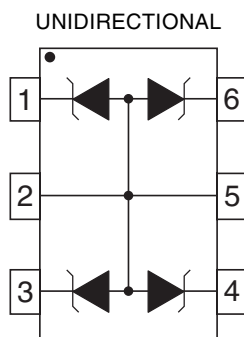
- ✓ 200 Watts Peak Pulse Power per Line (tp=8/20 μ s)
- ✓ Monolithic Design
- ✓ Available in Multiple Voltage Types Ranging From 5V to 24V
- ✓ Protect 4 Bidirectional Lines & 5 Unidirectional Lines
- ✓ ESD Protection > 25 kilovolts
- ✓ Low Clamping Voltage
- ✓ Unidirectional & Bidirectional Configurations
- ✓ Low Leakage Current
- ✓ RoHS Compliant in Lead-Free Versions

MECHANICAL CHARACTERISTICS

- ✓ Molded JEDEC SOT-23-6 Package
- ✓ Weight 16 milligrams (Approximate)
- ✓ Available in Tin-Lead or Lead-Free Pure-Tin Plating(Annealed)
- ✓ Solder Reflow Temperature:
 - Tin-Lead - Sn/Pb, 85/15: 240-245°C
 - Pure-Tin - Sn, 100: 260-270°C
- ✓ Flammability rating UL 94V-0
- ✓ 8mm Tape and Reel Per EIA Standard 481
- ✓ Marking: Marking Code & Pin One Defined By DOT on Package



PIN CONFIGURATIONS



DEVICE CHARACTERISTICS

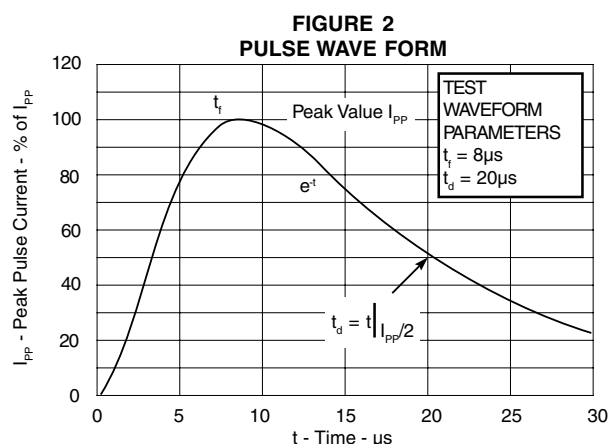
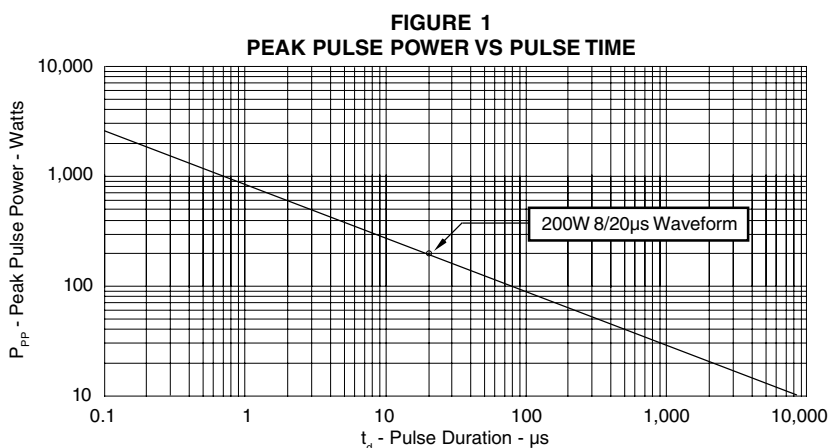
MAXIMUM RATINGS @ 25°C Unless Otherwise Specified			
PARAMETER	SYMBOL	VALUE	UNITS
Peak Pulse Power ($t_p = 8/20\mu s$) - See Figure 1	P_{PP}	200	Watts
Operating Temperature	T_J	-55°C to 150°C	°C
Storage Temperature	T_{STG}	-55°C to 150°C	°C

ELECTRICAL CHARACTERISTICS PER LINE @ 25°C Unless Otherwise Specified							
PART NUMBER (See Notes 1-3)	DEVICE MARKING	RATED STAND-OFF VOLTAGE	MINIMUM BREAKDOWN VOLTAGE	MAXIMUM CLAMPING VOLTAGE (See Fig. 2)	MAXIMUM CLAMPING VOLTAGE (See Fig. 2)	MAXIMUM LEAKAGE CURRENT	TYPICAL CAPACITANCE
CP05	QRH	5.0	6.0	9.8	11.8V @ 17.0A	20	70
CP05C	QRL	5.0	6.0	9.8	11.8V @ 17.0A	20	70
CP12	QRI	12.0	13.3	19	28.3V @ 7.0A	1	50
CP12C	QRM	12.0	13.3	19	28.3V @ 7.0A	1	50
CP15	QRJ	15.0	16.7	24	45.0V @ 5.0A	1	30
CP15C	QRN	15.0	16.7	24	45.0V @ 5.0A	1	30
CP24	QRK	24.0	26.7	43	65.0V @ 3.0A	1	25
CP24C	QRO	24.0	26.7	43	65.0V @ 3.0A	1	25

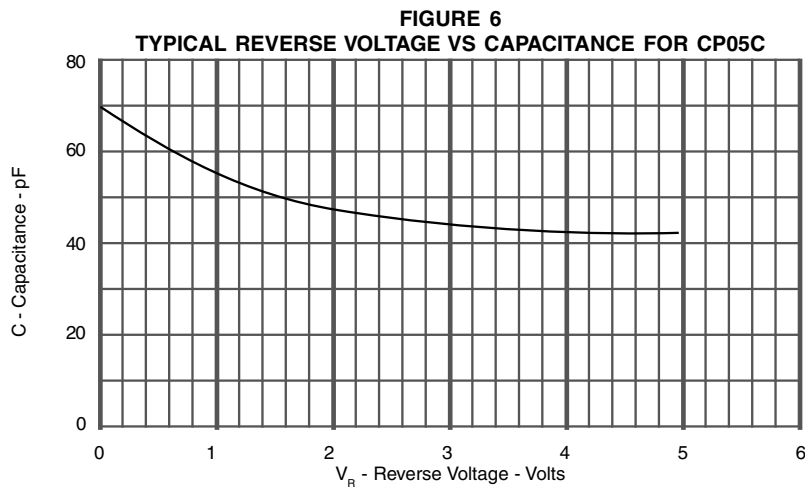
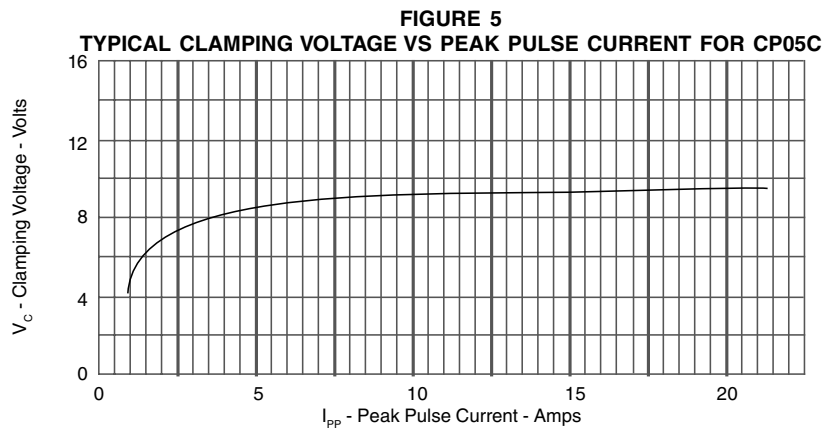
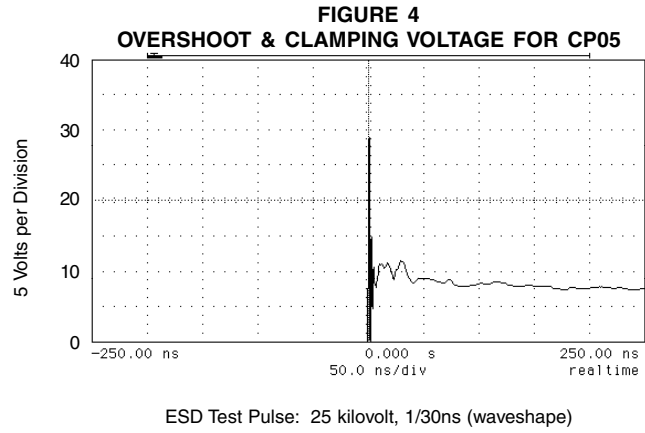
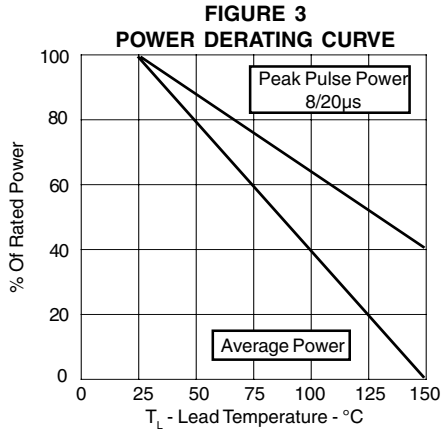
Note 1: Part numbers with an additional "C" suffix are bidirectional devices, i.e., CP05C.

Note 2: *Unidirectional Only:* Test between pin 1, 3, 4 and 6 to pin 2 or 5.

Note 3: *Bidirectional Only:* Test between pin 5 to 1 or 3 or 4 or 6. Electrical characteristics apply in both directions.



GRAPHS



APPLICATION NOTE

The CP Series are TVS arrays designed to protect I/O or data lines from the damaging effects of ESD or EFT. This product series provides both unidirectional and bidirectional protection, with a surge capability of 200 Watts P_{pp} per line for an 8/20 μ s waveform and ESD protection > 25 kilovolts.

UNIDIRECTIONAL COMMON-MODE CONFIGURATION (Figure 1)

The CP Series provides up to four (4) lines of protection in a common-mode configuration as depicted in Figure 1.

Circuit connectivity is as follows:

- ✓ Line 1 is connected to Pin 1.
- ✓ Line 2 is connected to Pin 3.
- ✓ Line 3 is connected to Pin 4.
- ✓ Line 4 is connected to Pin 6.
- ✓ Pin 5 is connected to ground.
- ✓ Pin 2 is not connected.

BIDIRECTIONAL COMMON-MODE CONFIGURATION (Figure 2)

The CPxxC Series provides up to four (4) lines of protection in a common-mode configuration as depicted in Figure 2.

Circuit connectivity is as follows:

- ✓ Line 1 is connected to Pin 1.
- ✓ Line 2 is connected to Pin 3.
- ✓ Line 3 is connected to Pin 4.
- ✓ Line 4 is connected to Pin 5.
- ✓ Pin 6 is connected to ground.
- ✓ Pin 2 is not connected.

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:

- ✓ The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.
- ✓ The path length between the TVS device and the protected line should be minimized.
- ✓ All conductive loops including power and ground loops should be minimized.
- ✓ The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.
- ✓ Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

Figure 1 - Unidirectional Configuration
Common-Mode I/O Port Protection

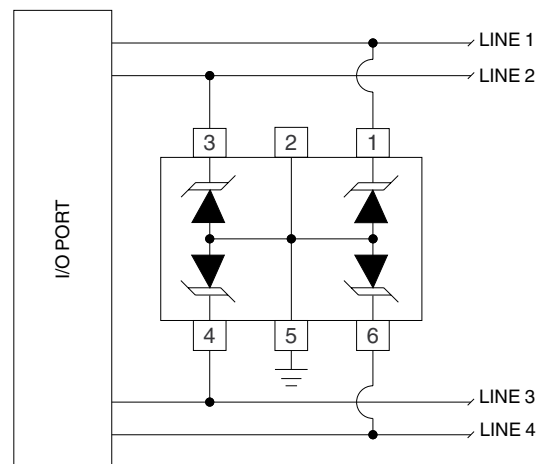
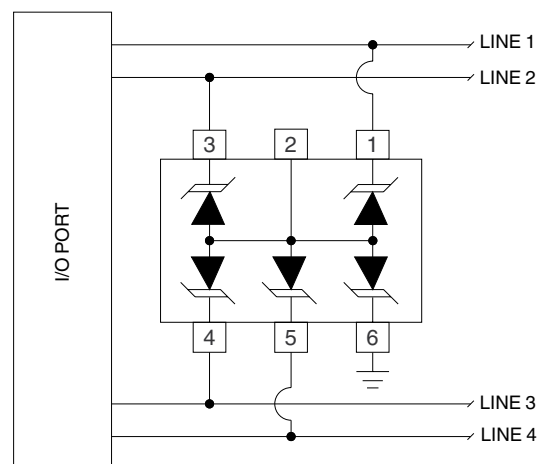
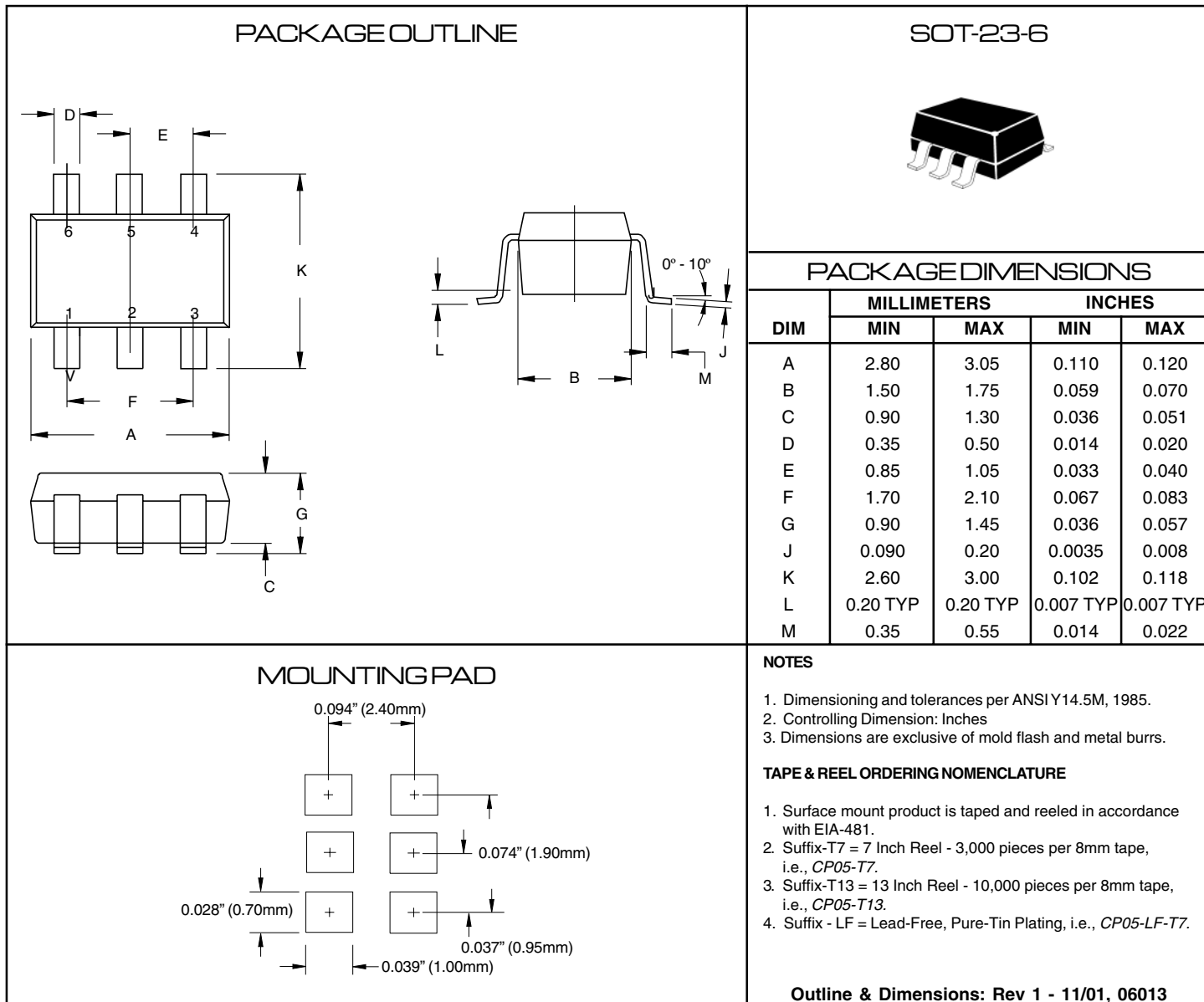


Figure 2 - Bidirectional Configuration
Common-Mode I/O Port Protection



PACKAGE OUTLINE & DIMENSIONS



COPYRIGHT © ProTek Devices 2005

SPECIFICATIONS: ProTek reserves the right to change the electrical and or mechanical characteristics described herein without notice (except JEDEC).

DESIGN CHANGES: ProTek reserves the right to discontinue product lines without notice, and that the final judgement concerning selection and specifications is the buyer's and that in furnishing engineering and technical assistance, ProTek assumes no responsibility with respect to the selection or specifications of such products.

ProTek Devices
2929 South Fair Lane, Tempe, AZ 85282
Tel: 602-431-8101 Fax: 602-431-2288
E-Mail: sales@protekdevices.com
Web Site: www.protekdevices.com