Dual 500mA/500mA Low Dropout, Low Noise, Micropower Linear Regulator

FEATURES

- **Output Current: 500mA per Channel**
- **Low Dropout Voltage: 300mV**
- **Low Noise: 20μV_{RMS} (10Hz to 100kHz)**
- **Low Quiescent Current: 55μA per Channel**
- Wide Input Voltage Range: 1.8V to 20V (Common or Independent Input Supply)
- Adjustable Output: 1.215V Reference Voltage
- Very Low Quiescent Current in Shutdown: <1μA per Channel
- Stable with 3.3μF Minimum Output Capacitor
- Stable with Ceramic, Tantalum or Aluminum Electrolytic Capacitors
- Reverse-Battery and Reverse Output-to-Input Protection
- Current Limit with Foldback and Thermal Shutdown
- Tracking/Sequencing Capability: Compatible with LTC292X Power Supply Tracking ICs
- Thermally Enhanced 16-Lead MSOP and 16-Lead (4mm × 3mm) DFN Packages

APPLICATIONS

- General Purpose Linear Regulator
- Battery-Powered Systems
- Microprocessor Core/Logic Supplies
- Post Regulator for Switching Supplies
- Tracking/Sequencing Power Supplies

DESCRIPTION

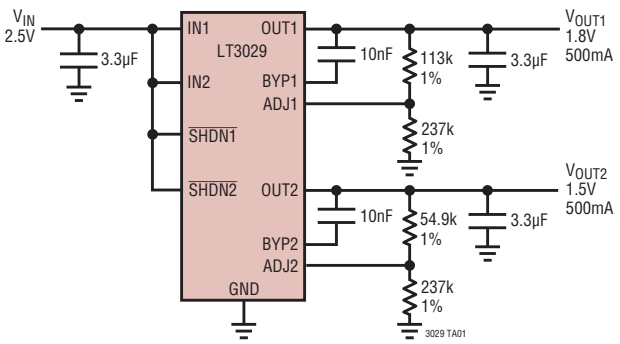
The LT®3029 is a dual, micropower, low noise, low dropout linear regulator. The device operates either with a common input supply or independent input supplies for each channel, over an input voltage range of 1.8V to 20V. Each output supplies up to 500mA of output current with a typical dropout voltage of 300mV. Quiescent current is well controlled in dropout. With an external 10nF bypass capacitor, output noise is only 20μV_{RMS} over a 10Hz to 100kHz bandwidth. Designed for use in battery-powered systems, the low 55μA quiescent current per channel makes it an ideal choice. In shutdown, quiescent current drops to less than 1μA. Shutdown control is independent for each channel, allowing for flexible power management.

The LT3029 optimizes stability and transient response with low ESR ceramic output capacitors, requiring a minimum of only 3.3μF. The regulator does not require the addition of ESR, as is common with other regulators.

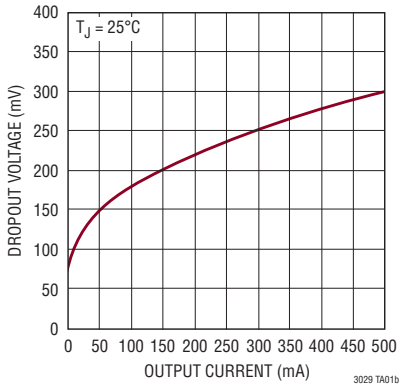
Internal circuitry provides reverse-battery protection, reverse-current protection, current limiting with foldback and thermal shutdown. The device is available as an adjustable output voltage device with a 1.215V reference voltage. The LT3029 is offered in the thermally enhanced 16-lead MSOP and 16-lead, low profile (4mm × 3mm × 0.75mm) DFN packages.

TYPICAL APPLICATION

2.5V_{IN} to 1.5V/1.8V Application



Dropout Voltage vs Load Current

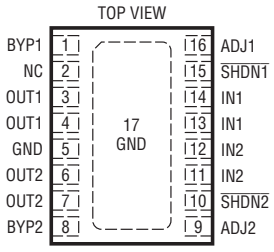


ABSOLUTE MAXIMUM RATINGS (Note 1)

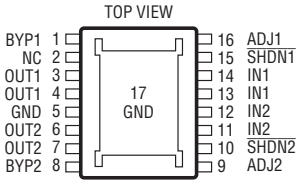
IN1, IN2 Pin Voltage ..... ±22V
OUT1, OUT2 Pin Voltage ..... ±22V
Input-to-Output Differential Voltage ..... ±22V
ADJ1, ADJ2 Pin Voltage ..... ±9V
BYP1, BYP2 Pin Voltage ..... ±0.6V
$\overline{SHDN1}$, $\overline{SHDN2}$ Pin Voltage ..... ±22V
Output Short-Circuit Duration ..... Indefinite

Operating Junction Temperature (Notes 2, 12)
LT3029E ..... –40°C to 125°C
LT3029I ..... –40°C to 125°C
LT3029H ..... –40°C to 150°C
LT3029MP ..... –55°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
(MSOP Only) ..... 300°C

PIN CONFIGURATION



DE PACKAGE
16-LEAD (4mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 38°C/W, θ_{JC} = 4.3°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB GND



MSE PACKAGE
16-LEAD PLASTIC MSOP

T_{JMAX} = 125°C (LT3029E/LT3029I, LT3029MP), θ_{JA} = 37°C/W, θ_{JC}: 5°C/W TO 10°C/W
T_{JMAX} = 150°C (LT3029H), θ_{JA} = 37°C/W, θ_{JC}: 5°C/W TO 10°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB GND

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3029EDE#PBF	LT3029EDE#TRPBF	3029	16-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LT3029IDE#PBF	LT3029IDE#TRPBF	3029	16-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LT3029EMSE#PBF	LT3029EMSE#TRPBF	3029	16-Lead Plastic MSOP	–40°C to 125°C
LT3029IMSE#PBF	LT3029IMSE#TRPBF	3029	16-Lead Plastic MSOP	–40°C to 125°C
LT3029HMSE#PBF	LT3029HMSE#TRPBF	3029	16-Lead Plastic MSOP	–40°C to 150°C
LT3029MPMSE#PBF	LT3029MPMSE#TRPBF	3029	16-Lead Plastic MSOP	–55°C to 125°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LT3029EDE	LT3029EDE#TR	3029	16-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LT3029IDE	LT3029IDE#TR	3029	16-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LT3029EMSE	LT3029EMSE#TR	3029	16-Lead Plastic MSOP	–40°C to 125°C
LT3029IMSE	LT3029IMSE#TR	3029	16-Lead Plastic MSOP	–40°C to 125°C
LT3029HMSE	LT3029HMSE#TR	3029	16-Lead Plastic MSOP	–40°C to 150°C
LT3029MPMSE	LT3029MPMSE#TR	3029	16-Lead Plastic MSOP	–55°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage (Notes 3, 11)	I_{LOAD} = 500mA	●		1.8	2.3	V
ADJ1, ADJ2 Pin Voltage (Notes 3, 4, 9)	V_{IN} = 2V, I_{LOAD} = 1mA		1.203	1.215	1.227	V
	2.3V < V_{IN} < 20V, 1mA < I_{LOAD} < 500mA (E, I, MP)	●	1.191	1.215	1.239	V
	2.3V < V_{IN} < 20V, 1mA < I_{LOAD} < 500mA (H)	●	1.173	1.215	1.239	V
Line Regulation (Note 3)	ΔV_{IN} = 2V to 20V, I_{LOAD} = 1mA	●		0.5	5	mV
Load Regulation (Note 3)	V_{IN} = 2.3V, ΔI_{LOAD} = 1mA to 500mA			2.5	6	mV
	V_{IN} = 2.3V, ΔI_{LOAD} = 1mA to 500mA (E, I, MP)	●			15	mV
	V_{IN} = 2.3V, ΔI_{LOAD} = 1mA to 500mA (H)	●			32	mV
Dropout Voltage V_{IN} = $V_{OUT(NOMINAL)}$ (Notes 5, 6, 11)	I_{LOAD} = 10mA			0.11	0.18	V
	I_{LOAD} = 10mA	●			0.25	V
	I_{LOAD} = 50mA			0.16	0.22	V
	I_{LOAD} = 50mA	●			0.31	V
	I_{LOAD} = 100mA			0.2	0.25	V
	I_{LOAD} = 100mA	●			0.34	V
	I_{LOAD} = 500mA			0.3	0.36	V
	I_{LOAD} = 500mA	●			0.46	V
GND Pin Current (per Channel) V_{IN} = $V_{OUT(NOMINAL)}$ (Notes 5, 7)	I_{LOAD} = 0mA	●		55	150	µA
	I_{LOAD} = 1mA	●		90	250	µA
	I_{LOAD} = 50mA	●		1.1	2	mA
	I_{LOAD} = 100mA	●		2	3.5	mA
	I_{LOAD} = 250mA	●		4.3	8	mA
	I_{LOAD} = 500mA	●		10	16	mA
Output Voltage Noise	C_{OUT} = 10µF, C_{BYP} = 10nF, I_{LOAD} = 500mA, BW = 10Hz to 100kHz			20		μV_{RMS}
ADJ1/ADJ2 Pin Bias Current	ADJ1, ADJ2 (Notes 3, 8)			30	100	nA
Shutdown Threshold	V_{OUT} = Off to On	●		0.45	1.1	V
	V_{OUT} = On to Off	●	0.20	0.40		V
$\overline{SHDN1}$/$\overline{SHDN2}$ Pin Current (Note 10)	$V_{\overline{SHDN1}}$, $V_{\overline{SHDN2}}$ = 0V	●		0	0.5	µA
	$V_{\overline{SHDN1}}$, $V_{\overline{SHDN2}}$ = 20V	●		0.6	3	µA
Quiescent Current in Shutdown (per Channel)	V_{IN} = 6V, $V_{\overline{SHDN1}}$ = 0V, $V_{\overline{SHDN2}}$ = 0V			0.01	0.1	µA
Ripple Rejection	V_{IN} = 2.715V (Avg), V_{RIPPLE} = 0.5V_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 500mA		55	67		dB
Current Limit (Note 9)	V_{IN} = 7V, V_{OUT} = 0V			1.5		A
	V_{IN} = 2.3V, ΔV_{OUT} = –0.1V	●	520			mA
Input Reverse Leakage Current	V_{IN} = –20V, V_{OUT} = 0V	●			1	mA
Reverse Output Current	V_{OUT} = 1.215V, V_{IN} = 0V			0.5	10	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3029 is tested and specified under pulse load conditions such that $T_J \approx T_A$. The LT3029E is 100% tested at T_A = 25°C. Performance of the LT3029E over the full –40°C to 125°C operating junction temperature range is assured by design, characterization and correlation with statistical process controls. The LT3029I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT3029MP is 100% tested and guaranteed over the –55°C to 125°C operating junction temperature range. The LT3029H is tested at 150°C operating junction temperature. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 3: The LT3029 is tested and specified for these conditions with the ADJ1/ADJ2 pin connected to the corresponding OUT1/OUT2 pin.

Note 4: Maximum junction temperature limits operating conditions. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, limit the output current range. When operating at maximum output current, limit the input voltage range.

Note 5: To satisfy minimum input voltage requirements, the LT3029 is tested and specified for these conditions with an external resistor divider (two 243k resistors) for an output voltage of 2.437V. The external resistor divider adds 5µA of DC load on the output.

Note 6: Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage equals: $V_{IN} - V_{DROPOUT}$.

ELECTRICAL CHARACTERISTICS

Note 7: GND pin current is tested with V_{IN} = 2.437V and a current source load. This means the device is tested while operating in its dropout region or at the minimum input voltage specification. This is the worst-case GND pin current. The GND pin current decreases slightly at higher input voltages. Total GND pin current equals the sum of output 1 and output 2 GND pin currents.

Note 8: ADJ1/ADJ2 pin bias current flows into the pin.

Note 9: The LT3029 contains current limit foldback circuitry. See the Typical Performance Characteristics for current limit as a function of the $V_{IN} – V_{OUT}$ differential voltage.

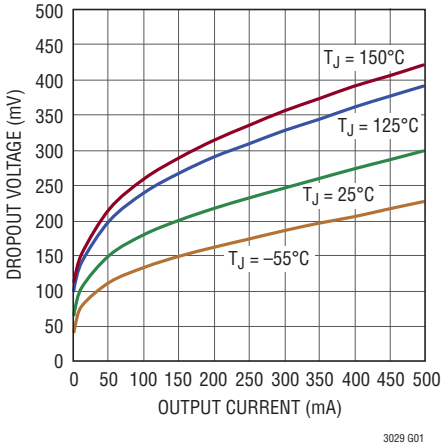
Note 10: $\overline{SHDN1}$/$\overline{SHDN2}$ pin current flows into the pin.

Note 11: The LT3029 minimum input voltage specification limits dropout voltage under some output voltage/load conditions. See the curve of Minimum Input Voltage in the Typical Performance Characteristics.

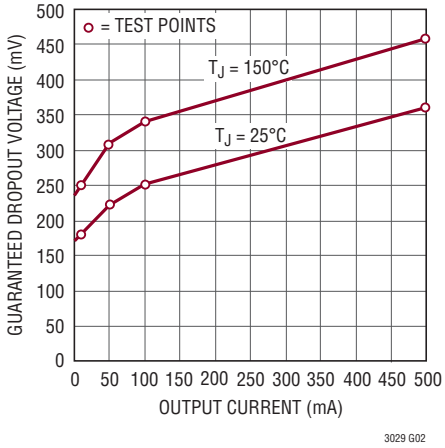
Note 12: The LT3029 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature exceeds the maximum operating junction temperature when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

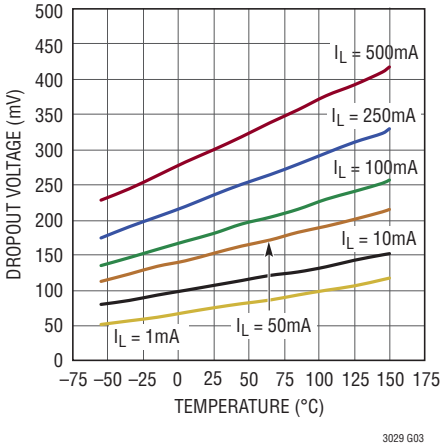
Typical Dropout Voltage



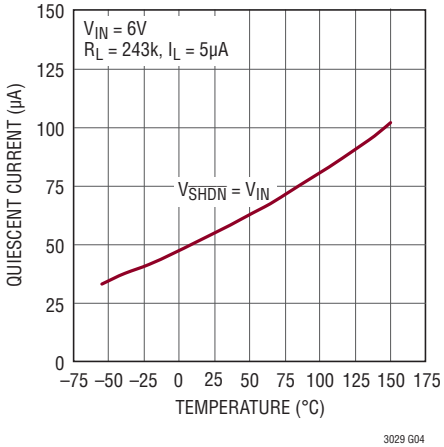
Guaranteed Dropout Voltage



Dropout Voltage vs Temperature

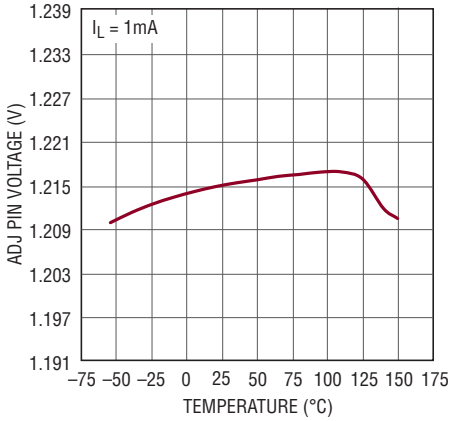


Quiescent Current (per Channel)

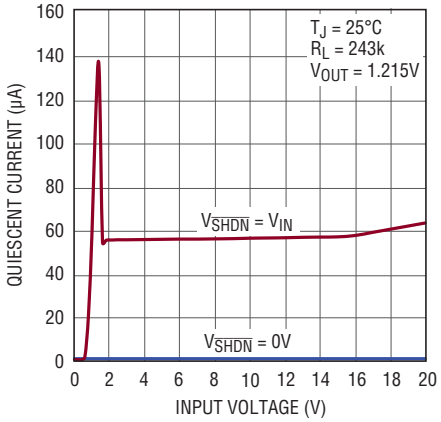


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

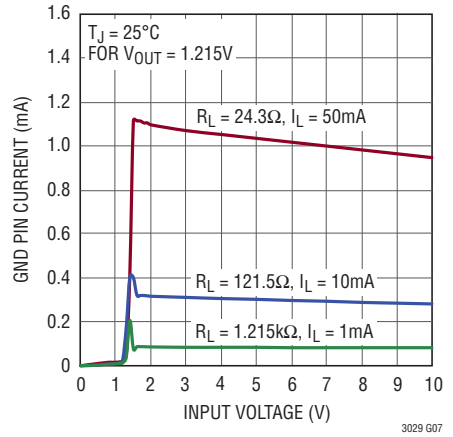
ADJ1 or ADJ2 Pin Voltage



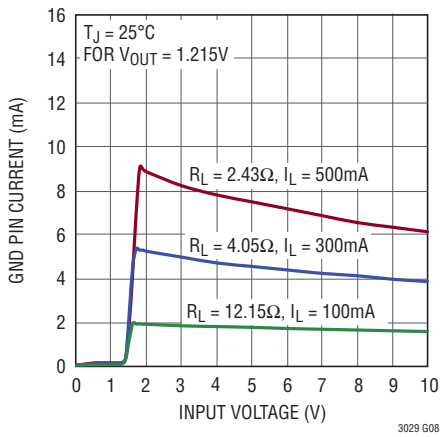
Quiescent Current (per Channel)



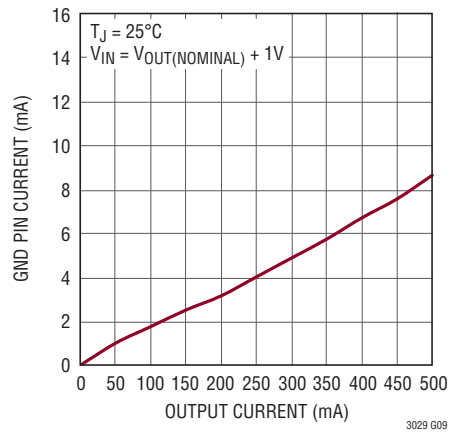
GND Pin Current (per Channel)



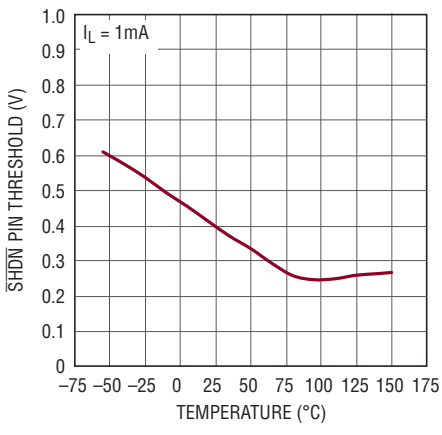
GND Pin Current (per Channel)



GND Pin Current vs I_{LOAD}

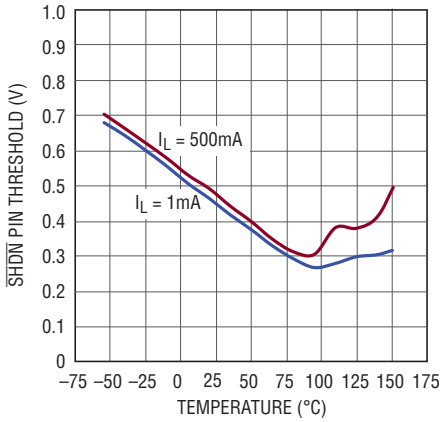


$\overline{SHDN1}$ or $\overline{SHDN2}$ Pin Threshold (On-to-Off)

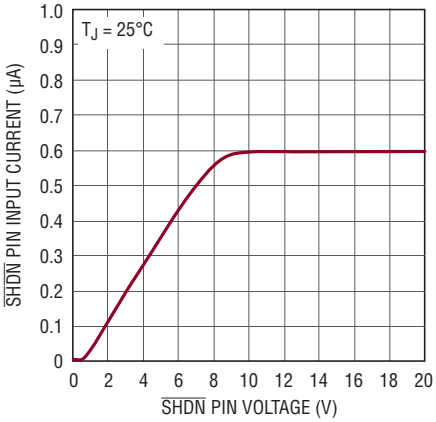


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

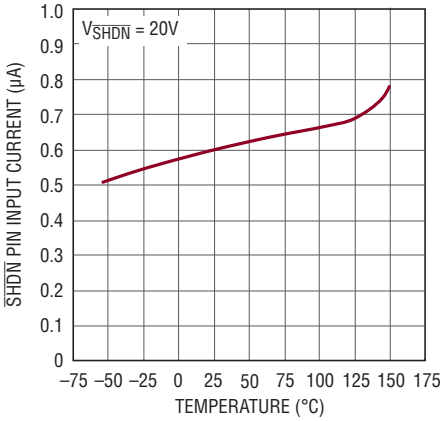
$\overline{SHDN1}$ or $\overline{SHDN2}$ Pin Threshold (Off-to-On)



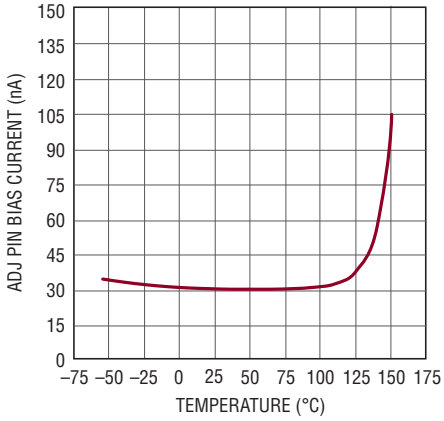
$\overline{SHDN1}$ or $\overline{SHDN2}$ Pin Input Current



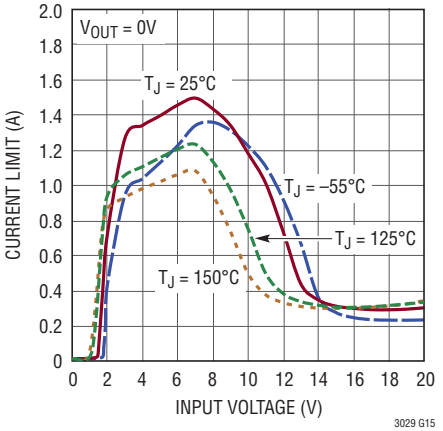
$\overline{SHDN1}$ or $\overline{SHDN2}$ Pin Input Current



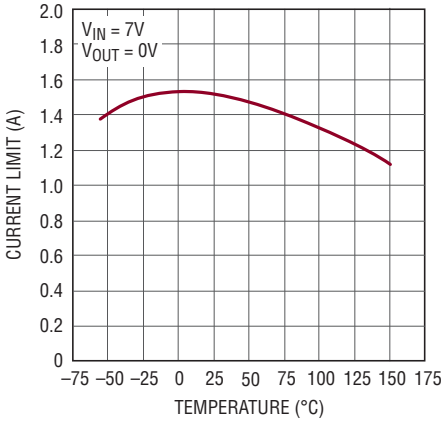
ADJ1 or ADJ2 Pin Bias Current



Current Limit

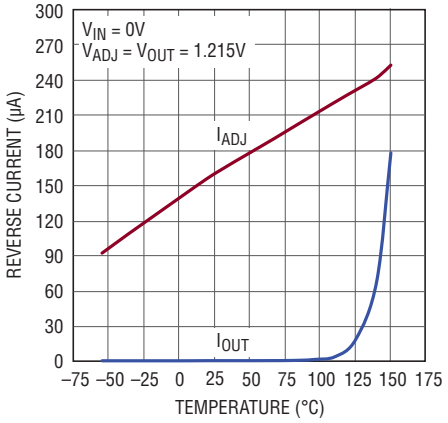


Current Limit



TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

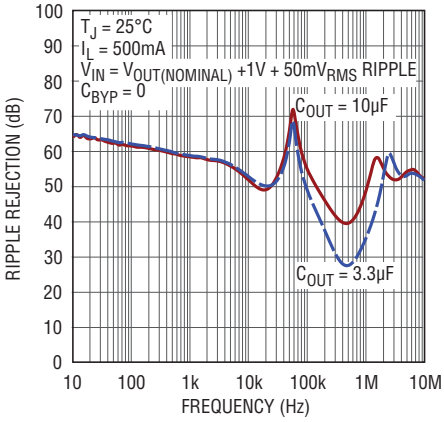
Reverse Current



I_{ADJ} FLOWS INTO ADJ PIN TO GND PIN
I_{OUT} FLOWS INTO OUT PIN TO IN PIN

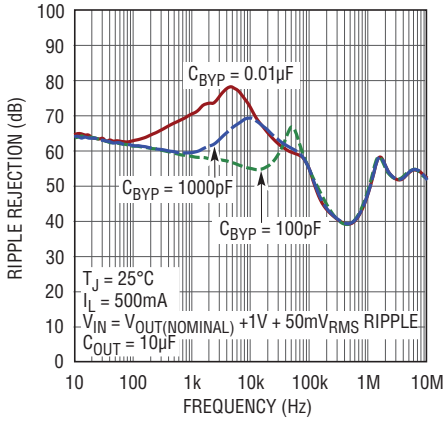
3029 G17

Input Ripple Rejection



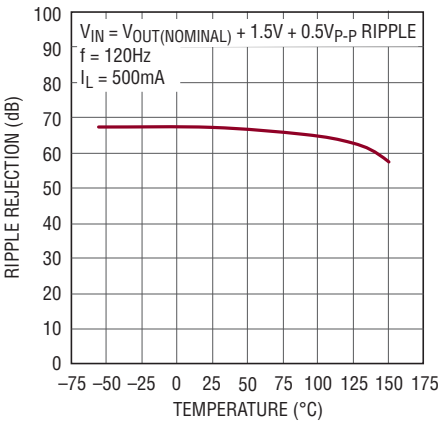
3029 G18

Input Ripple Rejection



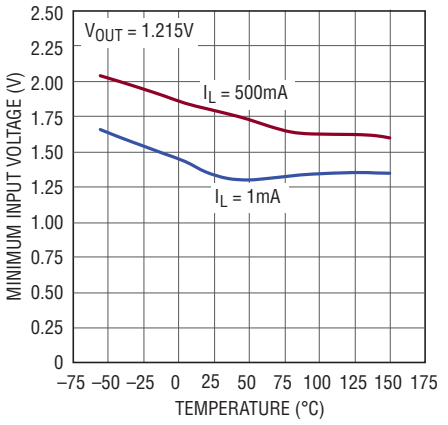
3029 G19

Input Ripple Rejection



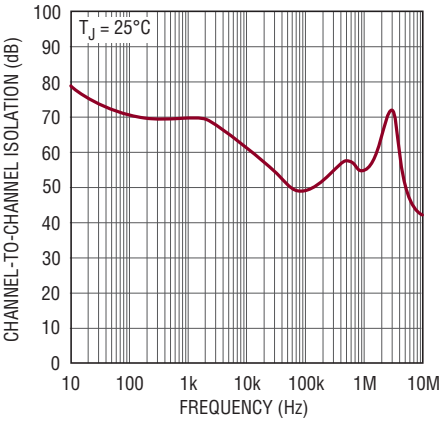
3029 G20

Minimum Input Voltage



3029 G21

Channel-to-Channel Isolation

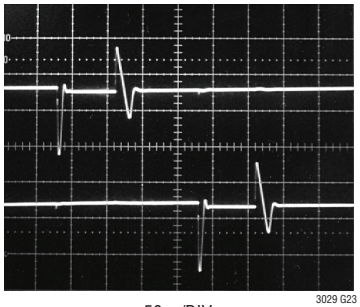


GIVEN CHANNEL IS TESTED WITH 50mVRMS SIGNAL ON OPPOSING CHANNEL, BOTH CHANNELS DELIVERING FULL CURRENT

3029 G22

TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

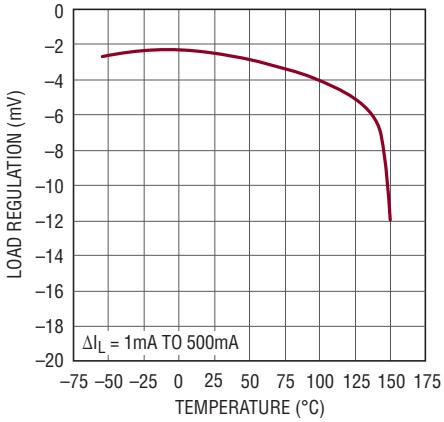
Channel-to-Channel Isolation



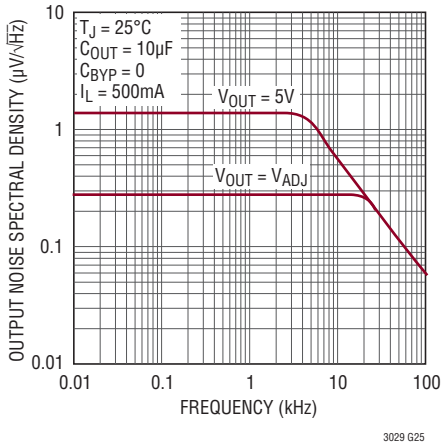
50µs/DIV

C_{OUT1} = 10µF
C_{OUT2} = 10µF
C_{BYP1} = C_{BYP2} = 0.01µF
ΔI_{L1} = 50mA TO 500mA
ΔI_{L2} = 50mA TO 500mA
V_{IN} = 6V, V_{OUT1} = V_{OUT2} = 5V

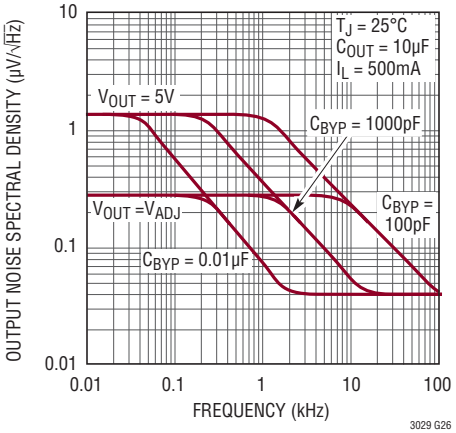
Load Regulation



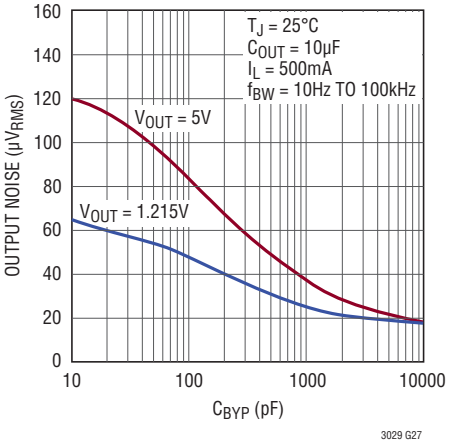
Output Noise Spectral Density



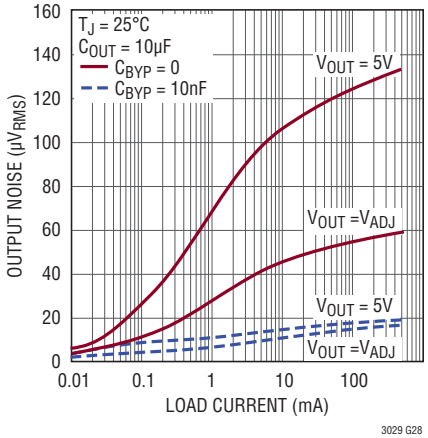
Output Noise Spectral Density



RMS Output Noise vs Bypass Capacitor

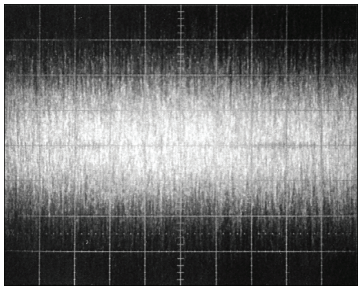


RMS Output Noise vs Load Current



TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

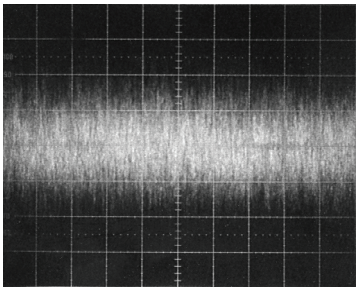
10Hz to 100kHz Output Noise, C_{BYP} = 0pF



1ms/DIV

C_{OUT} = 10µF
I_L = 500mA
V_{OUT} = 5V

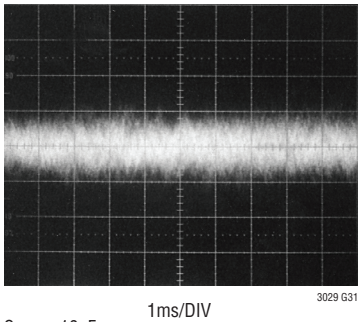
10Hz to 100kHz Output Noise, C_{BYP} = 100pF



1ms/DIV

C_{OUT} = 10µF
I_L = 500mA
V_{OUT} = 5V

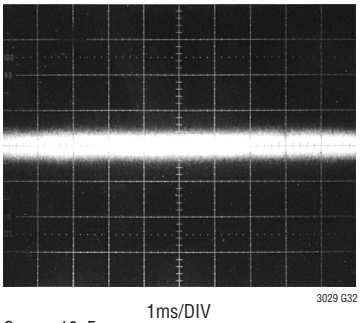
10Hz to 100kHz Output Noise, C_{BYP} = 1000pF



1ms/DIV

C_{OUT} = 10µF
I_L = 500mA
V_{OUT} = 5V

10Hz to 100kHz Output Noise, C_{BYP} = 0.01µF

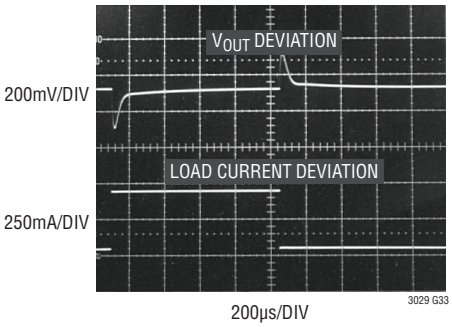


1ms/DIV

C_{OUT} = 10µF
I_L = 500mA
V_{OUT} = 5V

TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

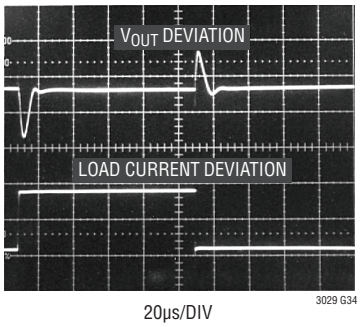
Transient Response, C_{BYP} = 0pF



200µs/DIV

V_{IN} = 6V I_L = 100mA
C_{IN} = 10µF T_J = 25°C
C_{OUT} = 10µF V_{OUT} = 5V

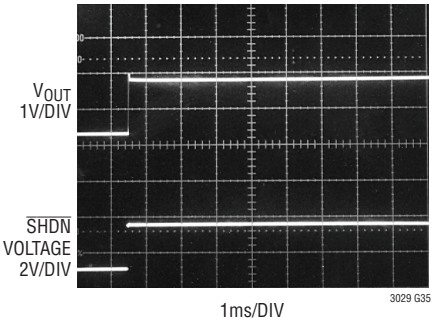
Transient Response, C_{BYP} = 0.01µF



20µs/DIV

V_{IN} = 6V I_L = 100mA
C_{IN} = 10µF T_J = 25°C
C_{OUT} = 10µF V_{OUT} = 5V

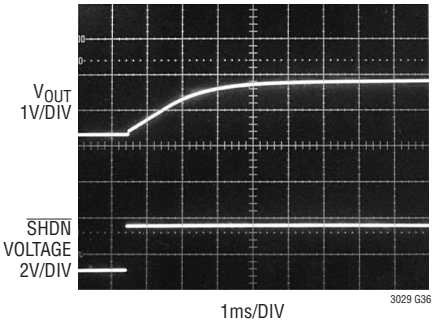
Start-Up Time from Shutdown, C_{BYP} = 0pF



1ms/DIV

V_{IN} = 2.5V I_L = 500mA
C_{OUT} = 10µF V_{OUT} = 1.5V
R_L = 3Ω

Start-Up Time from Shutdown, C_{BYP} = 0.01µF



1ms/DIV

V_{IN} = 2.5V I_L = 500mA
C_{OUT} = 10µF V_{OUT} = 1.5V
R_L = 3Ω

PIN FUNCTIONS

BYP1/BYP2 (Pin 1/Pin 8): Bypass. Use the BYP1/BYP2 pins to bypass the reference of the LT3029 regulator and achieve low output noise performance. Internal circuitry clamps the BYP1/BYP2 pins to ±0.6V (one V_{BE}) from ground. A small capacitor from the corresponding output to this pin bypasses the reference to lower the output voltage noise. Using a maximum value of 10nF reduces the output voltage noise to a typical 20μV_{RMS} over a 10Hz to 100kHz bandwidth. If not used, this pin must be left unconnected.

NC (Pin 2): No Connect. This pin is not connected to any internal circuitry. It may be floated, tied to V_{IN} or tied to GND.

OUT1/OUT2 (Pins 3, 4/Pins 6, 7): Output. The outputs supply power to the loads. A minimum 3.3μF output capacitor prevents oscillations on each output. Applications with large output load transients require larger values of output capacitance to limit peak voltage transients. See the Applications Information section for more on output capacitance and reverse output characteristics.

GND (Pin 5, 17): Ground. The exposed pad (Pin 17) of the DFN and MSOP packages is an electrical connection to GND. To ensure proper electrical and thermal performance, solder Pin 17 to the PCB ground and tie directly to Pin 5. Connect the bottom of the output voltage setting resistor divider directly to GND (Pin 5) for optimum load regulation performance.

IN1/IN2 (Pins 13, 14/Pins 11, 12): Inputs. The IN1/IN2 pins supply power to each channel. The LT3029 requires a bypass capacitor at the IN1/IN2 pins if located more than six inches away from the main input filter capacitor. Include a bypass capacitor in battery-powered circuits, as a battery's output impedance rises with frequency. A bypass capacitor in the range of 1μF to 10μF suffices. The LT3029's design withstands reverse voltages on the IN pins with respect to ground and the OUT pins. In the case of a reversed input, which occurs if a battery is plugged in backwards, the LT3029 acts as if a diode is in series with its input. No reverse current flows into the LT3029 and no reverse voltage appears at the load. The device protects itself and the load.

$\overline{\text{SHDN1}}$/$\overline{\text{SHDN2}}$ (Pin 15/Pin 10): Shutdown. Pulling the $\overline{\text{SHDN1}}$ or $\overline{\text{SHDN2}}$ pin low puts its corresponding LT3029 channel into a low power state and turns its output off. The $\overline{\text{SHDN1}}$ and $\overline{\text{SHDN2}}$ pins are completely independent of each other, and each $\overline{\text{SHDN}}$ pin only affects operation on its corresponding channel. Drive the $\overline{\text{SHDN1}}$ and $\overline{\text{SHDN2}}$ pins with either logic or an open collector/drain with pull-up resistors. The resistors supply the pull-up current to the open collectors/drains and the $\overline{\text{SHDN1}}$ or $\overline{\text{SHDN2}}$ current, typically less than 1μA. If unused, connect the $\overline{\text{SHDN1}}$ and $\overline{\text{SHDN2}}$ to their corresponding IN pins. Each channel will be in its low power shutdown state if its corresponding $\overline{\text{SHDN}}$ pin is not connected.

ADJ1/ADJ2: (Pin 16/Pin 9) Adjust Pin. These are the error amplifier inputs. These pins are internally clamped to ±9V. A typical input bias current of 30nA flows into the pins (see curve of ADJ1/ADJ2 Pin Bias Current vs Temperature in the Typical Performance Characteristics section). The ADJ1 and ADJ2 pin voltage is 1.215V referenced to ground and the output voltage range is 1.215V to 19.5V.

APPLICATIONS INFORMATION

The LT3029 is a dual 500mA/500mA low dropout regulator with independent inputs, micropower quiescent current and shutdown. The device supplies up to 500mA from each channel's output at a typical dropout voltage of 300mV. The two regulators share a common GND pin and are thermally coupled. However, the two inputs and outputs of the LT3029 operate independently. **Each channel can be shut down independently, but a thermal shutdown fault on either channel shuts off the output on both channels.** The addition of a 10nF reference bypass capacitor lowers output voltage noise to 20μV_{RMS} over a 10Hz to 100kHz bandwidth. Additionally, the reference bypass capacitor improves transient response of the regulator, lowering the settling time for transient load conditions. The low operating quiescent current (55μA per channel) drops to less than 1μA in shutdown. In addition to the low quiescent current, the LT3029 regulator incorporates several protection features that make it ideal for use in battery-powered systems. Most importantly, the device protects itself against reverse input voltages. Current limiting with foldback necessitates a minimum load current of 20μA for input/output voltage differentials of more than 10V to keep the output regulated.

Adjustable Operation

Each of the LT3029's channels has an output voltage range of 1.215V to 19.5V. Figure 1 illustrates that output voltage is set by the ratio of two external resistors. The device regulates the output to maintain the corresponding ADJ pin voltage at 1.215V referenced to ground. R1's current equals 1.215V/R1. R2's current equals R1's current plus the ADJ pin bias current. The ADJ pin bias current, 30nA at 25°C, flows through R2 into the ADJ pin. Use the formula in Figure 1 to calculate output voltage. Linear Technology recommends that the value of R1 be less than 243k to minimize errors in the output voltage due to the ADJ pin bias current. In shutdown, the output turns off and the divider current is zero. Curves of ADJ Pin Voltage vs Temperature and ADJ Pin Bias Current vs Temperature appear in the Typical Performance Characteristics section.

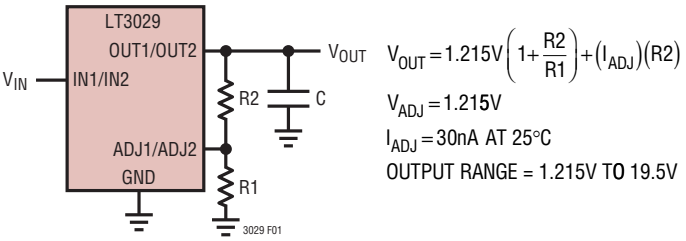


Figure 1. Adjustable Operation

Linear Technology tests and specifies each LT3029 channel with its ADJ pin tied to the corresponding OUT pin for a 1.215V output voltage. Specifications for output voltages greater than 1.215V are proportional to the ratio of desired output voltage to 1.215V:

$$\frac{V_{OUT}}{1.215V}$$

For example, load regulation on either output for an output current change of 1mA to 500mA is typically –2.5mV at V_{OUT} = 1.215V. At V_{OUT} = 2.5V, load regulation is:

$$\frac{2.5V}{1.215V} \bullet (-2.5mV) = -5.14mV$$

Table 1 shows 1% resistor divider values for some common output voltages with a resistor divider current of approximately 5μA.

Table 1. Output Voltage Resistor Divider Values

V_{OUT} (V)	R1 (k)	R2 (k)
1.5	237	54.9
1.8	237	113
2.5	243	255
3	232	340
3.3	210	357
5	200	619

APPLICATIONS INFORMATION

Bypass Capacitance and Low Noise Performance

Using a bypass capacitor connected between a channel's BYP pin and its corresponding OUT pin significantly lowers LT3029 output voltage noise, but is not required in all applications. Linear Technology recommends a good quality low leakage capacitor. This capacitor bypasses the regulator's reference, providing a low frequency noise pole. A 10nF bypass capacitor introduces a noise pole that decreases output voltage noise to as low as $20\mu V_{RMS}$. Using a bypass capacitor provides the added benefit of improving transient response. With no bypass capacitor, and a 10µF output capacitor, a 100mA to 500mA load step settles to within 1% of its final value in approximately 100µs. With the addition of a 10nF bypass capacitor and evaluating the same load step, output voltage excursion stays within 1% (see Transient Response in the Typical Performance Characteristics section). Using a bypass capacitor makes regulator start-up time proportional to the value of the bypass capacitor. For example, a 10nF bypass capacitor and 10µF output capacitor slow start-up time to 15ms.

Output Capacitance and Transient Response

The LT3029 design is stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. Linear Technology recommends a minimum output capacitor of 3.3µF with an ESR of 3Ω, or less, to prevent oscillations. The LT3029 is a micropower device, and output transient response is a function of output capacitance. Larger values of output capacitance decrease the peak deviations and provide improved transient response for larger load current changes.

Ceramic capacitors require extra consideration. Manufacturers make ceramic capacitors with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics specify the EIA temperature characteristic codes of Z5U, Y5V, X5R and X7R. Z5U and Y5V dielectrics provide high C-V products in a small package at low cost, but exhibit strong voltage and temperature coefficients, as shown in Figures 2 and 3. When used with a 5V regulator, a 16V 10µF Y5V capacitor can exhibit an effective value as low as 1µF to

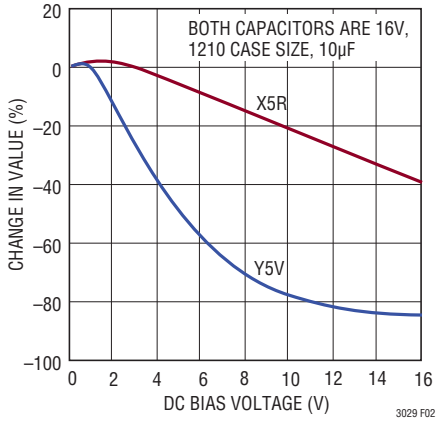


Figure 2. Ceramic Capacitor DC Bias Characteristics

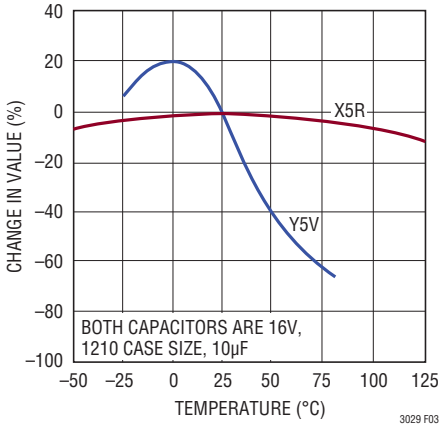


Figure 3. Ceramic Capacitor Temperature Characteristics

APPLICATIONS INFORMATION

2µF for the applied DC bias voltage and over the operating temperature range. X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values.

Exercise care even when using X5R and X7R capacitors; the X5R and X7R codes only specify operating temperature range and maximum capacitance change over temperature. Capacitance change due to DC bias (voltage coefficient) with X5R and X7R capacitors is better than with Y5V and Z5U capacitors, but can still be significant enough to drop capacitor values below appropriate levels. Capacitor DC bias characteristics tend to improve as case size increases. Linear Technology recommends verifying expected versus actual capacitance values at operating voltage in situ for an application.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor, the stress can be induced by vibrations in the system or thermal transients. The resulting voltages produced can cause appreciable amounts of noise, especially when a ceramic capacitor is used for noise bypassing. A ceramic capacitor produced Figure 4's trace in response to light tapping from a pencil. Similar vibration induced behavior can masquerade as increased output voltage noise.

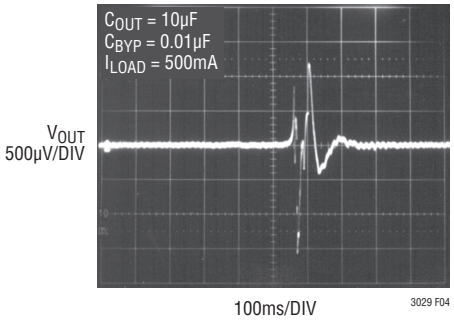


Figure 4. Noise Resulting from Tapping on a Ceramic Capacitor

APPLICATIONS INFORMATION

Thermal Considerations

The LT3029's power handling capability limits the maximum rated junction temperature (125°C, LT3029E/LT3029I/LT3029MP or 150°C, LT3029H). Two components comprise the power dissipated by each channel:

1. Output current multiplied by the input/output voltage differential: $(I_{OUT})(V_{IN} – V_{OUT})$, and
2. GND pin current multiplied by the input voltage: $(I_{GND})(V_{IN})$.

Ground pin current is found by examining the GND Pin Current curves in the Typical Performance Characteristics section.

Power dissipation for each channel equals the sum of the two components listed above. Total power dissipation for the LT3029 equals the sum of the power dissipated by each channel.

The LT3029's internal thermal shutdown circuitry protects both channels of the device if either channel experiences an overload or fault condition. Activation of the thermal shutdown circuitry turns both channels off. If the overload or fault condition is removed, both outputs are allowed to turn back on. For continuous normal conditions, do not exceed the maximum junction temperature rating of 125°C (LT3029E/LT3029I/LT3029MP) or 150°C (LT3029H). Carefully consider all sources of thermal resistance from junction-to-ambient, including additional heat sources mounted in proximity to the LT3029. For surface mount devices, use the heat spreading capabilities of the PC board and its copper traces to accomplish heat sinking. Copper board stiffeners and plated through-holes can also spread the heat generated by power devices.

The following tables list thermal resistance as a function of copper area in a fixed board size. All measurements were taken in still air on a four-layer FR-4 board with 1oz solid internal planes, and 2oz external trace planes with a total board thickness of 1.6mm. For further information on thermal resistance and using thermal information, refer to JEDEC standard JESD51, notably JESD51-12.

Table 2. DE Package, 16-Lead DFN

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOPSIDE*	BACKSIDE		
2500mm^2	2500mm^2	2500mm^2	36°C/W
1000mm^2	2500mm^2	2500mm^2	37°C/W
225mm^2	2500mm^2	2500mm^2	38°C/W
100mm^2	2500mm^2	2500mm^2	40°C/W

*Device is mounted on topside.

Table 3. MSE Package, 16-Lead MSOP

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOPSIDE*	BACKSIDE		
2500mm^2	2500mm^2	2500mm^2	35°C/W
1000mm^2	2500mm^2	2500mm^2	36°C/W
225mm^2	2500mm^2	2500mm^2	37°C/W
100mm^2	2500mm^2	2500mm^2	39°C/W

*Device is mounted on topside.

The junction-to-case thermal resistance (θ_{JC}), measured at the Exposed Pad on the back of the die, is 4.3°C/W for the DFN package, and 5°C/W to 10°C/W for the MSOP package.

APPLICATIONS INFORMATION

Calculating Junction Temperature

Example: Channel 1's output voltage is set to 1.8V. Channel 2's output voltage is set to 1.5V. Each channel's input voltage is 2.5V. Each channel's output current range is 0mA to 500mA. The application has a maximum ambient temperature of 50°C. What is the LT3029's maximum junction temperature?

The power dissipated by each channel equals:

$$I_{OUT(MAX)}(V_{IN} - V_{OUT}) + I_{GND}(V_{IN})$$

where for each output:

$I_{OUT(MAX)}$ = 500mA

V_{IN} = 2.5V

I_{GND} at (I_{OUT} = 500mA, V_{IN} = 2.5V) = 8.5mA

So, for output 1:

P = 500mA (2.5V – 1.8V) + 8.5mA (2.5V) = 0.37W

For output 2:

P = 500mA (2.5V – 1.5V) + 8.5mA (2.5V) = 0.52W

The thermal resistance is in the range of 35°C/W to 40°C/W, depending on the copper area. So, the junction temperature rise above ambient temperature approximately equals:

(0.37W + 0.52W) 39°C/W = 34.7°C

The maximum junction temperature then equals the maximum ambient temperature plus the maximum junction temperature rise above ambient temperature, or:

T_{JMAX} = 50°C + 34.7°C = 84.7°C

Protection Features

The LT3029 regulator incorporates several protection features that make it ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the device protects itself against reverse input voltages and reverse voltages from output to input. The two regulators have independent inputs, a common GND pin and are thermally coupled. However, the two channels of the LT3029 operate independently. Each channel's output can be shut down independently, and a fault condition on one output does not affect the other output electrically, unless the thermal shutdown circuitry is activated.

Current limit protection and thermal overload protection protect the device against current overload conditions at each output of the LT3029. For normal operation, do not allow the junction temperature to exceed 125°C (LT3029E/LT3029I/LT3029MP) or 150°C (LT3029H). The typical thermal shutdown temperature threshold is 165°C and the circuitry incorporates approximately 5°C of hysteresis.

Each channel's input withstands reverse voltages of 22V. Current flow into the device is limited to less than 1mA (typically less than 100µA) and no negative voltage appears at the respective channel's output. The device protects both itself and the load against batteries that are plugged in backwards.

The LT3029 incurs no damage if either channel's output is pulled below ground. If the input is left open-circuit, or grounded, the output can be pulled below ground by

APPLICATIONS INFORMATION

22V. The output acts like an open circuit, and no current flows from the output. However, current flows in (but is limited by) the external resistor divider that sets the output voltage.

The LT3029 incurs no damage if either ADJ pin is pulled above or below ground by 9V. If the input is left open circuit or grounded, the ADJ pins perform like an open circuit down to –1.5V, and then like a 1.2k resistor down to –9V when pulled below ground. When pulled above ground, the ADJ pins perform like an open circuit up to 0.5V, then like a 5.7k resistor up to 3V, then like a 1.8k resistor up to 9V.

In situations where an ADJ pin connects to a resistor divider that would pull the pin above its 9V clamp voltage if the output is pulled high, the ADJ pin input current must be limited to less than 5mA. For example, assume a resistor divider sets the regulated output voltage to 1.5V, and the output is forced to 20V. The top resistor of the resistor divider must be chosen to limit the current into the ADJ pin to less than 5mA when the ADJ pin is at 9V. The 11V difference between the OUT and ADJ pins divided by the 5mA maximum current into the ADJ pin yields a minimum top resistor value of 2.2k.

In circuits where a backup battery is required, several different input/output conditions can occur. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage or is left open-circuit. Current flow back into the output follows the curve shown in Figure 5.

If either of the LT3029's IN pins is forced below its corresponding OUT pin, or the OUT pin is pulled above its corresponding IN pin, input current for that channel typically drops to less than 2µA. This occurs if the IN pin is connected to a discharged (low voltage) battery, and either a backup battery or a second regulator circuit holds up the output. The state of that channel's $\overline{SHDN}$ pin has no effect on the reverse output current if the output is pulled above the input.

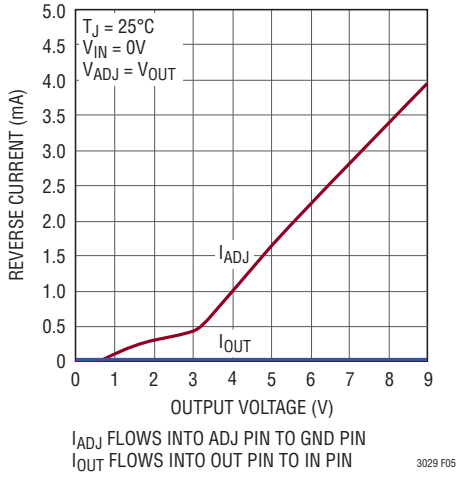
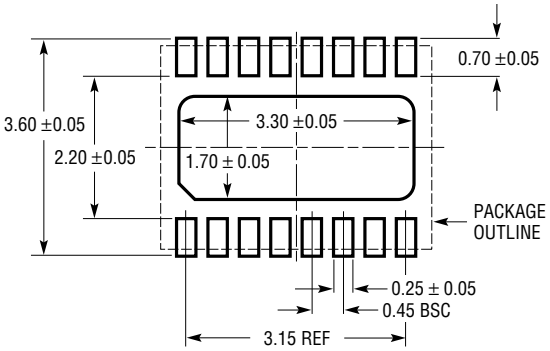


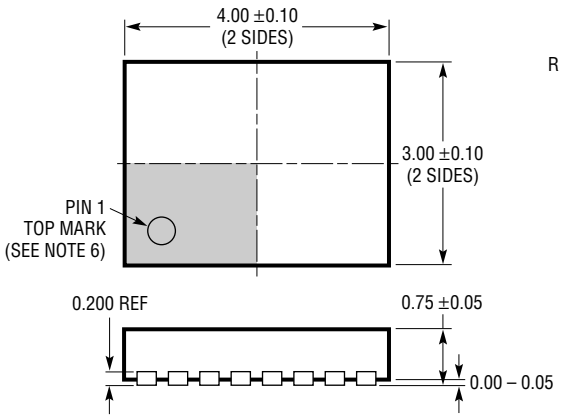
Figure 5. Reverse Output Current

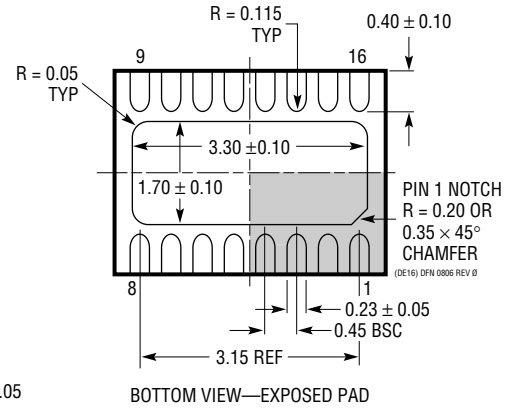
PACKAGE DESCRIPTION

DE Package
16-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1732 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



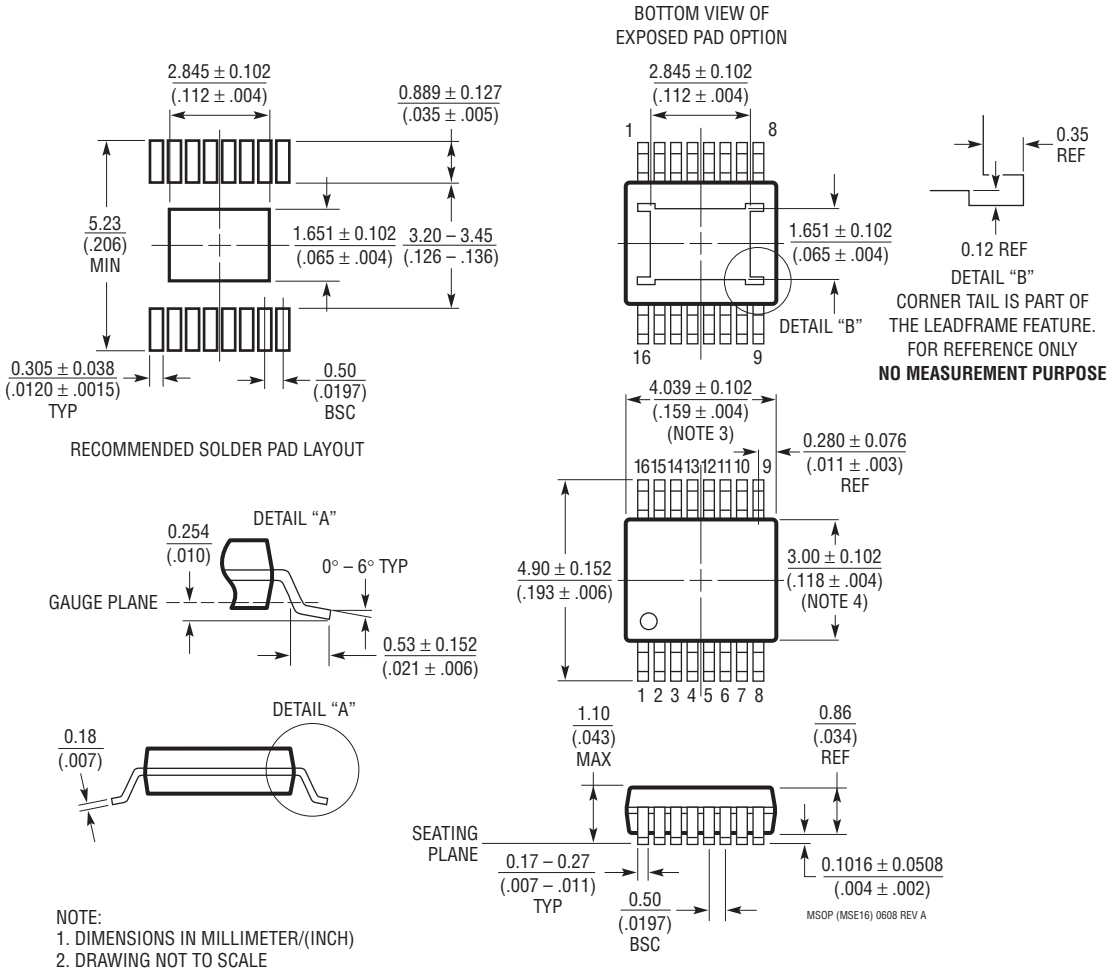


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WGED-3) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

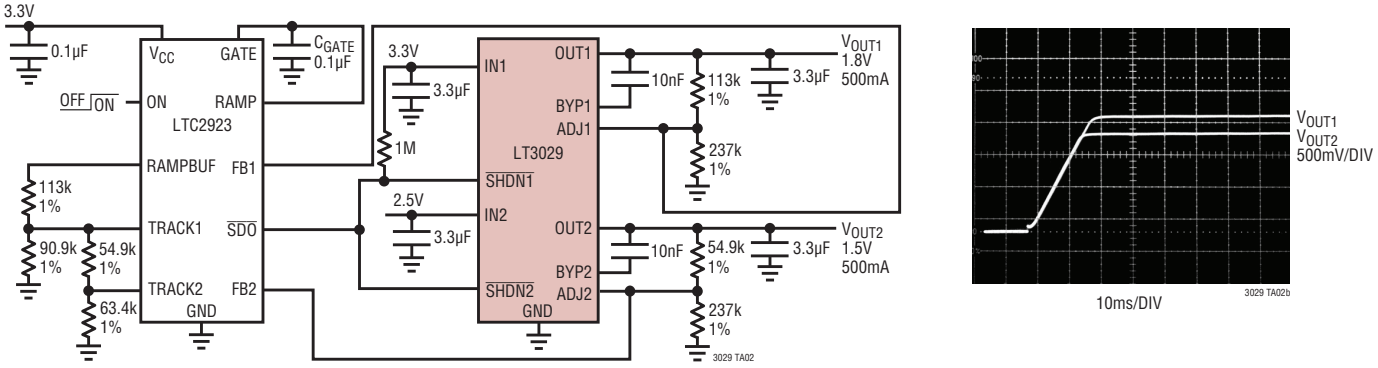
MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev A)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

TYPICAL APPLICATION

Coincident Tracking Supply Application



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1761	100mA, Low Noise Micropower LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.3V, I_Q = 20µA, I_{SD} < 1µA, Low Noise < 20µV_{RMS}, Stable with 1µF Ceramic Capacitors, ThinSOT™ Package
LT1763	500mA, Low Noise Micropower LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.3V, I_Q = 30µA, I_{SD} < 1µA, Low Noise < 20µV_{RMS}, S8 and DFN Packages
LT1963/ LT1963A	1.5A, Low Noise, Fast Transient Response LDOs	V_{IN}: 2.1V to 20V, $V_{OUT(MIN)}$ = 1.21V, V_{DO} = 0.34V, I_Q = 1mA, I_{SD} < 1µA, Low Noise: < 40µV_{RMS}, "A" Version Stable with Ceramic Capacitors; DD, TO220-5, SOT223, S8 and TSSOP Packages
LT1964	200mA, Low Noise Micropower, Negative LDO	V_{IN}: –1.9V to –20V, $V_{OUT(MIN)}$ = –1.22V, V_{DO} = 0.34V, I_Q = 30µA, I_{SD} = 3µA, Low Noise: <30µV_{RMS}, Stable with Ceramic Capacitors, ThinSOT Package
LT1965	1.1A, Low Noise LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.20V, V_{DO} = 0.31V, I_Q = 0.5mA, I_{SD} < 1µA, Low Noise: <40µV_{RMS}, Stable with Ceramic Capacitors; 3mm × 3mm DFN, MS8E, DD-Pak and TO-220 Packages
LT3020	100mA, Low Voltage VLDO	V_{IN}: 0.9V to 10V, $V_{OUT(MIN)}$ = 0.20V, V_{DO} = 0.15V, I_Q = 120µA, I_{SD} < 3µA; 3mm × 3mm DFN and MS8 Packages
LT3021	500mA, Low Voltage VLDO	V_{IN}: 0.9V to 10V, $V_{OUT(MIN)}$ = 0.20V, V_{DO} = 0.16V, I_Q = 120µA, I_{SD} < 3µA; 5mm × 5mm DFN and SO8 Packages
LT3023	Dual 100mA, Low Noise, Micropower LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.30V, I_Q = 40µA, I_{SD} < 1µA; DFN and MS10E Packages
LT3024	Dual 100mA/500mA, Low Noise, Micropower LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.30V, I_Q = 60µA, I_{SD} < 1µA; DFN and TSSOP-16E Packages
LTC3025	300mA, Low Voltage Micropower VLDO	V_{IN}: 0.9V to 5.5V, Low I_Q: 54µA, Low Noise < 80µV_{RMS}, 45mV Dropout Voltage; 2mm × 2mm 6-Lead DFN Package
LTC3026	1.5A, Low Input Voltage VLDO	V_{IN}: 1.14V to 5.5V, Low I_Q: 950µA, Low Noise < 110µV_{RMS}, 100mV Dropout Voltage; 10-Lead 3mm × 3mm DFN and MS10E Packages
LT3027	Dual 100mA, Low Noise, Micropower LDO with Independent Inputs	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.30V, I_Q = 50µA, I_{SD} < 1µA; DFN and MS10E Packages
LT3028	Dual 100mA/500mA, Low Noise, Micropower LDO with Independent Inputs	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.32V, I_Q = 60µA, I_{SD} < 1µA; DFN and TSSOP-16E Packages
LT3080/ LT3080-1	1.1A, Parallelable, Low Noise LDO	V_{IN}: 1.2V to 36V, V_{OUT}: 0V to 35.7V, Low Noise < 40µV_{RMS}, 300mV Dropout Voltage (2-Supply Operation), Current-Based Reference with 1-Resistor V_{OUT} Set, Directly Parallelable (No Op Amp Required), Stable with Ceramic Capacitors; TO-220, SOT-223, MS8E and 3mm × 3mm DFN Packages

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LT 0110 • PRINTED IN USA