National Semiconductor

ADVANCE INFORMATION
January 2005

LM2652
1.5A, Dual High Performance Synchronous Buck Regulator

General Description

The LM2652 is a monolithic dual synchronous buck regulator designed for low output voltages. Special attention to power sequencing, voltage accuracy and start-up characteristics has been made to enable a simple solution to the challenging requirements of FPGA & DSP power. Four integrated FET power switches ensure high efficiency, minimal external components and maximum ease-of-use. The IC can accept an input of 2.7V to 5.5V and deliver 1.5A per channel. The bias and power inputs can run from different rails to balance system power. Output voltages are factory programmable from 0.8V to 3.3V in 50mV steps. The LM2652 is available in two switching frequency options (650kHz and 1300kHz) and both options can be synchronized to an external clock of 300-1600kHz. The two switching channels run 180˚ out of phase to reduce input capacitor size and cost. Output fault protection is provided by the use of cycle-by-cycle current limit and frequency fold-back. Separate soft-start, power good flags and output enables allow for power sequencing flexibility.

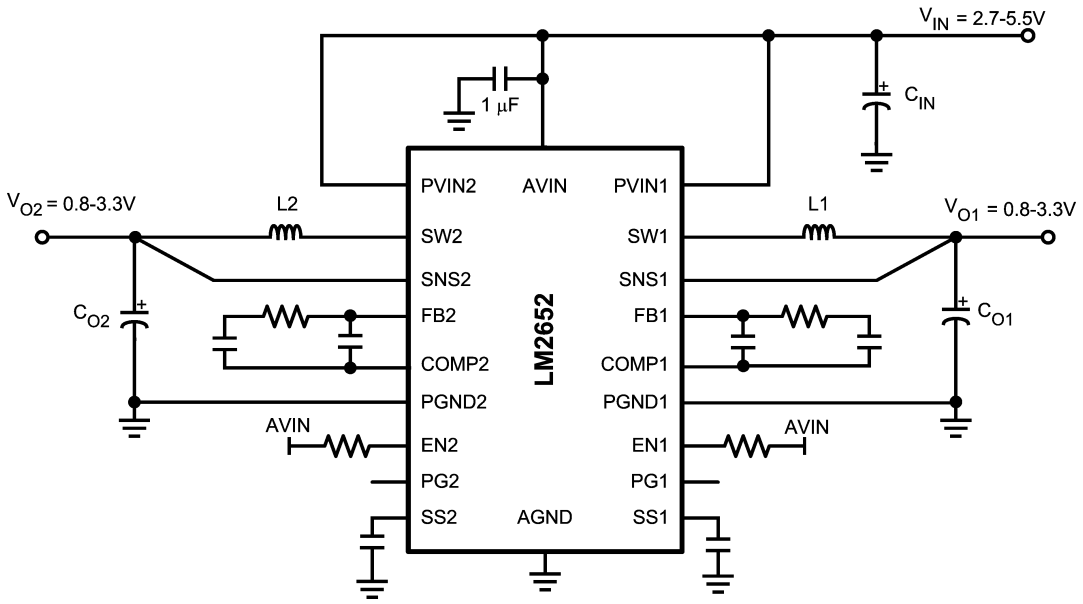
Features

- Dual 1.5 Amp outputs
- Output voltage factory set in 50mV steps from 0.8V to 3.3V
- Input voltage from 2.7V to 5.5V
- 2% reference accuracy
- 4 internal 80mΩ synchronous switches
- 180˚ out of phase operation
- Independent enables (CMOS compatible)
- Separate Power Good flags
- 650kHz or 1300kHz switching frequency
- PLL synchronization to an external clock
- Programmable soft-start
- Supports all-ceramic output capacitors
- TSSOP-28 Exposed Pad package
- Current limit and thermal shutdown protection

Applications

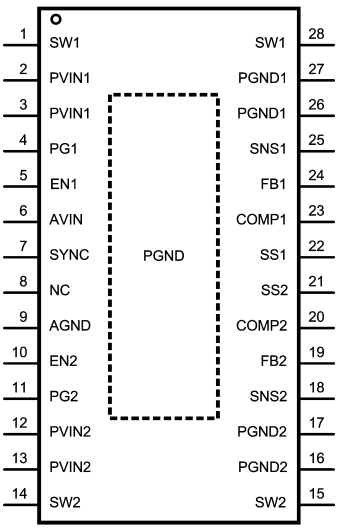
- Cable Modems
- xDSL Modems
- DSP, FPGA and microprocessor power
- Local Regulation
- Set-Top Box

Typical Application



Connection Diagram

TOP VIEW



20117202

28-Lead Plastic (TSSOP Exposed Pad)
See NS Package Number MXA28A

Pin Descriptions

SW1 (Pins 1, 28): The switch node pins for Channel 1. Connect the Channel 1 output inductor to these pins.

PVIN1 (Pins 2, 3): Input voltage supply for the Channel 1 switch. In a split-rail system, this supply should not exceed the voltage at the AVIN pin.

PG1 (Pin 4): Open drain Power Good flag for Channel 1. When this pin voltage is high, the output voltage is ready to deliver power to the load. Connect to AVIN through a 10kΩ pull-up resistor.

EN1 (Pin 5): Channel 1 logic enable. Input to a CMOS Schmitt trigger. Set this input high for normal operation. When low, Channel 1 is in shutdown mode. Connect to ground through a 100kΩ pull-down resistor.

AVIN (Pin 6): Power supply for the system. Bypass this pin with a small (0-10Ω, 1 µF) filter if it is connected to the same rail as PVIN.

SYNC (Pin 7): PWM frequency adjust. Connect a PWM clock to this pin. If unused, connect this pin to ground.

NC (Pin 8): No internal connection. This pin should be connected to ground.

AGND (Pin 9): Ground pin for the signal level circuitry. Must be connected to the system ground.

EN2 (Pin 10): Channel 2 logic enable. Input to a CMOS Schmitt trigger. Set this input high for normal operation. When low, Channel 2 is in shutdown mode. Connect to ground through a 100kΩ pull-down resistor

PG2 (Pin 11): Open drain Power Good flag for Channel 2. When this pin level is high, the Output voltage is ready to deliver power to the load. Connect to AVIN through a 10kΩ pull-up resistor.

PVIN2 (Pin 12,13): Input voltage supply for the Channel 2 switch. In a split-rail system, this supply should not exceed the voltage at the AVIN pin.

SW2 (Pin 14, 15): The switch node pins for Channel 2. Connect the Channel 2 output inductor to these pins.

PGND2 (Pin 26, 27): Ground pins for the high current circuitry. Must be connected to the system ground.

SNS2 (Pin 18): The output voltage (V_O) sense pin for Channel 2. Connect this pin directly to the load.

FB2 (Pin 19): The input to the error amplifier of Channel 2.

COMP2 (Pin 20): The output of the Channel 2 error amplifier.

SS2 (Pin 21): Soft start pin for Channel 2. Connect a small capacitor to this pin to control the slew rate of V_{O2} during start-up.

SS1 (Pin 22): Soft start pin for Channel 1. Connect a small capacitor to this pin to control the slew rate of V_{O1} during start-up.

COMP1 (Pin 23): The output of the Channel 1 error amplifier.

FB1 (Pin 24): The input to the error amplifier of Channel 1.

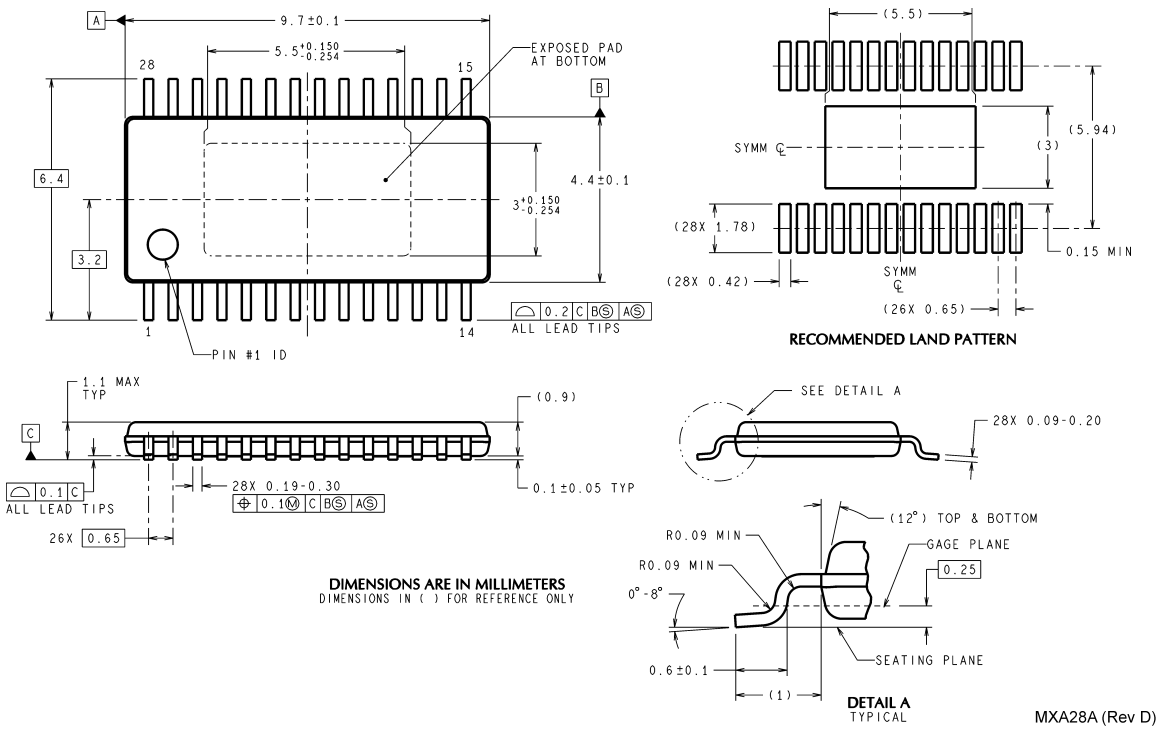
SNS1 (Pin 25): The output voltage (V_O) sense pin for Channel 1. Connect this pin directly to the load.

PGND2 (Pins 16, 17): Ground pins for the high current circuitry. Must be connected to the system ground.

EXPOSED PAD: Connect to power ground.

Physical Dimensions inches (millimeters)

unless otherwise noted



MXA28A (Rev D)

28-Lead Plastic (TSSOP Exposed Pad)
Order Number LM2652MTC
NS Package Number MXA28A

National Semiconductor
Americas Customer
Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

www.national.com

National Semiconductor
Europe Customer Support Center
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor
Asia Pacific Customer
Support Center
Email: ap.support@nsc.com

National Semiconductor
Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560