High-Accuracy Ultralow I_Q, 1.5 A, anyCAP® Low Dropout Regulator

ADP3339

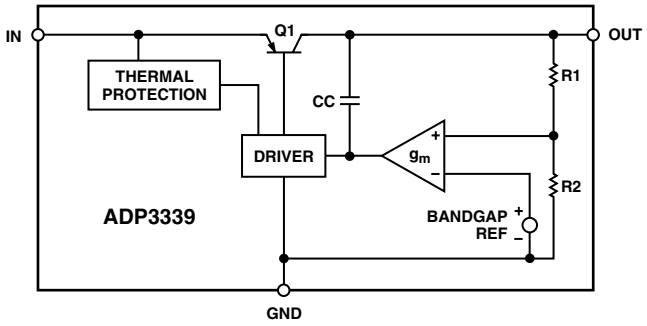
FEATURES

High Accuracy Over Line and Load: ±0.9% @ 25°C, ±1.5% Over Temperature
Ultralow Dropout Voltage: 230 mV (Typ) @ 1.5 A
Requires Only C_O = 1.0 μF for Stability
anyCAP = Stable with Any Type of Capacitor (Including MLCC)
Current and Thermal Limiting
Low Noise
2.8 V to 6 V Supply Range
–40°C to +85°C Ambient Temperature Range
SOT-223 Package

APPLICATIONS

Notebook, Palmtop Computers
SCSI Terminators
Battery-Powered Systems
PCMCIA Regulator
Bar Code Scanners
Camcorders, Cameras

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADP3339 is a member of the ADP33xx family of precision low dropout anyCAP voltage regulators. The ADP3339 operates with an input voltage range of 2.8 V to 6 V and delivers a load current up to 1.5 A. The ADP3339 stands out from the conventional LDOs with a novel architecture and an enhanced process that enables it to offer performance advantages and higher output current than its competition. Its patented design requires only a 1.0 μF output capacitor for stability. This device is insensitive to output capacitor Equivalent Series Resistance (ESR), and is stable with any good quality capacitor, including ceramic (MLCC) types for space-restricted applications. The ADP3339 achieves exceptional accuracy of ±0.9% at room temperature and ±1.5% over temperature, line and load variations. The dropout voltage of the ADP3339 is only 230 mV (typical) at 1.5 A. This device also includes a safety current limit and thermal overload protection. The ADP3339 has ultralow quiescent current 130 μA (typical) in light load situations.

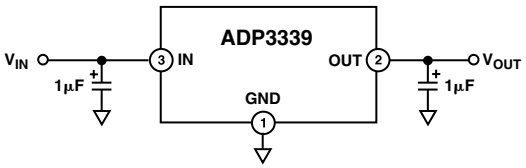


Figure 1. Typical Application Circuit

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REV. 0

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ADP3339–SPECIFICATIONS[1, 2] (V_{IN} = 6.0 V, C_{IN} = C_{OUT} = 1 µF, T_J = –40°C to +125°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT						
Voltage Accuracy[3]	V_{OUT}	V_{IN} = V_{OUTNOM} + 0.5 V to 6 V I_L = 0.1 mA to 1.5 A T_J = 25°C	–0.9		+0.9	%
		V_{IN} = V_{OUTNOM} + 0.5 V to 6 V I_L = 0.1 mA to 1.5 A T_J = –40°C to +125°C	–1.5		+1.5	%
		V_{IN} = V_{OUTNOM} + 0.5 V to 6 V I_L = 100 mA to 1.5 A T_J = 150°C	–1.9		+1.9	%
Line Regulation[3]		V_{IN} = V_{OUTNOM} + 0.5 V to 6 V T_J = 25°C		0.04		mV/V
Load Regulation		I_L = 0.1 mA to 1.5 A T_J = 25°C		0.04		mV/mA
Dropout Voltage	V_{DROP}	V_{OUT} = 98% of V_{OUTNOM}				
		I_L = 1.5 A		230	480	mV
		I_L = 1 A		180	380	mV
		I_L = 500 mA		150	300	mV
		I_L = 100 mA		100		mV
Peak Load Current	I_{LDPK}	V_{IN} = V_{OUTNOM} + 1 V		2.0		A
Output Noise	V_{NOISE}	f = 10 Hz–100 kHz, C_L = 10 µF I_L = 1.5 A		95		µV rms
GROUND CURRENT						
In Regulation	I_{GND}	I_L = 1.5 A		13	40	mA
		I_L = 1 A		9	25	mA
		I_L = 500 mA		5	15	mA
		I_L = 100 mA		1	3	mA
		I_L = 0.1 mA		130	200	µA
In Dropout	I_{GND}	V_{IN} = V_{OUTNOM} – 100 mV I_L = 0.1 mA		100	300	µA

NOTES

[1]All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.

[2]Application stable with no load.

[3]V_{IN} = 2.8 V for models with V_{OUTNOM} ≤ 2.3 V.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

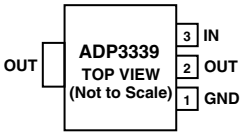
Input Supply Voltage . . . . . –0.3 V to +8.5 V
Power Dissipation . . . . . Internally Limited
Operating Ambient Temperature Range . . . . –40°C to +85°C
Operating Junction Temperature Range . . . –40°C to +150°C
θ_{JA} Four-Layer Board . . . . . 62.3°C/W
θ_{JC} . . . . . 26.8°C/W
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 10 sec) . . . . . 300°C
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C

*This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged. Unless otherwise specified, all voltages are referenced to GND.

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	GND	Ground Pin.
2	OUT	Output of the Regulator. Bypass to ground with a 1 µF or larger capacitor.
3	IN	Regulator Input. Bypass to ground with a 1 µF or larger capacitor.

PIN CONFIGURATION



NOTE
PIN 2 AND TAB ARE
INTERNALLY CONNECTED

ORDERING GUIDE

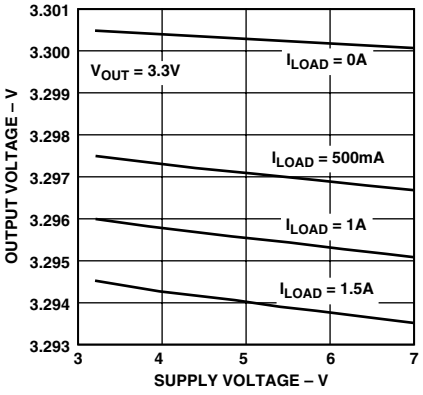
Model	Output Voltage*	Package Option	Package Description
ADP3339AKC-1.8	1.8 V	KC (SOT-223)	Plastic Surface Mount
ADP3339AKC-2.5	2.5 V	KC (SOT-223)	Plastic Surface Mount
ADP3339AKC-2.85	2.85 V	KC (SOT-223)	Plastic Surface Mount
ADP3339AKC-3.3	3.3 V	KC (SOT-223)	Plastic Surface Mount
ADP3339AKC-5	5 V	KC (SOT-223)	Plastic Surface Mount

*Contact the factory for other voltage options.

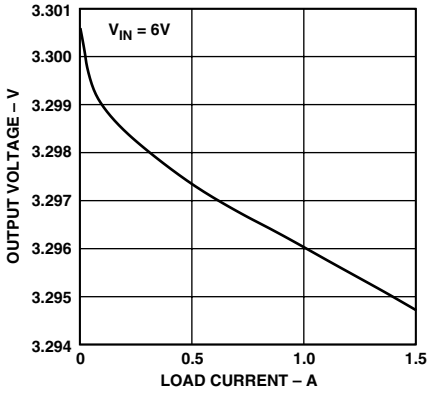
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3339 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

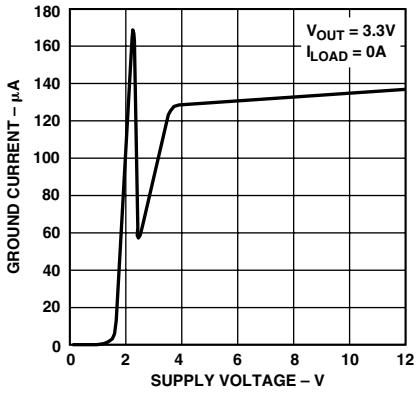
ADP3339–Typical Performance Characteristics (T_A = 25°C unless otherwise noted.)



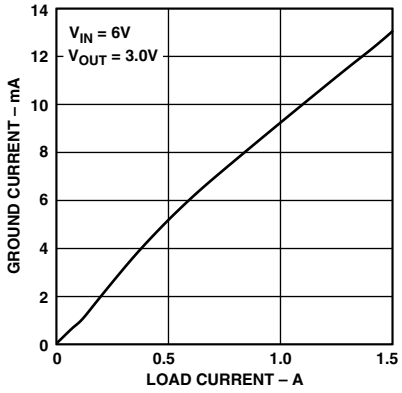
TPC 1. Output Voltage vs. Supply Voltage



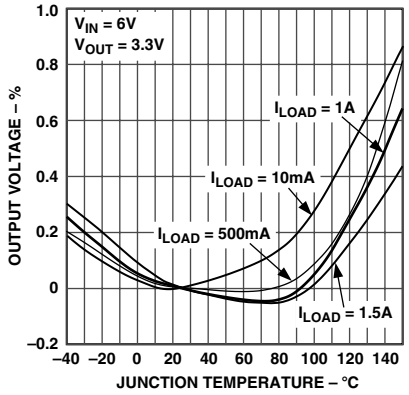
TPC 2. Output Voltage vs. Load Current



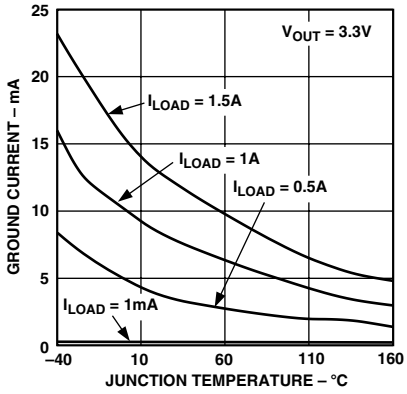
TPC 3. Ground Current vs. Supply Voltage



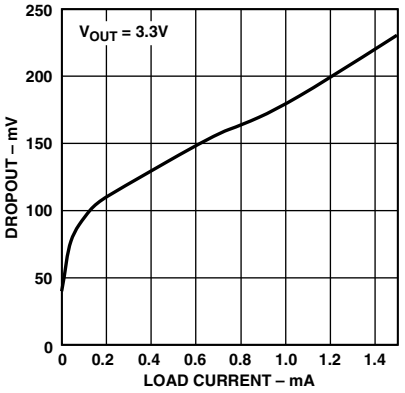
TPC 4. Ground Current vs. Load Current



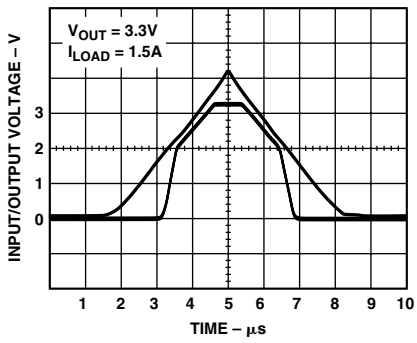
TPC 5. Output Voltage Variation % vs. Junction Temperature



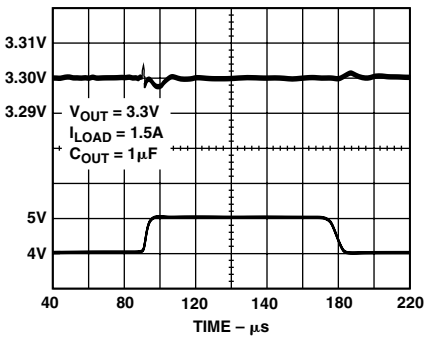
TPC 6. Ground Current vs. Junction Temperature



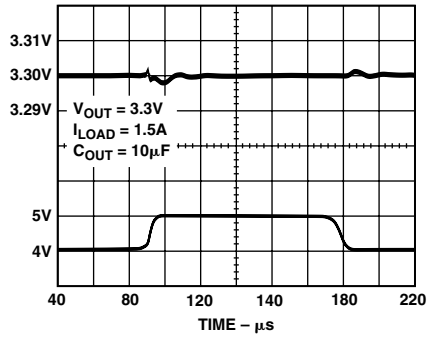
TPC 7. Dropout Voltage vs. Load Current



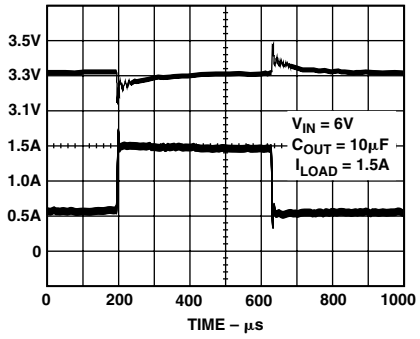
TPC 8. Power-Up/Power-Down



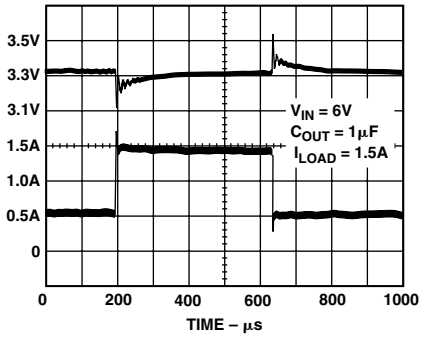
TPC 9. Line Transient Response



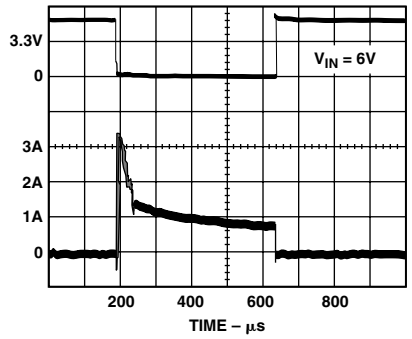
TPC 10. Line Transient Response



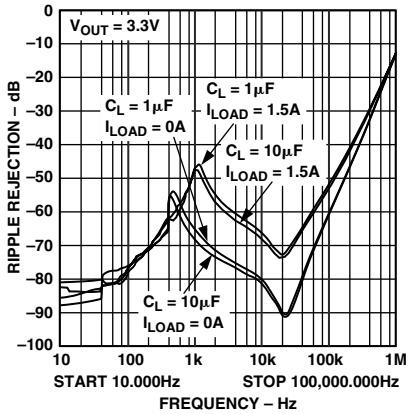
TPC 11. Load Transient Response



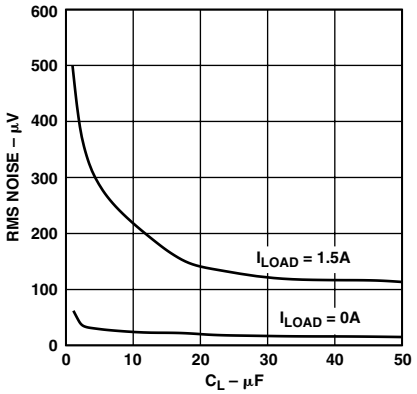
TPC 12. Load Transient Response



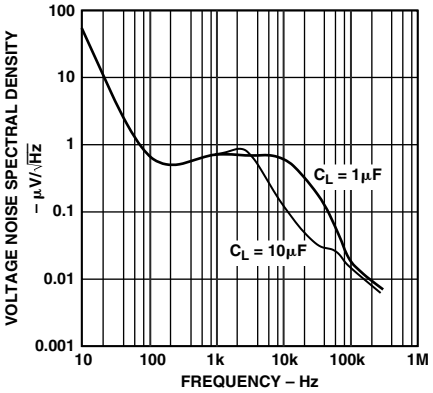
TPC 13. Short-Circuit Current



TPC 14. Power Supply Ripple Rejection



TPC 15. RMS Noise vs. C_L (10 Hz–100 kHz)



TPC 16. Output Noise Density

THEORY OF OPERATION

The new anyCAP LDO ADP3339 uses a single control loop for regulation and reference functions. The output voltage is sensed by a resistive voltage divider consisting of R1 and R2 which is varied to provide the available output voltage option. Feedback is taken from this network by way of a series diode (D1) and a second resistor divider (R3 and R4) to the input of an amplifier.

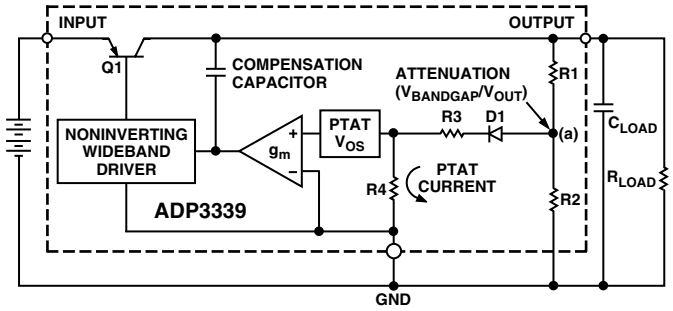


Figure 2. Functional Block Diagram

A very high-gain error amplifier is used to control this loop. The amplifier is constructed in such a way that equilibrium produces a large, temperature-proportional input, "offset voltage" that is repeatable and very well controlled. The temperature-proportional offset voltage is combined with the complementary diode voltage to form a "virtual bandgap" voltage, implicit in the network, although it never appears explicitly in the circuit. Ultimately, this patented design makes it possible to control the loop with only one amplifier. This technique also improves the noise characteristics of the amplifier by providing more flexibility on the trade-off of noise sources that leads to a low noise design.

The R1, R2 divider is chosen in the same ratio as the bandgap voltage to the output voltage. Although the R1, R2 resistor divider is loaded by the diode D1 and a second divider consisting of R3 and R4, the values can be chosen to produce a temperature-stable output. This unique arrangement specifically corrects for the loading of the divider, thus avoiding the error resulting from base current loading in conventional circuits.

The patented amplifier controls a new and unique noninverting driver that drives the pass transistor, Q1. The use of this special noninverting driver enables the frequency compensation to include the load capacitor in a pole-splitting arrangement to achieve reduced sensitivity to the value, type, and ESR of the load capacitance.

Most LDOs place very strict requirements on the range of ESR values for the output capacitor because they are difficult to stabilize due to the uncertainty of load capacitance and resistance. Moreover, the ESR value, required to keep conventional LDOs stable, changes depending on load and temperature. These ESR limitations make designing with LDOs more difficult because of their unclear specifications and extreme variations over temperature.

With the ADP3339 anyCAP LDO, this is no longer true. It can be used with virtually any good quality capacitor, with no constraint on the minimum ESR. This innovative design allows the circuit to be stable with just a small 1 μF capacitor on the output. Additional advantages of the pole-splitting scheme include superior line noise rejection and very high regulator gain, which leads to excellent line and load regulation. An impressive ±1.5 accuracy is guaranteed over line, load, and temperature.

Additional features of the circuit include current limit and thermal shutdown.

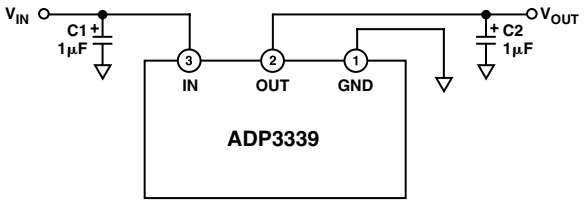


Figure 3. Typical Application Circuit

APPLICATION INFORMATION

CAPACITOR SELECTION

Output Capacitor

The stability and transient response of the LDO is a function of the output capacitor. The ADP3339 is stable with a wide range of capacitor values, types, and ESR (anyCAP). A capacitor as low as 1 μF is all that is needed for stability. A higher capacitance may be necessary if high output current surges are anticipated or if the output capacitor cannot be located near the output and ground pins. The ADP3339 is stable with extremely low ESR capacitors (ESR ≈ 0), such as Multilayer Ceramic Capacitors (MLCC) or OSCON. Note that the effective capacitance of some capacitor types fall below the minimum over temperature or with dc voltage.

Input Capacitor

An input bypass capacitor is not strictly required but it is recommended in any application involving long input wires or high source impedance. Connecting a 1 μF capacitor from the input to ground reduces the circuit's sensitivity to PC board layout and input transients. If a larger output capacitor is necessary, then a larger value input capacitor is also recommended.

OUTPUT CURRENT LIMIT

The ADP3339 is short-circuit protected by limiting the pass transistor's base drive current. The maximum output current is limited to about 3 A, see TPC 13.

THERMAL OVERLOAD PROTECTION

The ADP3339 is protected against damage due to excessive power dissipation by its thermal overload protection circuit. Thermal protection limits the die temperature to a maximum of 160°C. Under extreme conditions (i.e., high ambient temperature and power dissipation) where the die temperature starts to rise above 160°C, the output current will be reduced until the die temperature has dropped to a safe level.

Current and thermal limit protections are intended to protect the device against accidental overload conditions. For normal operation, the device's power dissipation should be externally limited so that the junction temperature will not exceed 125°C.

CALCULATING POWER DISSIPATION

Device power dissipation is calculated as follows:

$$P_D = (V_{IN} - V_{OUT}) \times I_{LOAD} + (V_{IN}) \times I_{GND}$$

Where I_{LOAD} and I_{GND} are load current and ground current, V_{IN} and V_{OUT} are the input and output voltages respectively.

Assuming worst-case operating conditions are I_{LOAD} = 1.5 A, I_{GND} = 14 mA, V_{IN} = 3.3 V, and V_{OUT} = 2.5 V, the device power dissipation is:

$$P_D = (3.3\,V - 2.5\,V)1500\,mA + (3.3\,V)14\,mA = 1246\,mW$$

So, for a maximum junction temperature of 125°C and a maximum ambient temperature of 85°C, the required thermal resistance from junction to ambient is:

$$\theta_{JA} = \frac{125°C - 85°C}{1.246\,W} = 32.1°C/W$$

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

The SOT-223's thermal resistance, θ_{JA}, is determined by the sum of the junction-to-case and the case-to-ambient thermal resistances. The junction-to-case thermal resistance, θ_{JC}, is determined by the package design and specified at 26.8°C/W. However, the case-to-ambient thermal resistance is determined by the printed circuit board design.

As shown in Figures 4a–4c, the amount of copper to which the ADP3339 is mounted affects the thermal performance. When mounted to just the minimal pads of 2 oz. copper (Figure 4a), the θ_{JA} is 126.6°C/W. By adding a small copper pad under the ADP3339 (Figure 4b), reduces the θ_{JA} to 102.9°C/W. Increasing the copper pad to 1 square inch (Figure 4c), reduces the θ_{JA} even further to 52.8°C/W.

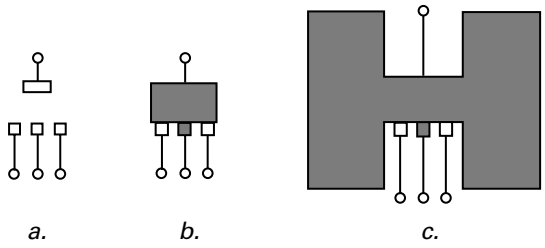


Figure 4. PCB Layouts

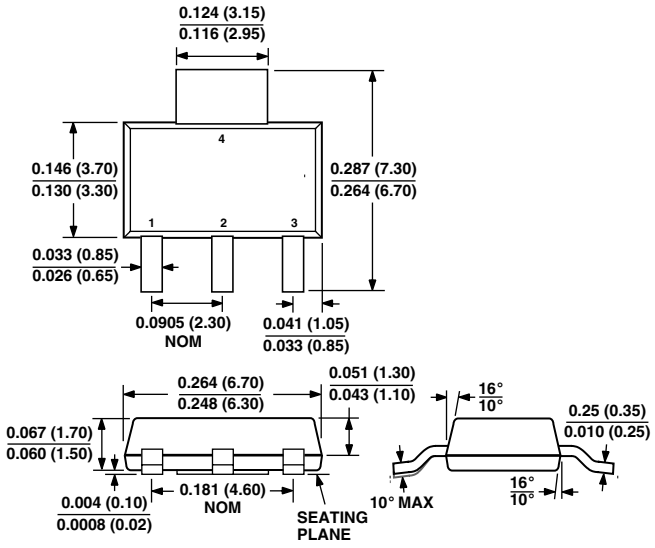
Use the following general guidelines when designing printed circuit boards:

1. Keep the output capacitor as close to the output and ground pins as possible.
2. Keep the input capacitor as close to the input and ground pins as possible.
3. PC board traces with larger cross sectional areas will remove more heat from the ADP3339. For optimum heat transfer, specify thick copper and use wide traces.
4. The thermal resistance can be decreased by adding a copper pad under the ADP3339 as shown in Figure 4b.
5. If possible, utilize the adjacent area to add more copper around the ADP3339. Connecting the copper area to the output of the ADP3339, as shown in Figure 4c, is best but will improve thermal performance even if it is connected to other pins.
6. Use additional copper layers or planes to reduce the thermal resistance. Again, connecting the other layers to the output of the ADP3339 is best, but not necessary. When connecting the output pad to other layers use multiple vias.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

3-Lead Surface Mount
KC (SOT-223)



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