Precision Voltage Regulator Controller

ADP3310

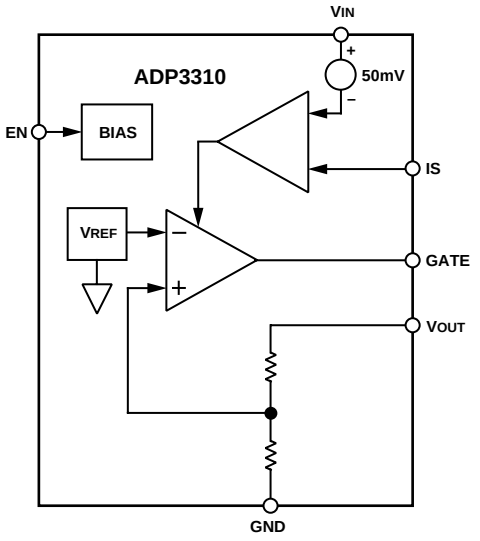
FEATURES

±1.5% Accuracy Over Line, Load and Temperature
Low 800 μA (Typical) Quiescent Current
Shutdown Current: 1 μA (Typical)
Stable with 10 μF Load Capacitor
+2.5 V to +15 V Operating Range
Fixed Output Voltage Options: 2.8 V, 3 V, 3.3 V, 5 V
Up to 10 A Output Current
SO-8 Package
–40°C to +85°C Ambient Temperature Range
Internal Gate to Source Protective Clamp
Current and Thermal Limiting
Programmable Current Limit
Foldback Current Limit

APPLICATIONS

Desktop Computers
Handheld Instruments
Cellular Telephones
Battery Operated Devices
Solar Powered Instruments
High Efficiency Linear Power Supplies
Battery Chargers

FUNCTIONAL BLOCK DIAGRAM



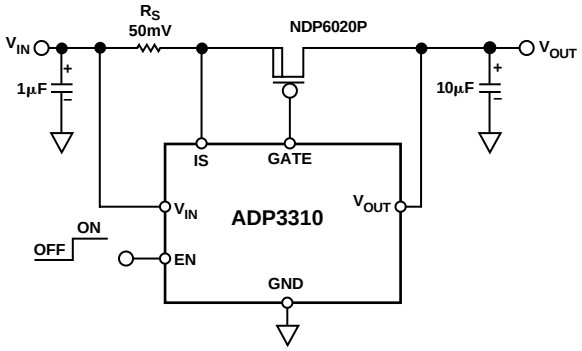


Figure 1. Typical Application Circuit

GENERAL DESCRIPTION

The ADP3310 is a precision voltage regulator controller that can be used with an external Power PMOS device such as the NDP6020P to form a two chip low dropout linear regulator. The low quiescent current (800 μA) and the Enable feature make this device especially suitable for battery powered systems. The dropout voltage at 1 A is only 70 mV when used with the NDP6020P, allowing operation with minimal headroom and prolonging battery useful life. The ADP3310 can drive a wide range of currents, depending on the external PMOS device used.

Additional features of this device include: high accuracy (±1.5%) over line, load and temperature, gate-to-source voltage clamp to protect the external MOSFET and foldback current limit. A current limit threshold voltage of 50 mV (typ) allows 50 mΩ of board metal trace resistance to provide a 1 A current limit.

The ADP3310 operates from a wide input voltage range from 2.5 V to 15 V and is available in a small SO-8 package.

REV. A

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ADP3310–SPECIFICATIONS ($V_{IN} = V_{OUT} + 1$ V, $T_A = -40°C$ to $+85°C$ unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Units
OUTPUT VOLTAGE ACCURACY (Figure 1)	$V_{IN} = V_{OUT}$ +1 V to 15 V V_{EN} = 2 V, I_{OUT} = 10 mA to 1 A	V_{OUT}	–1.5		+1.5	%
QUIESCENT CURRENT						
Shutdown Mode	V_{EN} = 0 V	I_{GND}		1	10	µA
Normal Mode	V_{EN} = 2 V, I_{OUT} = 500 µA	I_{GND}		800	1000	µA
GATE TO SOURCE CLAMP VOLTAGE	V_{OUT} = 0 V, V_{IN} = 15 V			8	10	V
GATE DRIVE MINIMUM VOLTAGE				0.7		V
GATE DRIVE CURRENT (SINK/SOURCE)			1			mA
GAIN $\left(\frac{\Delta V_{GS}}{\Delta V_{OUT}}\right)$				80		dB
CURRENT LIMIT THRESHOLD VOLTAGE	$V_{IN} - V_{IS}$		40	50	80	mV
LOAD REGULATION	I_{OUT} = 10 mA to 1 A		–10		10	mV
LINE REGULATION	$V_{IN} = V_{OUT}$ +1 V to 15 V I_{OUT} = 100 mA		–10		10	mV
SHUTDOWN INPUT VOLTAGE	V_{IH}	V_{EN}	2.0			V
	V_{IL}				0.4	V
SHUTDOWN INPUT CURRENT	V_{EN} = 0 V to 5.0 V	I_{EN}	–10		+10	µA

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Input Voltage, V_{IN} . . . . . +20 V
Enable Input Voltage . . . . . 0.3 V to V_{IN} + 0.3 V
Operating Junction Temperature Range . . . –40°C to +125°C
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C
θ_{JA} (4-Layer Board) . . . . . +121°C/W
θ_{JA} (2-Layer Board . . . . . +150°C/W

*This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged.

CAUTION

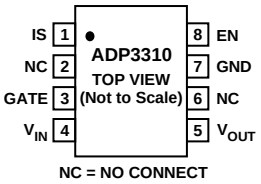
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3310 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model	Output Voltage	Package Option*
ADP3310AR-2.8	2.8 V	SO-8
ADP3310AR-3	3 V	SO-8
ADP3310AR-3.3	3.3 V	SO-8
ADP3310AR-5	5 V	SO-8

*SO = Small Outline. Contact the factory for the availability of other output voltage options from 5 V to 16.5 V.
Refer to the ADP3319 data sheet for 1.8 V and 2.5 V output voltage options.
Refer to the ADP3328 data sheet for adjustable output version.

PIN CONFIGURATION
SO-8



NC = NO CONNECT

PIN FUNCTION DESCRIPTIONS

Pin SO-8	Name	Function
1	IS	Current Sense. Connected to the more negative terminal of the sense resistor as well as the Power MOSFET's source pin. IS must be tied to V_{IN} pin if the current limit feature is not used.
2, 6	NC	No Connect.
3	GATE	Gate Drive for the external MOSFET.
4	V_{IN}	Input Voltage. This is also the positive terminal connection of the current sense resistor.
5	V_{OUT}	Output Voltage Sense. This pin is connected to the MOSFET's drain and directly to the load for optimal load regulation. Bypass to ground with a 10 µF or larger capacitor.
7	GND	Device Ground. This pin should be tied to system ground closest to the load.
8	EN	Enable. Pulling this pin to a logic High or tying the pin to the input voltage will enable the output. Pulling this pin low will disable the regulator output.

Table I. Alternate PMOS Devices

PMOS	NDP6020P	IRF7404	Si9434DY
Manufacturer	Fairchild	IR	Temic
$R_{DS(ON)}$	0.075 Ω @ V_{GS} = –2.5 V	0.06 Ω @ V_{GS} = –2.7 V	0.06 Ω @ V_{GS} = –2.5 V
I_D Continuous @ 25°C	–27 A @ V_{GS} = –4.5 V	–5.3 A @ V_{GS} = –4.5 V	–6.4 A
P_D @ 25°C	75 W	1.6 W	2.5 W
Derating Factor	0.5 W/°C	0.011 W/°C	1.6 W @ 70°C
Package	TO-220	SO-8	SO-8

ADP3310–Typical Performance Characteristics (Circuit of Figure 1)

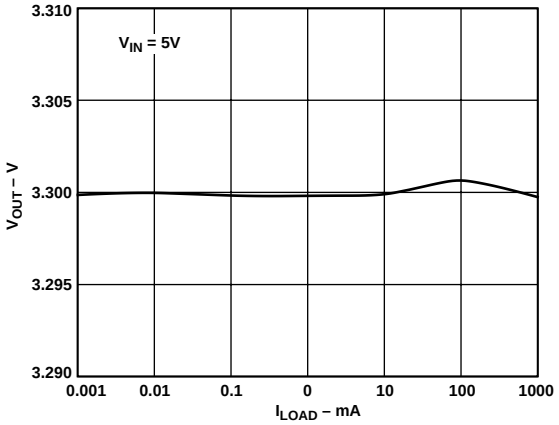


Figure 2. V_{OUT} vs. I_{LOAD} (V_{IN} = 5 V)

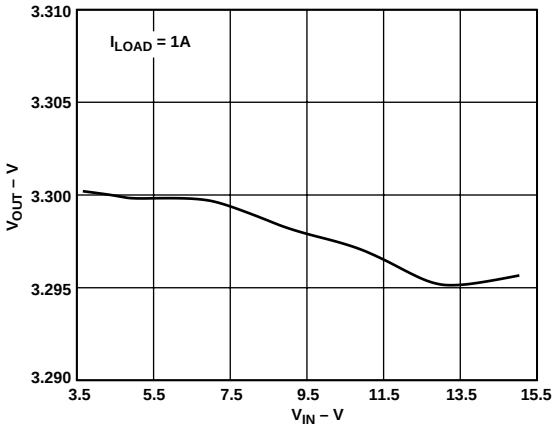


Figure 3. V_{OUT} vs. V_{IN} (I_{LOAD} = 1 A)

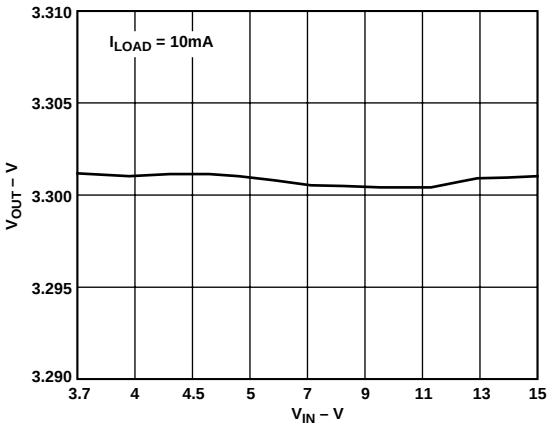


Figure 4. V_{OUT} vs. V_{IN} (I_{LOAD} = 10 mA)

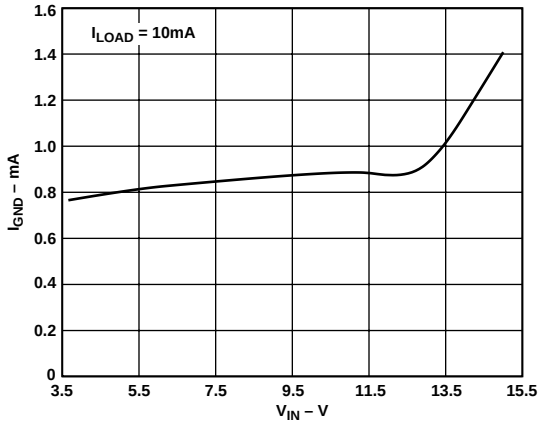


Figure 5. I_{GND} vs. V_{IN} (I_{LOAD} = 10 mA)

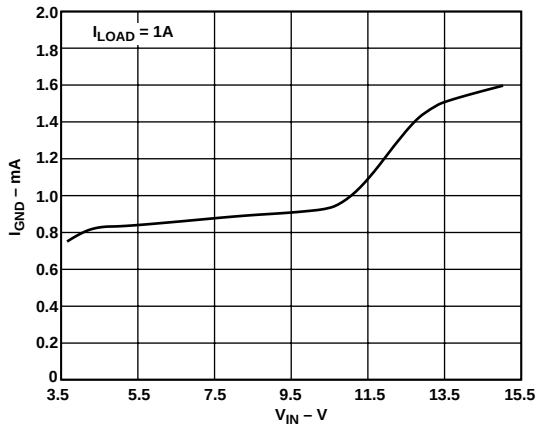


Figure 6. I_{GND} vs. V_{IN} (I_{LOAD} = 1 A)

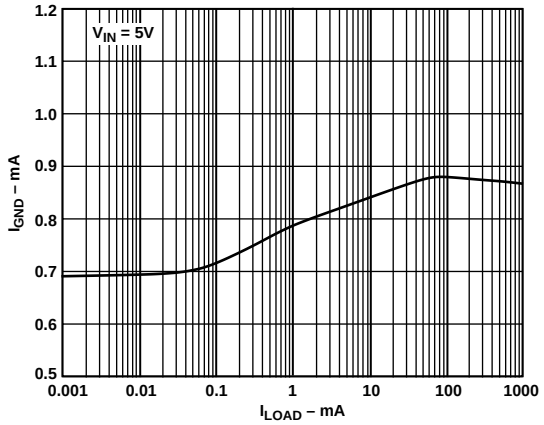


Figure 7. I_{GND} vs. I_{LOAD} (V_{IN} = 5 V)

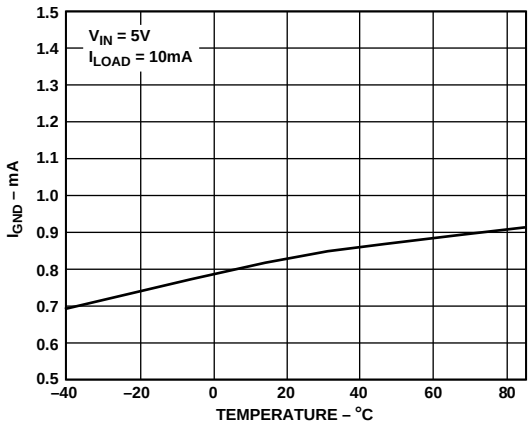


Figure 8. Quiescent Current vs. Temperature

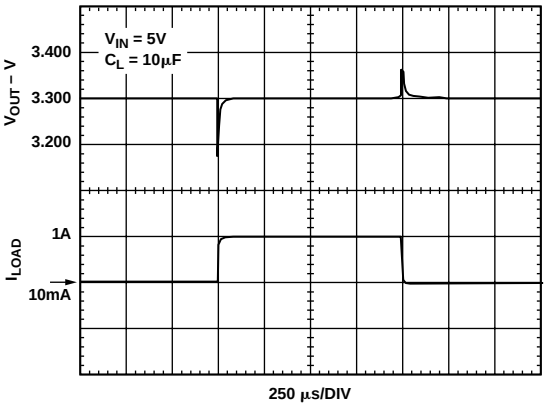


Figure 11. Load Transient Response

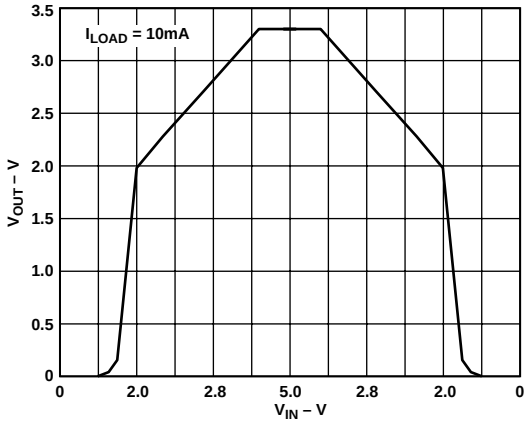


Figure 9. Power-Up/Power-Down

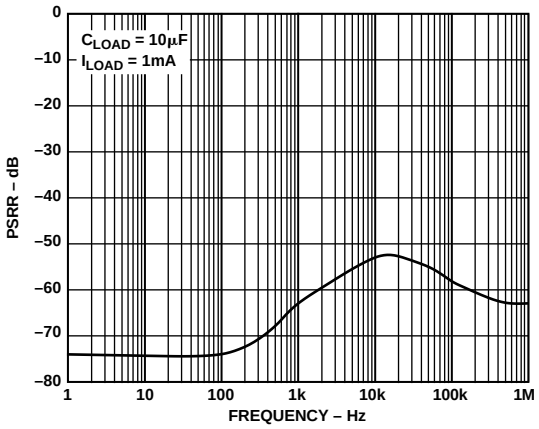


Figure 12. Ripple Rejection

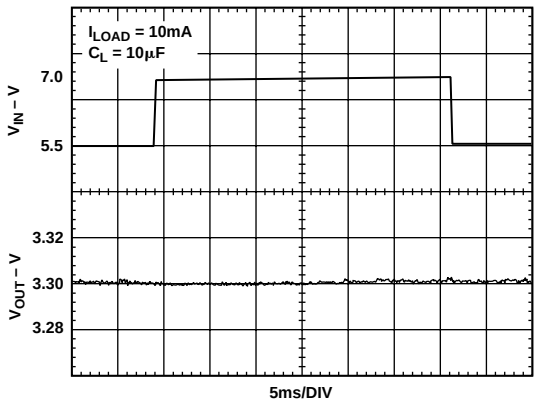


Figure 10. Line Transient Response—(10 µF Load)

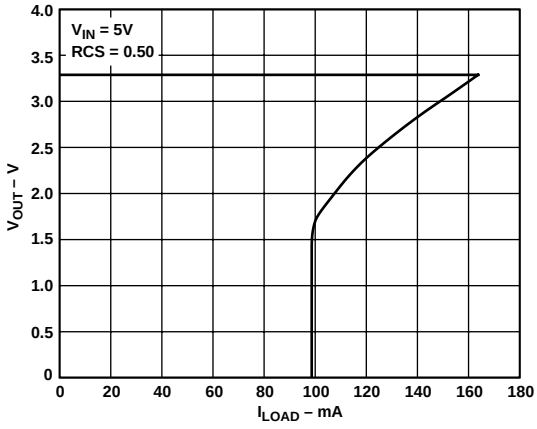


Figure 13. Foldback Current

APPLICATION INFORMATION

The ADP3310 is very easy to use. A P-channel power MOSFET and a small capacitor on the output is all that is needed to form an inexpensive ultralow dropout regulator. The advantage of using the ADP3310 controller is that it can drive a pass PMOS FET to provide a regulated output at high current.

FET Selection

The type and size of the pass transistor are determined by the threshold voltage, input-output voltage differential and load current. The selected PMOS must satisfy the physical and thermal design requirements. Table I shows a partial list of manufacturers providing the PMOS devices. To ensure that the maximum V_{GS} provided by the controller will turn on the FET at worst case conditions (i.e., temperature and manufacturing tolerances), the maximum available V_{GS} must be determined. Maximum V_{GS} is calculated as follows:

(1) $V_{GS} = V_{IN} - V_{BE} - I_{OMAX} \times R_S$
I_{OMAX} = Maximum Output Current
R_S = Current Sense Resistor
V_{BE} ~ 0.7 V (Room Temp)
~ 0.5 V (Hot)
~ 0.9 V (Cold)

For Example: V_{IN} = 5 V, V_O = 3.3 V and I_{OMAX} = 3 A,
V_{GS} = 5 V – 0.7 V – 3 A × 11 mΩ = 4.27 V

Equation (1) applies to a gate-to-source voltage less than the gate to source clamp voltage.

(2) $V_{DS} = V_{IN} - V_O$
V_{DS} = 5 V – 3.3 V = 1.7 V

If $V_{IN} \le 5$ V, logic level FET should be considered.
If $V_{IN} > 5$ V, either logic level or standard MOSFET can be used.

The difference between V_{IS} and V_{OUT} (V_{DS}) must exceed the voltage drop due to the load current and the ON resistance of the FET. As a safety margin, it is recommended to use a MOSFET with a V_{GS} at least 1.5 times lower than the calculated V_{GS} value from Equation 1. Also, in the event the circuit is shorted to ground, the MOSFET must be able to conduct the maximum short circuit current. The selected MOSFET must satisfy these criteria; otherwise, a different pass device should be used. If the FET data is not available in the catalogue, contact the FET manufacturer.

Thermal Design

The maximum allowable thermal resistance between the FET junction and the highest ambient temperature must be taken into account to determine the type of FET package used. One square inch of PCB copper area as heatsink yields a typical θ_{JA} ~ 60°C/W for the SOT-223 package and θ_{JA} ~ 50°C/W for the SO-8 package. For substantially lower thermal resistances, D^2PAK or TO-220 type of packages are recommended.

For normal applications, the FET can be directly mounted to the PCB. But, for higher power applications, an external heat sink is required to satisfy the θ_{JA} requirement and provide adequate heatsink.

Calculating thermal resistance for V_{IN} = 5 V, V_O = 3.3 V, and I_O = 3 A:

$$\theta_{JA} = \frac{T_J - T_{AMBMAX}}{(V_{DSMAX} \times I_{OMAX})}$$

T_J = Junction Temperature
T_{AMBMAX} = Maximum Ambient Temperature
V_{DSMAX} = Maximum Drain to Source Voltage
I_{OMAX} = Maximum Output Current

$$\theta_{JA} = \frac{125 - 50}{1.7 \times 3} = 14.7°C/W$$

For such a low θ_{JA}, a P-channel FET from Fairchild, such as NDP6020P in a heatsink mountable TO-220 package, is required. The required external heatsink is determined as follows:

$\theta_{CA} = \theta_{JA} - \theta_{JC}$
θ_{CA} = Case-to-Ambient Thermal Resistance
θ_{JA} = Junction-to-Ambient Thermal Resistance
θ_{JC} = Junction-to-Case Thermal Resistance
θ_{JC} = 2°C/W for NDP6020P
θ_{CA} = 14.7°C/W – 2°C/W = 12.7°C/W

For a safety margin, select a heatsink with a θ_{CA} less than half of the value calculated above to allow extended duration of short circuit. In a natural convection environment, a large heatsink such as 3" length of Type 63020 extrusion from Aavid Engineering is required.

External Capacitors

The ADP3310 is stable with virtually any good quality capacitors (anyCAP™), independent of the capacitor's minimum ESR (Effective Series Resistance) value. The actual value of the capacitor and its associated ESR depends on the g_m and capacitance of the external PMOS device. A 10 µF capacitor at the output is sufficient to ensure stability for up to 10 A output current. Larger capacitors can be used if high output current surges are anticipated. Extremely low ESR capacitors (ESR≈0) such as multilayer ceramic or OSCON are preferred because they offer lower ripple on the output. For less demanding requirements, a standard tantalum or even an aluminum electrolytic is adequate. However, if an aluminum electrolytic is used, be sure it meets the temperature requirements because aluminum electrolytic has poor performance over temperature.

Shutdown Mode

Applying a TTL high signal to the EN pin or tying it to the input pin will enable the output. Pulling this pin low or tying it to ground will disable the output. In shutdown mode, the controller's quiescent current is reduced to less than 1 µA.

Gate-to-Source Clamp

An 8 V gate-to-source voltage clamp is provided to protect the MOSFET in the event the output is suddenly shorted to ground. This allows the use of the new, low on-state resistance (R_{DSON}) FETs.

Short Circuit Protection

The power FET is protected during short circuit conditions with a foldback type of current limiting which significantly reduces the current.

Current Sense Resistor

Current limit is achieved by setting an appropriate current sense resistor (R_S) across the current limit threshold voltage. Current limit sense resistor R_S is calculated as follows:

$$R_S = \frac{0.05}{(1.5 \times I_O)}$$

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Current Limit Threshold Voltage = 0.05 V
Safety Factor = 1.5
I_O = Output Current

R_S is not needed in circuits that do not require current limiting. In that case, the I_S pin must be tied to the input pin.

The simplest and cheapest sense resistor for high current applications, (i.e., Figure 1) is a PCB trace. The temperature dependence of the copper trace and the thickness tolerances of the trace must be taken into account in the design. The resistivity of copper has a positive temperature coefficient of +0.39%/°C. Copper's Tempco in conjunction with the proportional-to-absolute temperature (PTAT) current limit voltage can provide an accurate current limit. Table II provides the resistance value for PCB copper traces. Alternately, an appropriate sense resistor such as surface mount sense resistors available from KRL can be used.

PCB-Layout Issues

For optimum voltage regulation, place the load as close as possible to the device's V_{OUT} and GND pins. It is recommended to use dedicated PCB traces to connect the MOSFET's drain to the positive terminal and GND to the negative terminal of the load to avoid voltage drops along the high current carrying PCB traces.

Application Circuits

Typical 3 A LDO Circuit

The ADP3310 and a power MOSFET can be used to power the new generation of CPUs and microprocessors from the standard +5 V supply at a very low cost (Figure 14). This circuit provides low dropout, fast switching and high switching load current from 0 A to 3 A. Due to the high switching load current, capacitors with high ripple current carrying capability, such as OSCON or special tantalum capacitors from Sprague (593D), are recommended for the output.

Table II. Printed Circuit Copper Resistance

Conductor Thickness	Conductor Width In	Resistance mΩ/In
1/2 oz/ft^2 (18 μm)	0.025	39.3
	0.050	19.7
	0.100	9.83
	0.200	4.91
	0.500	1.97
1 oz/ft^2 (35 μm)	0.025	19.7
	0.050	9.83
	0.100	4.91
	0.200	2.46
	0.500	0.98
2 oz/ft^2 (70 μm)	0.025	9.83
	0.050	4.91
	0.100	2.46
	0.200	1.23
	0.500	0.49
3 oz/ft^2 (106 μm)	0.025	6.5
	0.050	3.25
	0.100	1.63
	0.200	0.81
	0.500	0.325

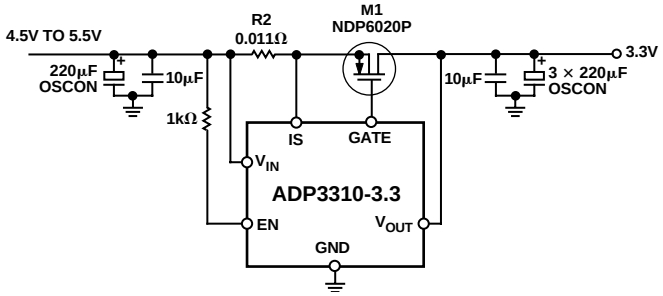


Figure 14. Typical 3 A Low Dropout Regulator Circuit

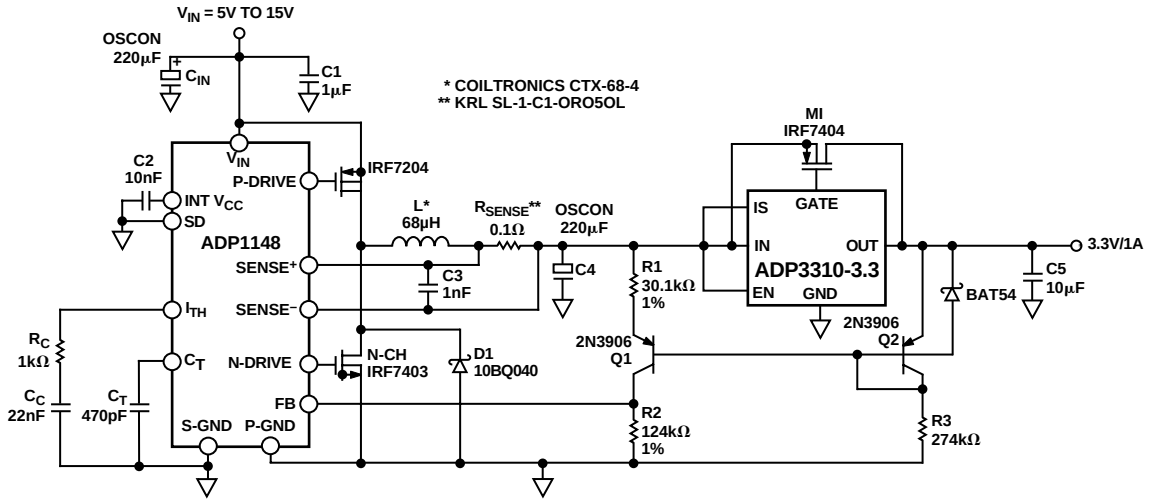


Figure 15. High Current Post Regulator with SOIC PMOS

High Current Post Regulator with SOIC PMOS

Post regulation for a switch-mode supply (Figure 15) can be implemented with a PMOS in an SO-8 package to provide a significant reduction in peak-to-peak ripple voltage. A constant dropout voltage in conjunction with low quiescent current yield a more efficient voltage regulator that can significantly extend battery life. The bottom waveform of Figure 16 is the output of the switching regulator. The top waveform is the output of the post regulator.

In applications where cost is a higher concern than efficiency, a resistor divider can be used to provide feedback instead of the current mirror. Power efficiency is lower in cases of light loads.

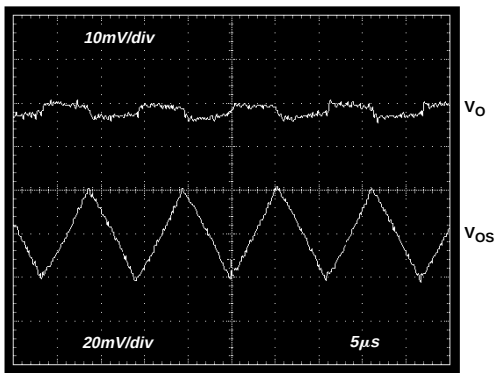
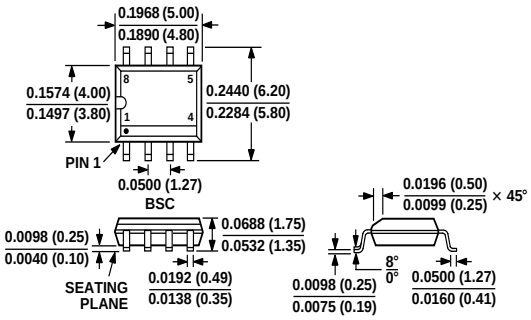


Figure 16. Pre-and Post-Regulated Voltage

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Small Outline (SO-8)



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