High Accuracy anyCAP®
50 mA Low Dropout Linear Regulator

ADP3300

FEATURES

High Accuracy (Over Line and Load Regulations at 25°C): ±0.8%
Ultralow Dropout Voltage: 80 mV Typical @ 50 mA
Requires Only C_O = 0.47 μF for Stability
anyCAP™ = Stable with All Types of Capacitors (Including MLCC)
Current and Thermal Limiting
Low Noise
Dropout Detector
Low Shutdown Current: 1 μA
3.0 V to 12 V Supply Range
–40°C to +85°C Ambient Temperature Range
Several Fixed Voltage Options
Ultrasmall SOT-23 6-Lead Package
Excellent Line and Load Regulations

APPLICATIONS

Cellular Telephones
Notebook, Palmtop Computers
Battery Powered Systems
PCMCIA Regulators
Bar Code Scanners
Camcorders, Cameras

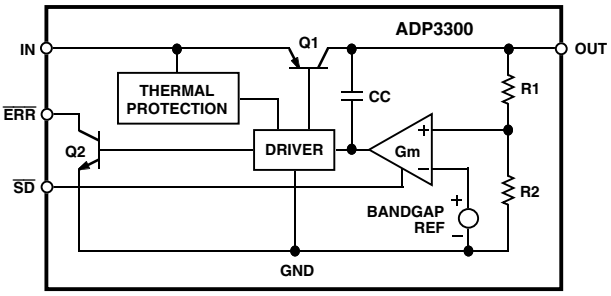
GENERAL DESCRIPTION

The ADP3300 is a member of the ADP330x family of precision low dropout anyCAP™ voltage regulators. The ADP3300 stands out from conventional LDOs with a novel architecture and an enhanced process. Its patented design requires only a 0.47 μF output capacitor for stability. This device is stable with any capacitor, regardless of its ESR (Equivalent Series Resistance) value, including ceramic types (MLCC) for space restricted applications. The ADP3300 achieves exceptional accuracy of ±0.8% at room temperature and ±1.4% overall accuracy over temperature, line and load regulations. The dropout voltage of the ADP3300 is only 80 mV (typical) at 50 mA.

The ADP3300 operates with a wide input voltage range from 3.0 V to 12 V and delivers a load current in excess of 50 mA. It features an error flag that signals when the device is about to lose regulation or when the short circuit or thermal overload protection is activated. Other features include shutdown and optional noise reduction capabilities. The ADP330x anyCAP™ LDO family offers a wide range of output voltages and output current levels from 50 mA to 200 mA:

ADP3301 (100 mA)
ADP3302 (100 mA, Dual Output)
ADP3303 (200 mA)

FUNCTIONAL BLOCK DIAGRAM



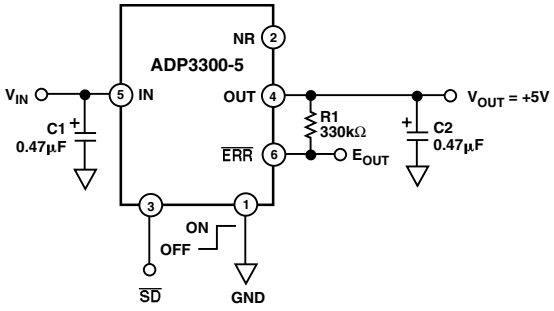


Figure 1. Typical Application Circuit

REV. A

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Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
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ADP3300–SPECIFICATIONS (@ T_A = –40°C to +85°C, V_{IN} = 7 V, C_{IN} = 0.47 µF, C_{OUT} = 0.47 µF, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
OUTPUT VOLTAGE ACCURACY	V_{OUT}	V_{IN} = $V_{OUT(NOM)}$ +0.3 V to 12 V I_L = 0.1 mA to 50 mA T_A = +25°C	–0.8		+0.8	%
		V_{IN} = $V_{OUT(NOM)}$ +0.3 V to 12 V I_L = 0.1 mA to 50 mA	–1.4		+1.4	%
LINE REGULATION	$\frac{\Delta V_O}{\Delta V_{IN}}$	V_{IN} = $V_{OUT(NOM)}$ +0.3 V to 12 V T_A = +25°C		0.02		mV/V
LOAD REGULATION	$\frac{\Delta V_O}{\Delta I_L}$	I_L = 0.1 mA to 50 mA T_A = +25°C		0.06		mV/mA
GROUND CURRENT	I_{GND}	I_L = 50 mA I_L = 0.1 mA		0.55 0.19	1.7 0.3	mA mA
GROUND CURRENT IN DROPOUT	I_{GND}	V_{IN} = 2.5 V I_L = 0.1 mA		0.6	1.2	mA
DROPOUT VOLTAGE	V_{DROP}	V_{OUT} = 98% of $V_{OUT(NOM)}$ I_L = 50 mA I_L = 10 mA I_L = 1 mA		0.08 0.025 0.004	0.17 0.07 0.03	V V V
SHUTDOWN THRESHOLD	V_{THSD}	ON OFF	2.0	0.75 0.75	 0.3	V V
SHUTDOWN PIN INPUT CURRENT	I_{SDIN}	0 < $V_{\overline{SD}}$ ≤ 5 V 5 < $V_{\overline{SD}}$ ≤ 12 V @ V_{IN} = 12 V			1 22	µA µA
GROUND CURRENT IN SHUTDOWN MODE	I_Q	$V_{\overline{SD}}$ = 0, V_{IN} = 12 V T_A = +25°C $V_{\overline{SD}}$ = 0, V_{IN} = 12 V T_A = +85°C		0.005 0.01	1 3	µA µA
OUTPUT CURRENT IN SHUTDOWN MODE	I_{OSD}	T_A = +25°C @ V_{IN} = 12 V T_A = +85°C @ V_{IN} = 12 V			2 4	µA µA
ERROR PIN OUTPUT LEAKAGE	I_{EL}	V_{EO} = 5 V			13	µA
ERROR PIN OUTPUT "LOW" VOLTAGE	V_{EOL}	I_{SINK} = 400 µA		0.12	0.3	V
PEAK LOAD CURRENT	I_{LDPK}	V_{IN} = $V_{OUT(NOM)}$ + 1 V		100		mA
OUTPUT NOISE @ 5 V OUTPUT	V_{NOISE}	f = 10 Hz–100 kHz C_{NR} = 0 C_{NR} = 10 nF, C_L = 10 µF		100 30		µV rms µV rms

NOTE
Ambient temperature of +85°C corresponds to a typical junction temperature of +125°C under typical full load test conditions.

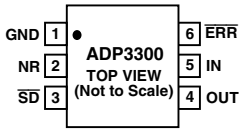
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Input Supply Voltage . . . . . –0.3 V to +16 V
Shutdown Input Voltage . . . . . –0.3 V to +16 V
Error Flag Output Voltage . . . . . –0.3 V to +16 V
Noise Bypass Pin Voltage . . . . . –0.3 V to +5 V
Power Dissipation . . . . . Internally Limited
Operating Ambient Temperature Range . . . . –55°C to +125°C
Operating Junction Temperature Range . . . . –55°C to +125°C
θ_{JA} . . . . . 165°C
θ_{JC} . . . . . 92°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 10 sec) . . . . . +300°C
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

*This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Function
1	GND	Ground Pin.
2	NR	Noise Reduction Pin. Used for further reduction of the output noise (see text for details). No connection if not used.
3	$\overline{SD}$	Active Low Shutdown Pin. Connect to ground to disable the regulator output. When shutdown is not used, this pin should be connected to the input pin.
4	OUT	Output of the Regulator, fixed 2.7, 3.0, 3.2, 3.3 or 5 volts output voltage. Bypass to ground with a 0.47 µF or larger capacitor.
5	IN	Regulator Input.
6	$\overline{ERR}$	Open Collector Output which goes low to indicate that the output is about to go out of regulation.

ORDERING GUIDE

Model	Voltage Output	Package Description	Package Options	Branding Information
ADP3300ART-2.7	2.7 V	Surface Mount	SOT-23-6	LAB
ADP3300ART-3	3.0 V	Surface Mount	SOT-23-6	LBB
ADP3300ART-3.2	3.2 V	Surface Mount	SOT-23-6	LCB
ADP3300ART-3.3	3.3 V	Surface Mount	SOT-23-6	LDB
ADP3300ART-5	5.0 V	Surface Mount	SOT-23-6	LEB

Contact the factory for the availability of other output voltage options.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3300 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ADP3300–Typical Performance Characteristics

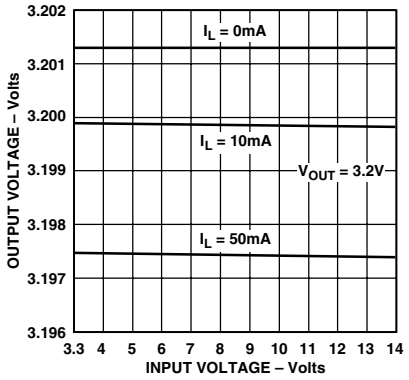


Figure 2. Line Regulation Output Voltage vs. Supply Voltage

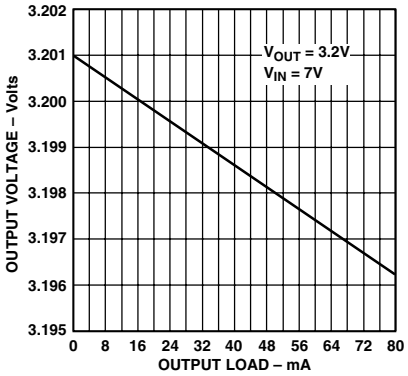


Figure 3. Output Voltage vs. Load Current

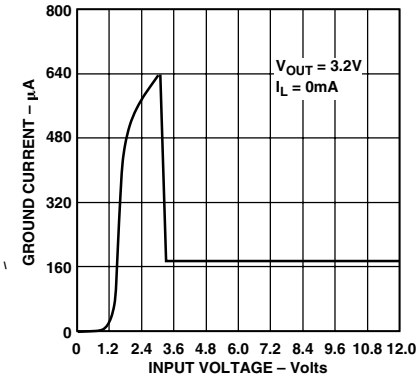


Figure 4. Quiescent Current vs. Supply Voltage

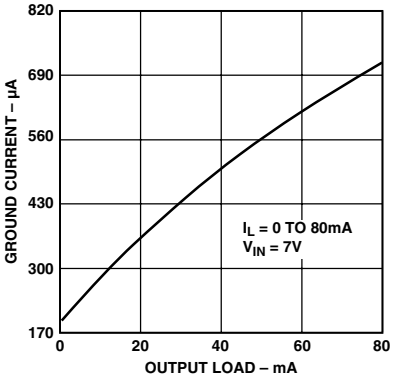


Figure 5. Quiescent Current vs. Load Current

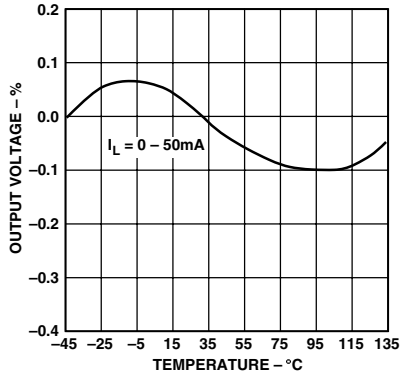


Figure 6. Output Voltage Variation % vs. Temperature

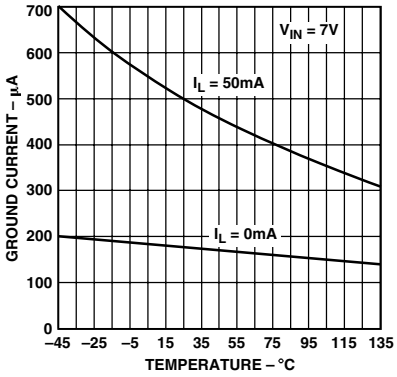


Figure 7. Quiescent Current vs. Temperature

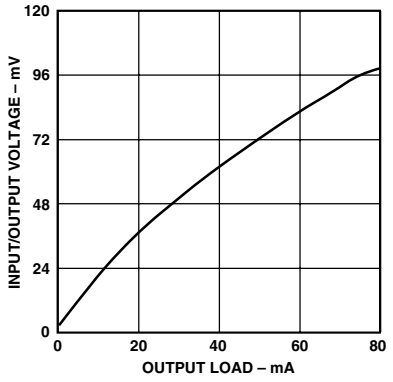


Figure 8. Dropout Voltage vs. Output Current

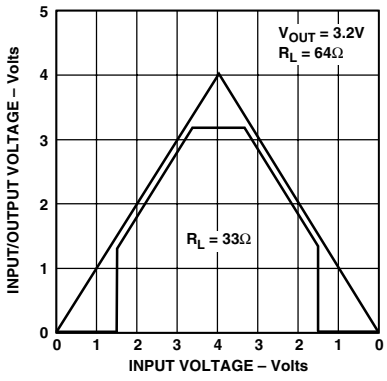


Figure 9. Power-Up/Power-Down

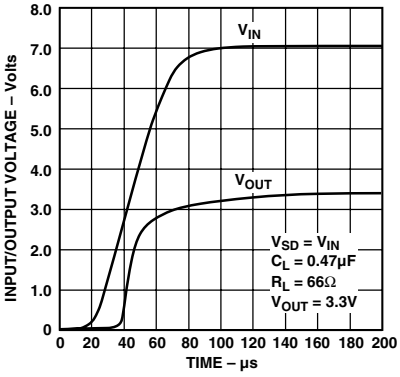


Figure 10. Power-Up Overshoot

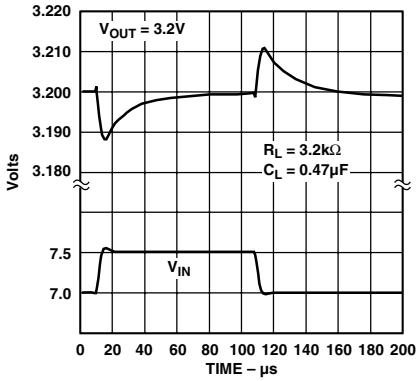


Figure 11. Line Transient Response

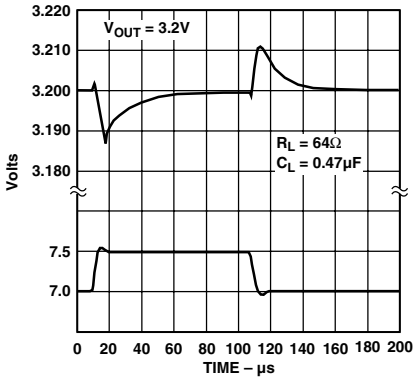


Figure 12. Line Transient Response

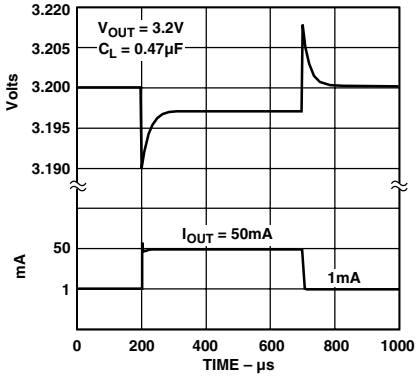


Figure 13. Load Transient

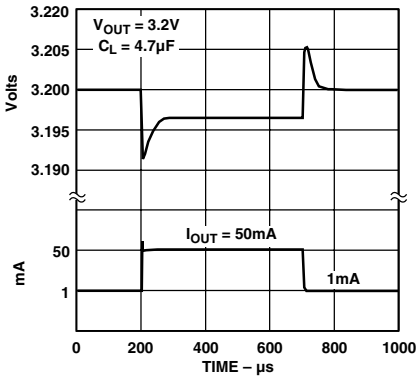


Figure 14. Load Transient

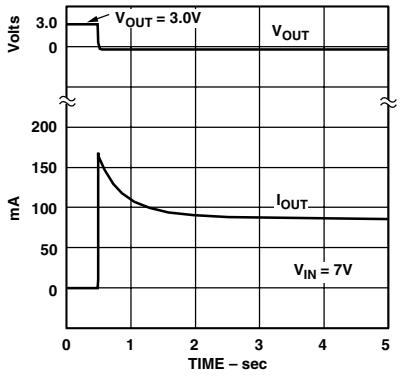


Figure 15. Short Circuit Current

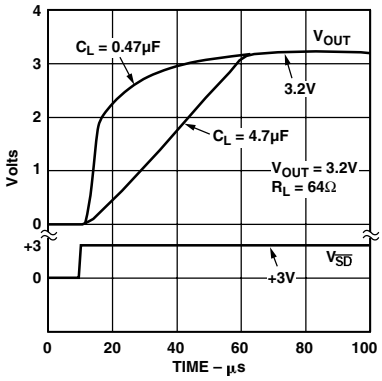


Figure 16. Turn On

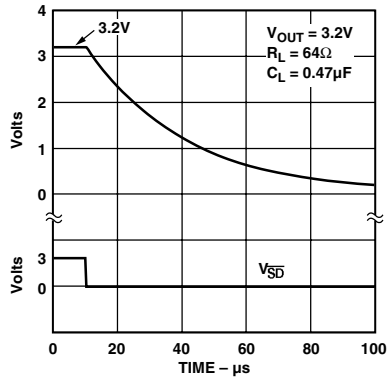


Figure 17. Turn Off

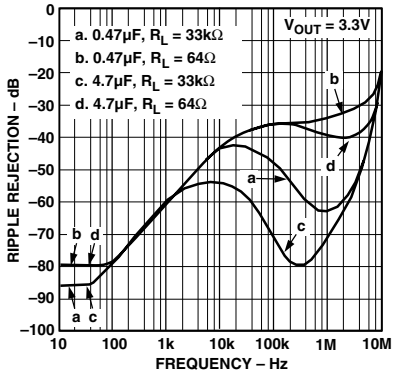


Figure 18. Power Supply Ripple Rejection

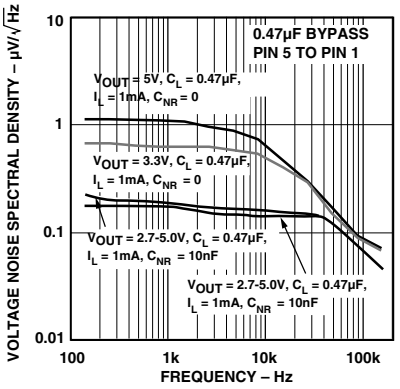


Figure 19. Output Noise Density

THEORY OF OPERATION

The new anyCAP™ LDO ADP3300 uses a single control loop for regulation and reference functions. The output voltage is sensed by a resistive voltage divider consisting of R1 and R2 which is varied to provide the available output voltage option. Feedback is taken from this network by way of a series diode (D1) and a second resistor divider (R3 and R4) to the input of an amplifier.

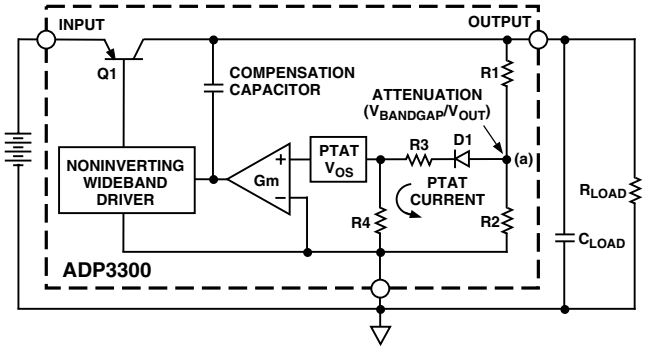


Figure 20. Functional Block Diagram

A very high gain error amplifier is used to control this loop. The amplifier is constructed in such a way that at equilibrium it produces a large, temperature proportional input "offset voltage" that is repeatable and very well controlled. The temperature-proportional offset voltage is combined with the complimentary diode voltage to form a "virtual bandgap" voltage, implicit in the network, although it never appears explicitly in the circuit. Ultimately, this patented design makes it possible to control the loop with only one amplifier. This technique also improves the noise characteristics of the amplifier by providing more flexibility on the trade-off of noise sources that leads to a low noise design.

The R1, R2 divider is chosen in the same ratio as the bandgap voltage to the output voltage. Although the R1, R2 resistor divider is loaded by the diode D1 and a second divider consisting of R3 and R4, the values are chosen to produce a temperature stable output. This unique arrangement specifically corrects for the loading of the divider so that the error resulting from base current loading in conventional circuits is avoided.

The patented amplifier controls a new and unique noninverting driver that drives the pass transistor, Q1. The use of this special noninverting driver enables the frequency compensation to include the load capacitor in a pole splitting arrangement to achieve reduced sensitivity to the value, type and ESR of the load capacitance.

Most LDOs place strict requirements on the range of ESR values for the output capacitor because they are difficult to stabilize due to the uncertainty of load capacitance and resistance. Moreover, the ESR value, required to keep conventional LDOs stable, changes depending on load and temperature. These ESR limitations make designing with LDOs more difficult because of their unclear specifications and extreme variations over temperature.

This is no longer true with the ADP3300 anyCAP™ LDO. It can be used with virtually any capacitor, with no constraint on the minimum ESR. The innovative design allows the circuit to be stable with just a small 0.47 µF capacitor on the output. Additional advantages of the pole splitting scheme include superior line noise rejection and very high regulator gain, which leads to excellent line and load regulation. An impressive ±1.4% accuracy is guaranteed over line, load and temperature.

Additional features of the circuit include current limit, thermal shutdown and noise reduction. Compared to the standard solutions that give warning after the output has lost regulation, the ADP3300 provides improved system performance by enabling the $\overline{\text{ERR}}$ pin to give warning before the device loses regulation.

As the chip's temperature rises above 165°C, the circuit activates a soft thermal shutdown, indicated by a signal low on the $\overline{\text{ERR}}$ pin, to reduce the current to a safe level.

To reduce the noise gain of the loop, the node of the main divider network (a) is made available at the noise reduction (NR) pin, which can be bypassed with a small capacitor (10 nF–100 nF).

APPLICATION INFORMATION

Capacitor Selection: anyCAP™

Output Capacitors: as with any micropower device, output transient response is a function of the output capacitance. The ADP3300 is stable with a wide range of capacitor values, types and ESR (anyCAP™). A capacitor as low as 0.47 µF is all that is needed for stability. However, larger capacitors can be used if high output current surges are anticipated. The ADP3300 is stable with extremely low ESR capacitors (ESR ≈ 0), such as multilayer ceramic capacitors (MLCC) or OSCON.

Input Bypass Capacitor: an input bypass capacitor is not required; however, for applications where the input source is high impedance or far from the input pins, a bypass capacitor is recommended. Connecting a 0.47 µF capacitor from the input to ground reduces the circuit's sensitivity to PC board layout. If a bigger output capacitor is used, the input capacitor should be 1 µF minimum.

Noise Reduction

A noise reduction capacitor (C_{NR}) can be used to further reduce the noise by 6 dB–10 dB (Figure 21). Low leakage capacitors in the 10 nF–100 nF range provide the best performance. For load current less than 200 µA, a 4.7 µF output capacitor provides the lowest noise and the best overall performance. Since the noise reduction pin (NR) is internally connected to a high impedance node, any connection to this node should be carefully done to avoid noise pickup from external sources. The pad connected to this pin should be as small as possible. Long PC board traces are not recommended.

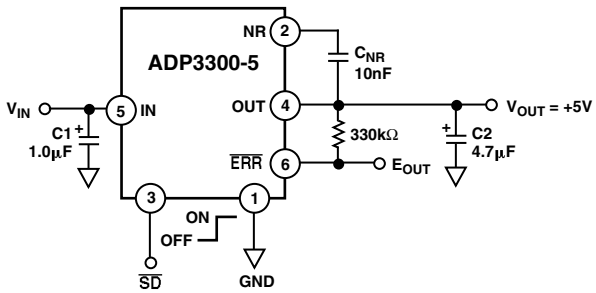


Figure 21. Noise Reduction Circuit

Thermal Overload Protection

The ADP3300 is protected against damage due to excessive power dissipation by its thermal overload protection circuit, which limits the die temperature to a maximum of 165°C. Under extreme conditions (i.e., high ambient temperature and high power dissipation), where die temperature starts to rise above 165°C, the output current is reduced until die temperature has dropped to a safe level. Output current is restored when the die temperature is reduced.

Current and thermal limit protections are intended to protect the device against accidental overload conditions. For normal operation, device power dissipation should be externally limited so that junction temperatures will not exceed 125°C.

Calculating Junction Temperature

Device power dissipation is calculated as follows:

$$PD = (V_{IN} - V_{OUT})\, I_{LOAD} + (V_{IN})\, I_{GND}$$

Where I_{LOAD} and I_{GND} are load current and ground current, V_{IN} and V_{OUT} are input and output voltages respectively.

Assuming I_{LOAD} = 50 mA, I_{GND} = 0.5 mA, V_{IN} = 8 V and V_{OUT} = 3.3 V, device power dissipation is:

$$PD = (8 - 3.3)\ 0.05 + 8 \times 0.5\ mA = 0.239\ W$$

$$\Delta T = T_J - T_A = PD \times \theta_{JA} = 0.239 \times 165 = 39.4°C$$

With a maximum junction temperature of 125°C, this yields a maximum ambient temperature of 85°C.

Printed Circuit Board Layout Consideration

Surface mount components rely on the conductive traces or pads to transfer heat away from the device. Appropriate PC board layout techniques should be used to remove heat from the immediate vicinity of the package.

The following general guidelines will be helpful when designing a board layout:

1. PC board traces with larger cross section areas will remove more heat. For optimum results, use PC boards with thicker copper and wider traces.
2. Increase the surface area exposed to open air so heat can be removed by convection or forced air flow.
3. Do not use solder mask or silkscreen on the heat dissipating traces because it will increase the junction to ambient thermal resistance of the package.

Shutdown Mode

Applying a TTL high signal to the shutdown pin or tying it to the input pin will turn the output ON. Pulling the shutdown pin down to 0.3 V or below, or tying it to ground, will turn the output OFF. In shutdown mode, quiescent current is reduced to less than 1 μA.

Error Flag Dropout Detector

The ADP3300 will maintain its output voltage over a wide range of load, input voltage and temperature conditions. If the output is about to lose regulation, for example, by reducing the supply voltage below the combined regulated output and dropout voltages, the $\overline{ERR}$ pin will be activated. The $\overline{ERR}$ output is an open collector that will be driven low.

Once set, the $\overline{ERR}$or flag's hysteresis will keep the output low until a small margin of operating range is restored either by raising the supply voltage or reducing the load.

APPLICATION CIRCUITS

Crossover Switch

The circuit in Figure 22 shows that two ADP3300s can be used to form a mixed supply voltage system. The output switches between two different levels selected by an external digital input. Output voltages can be any combination of voltages from the Ordering Guide.

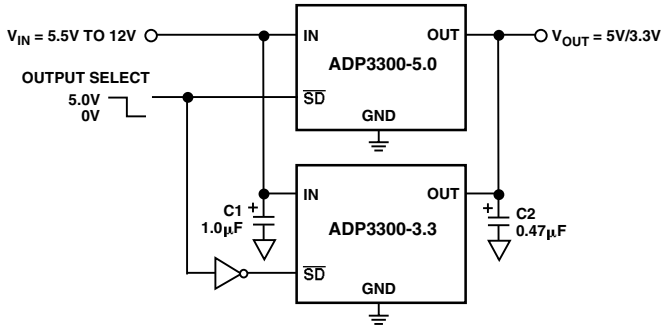


Figure 22. Crossover Switch

Higher Output Current

If higher current is needed, an appropriate pass transistor can be used, as in Figure 23, to increase the output current to 1 A.

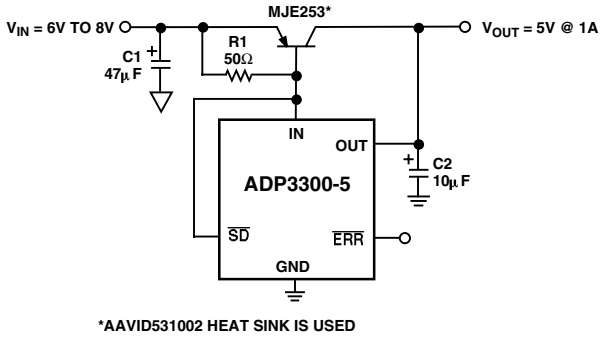


Figure 23. High Output Current Linear Regulator

Constant Dropout Post Regulator

The circuit in Figure 24 provides high precision with low dropout for any regulated output voltage. It significantly reduces the ripple from a switching regulator while providing a constant dropout voltage, which limits the power dissipation of the LDO to 15 mW. The ADP3000 used in this circuit is a switching regulator in the step-up configuration.

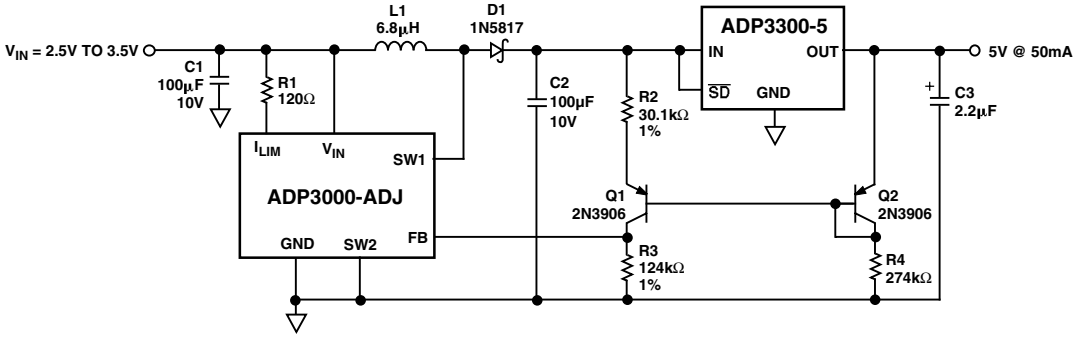
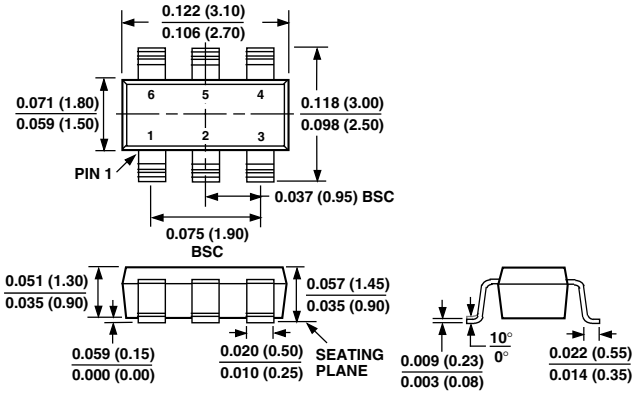


Figure 24. Constant Dropout Post Regulator

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

6-Lead Surface Mount Package (SOT-23)



C00132–0–7/00 (rev .A)

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