

## BATTERY PROTECTION IC FOR 2-SERIAL-CELL PACK S-8232 Series

The 8232 series is a lithium-ion / lithium-polymer rechargeable battery protection IC incorporating high-accuracy voltage detection circuit and delay circuit. The S-8232 series is suitable for 2-cell serial lithium-ion / lithium-polymer battery packs.

### ■ Features

- (1) Internal high-accuracy voltage detection circuit
  - Overcharge detection voltage 3.85 V  $\pm$  25 mV to 4.60 V  $\pm$  25 mV Applicable in 5 mV step
  - Overcharge release voltage 3.60 V  $\pm$  50 mV to 4.60 V  $\pm$  50 mV Applicable in 5 mV step  
(The overcharge release voltage can be selected within the range where a difference from overcharge detection voltage is 0 to 0.3 V.)
  - Overdischarge detection voltage 1.70 V  $\pm$  80 mV to 2.60 V  $\pm$  80 mV Applicable in 50 mV step
  - Overdischarge release voltage 1.70 V  $\pm$  100 mV to 3.80 V  $\pm$  100 mV Applicable in 50 mV step  
(The overdischarge release voltage can be selected within the range where a difference from overdischarge detection voltage is 0 to 1.2 V.)
  - Overcurrent detection voltage 1 0.07 V  $\pm$  20 mV to 0.30 V  $\pm$  20 mV Applicable in 5 mV step
- (2) High input-voltage device : Absolute maximum ratings 18 V.
- (3) Wide operating voltage range : 2 to 16 V
- (4) The delay time for every detection can be set via an external capacitor.  
(Each delay time for Overcharge detection, Overdischarge detection, Overcurrent detection are "Proportion of hundred to ten to one".)
- (5) Two overcurrent detection levels (Protection for short-circuiting)
- (6) Internal auxiliary over voltage detection circuit (Fail-safe for overcharge detection voltage)
- (7) Internal charge circuit for 0 V battery (Unavailable is option)
- (8) Low current consumption
  - Operation mode 7.5  $\mu$ A typ. 14.2  $\mu$ A max. (– 40 to + 85 °C)
  - Power-down mode 0.2 nA typ. 0.1  $\mu$ A max. (– 40 to + 85 °C)
- (9) Lead-free products

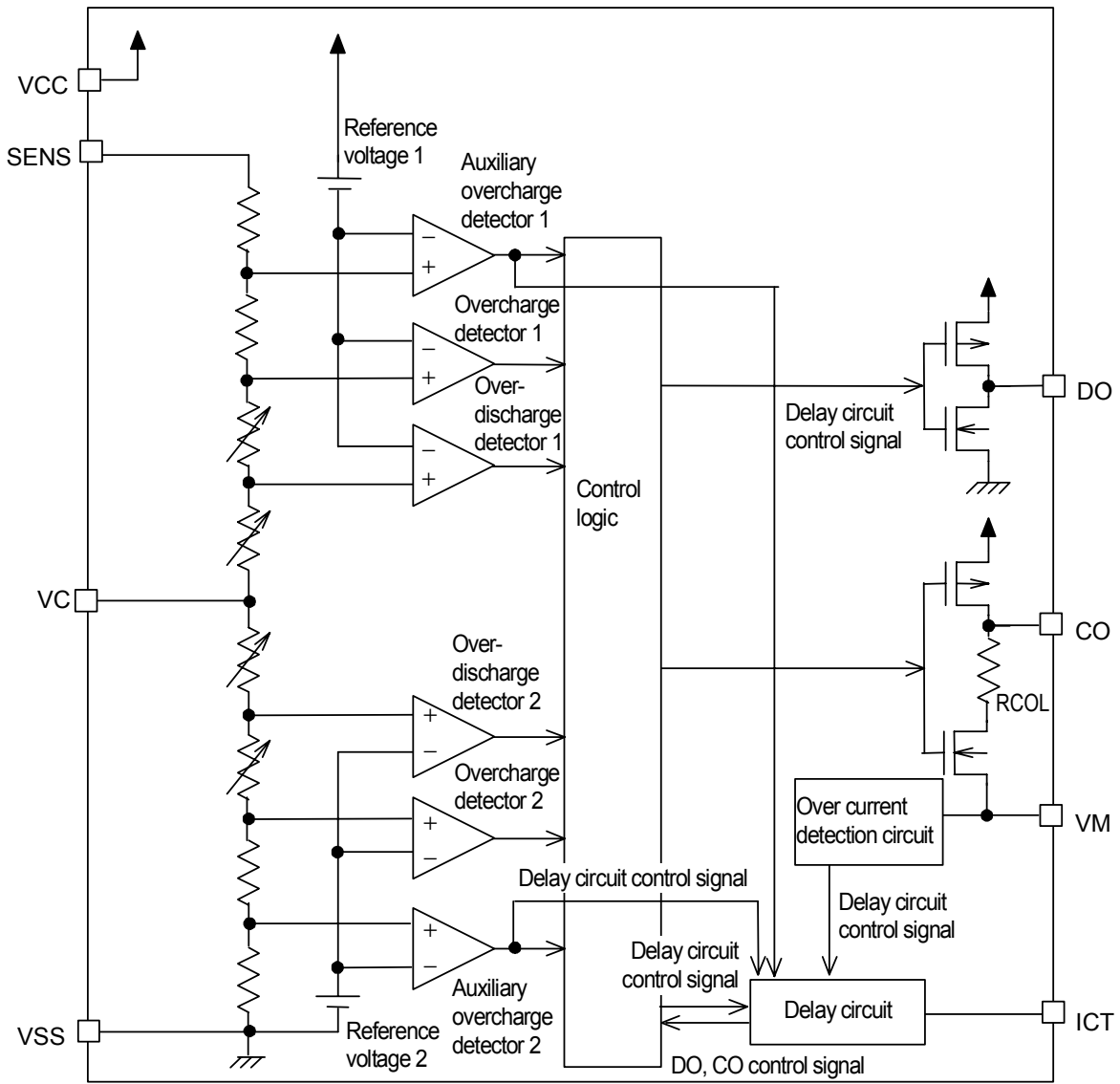
### ■ Application

- Lithium-ion rechargeable battery packs
- Lithium- polymer rechargeable battery packs

### ■ Package

Package Name	Drawing Code		
	Package	Tape	Reel
8-Pin TSSOP	FT008-A	FT008-E	FT008-E

■ **Block Diagram**



**Remark** Resistor (RCOL) is connected to the Nch transistor although CO pin serves as a CMOS output. For this, impedance becomes high when outputting "L" from CO pin. Refer to the "■ **Electrical Characteristics**" for the impedance value.

**Figure 1**

# BATTERY PROTECTION IC FOR 2-SERIAL-CELL PACK

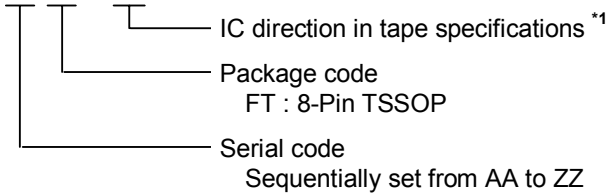
## S-8232 Series

Rev.5.4\_00

### ■ Product Name Structure

#### 1. Product Name

**S-8232 xx FT - T2 - G**



\*1. Refer to the taping specifications.

#### 2. Product Name List

**Table 1 (1 / 2)**

Product name / Item	Overcharge detection voltage 1, 2 $V_{CU}$	Overcharge release voltage 1, 2 $V_{CD}$	Overdischarge detection voltage 1, 2 $V_{DD}$	Overdischarge release voltage 1, 2 $V_{DU}$	Overcurrent detection voltage 1 $V_{IOV1}$	Overcharge detection delay time $t_{CU}$ ( $C3 = 0.22 \mu F$ )	0 V battery charging function
S-8232AAFT-T2-G	4.25 V ± 25 mV	4.05 V ± 50 mV	2.40 V ± 80 mV	3.00 V ± 100 mV	0.150 V ± 20 mV	1.0 s	Available
S-8232ABFT-T2-G	4.35 V ± 25 mV	4.15 V ± 50 mV	2.30 V ± 80 mV	3.00 V ± 100 mV	0.300 V ± 20 mV	1.0 s	Available
S-8232ACFT-T2-G	4.35 V ± 25 mV	4.15 V ± 50 mV	2.30 V ± 80 mV	3.00 V ± 100 mV	0.300 V ± 20 mV	1.0 s	Unavailable
S-8232AEFT-T2-G	4.35 V ± 25 mV	4.28 V ± 50 mV	2.15 V ± 80 mV	2.80 V ± 100 mV	0.100 V ± 20 mV	1.0 s	Available
S-8232AFFT-T2-G	4.25 V ± 25 mV	4.05 V ± 50 mV	2.30 V ± 80 mV	2.70 V ± 100 mV	0.300 V ± 20 mV	1.0 s	Available
S-8232AGFT-T2-G	4.25 V ± 25 mV	4.05 V ± 50 mV	2.20 V ± 80 mV	2.40 V ± 100 mV	0.200 V ± 20 mV	1.0 s	Available
S-8232AHFT-T2-G	4.25 V ± 25 mV	4.05 V ± 50 mV	2.20 V ± 80 mV	2.40 V ± 100 mV	0.300 V ± 20 mV	1.0 s	Available
S-8232AIFT-T2-G	4.325 V ± 25 mV	4.325 V ± 25 mV <sup>*1*2</sup>	2.40 V ± 80 mV	3.00 V ± 100 mV	0.300 V ± 20 mV	1.0 s	Unavailable
S-8232AJFT-T2-G	4.25 V ± 25 mV	4.05 V ± 50 mV	2.40 V ± 80 mV	3.00 V ± 100 mV	0.150 V ± 20 mV	1.0 s	Unavailable
S-8232AKFT-T2-G	4.20 V ± 25 mV	4.00 V ± 50 mV	2.30 V ± 80 mV	2.90 V ± 100 mV	0.200 V ± 20 mV	1.0 s	Available
S-8232ALFT-T2-G	4.30 V ± 25 mV	4.05 V ± 50 mV	2.00 V ± 80 mV	3.00 V ± 100 mV	0.200 V ± 20 mV	1.0 s	Available
S-8232AMFT-T2-G	4.19 V ± 25 mV	4.19 V ± 25 mV <sup>*1</sup>	2.00 V ± 80 mV	3.00 V ± 100 mV	0.190 V ± 20 mV	1.0 s	Available
S-8232ANFT-T2-G	4.325 V ± 25 mV	4.325 V ± 25 mV <sup>*1*3</sup>	2.40 V ± 80 mV	3.00 V ± 100 mV	0.300 V ± 20 mV	1.0 s	Unavailable
S-8232AOFT-T2-G	4.30 V ± 25 mV	4.05 V ± 50 mV	2.00 V ± 80 mV	3.00 V ± 100 mV	0.230 V ± 20 mV	1.0 s	Available
S-8232APFT-T2-G	4.28 V ± 25 mV	4.05 V ± 50 mV	2.30 V ± 80 mV	2.90 V ± 100 mV	0.100 V ± 20 mV	1.0 s	Unavailable
S-8232ARFT-T2-G	4.325 V ± 25 mV	4.325 V ± 25 mV <sup>*1*3</sup>	2.00 V ± 80 mV	2.50 V ± 100 mV	0.300 V ± 20 mV	1.0 s	Unavailable
S-8232ASFT-T2-G <sup>*4</sup>	4.295 V ± 25 mV	4.20 V ± 50 mV <sup>*3</sup>	2.30 V ± 80 mV	3.00 V ± 100 mV	0.300 V ± 20 mV	1.0 s	Unavailable
S-8232ATFT-T2-G	4.125 V ± 25 mV	4.125 V ± 25 mV <sup>*1</sup>	2.00 V ± 80 mV	3.00 V ± 100 mV	0.190 V ± 20 mV	1.0 s	Available
S-8232AUFT-T2-G	4.30 V ± 25 mV	4.10 V ± 50 mV	2.40 V ± 80 mV	3.00 V ± 100 mV	0.200 V ± 20 mV	1.0 s	Unavailable
S-8232AVFT-T2-G	4.30 V ± 25 mV	4.05 V ± 50 mV	2.00 V ± 80 mV	3.00 V ± 100 mV	0.300 V ± 20 mV	1.0 s	Available
S-8232AWFT-T2-G	4.35 V ± 25 mV	4.15 V ± 50 mV	2.30 V ± 80 mV	3.00 V ± 100 mV	0.150 V ± 20 mV	1.0 s	Unavailable
S-8232AXFT-T2-G	4.325 V ± 25 mV	4.200 V ± 50 mV	2.30 V ± 80 mV	3.00 V ± 100 mV	0.20 V ± 20 mV	1.0 s	Unavailable
S-8232AYFT-T2-G	4.30 V ± 25 mV	4.05 V ± 50 mV	2.00 V ± 80 mV	2.00 V ± 80 mV	0.20 V ± 20 mV	1.0 s	Available
S-8232AZFT-T2-G	4.30 V ± 25 mV	4.05 V ± 50 mV	2.30 V ± 80 mV	2.30 V ± 80 mV	0.20 V ± 20 mV	1.0 s	Available

**Table 1 (2 / 2)**

Product name / Item	Overcharge detection voltage 1, 2 $V_{CU}$	Overcharge release voltage 1, 2 $V_{CD}$	Overdischarge detection voltage 1, 2 $V_{DD}$	Overdischarge release voltage 1, 2 $V_{DU}$	Overcurrent detection voltage 1 $V_{IOV1}$	Overcharge detection delay time $t_{CU}$ ( $C3 = 0.22 \mu F$ )	0 V battery charging function
S-8232NAFT-T2-G	4.325 V ± 25 mV	4.325 V ± 25 mV <sup>*1 *3</sup>	2.40 V ± 80 mV	3.00 V ± 100 mV	0.15 V ± 20 mV	1.0 s	Unavailable
S-8232NBFT-T2-G	4.35 V ± 25 mV	4.25 V ± 50 mV	3.00 V ± 80 mV	3.70 V ± 100 mV	0.30 V ± 20 mV	1.0 s	Unavailable
S-8232NCFT-T2-G	4.275 V ± 25 mV	4.05 V ± 50 mV	2.20 V ± 80 mV	3.00 V ± 100 mV	0.20 V ± 20 mV	1.0 s	Unavailable
S-8232NDFT-T2-G	4.35 V ± 25 mV	4.15 V ± 50 mV	2.30 V ± 80 mV	2.30 V ± 80 mV	0.15 V ± 20 mV	1.0 s	Available
S-8232NEFT-T2-G	4.35 V ± 25 mV	4.15 V ± 50 mV	2.30 V ± 80 mV	3.00 V ± 100 mV	0.23 V ± 20 mV	1.0 s	Available
S-8232NFFT-T2-G	4.325 V ± 25 mV	4.1 V ± 50 mV <sup>*3</sup>	2.30 V ± 80 mV	2.90 V ± 100 mV	0.21 V ± 20 mV	1.0 s	Unavailable
S-8232NGFT-T2-G	4.35 V ± 25 mV	4.15 V ± 50 mV	2.60 V ± 80 mV	3.00 V ± 100 mV	0.30 V ± 20 mV	1.0 s	Available
S-8232NHFT-T2-G	4.28 V ± 25 mV	4.05 V ± 50 mV	2.30 V ± 80 mV	2.90 V ± 100 mV	0.11 V ± 20 mV	1.0 s	Unavailable
S-8232NIFT-T2-G	4.25 V ± 25 mV	4.05 V ± 50 mV <sup>*3</sup>	2.50 V ± 80 mV	3.00 V ± 100 mV	0.15 V ± 20 mV	1.0 s	Unavailable
S-8232NJFT-T2-G	4.28 V ± 25 mV	4.05 V ± 50 mV	2.30 V ± 80 mV	2.90 V ± 100 mV	0.11 V ± 20 mV	1.0 s	Available
S-8232NKFT-T2-G	4.35 V ± 25 mV	4.15 V ± 50 mV	2.30 V ± 80 mV	2.30 V ± 80 mV	0.12 V ± 20 mV	1.0 s	Available
S-8232NLFT-T2-G	4.30 V ± 25 mV	4.05 V ± 50 mV	2.30 V ± 80 mV	3.00 V ± 100 mV	0.23 V ± 20 mV	1.0 s	Available
S-8232NMFT-T2-G	4.28 V ± 25 mV	4.05 V ± 50 mV	2.30 V ± 80 mV	2.90 V ± 100 mV	0.08 V ± 20 mV	1.0 s	Available
S-8232NNFT-T2-G	4.28 V ± 25 mV	4.08 V ± 50 mV <sup>*3</sup>	2.20 V ± 80 mV	2.40 V ± 100 mV	0.13 V ± 20 mV	1.0 s	Unavailable
S-8232NOFT-T2-G	4.295 V ± 25 mV	4.045 V ± 50 mV <sup>*3</sup>	2.20 V ± 80 mV	2.40 V ± 100 mV	0.13 V ± 20 mV	1.0 s	Unavailable
S-8232NPFT-T2-G	4.25 V ± 25 mV	4.05 V ± 50 mV	2.30 V ± 80 mV	3.00 V ± 100 mV	0.30 V ± 20 mV	1.0 s	Unavailable
S-8232NQFT-T2-G	4.25 V ± 25 mV	4.05 V ± 50 mV	2.60 V ± 80 mV	3.00 V ± 100 mV	0.30 V ± 20 mV	1.0 s	Unavailable
S-8232NRFT-T2-G	4.15 V ± 25 mV	3.95 V ± 50 mV	2.60 V ± 80 mV	3.00 V ± 100 mV	0.30 V ± 20 mV	1.0 s	Unavailable
S-8232NSFT-T2-G	4.15 V ± 25 mV	3.95 V ± 50 mV	2.30 V ± 80 mV	3.00 V ± 100 mV	0.30 V ± 20 mV	1.0 s	Unavailable
S-8232NTFT-T2-G	4.225 V ± 25 mV	4.15 V ± 50 mV	2.00 V ± 80 mV	2.00 V ± 100 mV	0.09 V ± 20 mV	1.0 s	Unavailable
S-8232NUFT-T2-G	3.85 V ± 25 mV	3.75 V ± 50 mV	2.23 V ± 80 mV	2.23 V ± 80 mV	0.15 V ± 20 mV	1.0 s	Available
S-8232NWFT-T2-G	4.210 V ± 25 mV	4.125 V ± 50 mV	2.00 V ± 80 mV	2.00 V ± 80 mV	0.09 V ± 20 mV	1.0 s	Unavailable

- \*1. No overcharge detection / release hysteresis
- \*2. The magnification of final overcharge is 1.11; the others are 1.25.
- \*3. No final overcharging function
- \*4. Refer to the \*2 in the “■ Operation”.

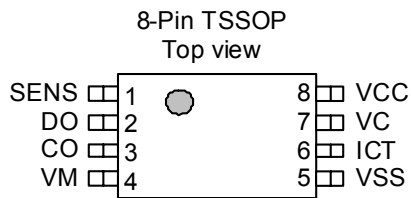
**Remark 1.** Please contact our sales office for the products with detection voltage value other than those specified above.

**2.** The overdischarge detection voltage can be selected within the range from 1.7 to 3.0 V. When the overdischarge detection voltage is higher than 2.6 V, the overcharge detection voltage and the overcharge release voltage are limited as “Table 2”.

**Table 2**

Overdischarge detection voltage 1, 2 $V_{DD}$	Overcharge detection voltage 1, 2 $V_{CU}$	Voltage difference between overcharge detection voltage and overcharge release voltage $V_{CU} - V_{CD}$
1.70 to 2.60 V	3.85 to 4.60 V	0 to 0.30 V
1.70 to 2.80 V	3.85 to 4.60 V	0 to 0.20 V
1.70 to 3.00 V	3.85 to 4.50 V	0 to 0.10 V

■ **Pin Configuration**



**Figure 2**

**Table 3**

Pin No.	Symbol	Description
1	SENS	Detection pin for voltage between SENS and VC (Detection for overcharge and overdischarge)
2	DO	FET gate connection pin for discharge control (CMOS output)
3	CO	FET gate connection pin for charge control (CMOS output)
4	VM	Detection pin for voltage between VM and VSS (Overcurrent detection pin)
5	VSS	Negative power input pin
6	ICT	Capacitor connection pin for detection delay
7	VC	Middle voltage input pin
8	VCC	Positive power input pin

■ **Absolute Maximum Ratings**

**Table 4**

(Ta = 25 °C unless otherwise specified)

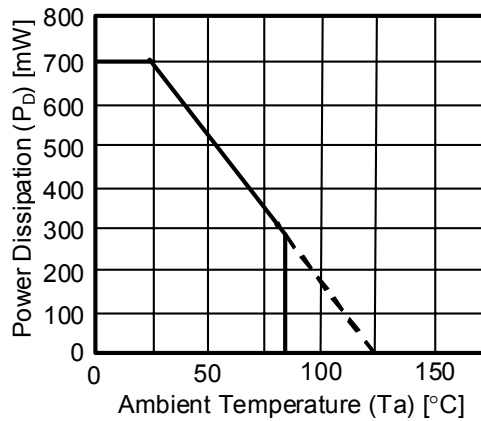
Item	Symbol	Applied Pin	Absolute Maximum Ratings	Unit
Input voltage between VCC and VSS	V <sub>DS</sub>	VCC	V <sub>SS</sub> - 0.3 to V <sub>SS</sub> + 18	V
SENS input pin voltage	V <sub>SENS</sub>	SENS	V <sub>SS</sub> - 0.3 to V <sub>CC</sub> + 0.3	V
ICT input pin voltage	V <sub>ICT</sub>	ICT	V <sub>SS</sub> - 0.3 to V <sub>CC</sub> + 0.3	V
VM input pin voltage	V <sub>VM</sub>	VM	V <sub>CC</sub> - 18 to V <sub>CC</sub> + 0.3	V
DO output pin voltage	V <sub>DO</sub>	DO	V <sub>SS</sub> - 0.3 to V <sub>CC</sub> + 0.3	V
CO output pin voltage	V <sub>CO</sub>	CO	V <sub>VM</sub> - 0.3 to V <sub>CC</sub> + 0.3	V
Power dissipation	P <sub>D</sub>	—	300 (When not mounted on board)	mW
			700*1	mW
Operating ambient temperature	T <sub>opr</sub>	—	- 40 to + 85	°C
Storage temperature	T <sub>stg</sub>	—	- 40 to + 125	°C

\*1. When mounted on board

**[Mounted board]**

- (1) Board size : 114.3 mm × 76.2 mm × t1.6 mm
- (2) Name : JEDEC STANDARD51-7

**Caution** The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.



**Figure 3 Power Dissipation of Package (When Mounted on Board)**

■ Electrical Characteristics

Table 5

(Ta = 25 °C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
<b>[DETECTION VOLTAGE]</b>								
Overcharge detection voltage 1, 2	$V_{CU1,2}$	3.85 to 4.60 V, Adjustable	$V_{CU1,2} - 0.025$	$V_{CU1,2}$	$V_{CU1,2} + 0.025$	V	1, 2	1
Auxiliary overcharge detection voltage 1, 2 *1 $V_{CUaux1}, V_{CUaux2} = V_{CU1}, V_{CU2} \times 1.25$ or $V_{CUaux1}, V_{CUaux2} = V_{CU1}, V_{CU2} \times 1.11$	$V_{CUaux1,2}$	$V_{CU1,2} \times 1.25$	$V_{CU1,2} \times 1.21$	$V_{CU1,2} \times 1.25$	$V_{CU1,2} \times 1.29$	V	1, 2	1
	$V_{CUaux1,2}$	$V_{CU1,2} \times 1.11$	$V_{CU1,2} \times 1.07$	$V_{CU1,2} \times 1.11$	$V_{CU1,2} \times 1.15$	V	1, 2	1
Overcharge release voltage 1, 2	$V_{CD1,2}$	3.60 to 4.60 V, Adjustable	$V_{CD1,2} - 0.050$	$V_{CD1,2}$	$V_{CD1,2} + 0.050$	V	1, 2	1
Overdischarge detection voltage 1, 2	$V_{DD1,2}$	1.70 to 2.60 V, Adjustable	$V_{DD1,2} - 0.080$	$V_{DD1,2}$	$V_{DD1,2} + 0.080$	V	1, 2	1
Overdischarge release voltage 1, 2	$V_{DU1,2}$	1.70 to 3.80 V, Adjustable	$V_{DU1,2} - 0.100$	$V_{DU1,2}$	$V_{DU1,2} + 0.100$	V	1, 2	1
Overcurrent detection voltage 1	$V_{IOV1}$	0.07 to 0.30 V, Adjustable	$V_{IOV1} - 0.020$	$V_{IOV1}$	$V_{IOV1} + 0.020$	V	3	1
Overcurrent detection voltage 2	$V_{IOV2}$	Load short circuit, $V_{CC}$ reference	-1.57	-1.20	-0.83	V	3	1
Temperature coefficient 1 for detection voltage *2	$T_{COE1}$	Ta = -40 to +85 °C	-0.6	0	0.6	mV/°C	—	—
Temperature coefficient 2 for detection voltage *3	$T_{COE2}$	Ta = -40 to +85 °C	-0.24	-0.05	0	mV/°C	—	—
<b>[DELAY TIME (C3 = 0.22 μF)]</b>								
Overcharge detection delay time 1, 2	$t_{CU1,2}$	1.0 s	0.73	1.00	1.35	s	8, 9	5
Overdischarge detection delay time 1, 2	$t_{DD1,2}$	0.1 s	68	100	138	ms	8, 9	5
Overcurrent detection delay time 1	$t_{IOV1}$	0.01 s	6.7	10	13.9	ms	10	5
<b>[INPUT VOLTAGE]</b>								
Input voltage between VCC and VSS	$V_{DS}$	Absolute maximum rating	-0.3	—	18	V	—	—
<b>[OPERATING VOLTAGE]</b>								
Operating voltage between VCC and VSS *4	$V_{DSOP}$	Output logic fixed	2.0	—	16	V	—	—
<b>[CURRENT CONSUMPTION]</b>								
Current consumption during normal operation	$I_{OPE}$	V1 = V2 = 3.6 V	2.1	7.5	12.7	μA	4	2
Current consumption at power down	$I_{PDN}$	V1 = V2 = 1.5 V	0	0.0002	0.04	μA	4	2
<b>[OUTPUT VOLTAGE]</b>								
DO voltage "H"	$V_{DO(H)}$	$I_{OUT} = 10 \mu A$	$V_{CC} - 0.05$	$V_{CC} - 0.003$	$V_{CC}$	V	6	3
DO voltage "L"	$V_{DO(L)}$	$I_{OUT} = 10 \mu A$	$V_{SS}$	$V_{SS} + 0.003$	$V_{SS} + 0.05$	V	6	3
CO voltage "H"	$V_{CO(H)}$	$I_{OUT} = 10 \mu A$	$V_{CC} - 0.15$	$V_{CC} - 0.019$	$V_{CC}$	V	7	4
<b>[CO PIN INTERNAL RESISTANCE]</b>								
Resistance between VSS and CO	$R_{COL}$	$V_{CC} - V_{SS} = 9.4 V$	0.29	0.6	1.44	MΩ	7	4
<b>[INTERNAL RESISTANCE]</b>								
Resistance between VCC and VM	$R_{VCM}$	$V_{CC} - V_{VM} = 0.5 V$	105	240	575	kΩ	5	2
Resistance between VSS and VM	$R_{VSM}$	$V_{VM} - V_{SS} = 1.1 V$	511	597	977	kΩ	5	2
<b>[0 V BATTERY CHARGE FUNCTION]</b>								
0 V battery charge starting charger voltage	$V_{OCHA}$	0 V battery charging function "available"	0.38	0.75	1.12	V	11	6
0 V battery charge inhibition battery voltage 1, 2	$V_{OINH1,2}$	0 V battery charging function "unavailable"	0.32	0.88	1.44	V	12, 13	6

\*1. Auxiliary overcharge detection voltage is equal to the overcharge detection voltage times 1.11 for the products without overcharge hysteresis, and times 1.25 for other products.

\*2. Temperature coefficient 1 for detection voltage should be applied to overcharge detection voltage, overcharge release voltage, overdischarge detection voltage, and overdischarge release voltage.

\*3. Temperature coefficient 2 for detection voltage should be applied to overcurrent detection voltage.

\*4. The DO and CO pin logic are established at the operating voltage.

**Table 6**

(Ta = - 20 to + 70 °C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
<b>[DETECTION VOLTAGE]</b>								
Overcharge detection voltage 1, 2	V <sub>CU1,2</sub>	3.85 to 4.60 V, Adjustable	V <sub>CU1,2</sub> - 0.045	V <sub>CU1,2</sub>	V <sub>CU1,2</sub> + 0.040	V	1, 2	1
Auxiliary overcharge detection voltage 1, 2 *1 V <sub>CUaux1</sub> , V <sub>CUaux2</sub> = V <sub>CU1</sub> , V <sub>CU2</sub> × 1.25 or V <sub>CUaux1</sub> , V <sub>CUaux2</sub> = V <sub>CU1</sub> , V <sub>CU2</sub> × 1.11	V <sub>CUaux1,2</sub>	V <sub>CU1,2</sub> × 1.25	V <sub>CU1,2</sub> × 1.19	V <sub>CU1,2</sub> × 1.25	V <sub>CU1,2</sub> × 1.31	V	1, 2	1
	V <sub>CUaux1,2</sub>	V <sub>CU1,2</sub> × 1.11	V <sub>CU1,2</sub> × 1.05	V <sub>CU1,2</sub> × 1.11	V <sub>CU1,2</sub> × 1.17	V	1, 2	1
Overcharge release voltage 1, 2	V <sub>CD1,2</sub>	3.60 to 4.60 V, Adjustable	V <sub>CD1,2</sub> - 0.070	V <sub>CD1,2</sub>	V <sub>CD1,2</sub> + 0.065	V	1, 2	1
Overdischarge detection voltage 1, 2	V <sub>DD1,2</sub>	1.70 to 2.60 V, Adjustable	V <sub>DD1,2</sub> - 0.100	V <sub>DD1,2</sub>	V <sub>DD1,2</sub> + 0.095	V	1, 2	1
Overdischarge release voltage 1, 2	V <sub>DU1,2</sub>	1.70 to 3.80 V, Adjustable	V <sub>DU1,2</sub> - 0.120	V <sub>DU1,2</sub>	V <sub>DU1,2</sub> + 0.115	V	1, 2	1
Overcurrent detection voltage 1	V <sub>IOV1</sub>	0.07 to 0.30 V, Adjustable	V <sub>IOV1</sub> - 0.029	V <sub>IOV1</sub>	V <sub>IOV1</sub> + 0.029	V	3	1
Overcurrent detection voltage 2	V <sub>IOV2</sub>	Load short circuit, V <sub>CC</sub> reference	- 1.66	- 1.20	- 0.74	V	3	1
Temperature coefficient 1 for detection voltage *2	T <sub>COE1</sub>	Ta = - 40 to + 85 °C	- 0.6	0	0.6	mV/°C	—	—
Temperature coefficient 2 for detection voltage *3	T <sub>COE2</sub>	Ta = - 40 to + 85 °C	- 0.24	- 0.05	0	mV/°C	—	—
<b>[DELAY TIME (C3 = 0.22 μF)]</b>								
Overcharge detection delay time 1, 2	t <sub>CU1,2</sub>	1.0 s	0.60	1.00	1.84	s	8, 9	5
Overdischarge detection delay time 1, 2	t <sub>DD1,2</sub>	0.1 s	67	100	140	ms	8, 9	5
Overcurrent detection delay time 1	t <sub>IOV1</sub>	0.01 s	6.5	10	14.5	ms	10	5
<b>[INPUT VOLTAGE]</b>								
Input voltage between VCC and VSS	V <sub>DS</sub>	Absolute maximum rating	- 0.3	—	18	V	—	—
<b>[OPERATING VOLTAGE]</b>								
Operating voltage between VCC and VSS *4	V <sub>DSOP</sub>	Output logic fixed	2.0	—	16	V	—	—
<b>[CURRENT CONSUMPTION]</b>								
Current consumption during normal operation	I <sub>OPe</sub>	V1 = V2 = 3.6 V	1.9	7.5	13.8	μA	4	2
Current consumption at power down	I <sub>PON</sub>	V1 = V2 = 1.5 V	0	0.0002	0.06	μA	4	2
<b>[OUTPUT VOLTAGE]</b>								
DO voltage "H"	V <sub>DO(H)</sub>	I <sub>OUT</sub> = 10 μA	V <sub>CC</sub> - 0.14	V <sub>CC</sub> - 0.003	V <sub>CC</sub>	V	6	3
DO voltage "L"	V <sub>DO(L)</sub>	I <sub>OUT</sub> = 10 μA	V <sub>SS</sub>	V <sub>SS</sub> + 0.003	V <sub>SS</sub> + 0.14	V	6	3
CO voltage "H"	V <sub>CO(H)</sub>	I <sub>OUT</sub> = 10 μA	V <sub>CC</sub> - 0.24	V <sub>CC</sub> - 0.019	V <sub>CC</sub>	V	7	4
<b>[CO PIN INTERNAL RESISTANCE]</b>								
Resistance between VSS and CO	R <sub>COL</sub>	V <sub>CC</sub> - V <sub>SS</sub> = 9.4 V	0.24	0.6	1.96	MΩ	7	4
<b>[INTERNAL RESISTANCE]</b>								
Resistance between VCC and VM	R <sub>VCM</sub>	V <sub>CC</sub> - V <sub>VM</sub> = 0.5 V	86	240	785	kΩ	5	2
Resistance between VSS and VM	R <sub>VSM</sub>	V <sub>VM</sub> - V <sub>SS</sub> = 1.1 V	418	597	1332	kΩ	5	2
<b>[0 V BATTERY CHARGE FUNCTION]</b>								
0 V battery charge starting charger voltage	V <sub>OCHA</sub>	0 V battery charging function "available"	0.29	0.75	1.21	V	11	6
0 V battery charge inhibition battery voltage 1, 2	V <sub>OINH1,2</sub>	0 V battery charging function "unavailable"	0.23	0.88	1.53	V	12, 13	6

- \*1. Auxiliary overcharge detection voltage is equal to the overcharge detection voltage times 1.11 for the products without overcharge hysteresis, and times 1.25 for other products.
- \*2. Temperature coefficient 1 for detection voltage should be applied to overcharge detection voltage, overcharge release voltage, overdischarge detection voltage, and overdischarge release voltage.
- \*3. Temperature coefficient 2 for detection voltage should be applied to overcurrent detection voltage.
- \*4. The DO pin and CO pin logic are established at the operating voltage.



# BATTERY PROTECTION IC FOR 2-SERIAL-CELL PACK S-8232 Series

Rev.5.4\_00

**Table 7**

(Ta = -40 to +85 °C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
<b>[DETECTION VOLTAGE]</b>								
Overcharge detection voltage 1, 2	V <sub>CU1,2</sub>	3.85 to 4.60 V, Adjustable	V <sub>CU1,2</sub> - 0.055	V <sub>CU1,2</sub>	V <sub>CU1,2</sub> + 0.045	V	1, 2	1
Auxiliary overcharge detection voltage 1, 2 *1 V <sub>CUaux1</sub> , V <sub>CUaux2</sub> = V <sub>CU1</sub> , V <sub>CU2</sub> × 1.25 or V <sub>CUaux1</sub> , V <sub>CUaux2</sub> = V <sub>CU1</sub> , V <sub>CU2</sub> × 1.11	V <sub>CUaux1,2</sub>	V <sub>CU1,2</sub> × 1.25	V <sub>CU1,2</sub> × 1.19	V <sub>CU1,2</sub> × 1.25	V <sub>CU1,2</sub> × 1.31	V	1, 2	1
	V <sub>CUaux1,2</sub>	V <sub>CU1,2</sub> × 1.11	V <sub>CU1,2</sub> × 1.05	V <sub>CU1,2</sub> × 1.11	V <sub>CU1,2</sub> × 1.17	V	1, 2	1
Overcharge release voltage 1, 2	V <sub>CD1,2</sub>	3.60 to 4.60 V, Adjustable	V <sub>CD1,2</sub> - 0.080	V <sub>CD1,2</sub>	V <sub>CD1,2</sub> + 0.070	V	1, 2	1
Overdischarge detection voltage 1, 2	V <sub>DD1,2</sub>	1.70 to 2.60 V, Adjustable	V <sub>DD1,2</sub> - 0.110	V <sub>DD1,2</sub>	V <sub>DD1,2</sub> + 0.100	V	1, 2	1
Overdischarge release voltage 1, 2	V <sub>DU1,2</sub>	1.70 to 3.80 V, Adjustable	V <sub>DU1,2</sub> - 0.130	V <sub>DU1,2</sub>	V <sub>DU1,2</sub> + 0.120	V	1, 2	1
Overcurrent detection voltage 1	V <sub>IOV1</sub>	0.07 to 0.30 V, Adjustable	V <sub>IOV1</sub> - 0.033	V <sub>IOV1</sub>	V <sub>IOV1</sub> + 0.033	V	3	1
Overcurrent detection voltage 2	V <sub>IOV2</sub>	Load short circuit, V <sub>CC</sub> reference	-1.70	-1.20	-0.71	V	3	1
Temperature coefficient 1 for detection voltage *2	T <sub>COE1</sub>	Ta = -40 to +85 °C	-0.6	0	0.6	mV/°C	—	—
Temperature coefficient 2 for detection voltage *3	T <sub>COE2</sub>	Ta = -40 to +85 °C	-0.24	-0.05	0	mV/°C	—	—
<b>[DELAY TIME (C3 = 0.22 μF)]</b>								
Overcharge detection delay time 1, 2	t <sub>CU1,2</sub>	1.0 s	0.55	1.00	2.06	s	8, 9	5
Overdischarge detection delay time 1, 2	t <sub>DD1,2</sub>	0.1 s	67	100	141	ms	8, 9	5
Overcurrent detection delay time 1	t <sub>IOV1</sub>	0.01 s	6.3	10	14.7	ms	10	5
<b>[INPUT VOLTAGE]</b>								
Input voltage between VCC and VSS	V <sub>DS</sub>	Absolute maximum rating	-0.3	—	18	V	—	—
<b>[OPERATING VOLTAGE]</b>								
Operating voltage between VCC and VSS *4	V <sub>DSOP</sub>	Output logic fixed	2.0	—	16	V	—	—
<b>[CURRENT CONSUMPTION]</b>								
Current consumption during normal operation	I <sub>OPe</sub>	V1 = V2 = 3.6 V	1.8	7.5	14.2	μA	4	2
Current consumption at power down	I <sub>PON</sub>	V1 = V2 = 1.5 V	0	0.0002	0.10	μA	4	2
<b>[OUTPUT VOLTAGE]</b>								
DO voltage "H"	V <sub>DO(H)</sub>	I <sub>OUT</sub> = 10 μA	V <sub>CC</sub> - 0.17	V <sub>CC</sub> - 0.003	V <sub>CC</sub>	V	6	3
DO voltage "L"	V <sub>DO(L)</sub>	I <sub>OUT</sub> = 10 μA	V <sub>SS</sub>	V <sub>SS</sub> + 0.003	V <sub>SS</sub> + 0.17	V	6	3
CO voltage "H"	V <sub>CO(H)</sub>	I <sub>OUT</sub> = 10 μA	V <sub>CC</sub> - 0.27	V <sub>CC</sub> - 0.019	V <sub>CC</sub>	V	7	4
<b>[CO PIN INTERNAL RESISTANCE]</b>								
Resistance between VSS and CO	R <sub>COL</sub>	V <sub>CC</sub> - V <sub>SS</sub> = 9.4 V	0.22	0.6	2.20	MΩ	7	4
<b>[INTERNAL RESISTANCE]</b>								
Resistance between VCC and VM	R <sub>VCM</sub>	V <sub>CC</sub> - V <sub>VM</sub> = 0.5 V	79	240	878	kΩ	5	2
Resistance between VSS and VM	R <sub>VSM</sub>	V <sub>VM</sub> - V <sub>SS</sub> = 1.1 V	387	597	1491	kΩ	5	2
<b>[0 V BATTERY CHARGE FUNCTION]</b>								
0 V battery charge starting charger voltage	V <sub>OCHA</sub>	0 V battery charging function "available"	0.26	0.75	1.25	V	11	6
0 V battery charge inhibition battery voltage 1, 2	V <sub>OINH1,2</sub>	0 V battery charging function "unavailable"	0.20	0.88	1.57	V	12, 13	6

\*1. Auxiliary overcharge detection voltage is equal to the overcharge detection voltage times 1.11 for the products without overcharge hysteresis, and times 1.25 for other products.

\*2. Temperature coefficient 1 for detection voltage should be applied to overcharge detection voltage, overcharge release voltage, overdischarge detection voltage, and overdischarge release voltage.

\*3. Temperature coefficient 2 for detection voltage should be applied to overcurrent detection voltage.

\*4. The DO pin and CO pin logic are established at the operating voltage.

## ■ Test Circuits

### (1) Test Condition 1, Test Circuit 1

Set S1 = OFF, V1 = V2 = 3.6 V, and V3 = 0 V under normal condition. Increase V1 from 3.6 V gradually. The V1 voltage when CO = "L" is overcharge detection voltage 1 ( $V_{CU1}$ ). Decrease V1 gradually. The V1 voltage when CO = "H" is overcharge release voltage 1 ( $V_{CD1}$ ). Further decrease V1. The V1 voltage when DO = "L" is overdischarge voltage 1 ( $V_{DD1}$ ). Increase V1 gradually. The V1 voltage when DO = "H" is overdischarge release voltage 1 ( $V_{DU1}$ ). Set S1 = ON, and V1 = V2 = 3.6 V and V3 = 0 V under normal condition. Increase V1 from 3.6 V gradually. The V1 voltage when CO = "L" is auxiliary overcharge detection voltage 1 ( $V_{CUaux1}$ ).

### (2) Test Condition 2, Test Circuit 1

Set S1 = OFF, V1 = V2 = 3.6 V, and V3 = 0 V under normal condition. Increase V2 from 3.6 V gradually. The V2 voltage when CO = "L" is overcharge detection voltage 2 ( $V_{CU2}$ ). Decrease V2 gradually. The V2 voltage when CO = "H" is overcharge release voltage 2 ( $V_{CD2}$ ). Further decrease V2. The V2 voltage when DO = "L" is overdischarge voltage 2 ( $V_{DD2}$ ). Increase V2 gradually. The V2 voltage when DO = "H" is overdischarge release voltage 2 ( $V_{DU2}$ ). Set S1 = ON, and V1 = V2 = 3.6 V and V3 = 0 V under normal condition. Increase V2 from 3.6 V gradually. The V2 voltage when CO = "L" is auxiliary overcharge detection voltage 2 ( $V_{CUaux2}$ ).

### (3) Test Condition 3, Test Circuit 1

Set S1 = OFF, V1 = V2 = 3.6 V, and V3 = 0 V under normal condition. Increase V3 from 0 V gradually. The V3 voltage when DO = "L" is overcurrent detection voltage 1 ( $V_{IOV1}$ ). Set S1 = ON, V1 = V2 = 3.6 V, V3 = 0 V under normal condition. Increase V3 from 0 V gradually. (The voltage change rate < 1.0 V / ms) V3 – (V1 + V2) voltage when DO = "L" is overcurrent detection voltage 2 ( $V_{IOV2}$ ).

### (4) Test Condition 4, Test Circuit 2

Set S1 = ON, V1 = V2 = 3.6 V, and V3 = 0 V under normal condition and measure current consumption. Current consumption I1 is the normal condition current consumption ( $I_{OPE}$ ). Set S1 = OFF, V1 = V2 = 1.5 V under overdischarge condition and measure current consumption. Current consumption I1 is the power-down current consumption ( $I_{PDN}$ ).

### (5) Test Condition 5, Test Circuit 2

Set S1 = ON, V1 = V2 = V3 = 1.5 V, and V3 = 2.5 V under overdischarge condition.  $(V1 + V2 - V3) / I2$  is the internal resistance between VCC and VM (RVCM).

Set S1 = ON, V1 = V2 = 3.6 V, and V3 = 1.1 V under overcurrent condition.  $V3 / I2$  is the internal resistance between VSS and VM (RVSM).

### (6) Test Condition 6, Test Circuit 3

Set S1 = ON, S2 = OFF, V1 = V2 = 3.6 V, and V3 = 0 V under normal condition. Increase V4 from 0 V gradually. The V4 voltage when I1 = 10  $\mu$ A is DO voltage "H" ( $V_{DO(H)}$ ).

Set S1 = OFF, S2 = ON, V1 = V2 = 3.6 V, and V3 = 0.5 V under overcurrent condition. Increase V5 from 0 V gradually. The V5 voltage when I2 = 10  $\mu$ A is the DO voltage "L" ( $V_{DO(L)}$ ).

**(7) Test Condition 7, Test Circuit 4**

Set S1 = ON, S2 = OFF, V1 = V2 = 3.6 V and V3 = 0 V under normal condition. Increase V4 from 0 V gradually. The V4 voltage when I1 = 10  $\mu$ A is the CO "H" voltage ( $V_{CO(H)}$ ).

Set S1 = OFF, S2 = ON, V1 = V2 = 4.7, V3 = 0 V, and V5 = 9.4 V under over voltage condition. (V5) / I2 is the CO pin internal resistance (RCO(L)).

**(8) Test Condition 8, Test Circuit 5**

Set V1 = V2 = 3.6 V, and V3 = 0 V under normal condition. Increase V1 from ( $V_{CU1} - 0.2$  V) to ( $V_{CU1} + 0.2$  V) immediately (within 10  $\mu$ s). The time after V1 becomes ( $V_{CU1} + 0.2$  V) until CO goes "L" is the overcharge detection delay time 1 ( $t_{CU1}$ ).

Set V1 = V2 = 3.6 V, and V3 = 0 V under normal condition. Decrease V1 from ( $V_{DD1} + 0.2$  V) to ( $V_{DD1} - 0.2$  V) immediately (within 10  $\mu$ s). The time after V1 becomes ( $V_{DD1} - 0.2$  V) until DO goes "L" is the overdischarge detection delay time 1 ( $t_{DD1}$ ).

**(9) Test Condition 9, Test Circuit 5**

Set V1 = V2 = 3.6 V, and V3 = 0 V under normal condition. Increase V2 from ( $V_{CU2} - 0.2$  V) to ( $V_{CU2} + 0.2$  V) immediately (within 10  $\mu$ s). The time after V2 becomes ( $V_{CU2} + 0.2$  V) until CO goes "L" is the overcharge detection delay time 2 ( $t_{CU2}$ ).

Set V1 = V2 = 3.6 V, and V3 = 0 V under normal condition. Decrease V2 from ( $V_{DD2} + 0.2$  V) to ( $V_{DD2} - 0.2$  V) immediately (within 10  $\mu$ s). The time after V2 becomes ( $V_{DD2} - 0.2$  V) until DO goes "L" is the overdischarge detection delay time 2 ( $t_{DD2}$ ).

**(10) Test Condition 10, Test Circuit 5**

Set V1 = V2 = 3.6 V, and V3 = 0 V under normal condition. Increase V3 from 0 V to 0.5 V immediately (within 10  $\mu$ s). The time after V3 becomes 0.5 V until DO goes "L" is the overcurrent detection delay time 1 ( $t_{OV1}$ ).

**(11) Test Condition 11, Test Circuit 6**

Set V1 = V2 = 0 V, and V3 = 0 V, and increase V3 gradually. The V3 voltage when CO = "L" ( $V_{VM} + 0.3$  V or higher) is the 0 V charge starting voltage ( $V_{0CHA}$ ).

**(12) Test Condition 12, Test Circuit 6**

Set V1 = 0 V, V2 = 3.6 V, and V3 = 12 V, and increase V1 gradually. The V1 voltage when CO = "H" ( $V_{VM} + 0.3$  V or higher) is the 0 V charge inhibiting voltage 1 ( $V_{0INH1}$ ).

**(13) Test Condition 13, Test Circuit 6**

Set V1 = 3.6 V, V2 = 0 V, and V3 = 12 V, and increase V2 gradually. The V2 voltage when CO = "H" ( $V_{VM} + 0.3$  V or higher) is the 0 V charge inhibiting voltage 2 ( $V_{0INH2}$ ).

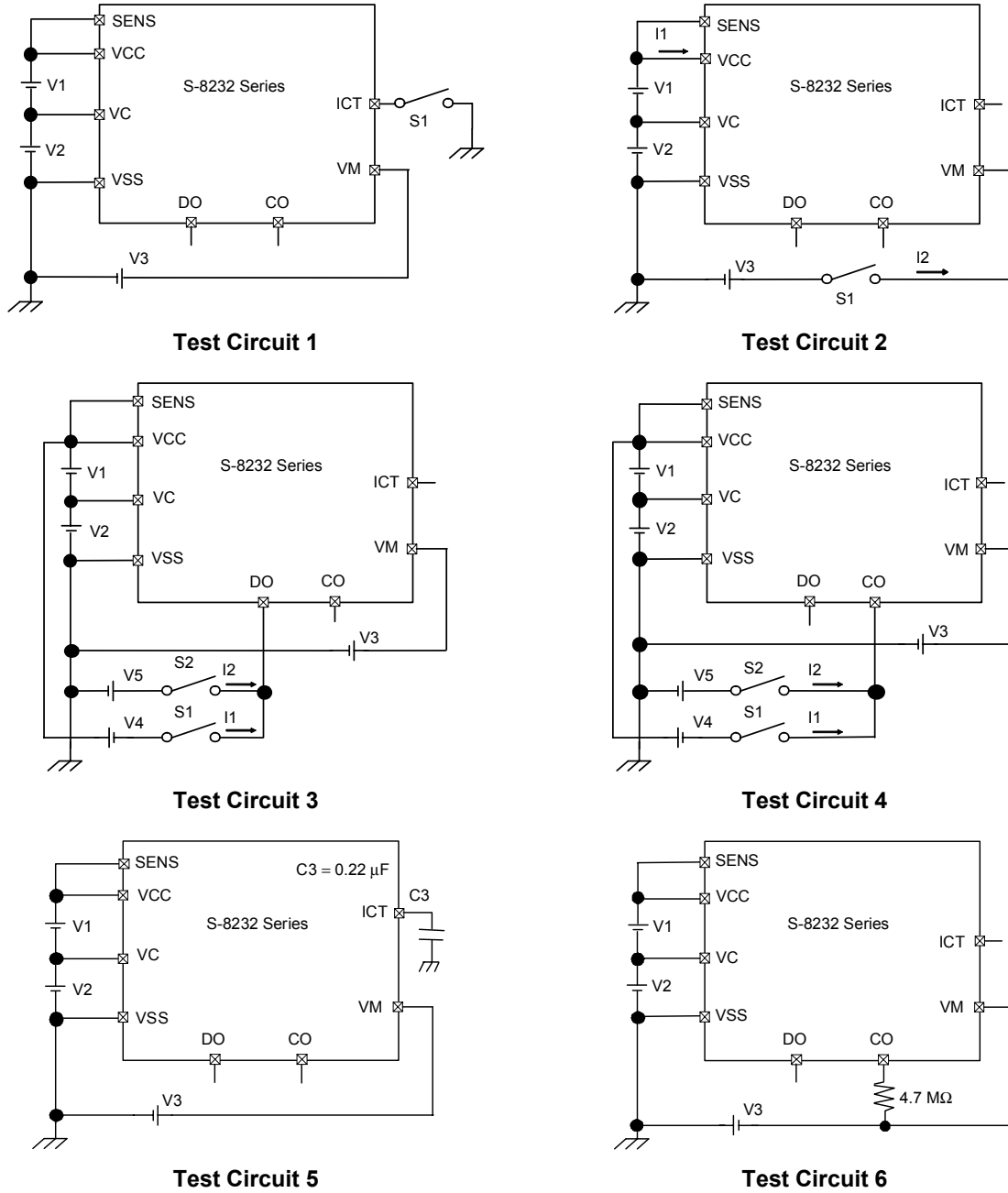


Figure 4

## ■ Operation

### Normal Condition <sup>\*1, \*2</sup>

This IC monitors the voltages of the two serially connected batteries and the discharge current to control charging and discharging. When the voltages of two batteries are in the range from the overdischarge detection voltage ( $V_{DD1,2}$ ) to the overcharge detection voltage ( $V_{CU1,2}$ ), and the current flowing through the batteries becomes equal or lower than a specified value (the VM pin voltage is equal or lower than overcurrent detection voltage 1), the charging and discharging FETs are turned on. In this condition, charging and discharging can be carried out freely. This condition is called normal condition. In this condition, the VM and VSS pins are shorted by the RVSM resistor.

### Overcurrent Condition

When the discharging current becomes equal to or higher than a specified value (the VM pin voltage is equal to or higher than the overcurrent detection voltage) during discharging under normal condition and it continues for the overcurrent detection delay time ( $t_{IOV}$ ) or longer, the discharging FET is turned off to stop discharging. This condition is called overcurrent condition. The VM and VSS pins are shorted by the RVSM resistor at this time. The charging FET is also turned off. When the discharging FET is off and a load is connected, the VM pin voltage equals the  $V_{CC}$  potential.

The overcurrent condition returns to the normal condition when the load is released and the impedance between the EB- and EB+ pins (refer to the **Figure 8**) is 200 M $\Omega$  or higher. When the load is released, the VM pin, which is shorted to the VSS pin with the RVSM resistor, goes back to the  $V_{SS}$  potential. The IC detects that the VM pin potential returns to overcurrent detection voltage 1 ( $V_{IOV1}$ ) or lower and returns to the normal condition.

### Overcharge Condition

Following two cases are detected as overcharge conditions :

- (1) If one of the battery voltages becomes higher than the overcharge detection voltage ( $V_{CU1,2}$ ) during charging under normal condition and it continues for the overcharge detection delay time ( $t_{CU1,2}$ ) or longer, the charging FET turns off to stop charging.
- (2) If one of the battery voltages becomes higher than the auxiliary overcharge detection voltage ( $V_{CUaux1,2}$ ) the charging FET turns off immediately to stop charging. The VM and VSS pins are shorted by the RVSM resistor under the overcharge condition.

The auxiliary overcharge detection voltages ( $V_{CUaux1,2}$ ) are correlated with the overcharge detection voltages ( $V_{CU1,2}$ ) and are defined by following equations :

$$V_{CUaux1,2} [V] = 1.25 \times V_{CU1,2} [V]$$

$$\text{or for no overcharge hysteresis type } (V_{CU1,2} = V_{CD1,2}) \quad V_{CUaux1,2} [V] = 1.11 \times V_{CU1,2} [V]$$

The overcharge condition is released in two cases :

- (1) The battery voltage which exceeded the overcharge detection voltage ( $V_{CU1,2}$ ) falls below the overcharge release voltage ( $V_{CD1,2}$ ), the charging FET turns on and the normal condition returns.
- (2) If the battery voltage which exceeded the overcharge detection voltage ( $V_{CU1,2}$ ) is equal or higher than the overcharge release voltage ( $V_{CD1,2}$ ), but the charger is removed, a load is placed, and discharging starts, the charging FET turns on and the normal condition returns.

The release mechanism is as follows : the discharge current flows through an internal parasitic diode of the charging FET immediately after a load is installed and discharging starts, and the VM pin voltage increases by about 0.6 V from the VSS pin voltage momentarily. The IC detects this voltage (overcurrent detection voltage 1 or higher), releases the overcharge condition and returns to the normal condition.

### Overdischarge Condition

If any one of the battery voltages falls below the overdischarge detection voltage ( $V_{DD1,2}$ ) during discharging under normal condition and it continues for the overdischarge detection delay time ( $t_{DD1,2}$ ) or longer, the discharging FET turns off and discharging stops. This condition is called the overdischarge condition. When the discharging FET turns off, the VM pin voltage becomes equal to the  $V_{CC}$  voltage and the IC's current consumption falls below the power-down current consumption ( $I_{PDN}$ ). This condition is called the power-down condition. The VM and VCC pins are shorted by the RVCM resistor under the overdischarge and power-down conditions.

The power-down condition is canceled when the charger is connected and the voltage between VM and VCC is overcurrent detection voltage 2 or higher. When all the battery voltages becomes equal to or higher than the overdischarge release voltage ( $V_{DU1,2}$ ) in this condition, the overdischarge condition changes to the normal condition.

**Delay Circuit**

The overcharge detection delay time ( $t_{CU1, 2}$ ), the overdischarge detection delay time ( $t_{DD1, 2}$ ), and the overcurrent detection delay time 1 ( $t_{IOV1}$ ) change with an external capacitor (C3). Since one capacitor determine each delay time, delay times are correlated by the following ratio :

Overcharge delay time : Overdischarge delay time : Overcurrent delay time = 100 : 10 : 1

The delay times are calculated by the following equations : ( $T_a = -40$  to  $+85$  °C)

		Min.,	Typ.,	Max.
Overcharge detection delay time $t_{CU}$ [s] = Delay factor	( 2.500,	4.545,	9.364 )	$\times C3$ [ $\mu$ F]
Overdischarge detection delay time $t_{DD}$ [s] = Delay factor	( 0.3045,	0.4545,	0.6409 )	$\times C3$ [ $\mu$ F]
Overcurrent detection delay time $t_{IOV1}$ [s] = Delay factor	( 0.02864,	0.04545,	0.06682 )	$\times C3$ [ $\mu$ F]

**Remark** The delay time for overcurrent detection 2 is fixed by an internal circuit. The delay time cannot be changed via an external capacitor.

**0 V Battery Charging Function \*3**

This function is used to recharge both of two serially-connected batteries after they self-discharge to 0 V. When the 0 V charging start voltage ( $V_{0CHA}$ ) or higher is applied to between VM and VCC by connecting the charger, the charging FET gate is fixed to  $V_{CC}$  potential.

When the voltage between the gate and the source of the charging FET becomes equal to or higher than the turn-on voltage by the charger voltage, the charging FET turns on to start charging. At this time, the discharging FET turns off and the charging current flows through the internal parasitic diode in the discharging FET. If all the battery voltages become equal to or higher than the overdischarge release voltage ( $V_{DU1, 2}$ ), the normal condition returns.

**0 V Battery Charge Inhibiting Function \*3**

This function is used for inhibiting charging when either of the connected batteries goes 0 V due to its self-discharge. When the voltage of either of the connected batteries goes below 0 V charge inhibit voltage 1 and 2 ( $V_{0INH1, 2}$ ), the charging FET gate is fixed to "EB-" to inhibit charging. Charging is possible only when the voltage of both connected batteries goes 0 V charge inhibit voltage 1 and 2 ( $V_{0INH1, 2}$ ) or more.

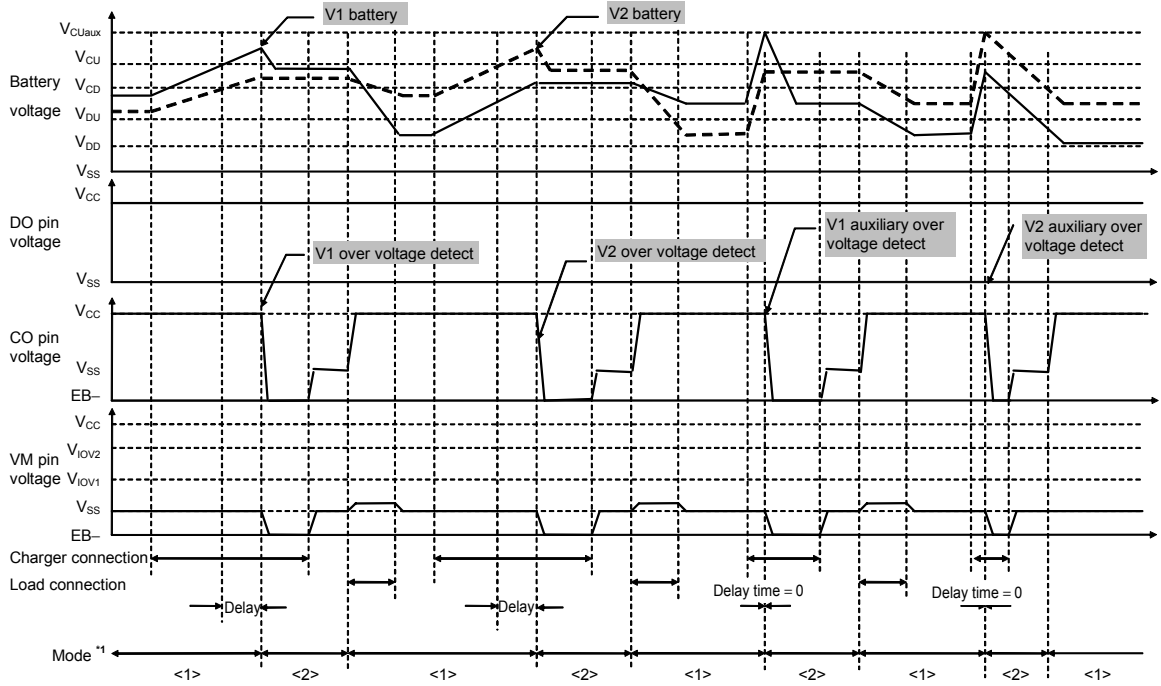
Note that charging may be possible when the total voltage of both connected batteries is less than the minimum value ( $V_{DSOPmin}$ ) of the operating voltage between VCC and VSS even if the voltage of either of the connected batteries is 0 V charge inhibit voltage 1 and 2 ( $V_{0INH1, 2}$ ) or less. Charging is prohibited when the total voltage of both connected batteries reaches the minimum value ( $V_{DSOPmin}$ ) of the operating voltage between VCC and VSS.

When using this optional function, a resistor of 4.7 M $\Omega$  is needed between the gate and the source of the charging control FET (refer to the **Figure 8**).

- \*1. When initially connecting batteries, the IC may fail to enter the normal condition (discharging ready state). If so, once set the VM pin to VSS voltage (short pins VM and VSS or connect a charger).
- \*2. The products indicated with \*4 of the **2. Product Name List** in the "**■ Product Name Structure**" are set to "overcharge detection / release hysteresis", "no final overcharge function", and "0 V battery charge inhibiting function." The following phenomena may be found, but there is no problem for practical use.  
 The product is an overcurrent condition due to overload connection when the battery voltage is overcharge release voltage ( $V_{CD1, 2}$ ) or more and overcharge detection voltage ( $V_{CU1, 2}$ ) or less. Usually, the IC returns to its normal condition when overload is removed under this condition. However, the charging FET may be turned OFF when overload is removed under this condition, leading to an overcharge condition. If so, attach load to start discharge. The charging FET is turned ON to return to the normal condition. Refer to the "**Overcharge condition**" in this section.
- \*3. Some lithium ion batteries are not recommended to be recharged after having been completely discharged. Please contact the battery manufacturer when you decide to select a 0 V battery charging function.

■ Timing Charts

1. Overcharge Detection

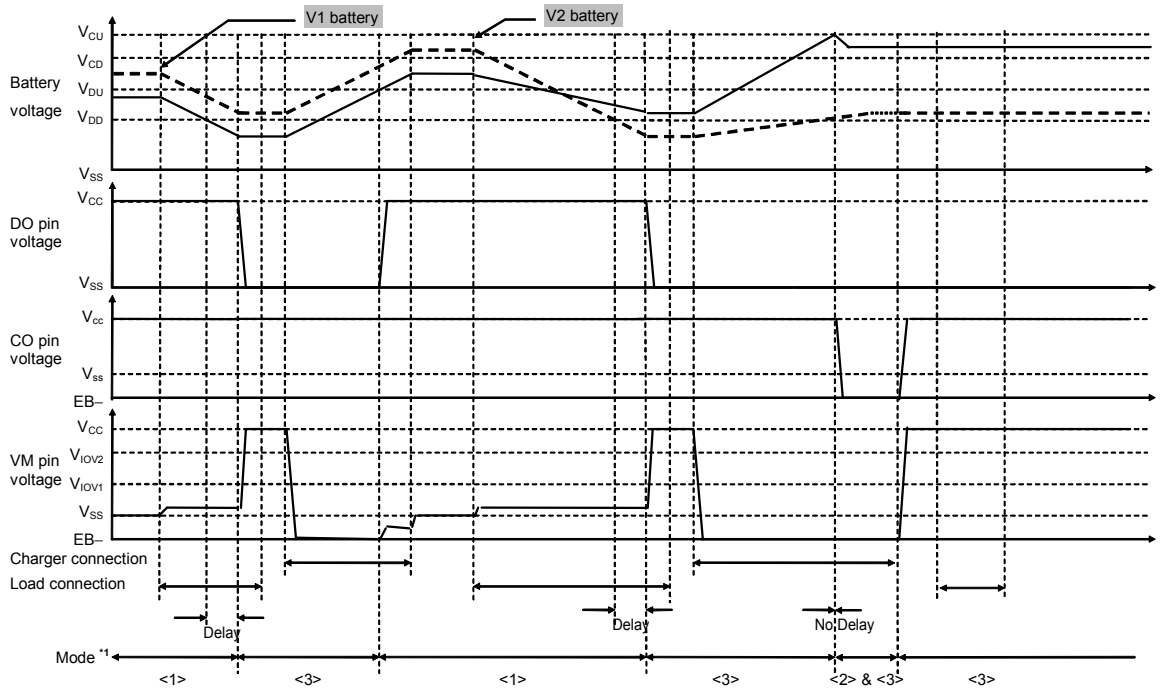


- \*1. <1> Normal mode
- <2> Over charge mode
- <3> Over discharge mode
- <4> Over current mode

**Remark** The charger is assumed to charge with a constant current.

Figure 5

**2. Overdischarge Detection**



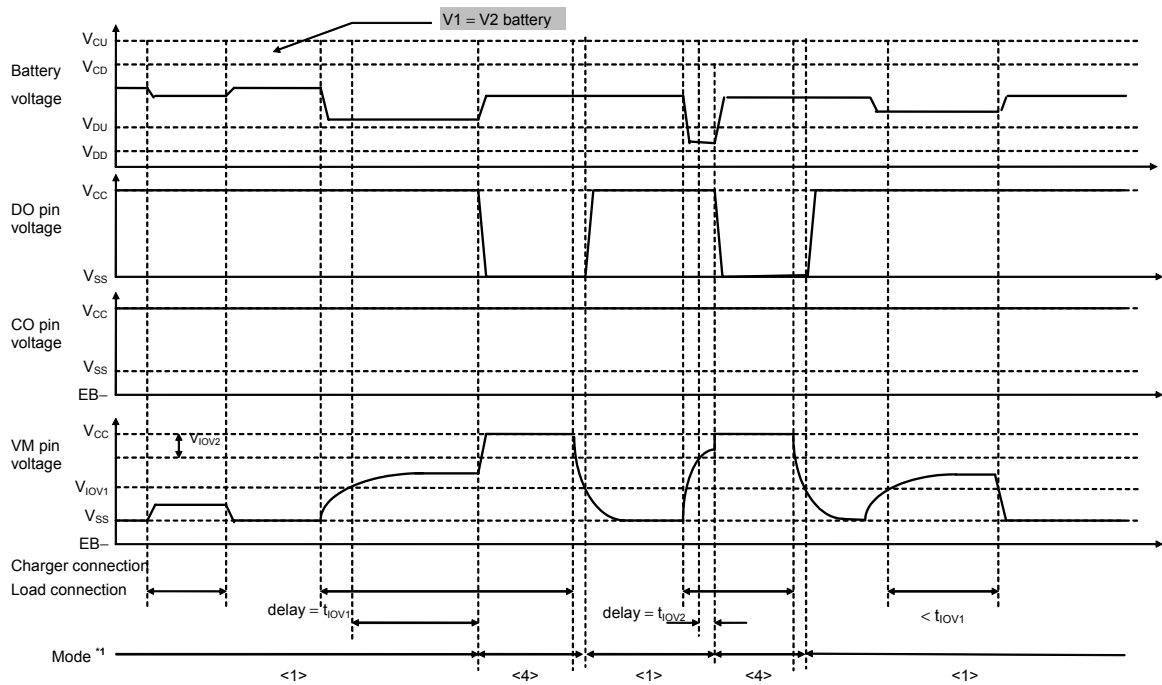
- \*1. <1> Normal mode
- <2> Over charge mode
- <3> Over discharge mode
- <4> Over current mode

**Remark** The charger is assumed to charge with a constant current.

**Figure 6**



3. Overcurrent Detection

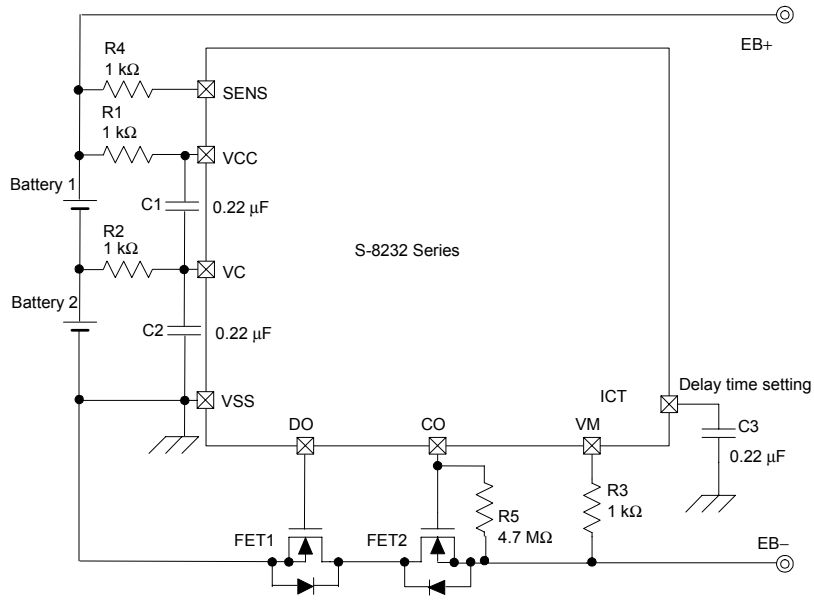


- \*1.  $\langle 1 \rangle$  Normal mode
- $\langle 2 \rangle$  Over charge mode
- $\langle 3 \rangle$  Over discharge mode
- $\langle 4 \rangle$  Over current mode

**Remark** The charger is assumed to charge with a constant current.

Figure 7

■ **Battery Protection IC Connection Example**



**Figure 8**

**Table 8 Constants for External Components**

Symbol	Parts	Purpose	Typ.	Min.	Max.	Remark
FET1	Nch MOS FET	Discharge control	—	—	—	—
FET2	Nch MOS FET	Charge control	—	—	—	—
R1	Chip resistor	ESD protection	1 kΩ	300 Ω	1 kΩ	—
C1	Chip capacitor	Filter	0.22 μF	0 μF	1 μF	—
R2	Chip resistor	ESD protection	1 kΩ	300 Ω	1 kΩ	—
C2	Chip capacitor	Filter	0.22 μF	0 μF	1 μF	—
R4	Chip resistor	ESD protection	1 kΩ	= R1 min.	= R1 max.	Same value as R1 and R2. <sup>*1</sup>
C3	Chip capacitor	Delay time setting	0.22 μF	0 μF	1 μF	Attention should be paid to leak current of C3. <sup>*2</sup>
R3	Chip resistor	Protection for charger reverse connection	1 kΩ	300 Ω	5 kΩ	Discharge can't be stopped at less than 300 Ω when a charger is reverse-connected. <sup>*3</sup>
R5	Chip resistor	0 V battery charging inhibition	(4.7 MΩ)	(1 MΩ)	(10 MΩ)	R5 should be added when the product has 0 V battery charge inhibition. Lower resistance increases current consumption. <sup>*4</sup>

<sup>\*1</sup>. R4 = R1 is required. Overcharge detection voltage increases by R4. For example 10 kΩ (R4) increases overcharge detection voltage by 20 mV.

<sup>\*2</sup>. The overcharge detection delay time ( $t_{CU}$ ), the overdischarge detection delay time ( $t_{CD}$ ), and the over current detection delay time ( $t_{IOV}$ ) change with the external capacitor C3. Refer to the “■ **Electrical Characteristics**”.

<sup>\*3</sup>. When the resistor R3 is set less than 300 Ω and a charger is reverse-connected, current which exceeds the power dissipation of the package will flow and the IC may break. But excessive R3 causes increase of overcurrent detection voltage 1 ( $V_{IOV1}$ ).  $V_{IOV1}$  changes to  $V_{IOV1} = (R3 + R_{VSM}) / R_{VSM} \times V_{IOV1}$ . For example, 50 kΩ resistor (R3) increases overcurrent detection voltage 1 ( $V_{IOV1}$ ) from 0.100 V to 0.113 V.

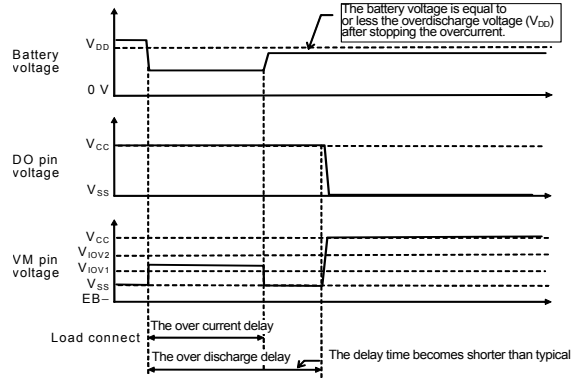
<sup>\*4</sup>. A 4.7 MΩ resistor is needed for R5 to inhibit 0 V battery charging. Current consumption increases when the R5 resistance is below 4.7 MΩ. R5 should be connected when the product has 0 V battery charging inhibition.

**Caution 1. The above constants may be changed without notice.**

**2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant do not guarantee proper operation. Perform through evaluation using the actual application to set the constant.**

■ **Precautions**

- After the overcurrent detection delay, if either one of battery voltages equals the overdischarge detection voltage ( $V_{DD1,2}$ ) or lower, the overdischarge detection delay time becomes shorter than 10ms (min.). It occurs because capacitor C3 sets all of delay times (refer to the **Figure 9**).



**Figure 9**

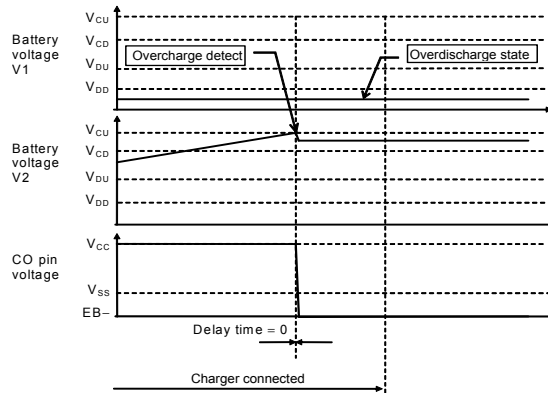
[Cause]

When overcurrent detection is released until  $t_{IOV1}$ , the capacitor C3 is charged by S-8232 Series. If all battery voltage is lower than  $V_{DD1,2}$  at that time, charging goes on. So delay time is shorter than typical.

[Conclusion]

This phenomenon occurs when all battery voltage is nearly equal to the overdischarge voltage ( $V_{DD1,2}$ ) after overcurrent detected. It means that the battery capacity is small and those must be charged in the future. Even if the state changes to overdischarge condition, the battery package capacity is same as typical.

- When one of the battery voltages is overdischarge detection voltage ( $V_{DD1,2}$ ) or lower and the other one becomes higher than the overcharge detection voltage ( $V_{CU1,2}$ ), the IC detects the overcharge without the overcharge detection delay time ( $t_{CU}$ ) (refer to the **Figure 10**).



**Figure 10**

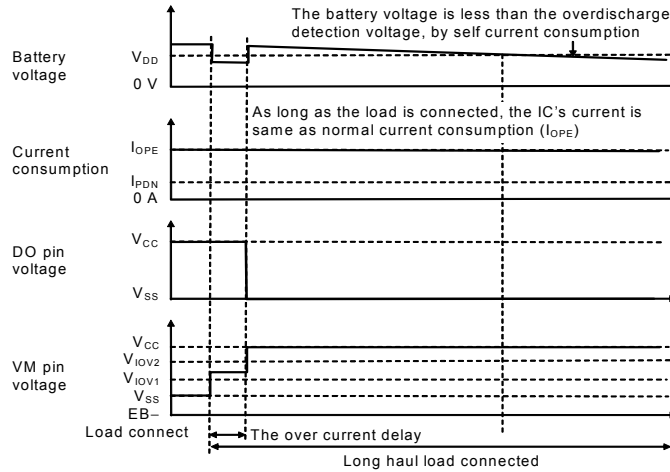
[Cause]

It is same as the overdischarge detection under the overcurrent condition. It occurs because capacitor C3 sets all of delay times.

[Conclusion]

This phenomenon occurs when one battery voltage is lower than overdischarge voltage ( $V_{DD1,2}$ ) and batteries are charged by charger. Since voltage difference between two batteries is large in this situation, the S-8232 Series immediately stops the charging of the other battery to reduce voltage difference. This action improves the safety of a battery pack and dose not do any harm to the pack.

- After the overcurrent detection, the load was connected for a long time, even if one of the battery voltage became lower than overdischarge detection voltage ( $V_{DD1, 2}$ ), the IC can't detect the overdischarge as long as the load is connected. Therefore the IC's current consumption at the one of the battery voltage is lower than the overdischarge detection voltage is same as normal condition current consumption ( $I_{OPE}$ ) (refer to the **Figure 11**).



**Figure 11**

[Cause]

The reason is as follows. If the overcurrent detection and overdischarge detection occur at same time, the overcurrent detection takes precedence the overdischarge detection. As long as the IC detects overcurrent, the IC can't detect overdischarge.

[Conclusion]

If the load is taken off at least one time, the overcurrent is released and the overdischarge detection works.

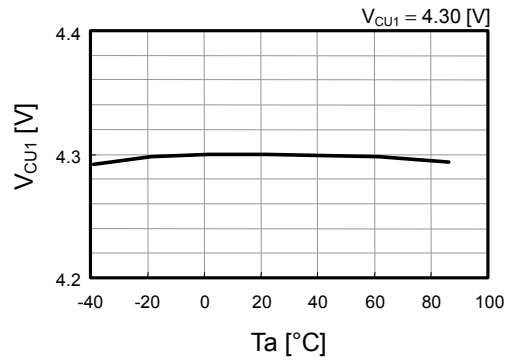
Unless keeping the IC with load for a long time, the reduction of battery voltage will be neglected, because of the IC's current consumption (typ. 7.5  $\mu$ A) is small.

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- SII claims no responsibility for any and all disputes arising out of or in connection with any infringement of the products including this IC upon patents owned by a third party.

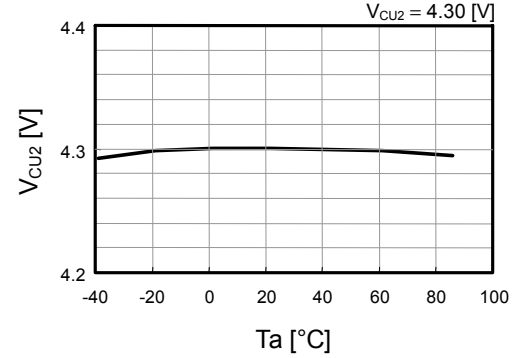
■ **Typical Characteristics**

**1. Detection Voltage Temperature Characteristics**

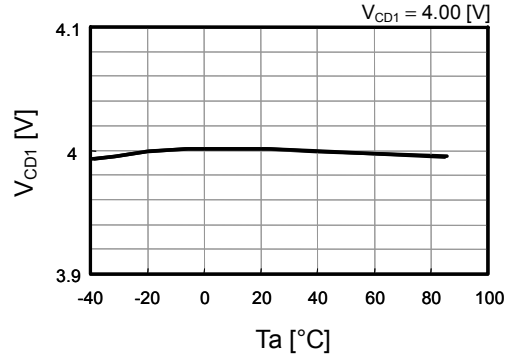
Overcharge detection voltage1 vs. temperature



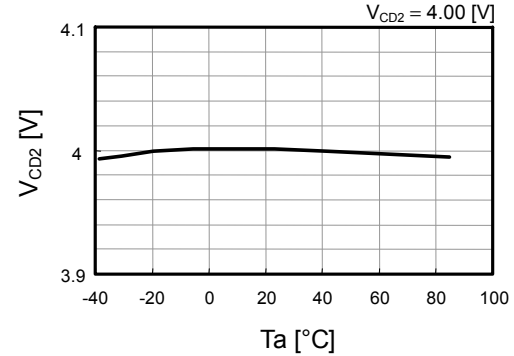
Overcharge detection voltage2 vs. temperature



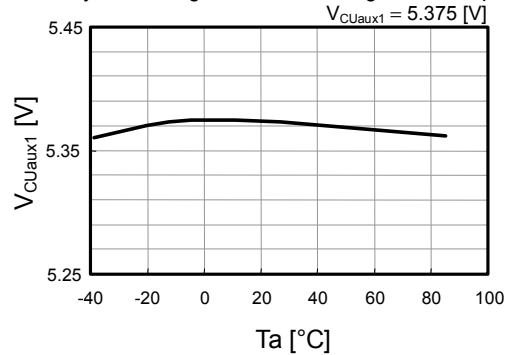
Overcharge release voltage1 vs. temperature



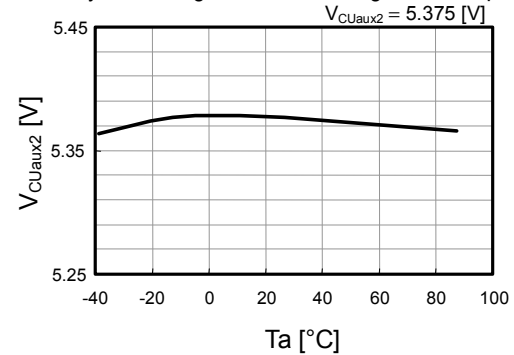
Overcharge release voltage2 vs. temperature

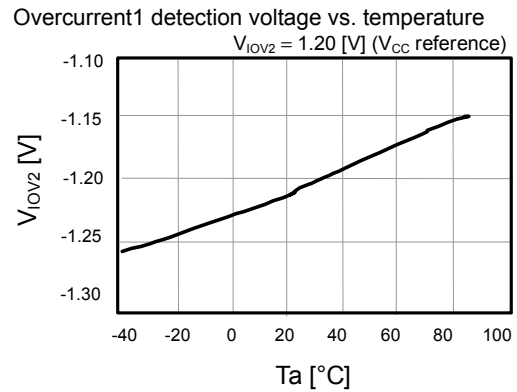
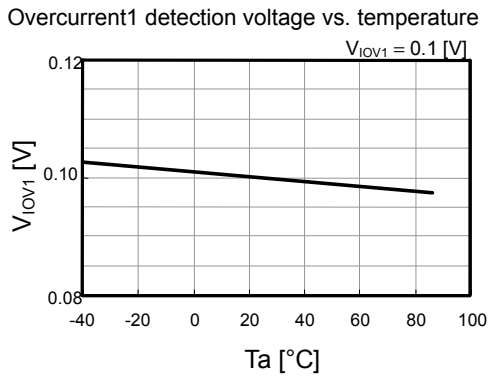
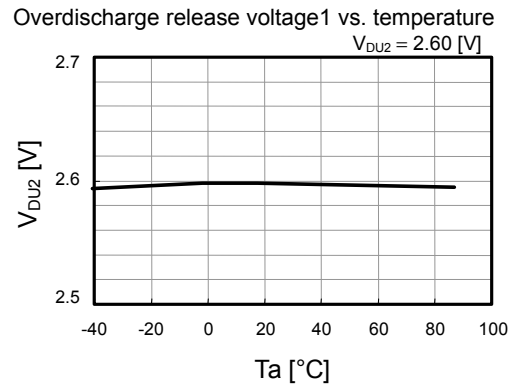
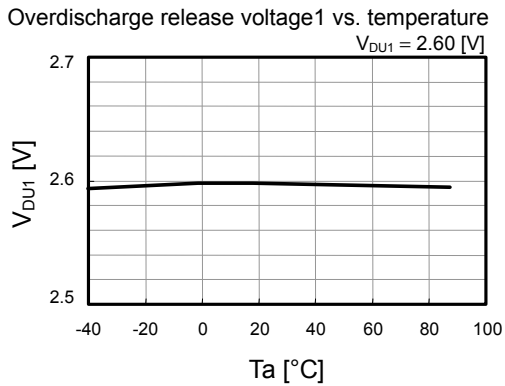
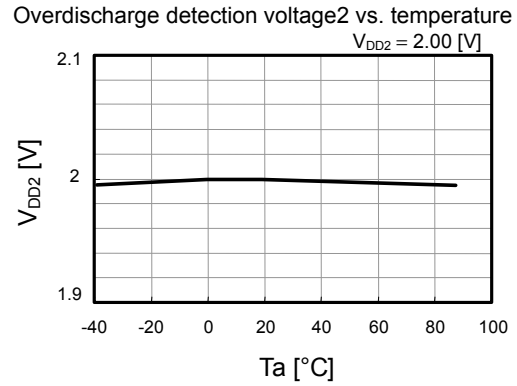
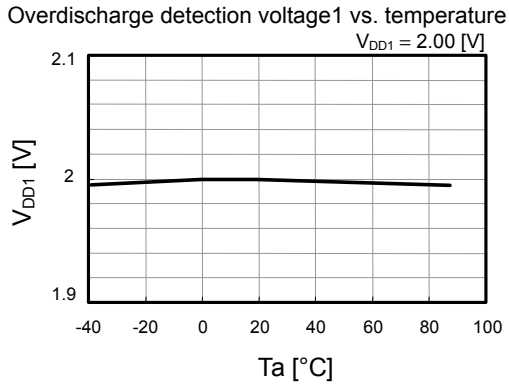


Auxiliary overcharge detection voltage1 vs. temperature



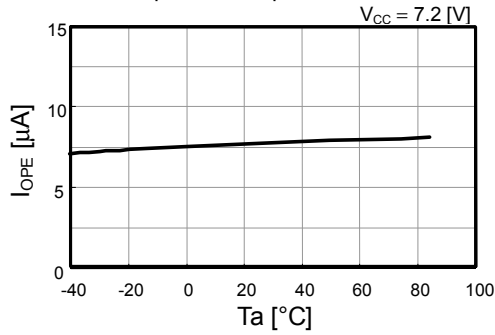
Auxiliary overcharge detection voltage2 vs. temperature



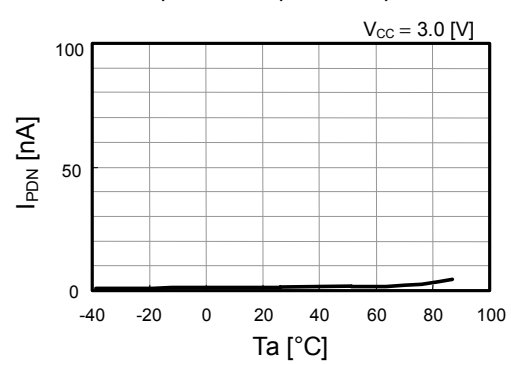


**2. Current Consumption Temperature Characteristics**

Current consumption vs. temperature in normal mode

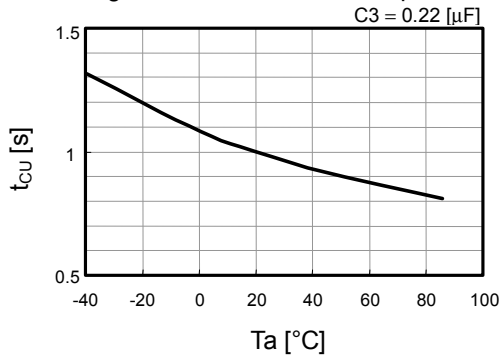


Current consumption vs. temperature in power-down mode

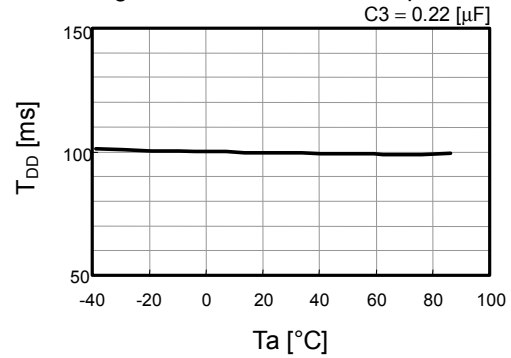


**3. Delay Time Temperature Characteristics**

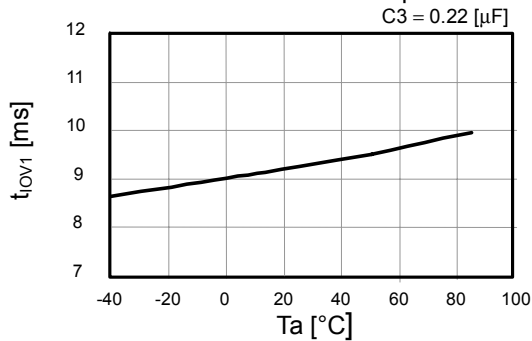
Overcharge detection1 time vs. temperature

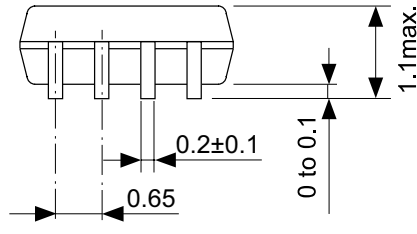
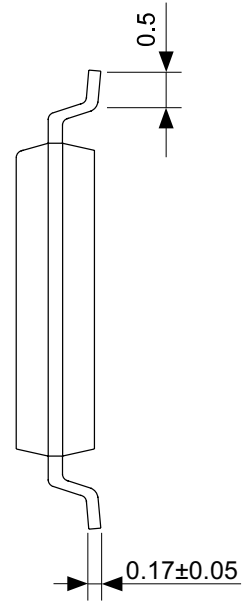
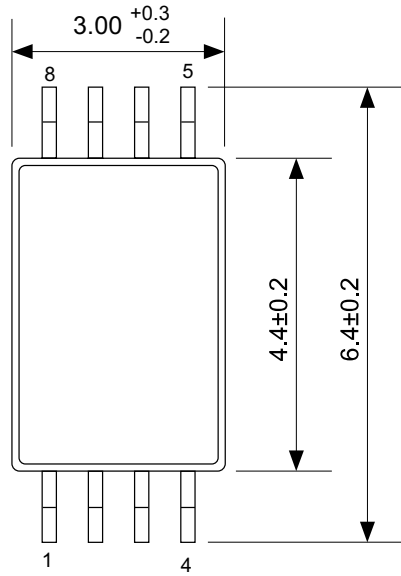


Overcharge detection1 time vs. temperature



Overcurrent1 detection time vs. temperature

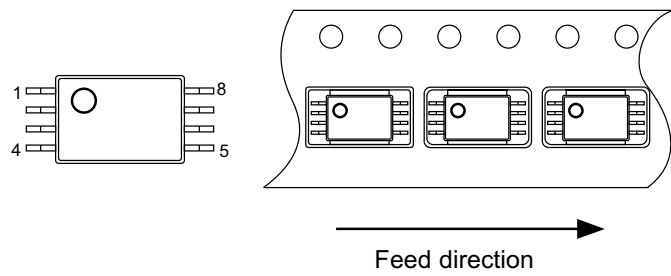
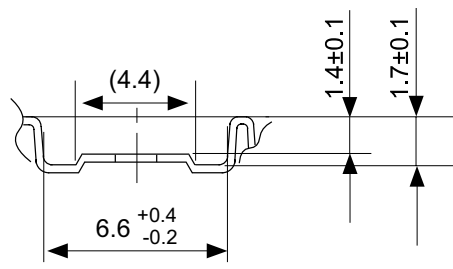
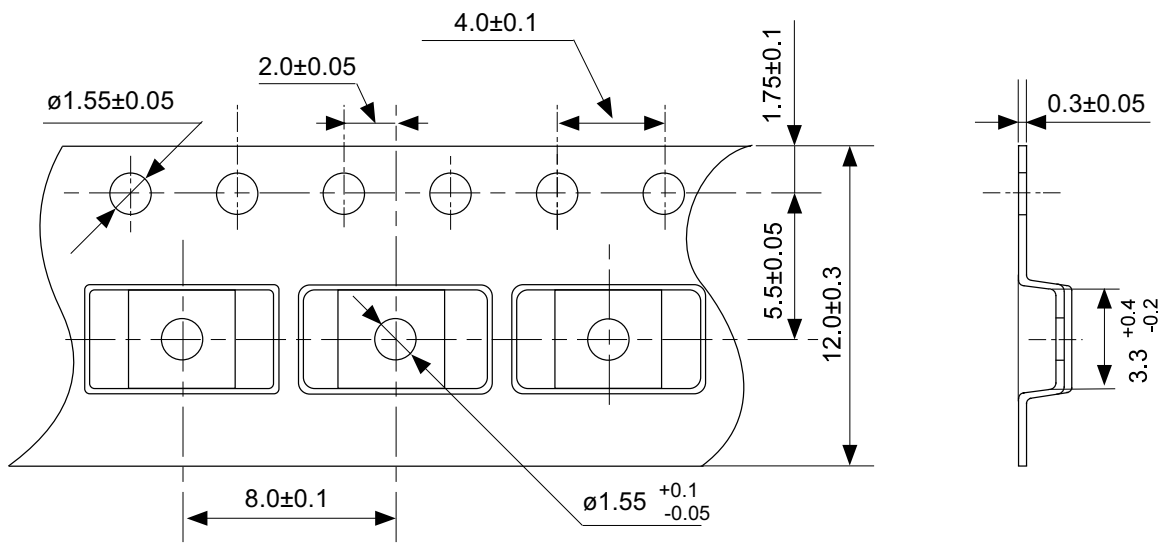




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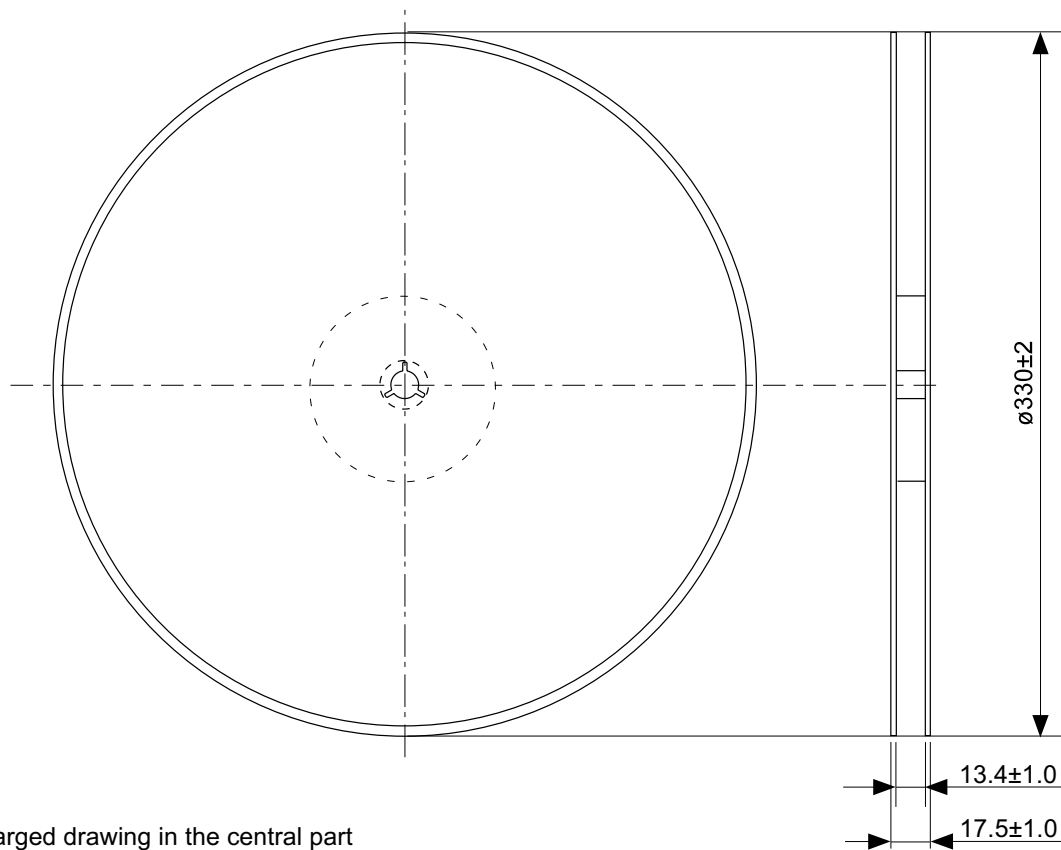
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No.	FT008-A-P-SD-1.1
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UNIT	mm
Seiko Instruments Inc.	



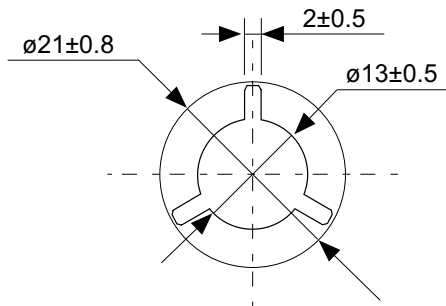


No. FT008-E-C-SD-1.0

TITLE	TSSOP8-E-Carrier Tape
No.	FT008-E-C-SD-1.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part



No. FT008-E-R-SD-1.0

TITLE	TSSOP8-E-Reel		
No.	FT008-E-R-SD-1.0		
SCALE		QTY.	3,000
UNIT	mm		
Seiko Instruments Inc.			

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