NCP1560

Full Featured Voltage Mode PWM Controller

The NCP1560 PWM controller contains all the features and flexibility needed to implement voltage−mode control in high performance single ended DC−DC converters. This device cost effectively reduces system part count with the inclusion of a high voltage startup regulator that operates over a wide input range of 21.5 V to 150 V. The NCP1560 provides two control outputs, OUT1 which controls the main PWM switch and OUT2 with adjustable overlap delay, which can control a synchronous rectifier switch or an active clamp/reset switch. Other distinctive features include: two mode over current protection, line under/overvoltage lockout, fast line feedforward, soft−start and a maximum duty cycle limit.

Features

- Minimum Operating Voltage of 21.5 V
- Internal High Voltage Startup Regulator
- Dual Control Outputs with Adjustable Overlap Delay
- Single Resistor Oscillator Frequency Setting
- Fast Line Feedforward
- Line Under/Overvoltage Lockout
- Dual Mode Overcurrent Protection
- Programmable Maximum Duty Cycle Control
- Maximum Duty Cycle Proportional to Line Voltage
- Programmable Soft−Start
- Precision 5.0 V Reference
- Pb−Free Package is Available*

Typical Applications

- Telecommunication Power Converters
- Industrial Power Converters
- High Voltage Power Modules
- +42 V Automotive Systems
- Control Driven Synchronous Rectifier Power Converters

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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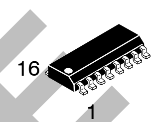
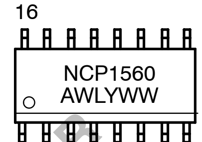


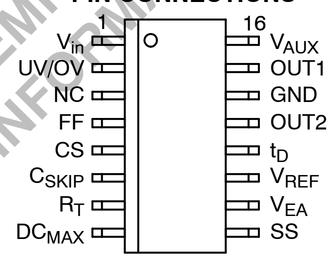
SO−16
D SUFFIX
CASE 751B

MARKING DIAGRAM



NCP1560 = Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCP1560HDR2	SO−16	2500/Tape & Reel
NCP1560HDR2G	SO−16 (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

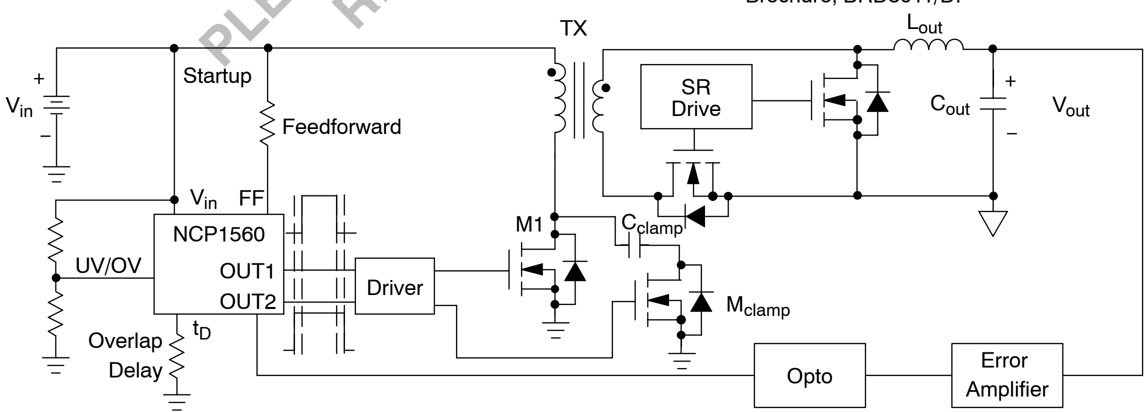


Figure 1. Active−Clamp Forward Converter

July, 2006 − Rev. 7

Publication Order Number
NCP1560/D

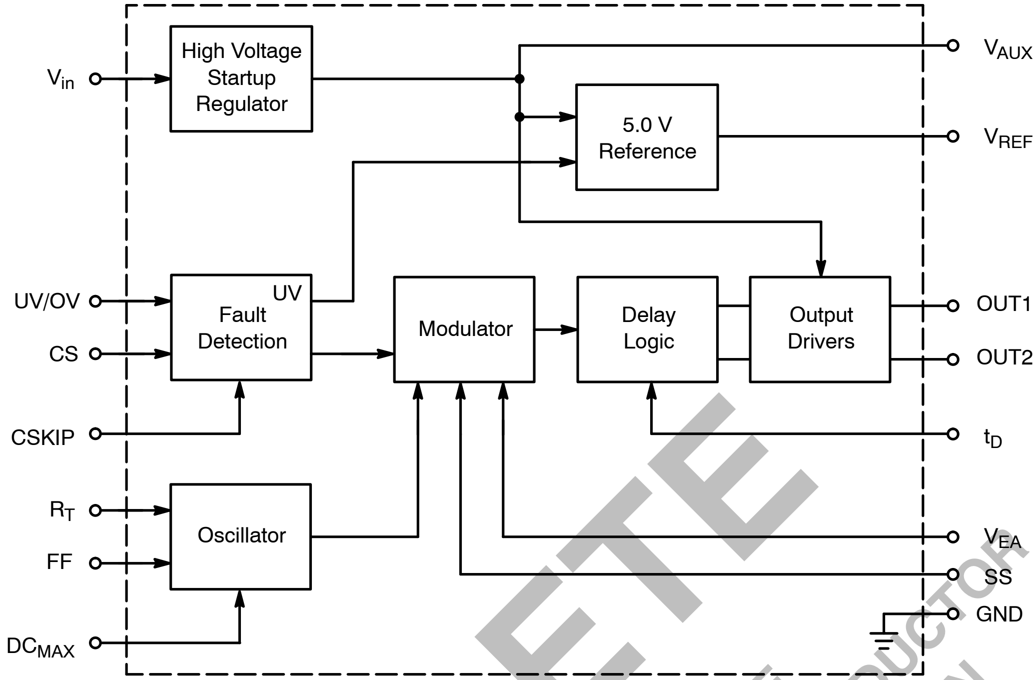


Figure 1. Simplified Block Diagram

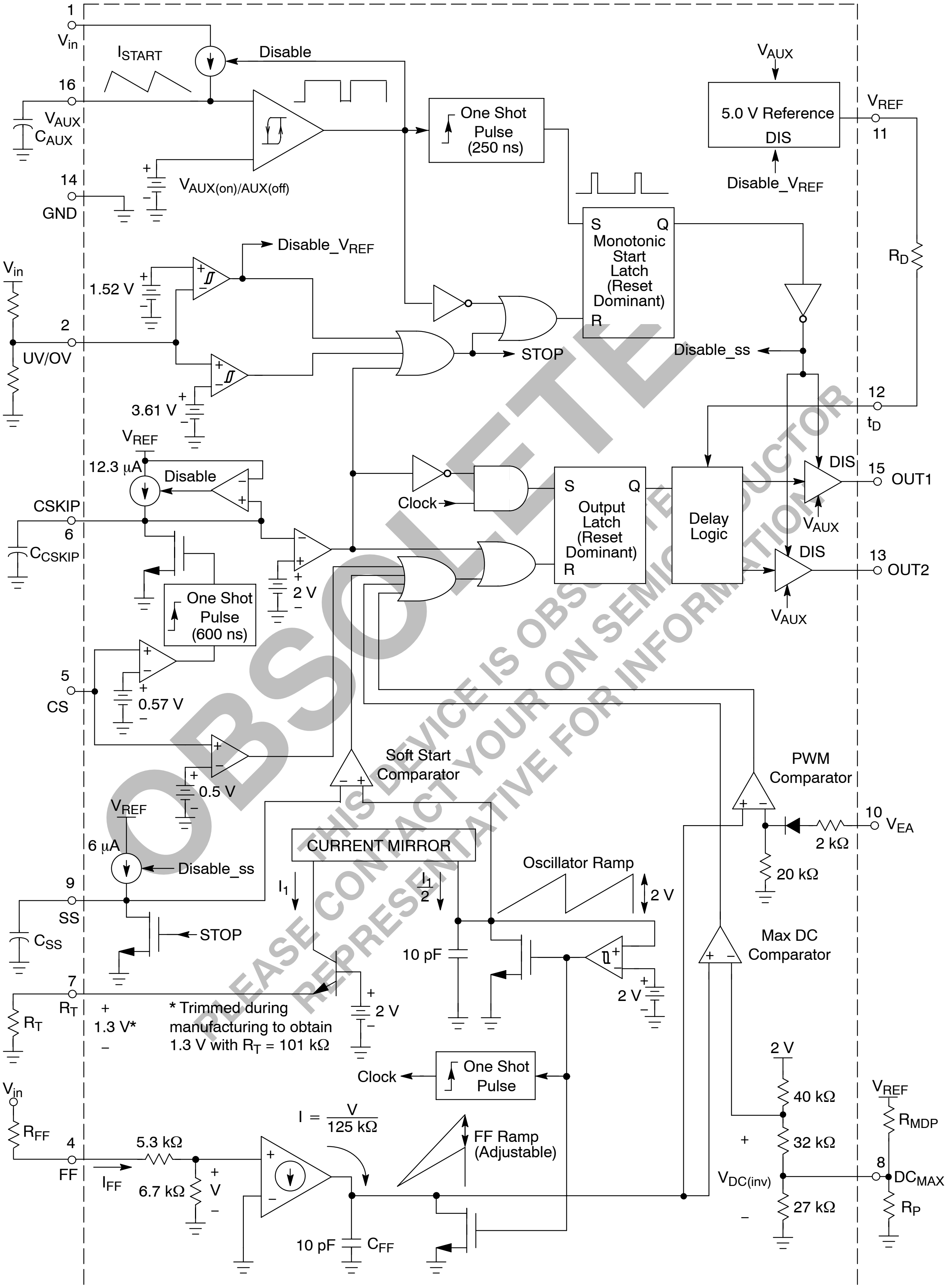


Figure 2. NCP1560 Functional Block Diagram

PIN DESCRIPTION

Pin	Name	Application Information
1	V_{in}	This pin is connected to the bulk DC input voltage supply. A constant current source supplies current from this pin to the capacitor connected on the V_{AUX} pin. The charge current is typically 13.8 mA. Input voltage range is 21.5 V to 150 V.
2	UV/OV	Input supply voltage is scaled down and sampled by means of a resistor divider. The supply voltage must be scaled down between 1.52 V and 3.61 V within the specified input voltage range.
3	NC	Not Connected.
4	FF	An external resistor between V_{in} and this pin adjusts the amplitude of the FF Ramp in proportion to V_{in}. By varying the feedforward ramp amplitude in proportion to the input voltage, changes in loop bandwidth are eliminated.
5	CS	Over current sense input. If the CS voltage exceeds 0.48 V or 0.57 V, the converter enters the Cycle−by−Cycle or Cycle Skip current limit mode, respectively.
6	C_{SKIP}	The capacitor connected between this pin and ground sets the Cycle Skip period. A soft−start sequence follows at the conclusion of the fault period.
7	R_T	A single external resistor between this pin and GND sets the oscillator fixed frequency.
8	DC_{MAX}	An external resistor between this pin and GND sets the voltage on the Max DC Comparator inverting input. The duty cycle is limited by comparing the voltage on the Max DC Comparator inverting input to the Feedforward Ramp.
9	SS	An internal 6.2 μA current source charges the external capacitor connected to this pin. The duty cycle is limited during startup by comparing the voltage on this pin to the Oscillator Ramp.
10	V_{EA}	The error signal from an external error amplifier is fed into this input and compared to the Feedforward Ramp. A series diode and resistor offset the voltage on this pin before it is applied to the PWM Comparator inverting input.
11	V_{REF}	Precision 5.0 V reference output. Maximum output current is 6.0 mA.
12	t_D	An external resistor between V_{REF} and this pin sets the overlap delay between OUT1 and OUT2 transitions.
13	OUT2	Output of the PWM controller with leading and trailing edge overlap delay. OUT2 can be used to drive a synchronous rectifier topology, an active clamp/reset switch, or both.
14	GND	Control circuit ground.
15	OUT1	Main output of the PWM controller.
16	V_{AUX}	Positive input supply voltage. This pin is connected to an external capacitor for energy storage. An internal current supplies current from V_{in} to this pin. Once the voltage on V_{AUX} reaches 11 V, the current source turns OFF. It turns ON again once V_{AUX} falls to 7.0 V. During normal operation, power is supplied to the IC via this pin, by means of an auxiliary winding.

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{in}	Input Line Voltage	−0.3 to 150	V
V_{AUX}	Auxiliary Supply Voltage	−0.3 to 16	V
I_{AUX}	Auxiliary Supply Input Current	35	mA
V_{OUT}	OUT1 and OUT2 Voltage	−0.3 to (V_{AUX} + 0.3 V)	V
I_{OUT}	OUT1 and OUT2 Output Current	10	mA
V_{REF}	5.0 V Reference Voltage	−0.3 to 6.0	V
I_{REF}	5.0 V Reference Output Current	6.0	mA
V_{IO}	All Other Inputs/Outputs Voltage	−0.3 to V_{REF}	V
I_{IO}	All Other Inputs/Outputs Current	10	mA
T_J	Operating Junction Temperature	−40 to 125	°C
T_{stg}	Storage Temperature Range	−55 to 150	°C
P_D	Power Dissipation at T_A = 25°C	0.77	W
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient	130	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series contains ESD protection and exceeds the following tests:
   Pin 1 is the HV startup of the device and is rated to the max rating of the part, or 150 V.
   Machine Model Method 150 V.
   Pins 2−16: Human Body Model 4000 V per MIL−STD−883, Method 3015.
   Machine Model Method 200 V.

ELECTRICAL CHARACTERISTICS (V_{in} = 48 V, V_{AUX} = 12 V, V_{EA} = 2 V, R_T = 101 kΩ, C_{CSKIP} = 6800 pF, R_D = 60.4 kΩ, R_{FF} = 432 kΩ, for typical values T_J = 25°C, for min/max values, T_J = −40°C to 125°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
STARTUP CONTROL AND V_{AUX} REGULATOR					
V_{AUX} Regulation Startup Threshold/V_{AUX} Regulation Peak (V_{AUX} increasing) Minimum Operating V_{AUX} Valley Voltage After Turn−On Hysteresis	 $V_{AUX(on)}$ $V_{AUX(off)}$ V_H	 10.5 6.6 –	 11.0 7.0 4.0	 11.5 7.4 –	V
Minimum Startup Voltage (Pin 1) I_{START} = 1.0 mA, V_{AUX} = $V_{AUX(on)}$ − 0.2 V	$V_{START(min)}$	 –	 19.3	 21.5	V
Startup Circuit Output Current V_{AUX} = 0 V T_J = 25°C T_J = −40°C to 125°C V_{AUX} = $V_{AUX(on)}$ − 0.2 V T_J = 25°C T_J = −40°C to 125°C	I_{START}	 13 10 10 8	 17.5 – 13.8 –	 21 25 17 19	mA
Startup Circuit Off−State Leakage Current (V_{in} = 150 V) T_J = 25°C T_J = −40°C to 125°C	$I_{START(off)}$	 – –	 23 –	 50 100	μA
Startup Circuit Breakdown Voltage (Note 2) $I_{START(off)}$ = 50 μA, T_J = 25°C	$V_{(BR)DS}$	150	–	–	V
Auxiliary Supply Current After V_{AUX} Turn−On Outputs Disabled V_{EA} = 0 V $V_{UV/OV}$ = 0.7 V Outputs Enabled	 I_{AUX1} I_{AUX2} I_{AUX3}	 – – –	 2.7 1.3 4.6	 5.0 2.5 6.5	mA
LINE UNDER/OVERVOLTAGE DETECTOR					
Undervoltage Threshold (V_{in} Increasing)	V_{UV}	1.40	1.52	1.64	V
Undervoltage Hysteresis	$V_{UV(H)}$	0.080	0.098	0.120	V
Overvoltage Threshold (V_{in} Increasing)	V_{OV}	3.47	3.61	3.75	V
Overvoltage Hysteresis	$V_{OV(H)}$	–	0.145	–	V
Undervoltage Propagation Delay to Output	t_{UV}	–	250	–	ns
Overvoltage Propagation Delay to Output	t_{OV}	–	160	–	ns
CURRENT LIMIT					
Cycle−by−Cycle Threshold Voltage	I_{LIM1}	0.44	0.48	0.52	V
Propagation Delay to Output (V_{EA} = 2.0 V) V_{CS} = I_{LIM1} to 2.0 V, measured when V_{OUT} reaches 0.5 V_{OH}	t_{ILIM}	–	90	150	ns
Cycle Skip Threshold Voltage	I_{LIM2}	0.54	0.57	0.62	V
Cycle Skip Charge Current (V_{CSKIP} = 0 V)	I_{CSKIP}	8.0	12.3	15	μA

2. Guaranteed by design only.

ELECTRICAL CHARACTERISTICS (V_{in} = 48 V, V_{AUX} = 12 V, V_{EA} = 2 V, R_T = 101 kΩ, C_{CSKIP} = 6800 pF, R_D = 60.4 kΩ, R_{FF} = 432 kΩ, for typical values T_J = 25°C, for min/max values, T_J = −40°C to 125°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency (R_T = 101 kΩ, V_{in} = 36 V) T_J = 25°C T_J = −40°C to 125°C	f_{OSC1}	 285 280	 300 –	 315 320	kHz
Frequency (R_T = 59 kΩ, V_{in} = 36 V, V_{EA} = 1 V) T_J = 25°C T_J = −40°C to 125°C	f_{OSC2}	 456 444	 480 –	 504 516	kHz
MAXIMUM DUTY CYCLE COMPARATOR					
Maximum Duty Cycle (V_{in} = 36 V, V_{EA} = 3 V, T_J = 25°C) R_P = 0 Ω, R_{MDP} = open R_P = open, R_{MDP} = open	DC_{MAX}	 57 75	 62 80	 66 85	%
Open Circuit Voltage	V_{DCMAX}	0.40	0.47	0.60	V
SOFT−START					
Charge Current (V_{SS} = 1.0 V)	$I_{SS(C)}$	5.0	6.2	7.4	μA
Discharge Current (V_{SS} = 5.0 V, $V_{UV/OV}$ = 3.7 V)	$I_{SS(D)}$	20	52.5	–	mA
PWM COMPARATOR					
Input Resistance (V_1 = 1.25 V, V_2 = 1.50 V) $R_{IN(VEA)} = (V_2 - V_1)/(I_2 - I_1)$	$R_{IN(VEA)}$	8.0	22	60	kΩ
Lower Input Threshold	$V_{EA(L)}$	0.3	0.7	0.9	V
Delay to Output (from V_{OH} to 0.5 V_{OH})	t_{PWM}	–	200	–	ns
5.0 V REFERENCE					
Output Voltage (I_{REF} = 0 mA)	V_{REF}	4.9	5.0	5.1	V
Load Regulation (I_{REF} = 0 to 6 mA)	$V_{REF(Load)}$	–	10	50	mV
Line Regulation (V_{AUX} = 7.5 V to 16 V)	$V_{REF(Line)}$	–	50	100	mV
CONTROL OUTPUTS					
Output Voltage (I_{OUT} = 0 mA) Low State High State	 V_{OL} V_{OH}	 – –	 0.25 11.8	 – –	V
Overlap Delay (V_{in} = 36 V) R_D = 1 MΩ Leading Trailing R_D = 60 kΩ Leading Trailing	t_D	 – – 50 32	 342 312 77 77	 – – 130 130	ns
Drive Resistance (V_{in} = 15 V) Sink (V_{EA} = 0 V, V_{OUT} = 2 V) Source (V_{EA} = 3 V, V_{OUT} = 10 V)	 R_{SNK} R_{SRC}	 20 50	 40 90	 80 170	Ω
Rise Time (C_L = 100 pF, 10% to 90% of V_{OH})	t_{on}	–	30	–	ns
Fall Time (C_L = 100 pF, 90% to 10% of V_{OH})	t_{off}	–	12	–	ns

TYPICAL CHARACTERISTICS

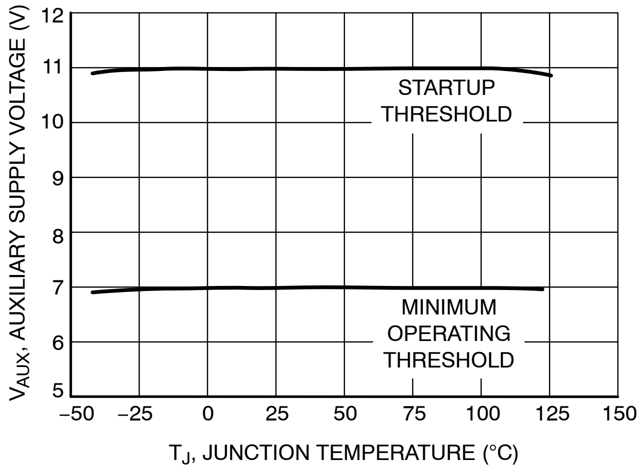


Figure 3. Auxiliary Supply Voltage Thresholds versus Junction Temperature

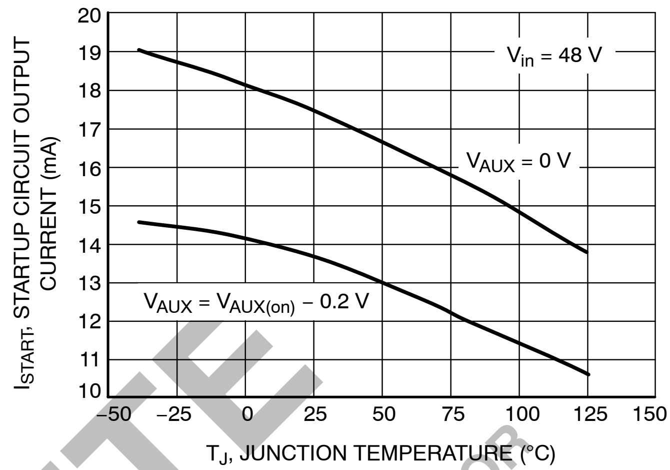


Figure 4. Startup Circuit Output Current versus Junction Temperature

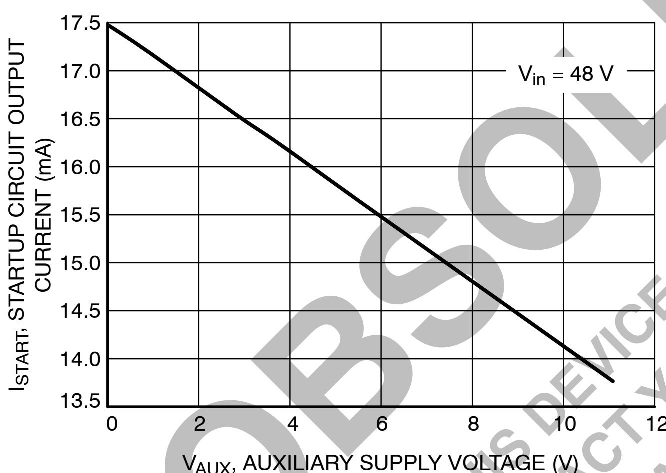


Figure 5. Startup Circuit Output Current versus Auxiliary Supply Voltage

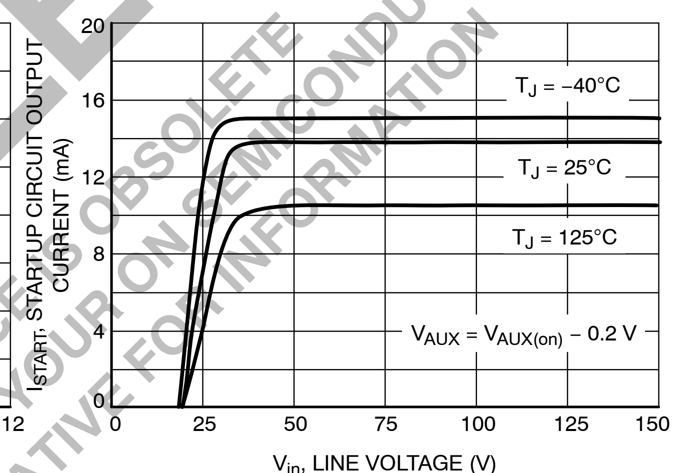


Figure 6. Startup Circuit Output Current versus Line Voltage

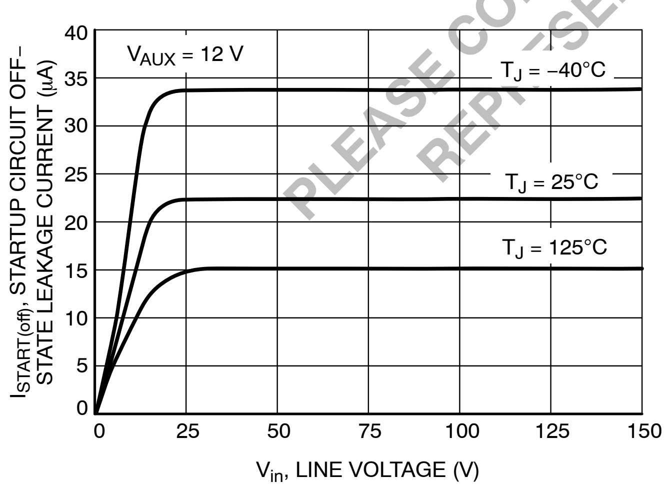


Figure 7. Startup Circuit Off−State Leakage Current versus Line Voltage

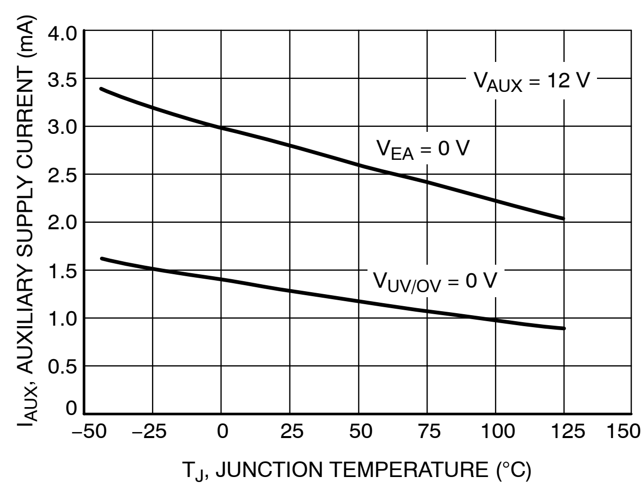


Figure 8. Auxiliary Supply Current versus Junction Temperature

TYPICAL CHARACTERISTICS

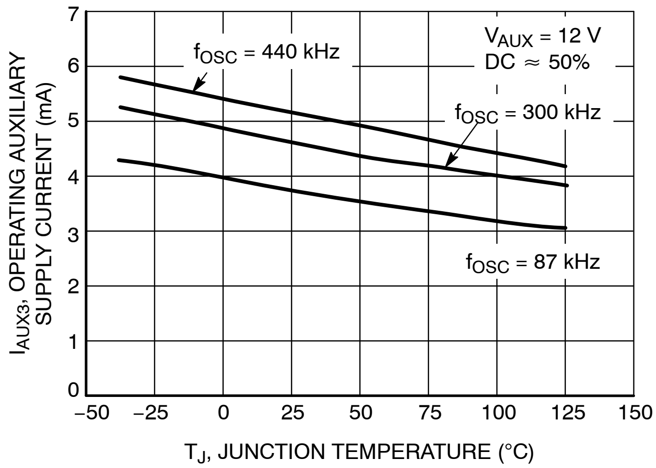


Figure 9. Operating Auxiliary Supply Current versus Junction Temperature

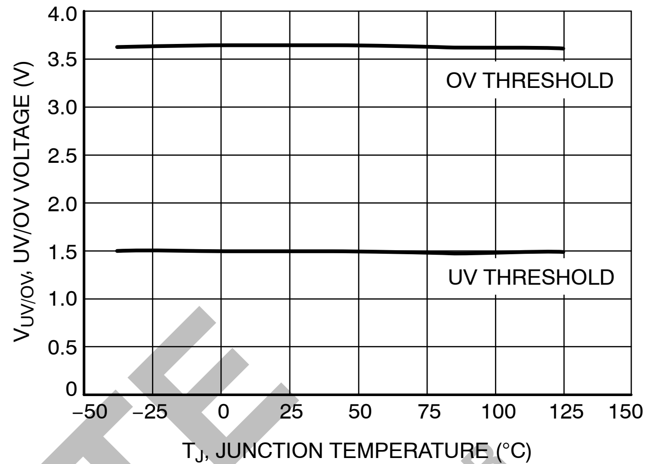


Figure 10. Line Under/Overvoltage Thresholds versus Junction Temperature

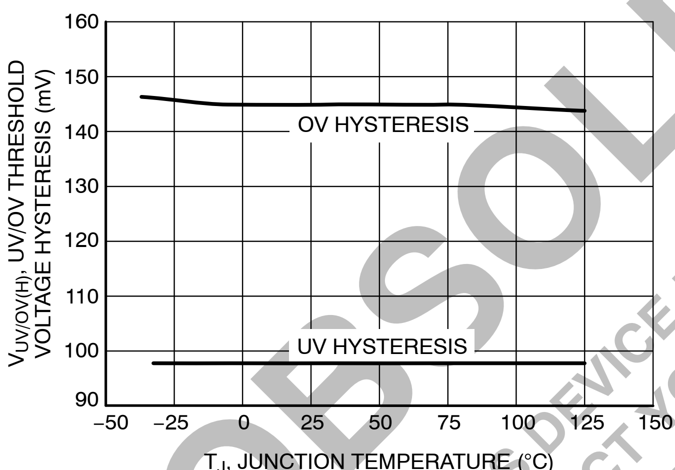


Figure 11. Line Under/Overvoltage Thresholds Hysteresis versus Junction Temperature

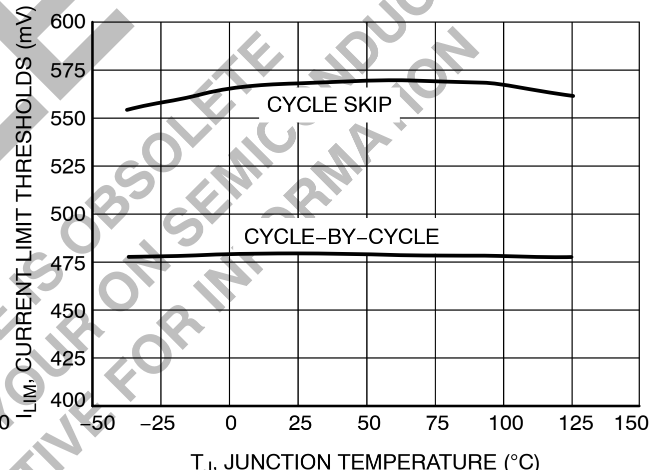


Figure 12. Current Limit Thresholds versus Junction Temperature

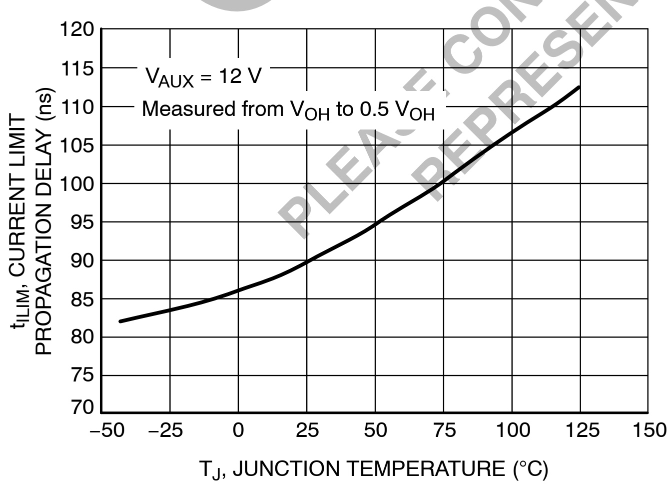


Figure 13. Current Limit Propagation Delay versus Junction Temperature

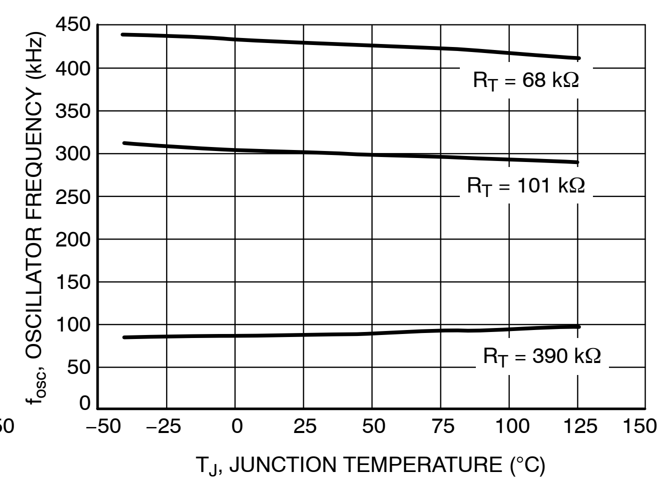


Figure 14. Oscillator Frequency versus Junction Temperature

TYPICAL CHARACTERISTICS

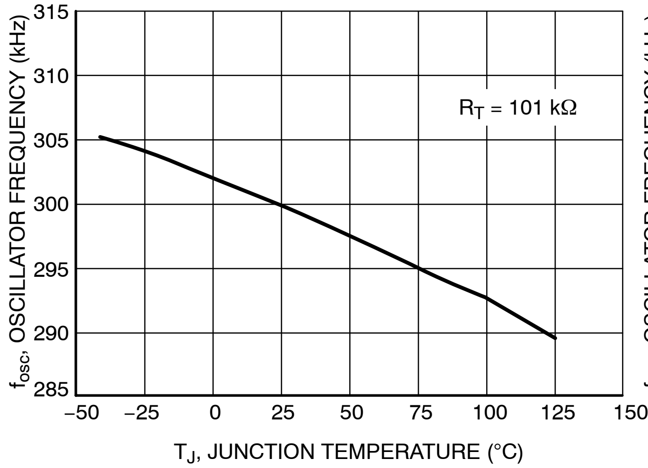


Figure 15. Oscillator Frequency versus Junction Temperature

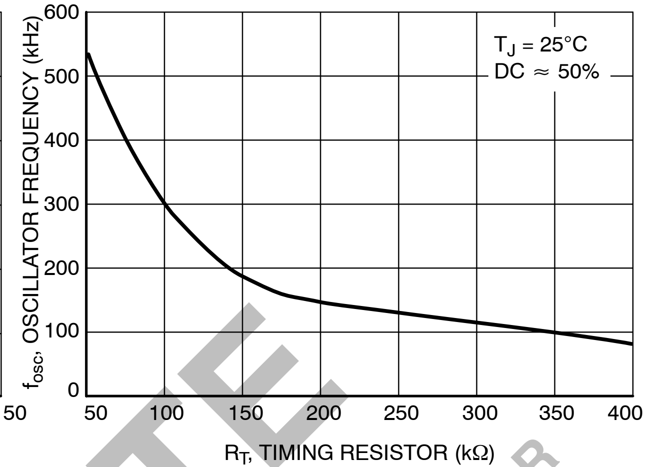


Figure 16. Oscillator Frequency versus Timing Resistor

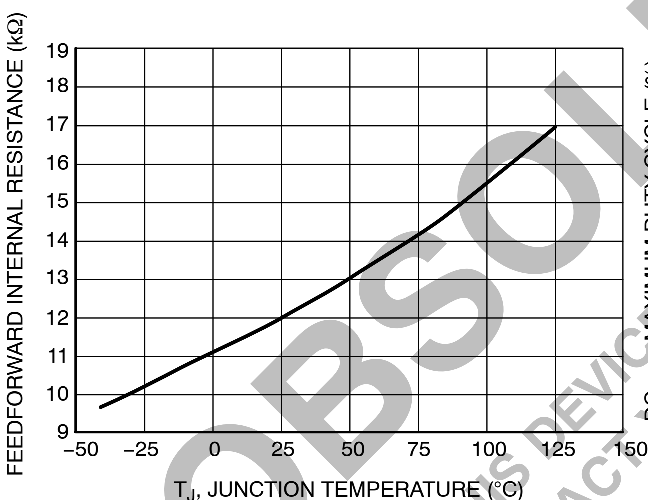


Figure 17. Feedforward Internal Resistance versus Junction Temperature

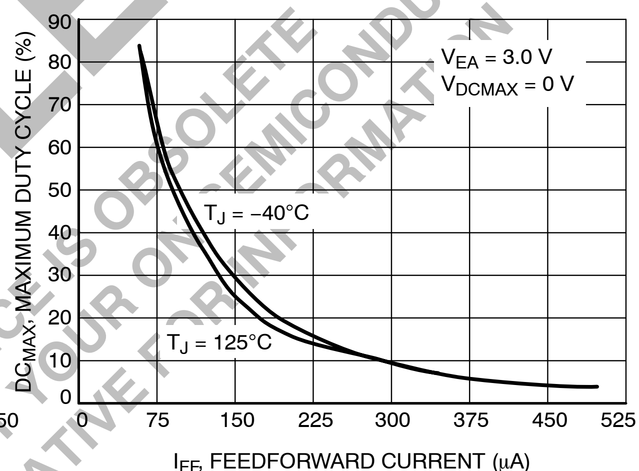


Figure 18. Maximum Duty Cycle versus Feedforward Current

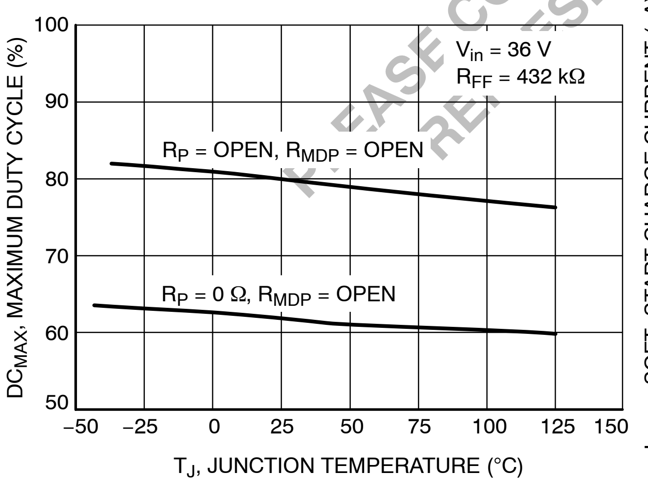


Figure 19. Maximum Duty Cycle versus Junction Temperature

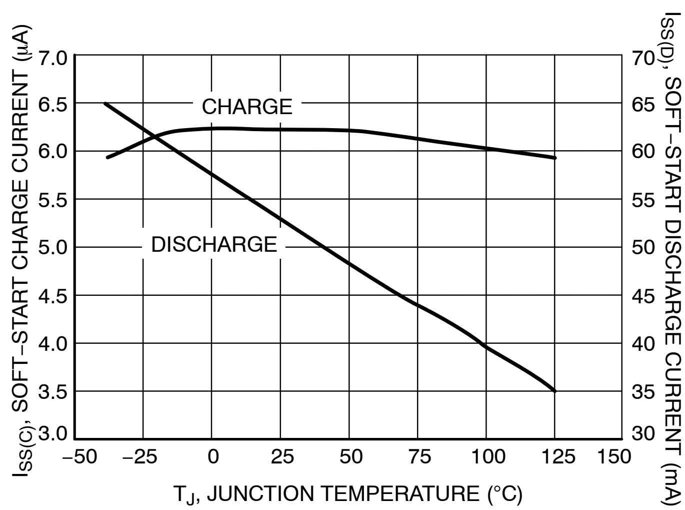


Figure 20. Soft−Start Charge/Discharge Currents versus Junction Temperature

TYPICAL CHARACTERISTICS

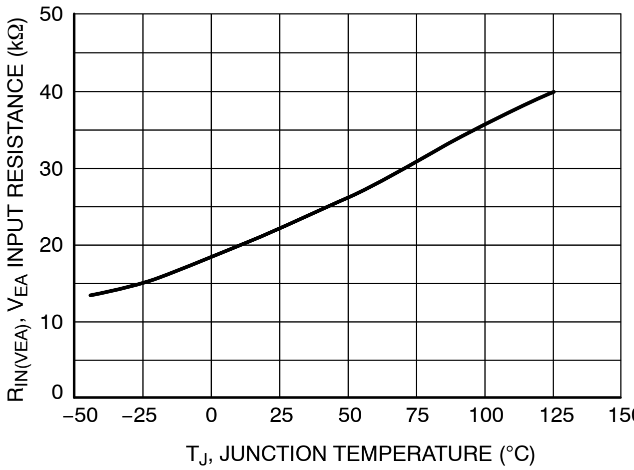


Figure 21. V_{EA} Input Resistance versus Junction Temperature

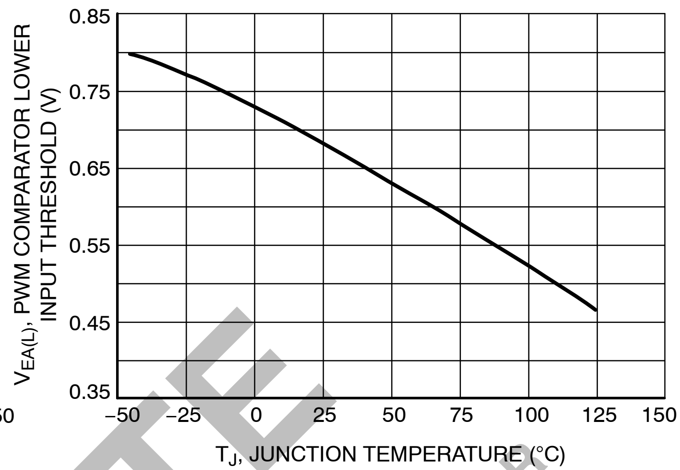


Figure 22. PWM Comparator Lower Input Threshold versus Junction Temperature

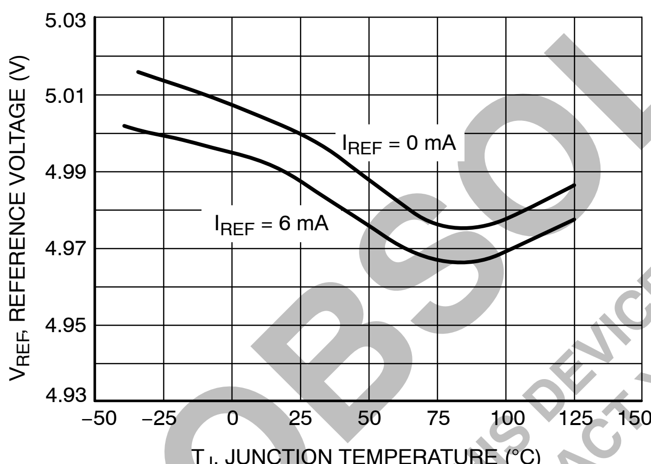


Figure 23. Reference Voltage versus Junction Temperature

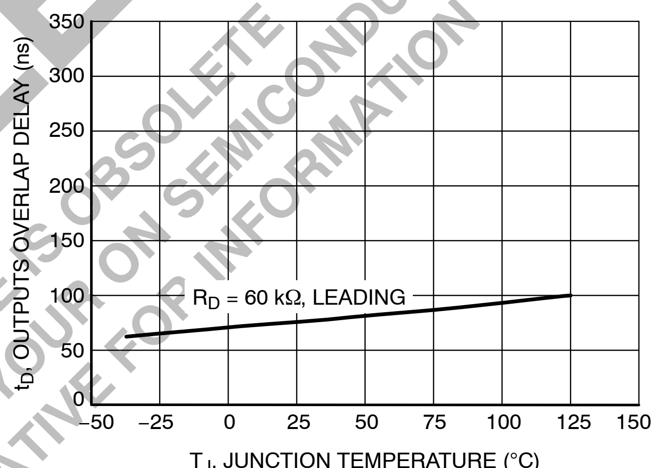


Figure 24. Outputs Overlap Delay versus Junction Temperature

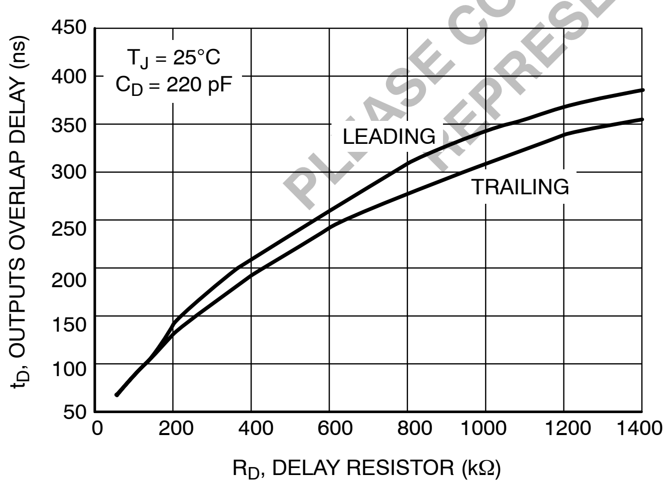


Figure 25. Outputs Overlap Delay versus Delay Resistor

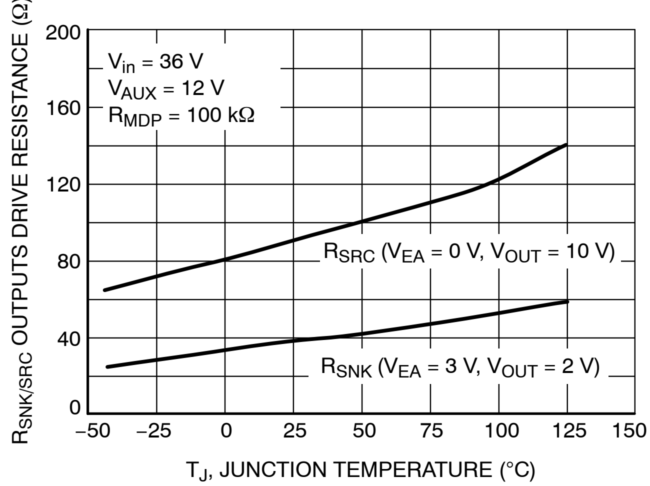


Figure 26. Outputs Drive Resistance Voltage versus Junction Temperature

TYPICAL CHARACTERISTICS

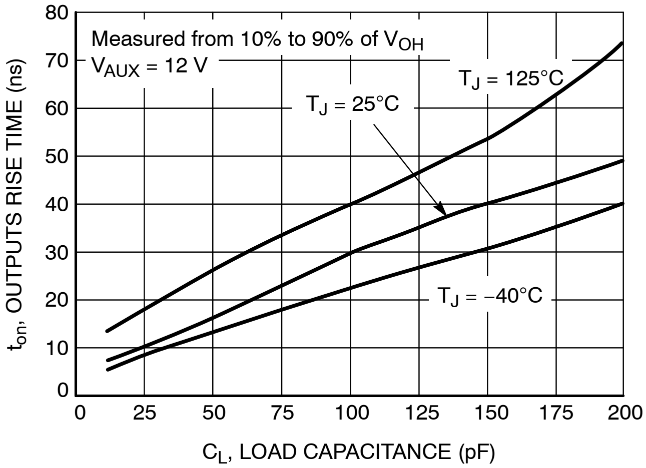


Figure 27. Outputs Rise Time versus Load Capacitance

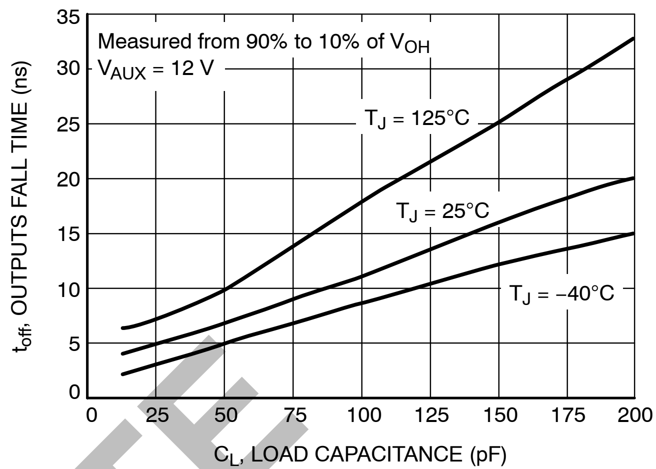


Figure 28. Outputs Fall Time versus Load Capacitance

DETAILED OPERATING DESCRIPTION

The NCP1560 PWM controller contains all the features and flexibility needed for implementation of Voltage−Mode Control in high performance DC−DC converters. This device cost effectively reduces system part count with the inclusion of a high voltage startup regulator. The NCP1560 provides two control outputs. Output 1 controls the main switch of a forward or flyback topology. Output 2 has an adjustable overlap delay, which can be used to control an active clamp/reset switch, a synchronous rectifier switch, or both. Other distinctive features include: two mode overcurrent protection, line under/overvoltage lockout, fast line feedforward, soft−start and a maximum duty cycle limit. The Functional Block Diagram is shown in Figure 2.

The features included in the NCP1560 provide all the advantages of Current−Mode Control, fast line feedforward, and cycle−by−cycle current limit. It eliminates the disadvantages of low power jitter, slope compensation and noise susceptibility.

High Voltage Startup Regulator

The NCP1560 contains an internal high voltage startup regulator that eliminates the need for external startup components. In addition, this regulator increases the efficiency of the supply as it uses no power when in the normal mode of operation, but instead uses power supplied by an auxiliary winding.

The startup regulator consists of a constant current source that supplies current from the input line voltage (V_{in}) to the capacitor on the V_{AUX} pin (C_{AUX}). The startup current is typically 13.8 mA. Once V_{AUX} reaches 11 V, the startup regulator turns OFF and the outputs are enabled. When V_{AUX} reaches 7.0 V, the outputs are disabled and the startup regulator turns ON. This "7 – 11" mode of operation is known as Dynamic Self Supply (DSS). The V_{AUX} pin can be biased externally above 7 V once the outputs are enabled to prevent the startup regulator from turning ON. It is recommended to bias the V_{AUX} pin using an auxiliary supply generated out of an auxiliary winding from the power transformer. An independent voltage supply can also be used. However, if V_{AUX} is biased before the outputs are enabled or while a fault is present, the One Shot Pulse Generator (Figure 2) will not be enabled and the outputs will remain OFF.

As the DSS sources current to the V_{AUX} pin, a diode should be placed between C_{AUX} and the auxiliary supply as shown in Figure 29. This will allow the NCP1560 to charge C_{AUX} while preventing the startup regulator from sourcing current into the auxiliary supply.

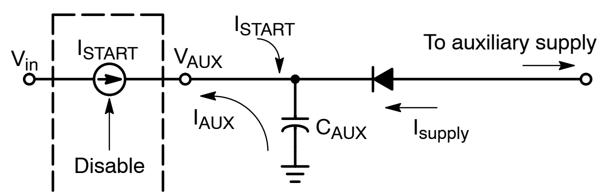


Figure 29. Recommended V_{AUX} Configuration

Power to the controller while operating in the self−bias or DSS mode is provided by C_{AUX}. Therefore, C_{AUX} must be sized such that a V_{AUX} voltage greater than 7 V is maintained while the outputs are switching and the converter reaches regulation. Also, the V_{AUX} discharge time (from 11 V to 7 V) must be greater that the soft−start charge period to assure the converter turns ON.

The startup circuit is rated at a maximum voltage of 150 V. If the device operates in the DSS mode, power dissipation should be controlled to avoid exceeding the maximum power dissipation of the controller.

Line Under/Overvoltage Shutdown

The NCP1560 incorporates a line under/overvoltage shutdown (UV/OV) circuit. The undervoltage (UV) threshold is 1.52 V and the overvoltage threshold (OV) is 3.61 V, for a ratio of 1:2.4.

The UV/OV circuit can be biased using an external resistor divider from the input line. The resistor divider must be sized to enable the controller once V_{in} is within the required operating range. If the UV or OV threshold is reached, the soft−start capacitor is discharged, and the outputs are immediately disabled with no overlap delay as shown in Figure 30. Also, if an UV condition is detected, the 5.0 V Reference Supply is disabled.

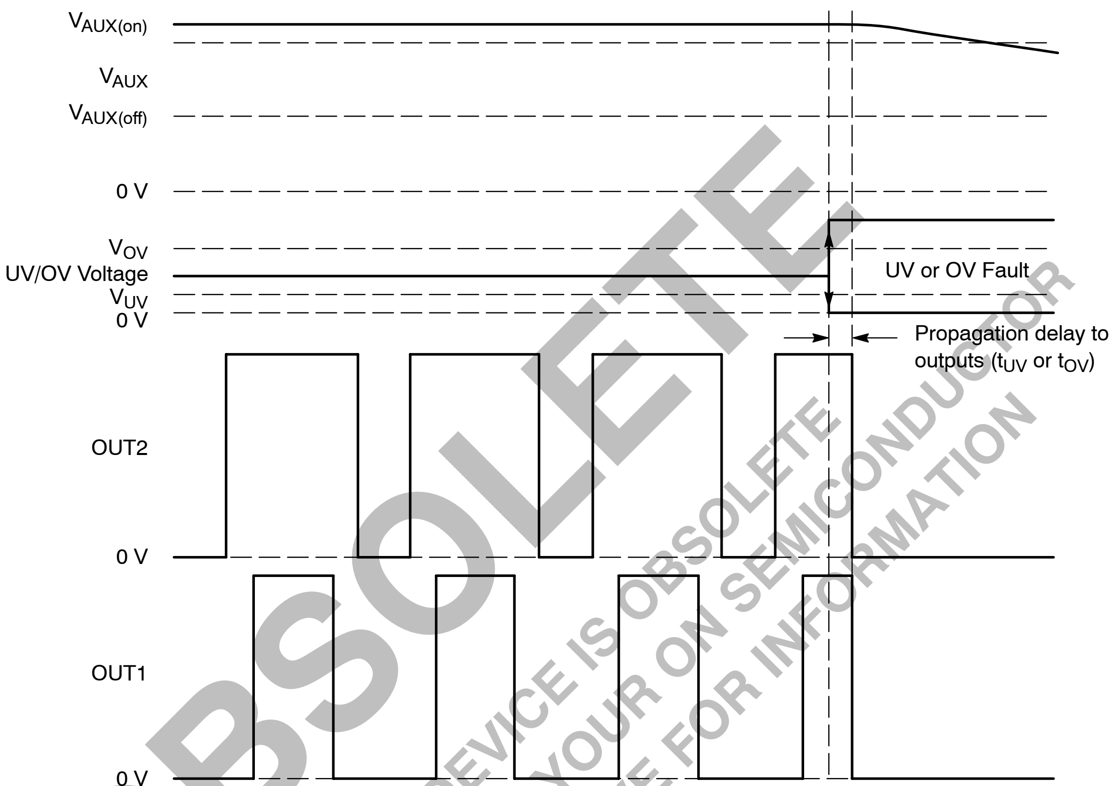


Figure 30. UV/OV Fault Timing Diagram

Once the UV or OV condition is removed and V_{AUX} reaches 11 V, the controller initiates a soft−start cycle. Figure 31 shows the relationship between the UV/OV voltage, the outputs and the soft−start voltage.

The UV/OV pin can also be used to implement a remote enable/disable function. Biasing the UV/OV pin below its UV threshold disables the converter.

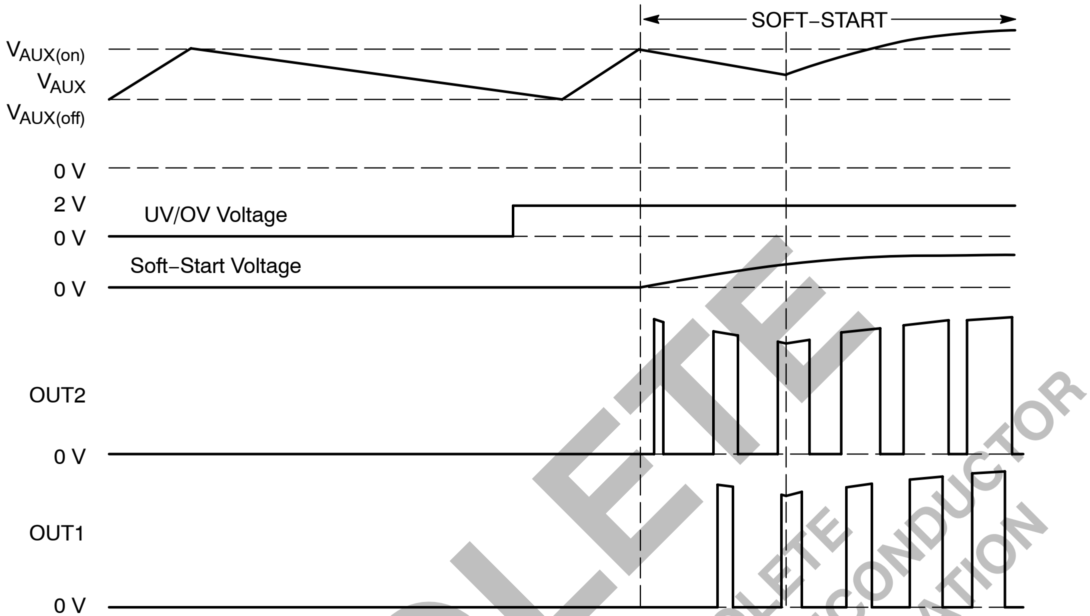


Figure 31. Soft−Start Timing Diagram (Using Auxiliary Winding)

Feedforward Ramp Generator

The NCP1560 incorporates line feedforward (FF) to compensate for changes in line voltage. A FF Ramp proportional to V_{in} is generated and compared to V_{EA}. If the line voltage changes, the FF Ramp slope changes accordingly. The duty cycle will be adjusted immediately instead of waiting for the line voltage change to propagate around the system and be reflected back on V_{EA}.

A resistor between V_{in} and the FF pin (R_{FF}) sets the feedforward current (I_{FF}). The FF Ramp is generated by charging an internal 10 pF capacitor (C_{FF}) with a constant current proportional to I_{FF}. The FF Ramp is finished (capacitor is discharged) once the Oscillator Ramp reaches 2.0 V. Please refer to Figure 2 for a functional drawing of the Feedforward Ramp generator.

I_{FF} is usually a few hundred μA, depending on the operating frequency and the required duty cycle. If the operating frequency and maximum duty cycle are known, I_{FF} is calculated using the equation below:

$$I_{FF} = \frac{C_{FF} \times V_{DC(inv)} \times 125\ k\Omega}{6.7\ k\Omega \times t_{on(max)}}$$

where $V_{DC(inv)}$ is the voltage on the inverting input of the Max DC Comparator and $t_{on(max)}$ is the maximum ON time. Figure 18 shows the relationship between I_{FF} and DC_{MAX}. For example, if a system is designed to operate at 300 kHz, with a 60% maximum duty cycle at 36 V, the DC_{MAX} pin can be grounded and I_{FF} is calculated as follows:

$$T = \frac{1}{f} = \frac{1}{300\ kHz} = 3.33\ \mu s$$

$$t_{on(max)} = DC_{MAX} \times T = 0.6 \times 3.33\ \mu s = 2.0\ \mu s$$

$$I_{FF} = \frac{C_{FF} \times V_{DC(inv)} \times 125\ k\Omega}{6.7\ k\Omega \times t_{on(max)}}$$

$$= \frac{10\ pF \times 0.888\ V \times 125\ k\Omega}{6.7\ k\Omega \times 2.0\ \mu s} = 82.8\ \mu A$$

As the minimum line voltage is 36 V, the required feedforward resistor is calculated using the equation below:

$$R_{FF} = \frac{V_{in}}{I_{FF}} - 12.0\ k\Omega = \frac{36\ V}{82.8\ \mu A} - 12.0\ k\Omega \approx 434\ k\Omega$$

From the above calculations it can be observed that I_{FF} is controlled predominantly by the value of R_{FF}, as the resistance seen into the FF pin is only 12 kΩ. If a tight maximum duty cycle control over temperature is required, R_{FF} should have a low thermal coefficient.

Current Limit

The NCP1560 has two over current protection modes, cycle−by−cycle and cycle skip. It allows the NCP1560 to handle momentary and hard shorts differently for the best tradeoff in performance and safety. The outputs are disabled typically 90 ns after a current limit fault is detected.

The cycle−by−cycle mode terminates the conduction cycle (reducing the duty cycle) if the voltage on the CS pin exceeds 0.48 V. The cycle skip mode is enabled if the voltage on the CS pin reaches 0.57 V. Once a cycle skip fault is detected, the outputs are disabled, the soft−start and cycle skip capacitors are discharged, and the cycle skip period (T_{CSKIP}) commences.

The cycle skip period is set by an external capacitor (C_{CSKIP}). Once a cycle skip fault is detected, the cycle skip capacitor is discharged followed by a charge cycle. The charge current is 12.3 μA. The cycle skip period ends when the voltage on the cycle skip capacitor reaches 2.0 V. The cycle skip capacitor is calculated using the equation below:

$$C_{CSKIP} \approx \frac{T_{CSKIP} \times 12.3\ \mu A}{2\ V}$$

Using the above equation, a cycle skip period of 11.0 μs requires a cycle skip capacitor of 68 pF. The differences between the cycle−by−cycle and cycle skip modes are observed in Figure 32.

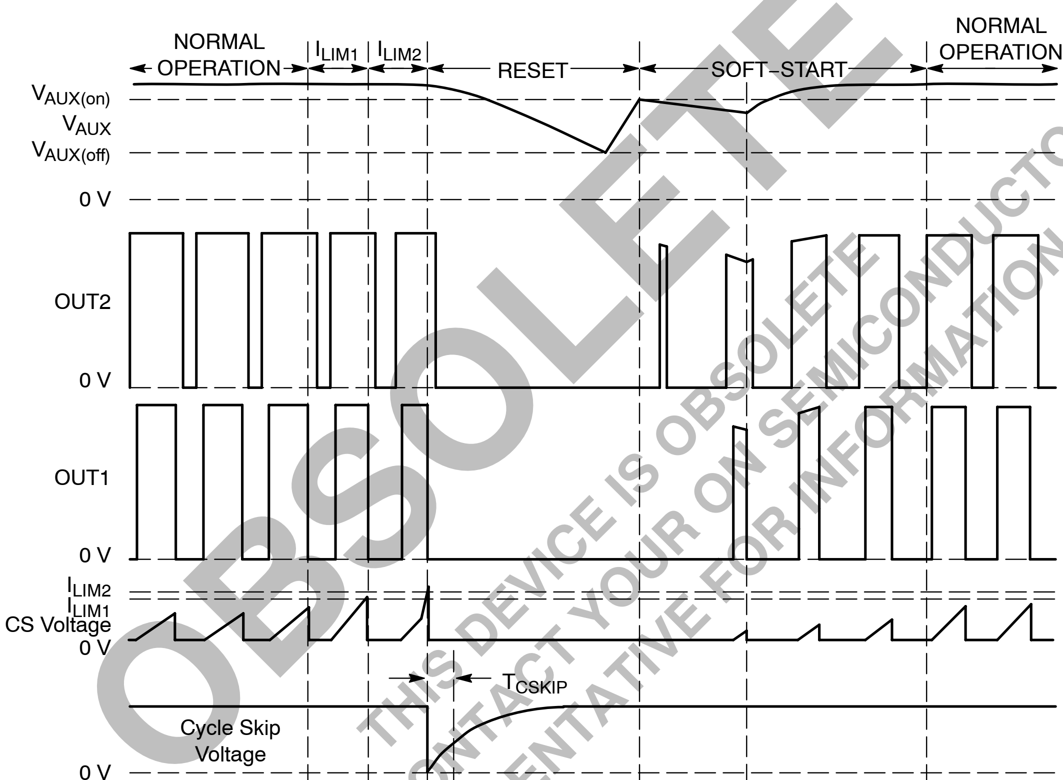


Figure 32. Over Current Faults Timing Diagram

Once the cycle skip period is complete and V_{AUX} reaches 11 V, a soft−start sequence commences. The possible minimum OFF time is set by C_{CSKIP}. However, the actual OFF time is generally greater than the cycle skip period because it is the cycle skip period added to the time it takes V_{AUX} to reach 11 V.

Oscillator

The NCP1560 oscillator frequency is set by a single external resistor connected between the R_T pin and GND. The oscillator is designed to operate up to 500 kHz.

The voltage on the R_T pin is laser trim adjusted during manufacturing to 1.3 V for an R_T of 101 kΩ. A current set by R_T generates an Oscillator Ramp by charging an internal 10 pF capacitor as shown in Figure 2. The period ends (capacitor is discharged) once the Oscillator Ramp reaches 2.0 V. If R_T increases, the current and the Oscillator Ramp slope decrease, thus reducing the frequency. If R_T decreases, the opposite effect is obtained. Figure 16 shows the relationship between R_T and the oscillator frequency.

Maximum Duty Cycle

A dedicated internal comparator limits the maximum ON time of OUT1 by comparing the FF Ramp to $V_{DC(inv)}$. If the FF Ramp voltage exceeds $V_{DC(inv)}$, the output of the Max DC Comparator goes high. This will reset the Output Latch, thus turning OFF the outputs and limiting the duty cycle.

Duty cycle is defined as:

$$DC = \frac{t_{on}}{T} = t_{on} \times f$$

Therefore, the maximum ON time can be set to yield the desired DC if the operating frequency is known. The maximum ON time is set by adjusting the FF Ramp to reach $V_{DC(inv)}$ in a time equal to $t_{on(max)}$ as shown in Figure 33. The maximum ON time should be set for the minimum line voltage. As line voltage increases, the slope of the FF Ramp increases. This reduces the duty cycle below DC_{MAX}, which is a desirable feature as the duty cycle is inversely proportional to line voltage.

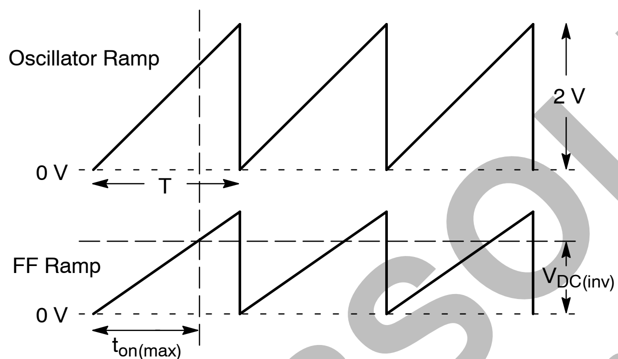


Figure 33. Maximum ON Time Limit Waveforms

An internal resistor divider from a 2.0 V reference is used to set $V_{DC(inv)}$. If the DC_{MAX} pin is grounded, $V_{DC(inv)}$ is 0.88 V. If the pin is floating, $V_{DC(inv)}$ is 1.19 V. This is equivalent to 60% or 80% of a 1.5 V FF Ramp. $V_{DC(inv)}$ can be adjusted to other values by using an external resistor network on the DC_{MAX} pin. For example, if the minimum line voltage is 36 V, R_{FF} is 434 kΩ, operating frequency is 300 kHz and a maximum duty cycle of 70% is required, $V_{DC(inv)}$ is calculated as follows:

$$V_{DC(inv)} = \frac{I_{FF} \times 6.7\ k\Omega \times t_{on(max)}}{C_{FF} \times 125\ k\Omega}$$

$$V_{DC(inv)} = \frac{88.2\ \mu A \times 6.7\ k\Omega \times 2.33\ \mu s}{10\ pF \times 125\ k\Omega} = 1.10\ V$$

This can be achieved by connecting a 45.3 kΩ resistor from the DC_{MAX} pin to GND. The maximum duty cycle limit can be disabled connecting a 100 kΩ resistor between the DC_{MAX} and V_{REF} pins.

5.0 V Reference

The NCP1560 includes a precision 5.0 V reference output. The reference output is biased directly from V_{AUX} and it can supply up to 6 mA. Load regulation is 50 mV and line regulation is 100 mV within the specified operating range.

It is recommended to bypass the reference output with a 0.1 μF ceramic capacitor. The reference output is disabled when an UV fault is present.

PWM Comparator

The output of an external error amplifier is compared to the FF Ramp by means of the PWM Comparator. The external error amplifier drives the V_{EA} input. There is a 0.7 V offset between the V_{EA} input and the PWM Comparator inverting input. The offset is provided by a series diode and resistor. If the voltage on the V_{EA} input is below 0.7 V, the outputs are disabled.

The PWM Comparator controls the duty cycle by turning OFF the outputs once the FF Ramp voltage exceeds the offset V_{EA} voltage. The V_{EA} range required to control the DC from 0% to DC_{MAX} is given by the equation below:

$$V_{EA(L)} < V_{EA} < \left(\frac{I_{FF} \times DC}{186.56\ pf \times f} + V_{EA(L)}\right)$$

where, $V_{EA(L)}$ is the PWM comparator lower input threshold.

Soft−Start

Soft−start (SS) allows the converter to gradually reach steady state operation, thus reducing startup stress and surges on the system. The duty cycle is limited during a soft−start sequence by comparing the Oscillator Ramp to the SS voltage (V_{SS}) by means of the Soft−Start Comparator.

A 6.2 μA current source starts to charge the capacitor on the SS pin once faults are removed and V_{AUX} reaches 11 V. The Soft−Start Comparator controls the duty cycle while the SS voltage is below 2.0 V. Once V_{SS} reaches 2.0 V, it exceeds the Oscillator Ramp voltage and the Soft−Start Comparator does not limit the duty cycle. Figure 34 shows the relationship between the outputs duty cycle and the soft−start voltage.

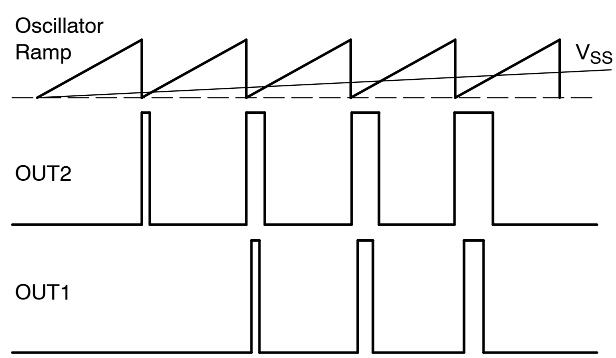


Figure 34. Soft−Start Timing Diagram

If the soft−start period is too long, V_{AUX} may discharge to 7.0 V before the converter output is completely in regulation causing the outputs to be disabled. If the converter output is not completely discharged when the outputs are reenabled, the converter will eventually reach regulation exhibiting a nonmonotonic startup behavior. But, if the converter output is completely discharged when the outputs are reenabled, the cycle may repeat and the converter will not start.

In the event of an UV, OV, or cycle skip fault, the soft−start capacitor is discharged. Once the fault is removed, a soft−start cycle commences. The soft−start steady state voltage is approximately 4.1 V.

Control Outputs

The NCP1560 has two in−phase control outputs, OUT1 and OUT2, with adjustable overlap delay (t_D). OUT2 precedes OUT1 during a low to high transition and OUT1 precedes OUT2 at any high to low transition. Figure 35 shows the relationship between OUT1 and OUT2.

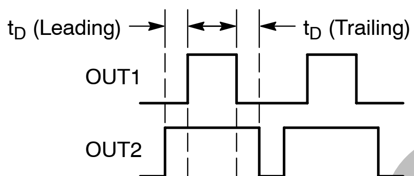


Figure 35. Control Outputs Timing Diagram

Generally, OUT1 controls the main switching element. Output 2, once inverted, can control a synchronous rectifier. The overlap delay prevents simultaneous conduction. Output 2 can also be used to control an active clamp reset.

Once V_{AUX} reaches 11 V, the internal startup circuit is disabled and the One Shot Pulse Generator is enabled. If no faults are present, the outputs turn ON. Otherwise, the outputs remain OFF until the fault is removed and V_{AUX} reaches 11 V again.

The control outputs are biased from V_{AUX}. The outputs can supply up to 10 mA each and their high state voltage is usually 0.2 V below V_{AUX}. Therefore, the auxiliary supply voltage should not exceed the maximum input voltage of the driver stage.

If the control outputs need to drive a large capacitive load, a driver should be used between the NCP1560 and the load. ON Semiconductor’s MC33152 is a good selection for an integrated driver. Figures 27 and 28 shows the relationship between the output’s rise and fall times vs capacitive load.

Time Delay

The overlap delay between the outputs is set connecting a resistor (R_D) between the t_D and V_{REF} pins. An overlap delay of 80 ns is obtained when R_D is 60 kΩ. A higher delay is obtained by increasing R_D. As R_D increases, the bias current of the time delay circuit is reduced, increasing its noise susceptibility. If a delay higher than 150 ns is required, it is recommended to place a small capacitor between the t_D pin and ground.

The output duty cycle can be adjusted from 0% to 85% selecting appropriate values of R_{FF} and $V_{DC(inv)}$. It should be noted that the overlap delay may cause OUT2 to reach 100% duty cycle. Therefore, if OUT2 is used, the maximum duty cycle of OUT2 needs to be kept below 100%. The maximum overlap delay, $t_{D(max)}$, depends on the maximum duty cycle and frequency of operation. The maximum overlap delay is calculated using the equation below.

$$t_{D(max)} \leq \frac{(1 - DC)}{2\,f}$$

For example, if the converter operates at a frequency of 300 kHz with a maximum duty cycle of 80%, the maximum allowed overlap delay is 333 ns. However, this is a theoretical limit and variations over the complete operating range should be considered when selecting the overlap delay.

Additional Information

A 100 W DC−DC converter for telecom systems is designed and implemented using the NCP1560. The converter delivers 100 W at 3.3 V and achieves a full load efficiency of 85%. The system is built using a 4 layer FR4, single sided board. The components location within the board is shown in Figure 36 and the complete circuit schematic is shown in Figure 37. The converter design is discussed in Application Note AND8105/D. Please contact your sales representative for board availability.

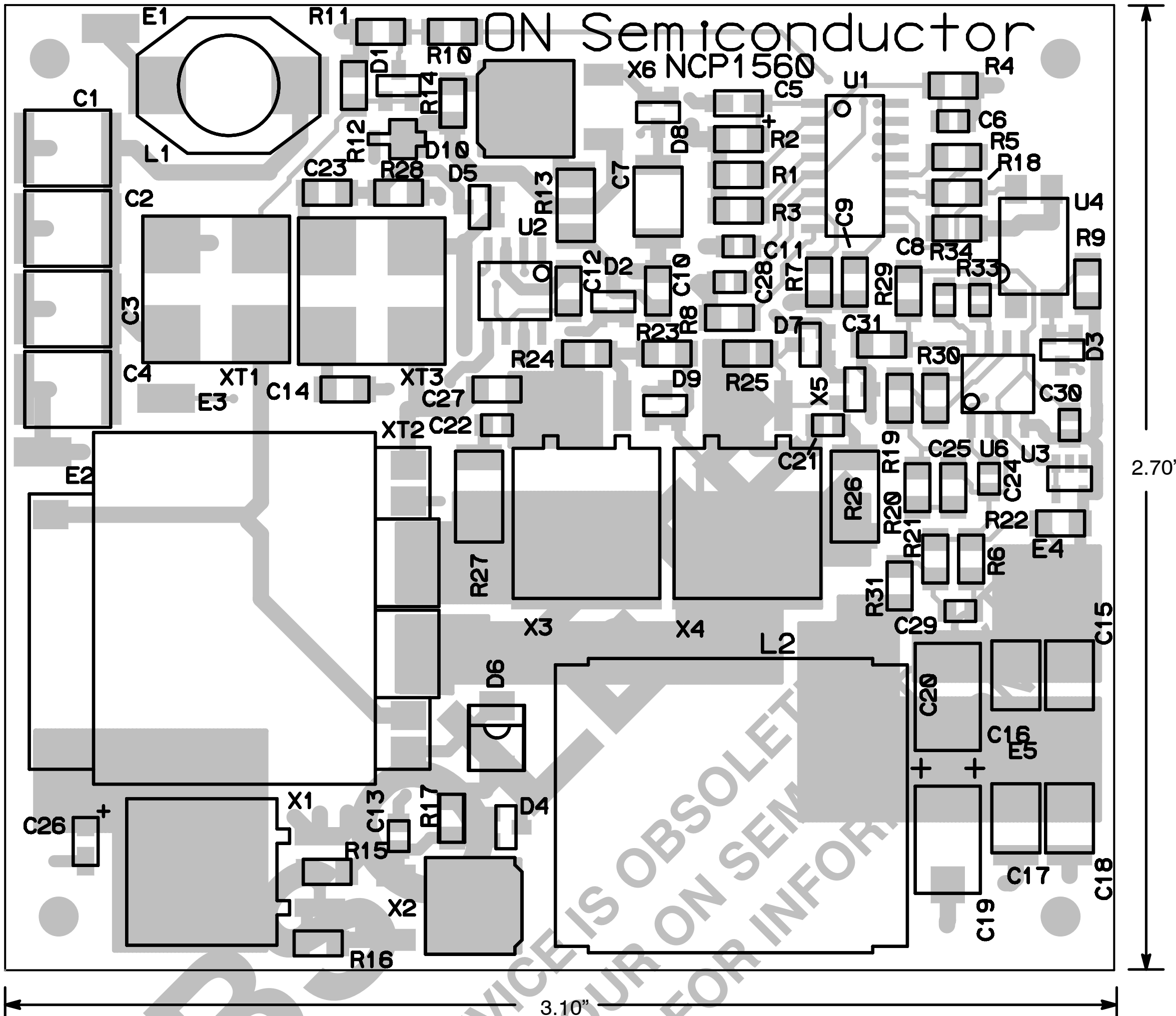


Figure 36. Board Arrangement

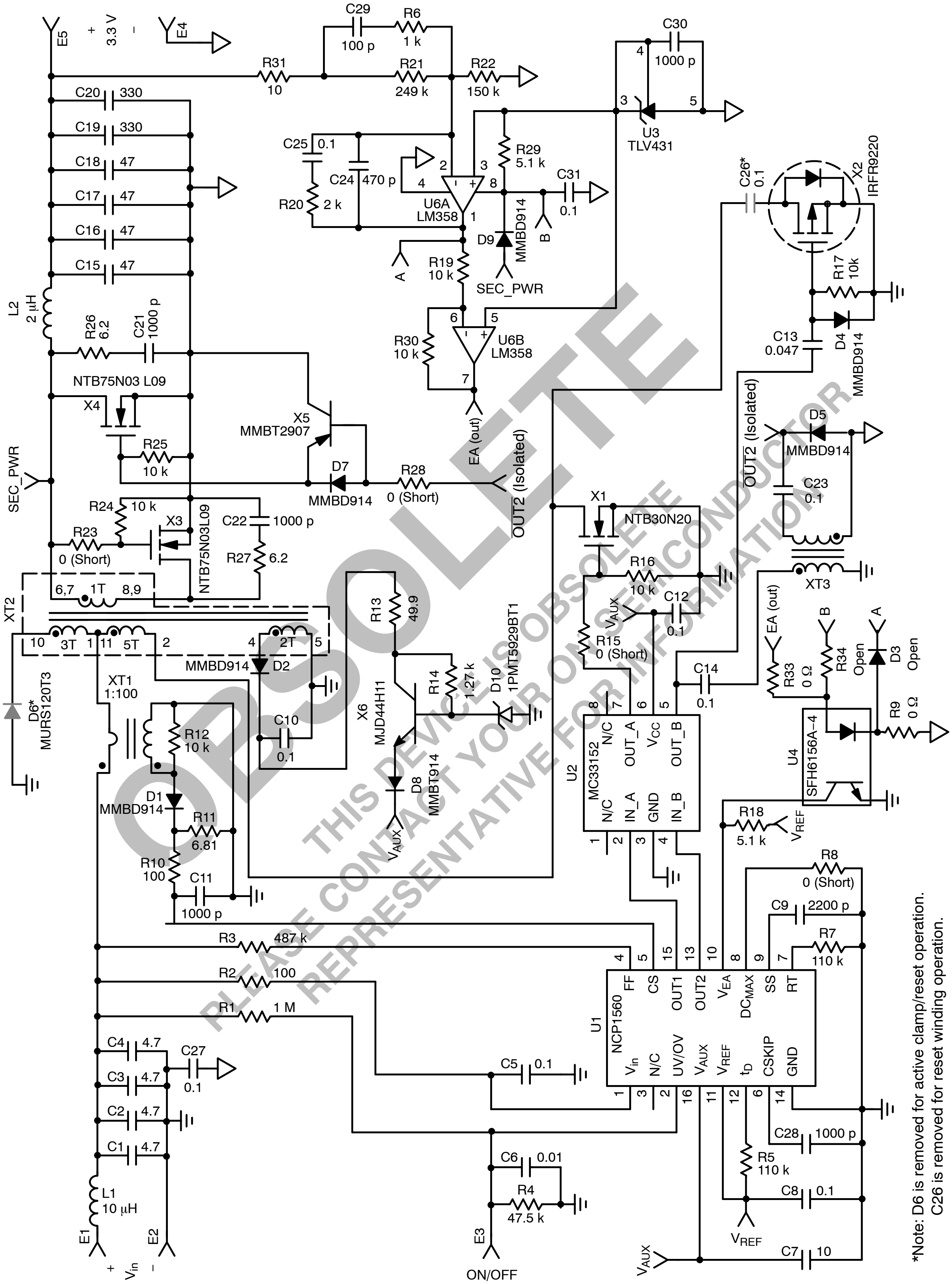
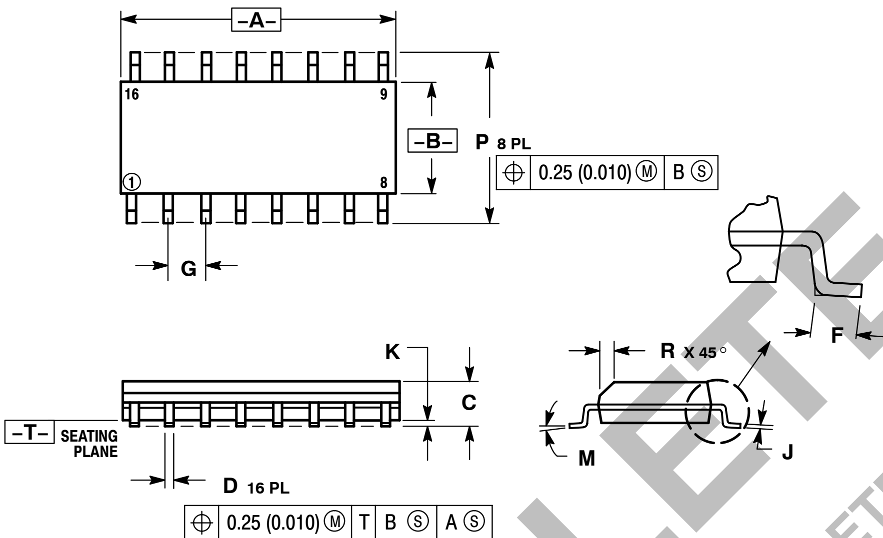


Figure 37. Complete Circuit Schematic

PACKAGE DIMENSIONS

SO−16
D SUFFIX
CASE 751B−05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

The product described herein (NCP1560) may be covered by one or more U.S. patents. There may be other patents pending.

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