

FS8S0765RCB

Fairchild Power Switch(FPS)

Features

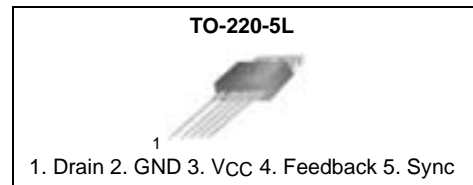
- Burst Mode Operation to Reduce the Power Consumption in the Standby Mode
- External pin for Synchronization and Soft Start
- Wide Operating Frequency Range up to 150kHz
- Low Start-up Current (Max:80uA)
- Low Operating Current (Max:15mA)
- Pulse by Pulse Current Limiting
- Over Voltage Protection (Auto Restart Mode)
- Over Load Protection (Auto Restart Mode)
- Abnormal Over Current Protection (Auto Restart Mode)
- Internal Thermal Shutdown (Auto Restart Mode)
- Under Voltage Lockout
- Internal High Voltage SenseFET

Application

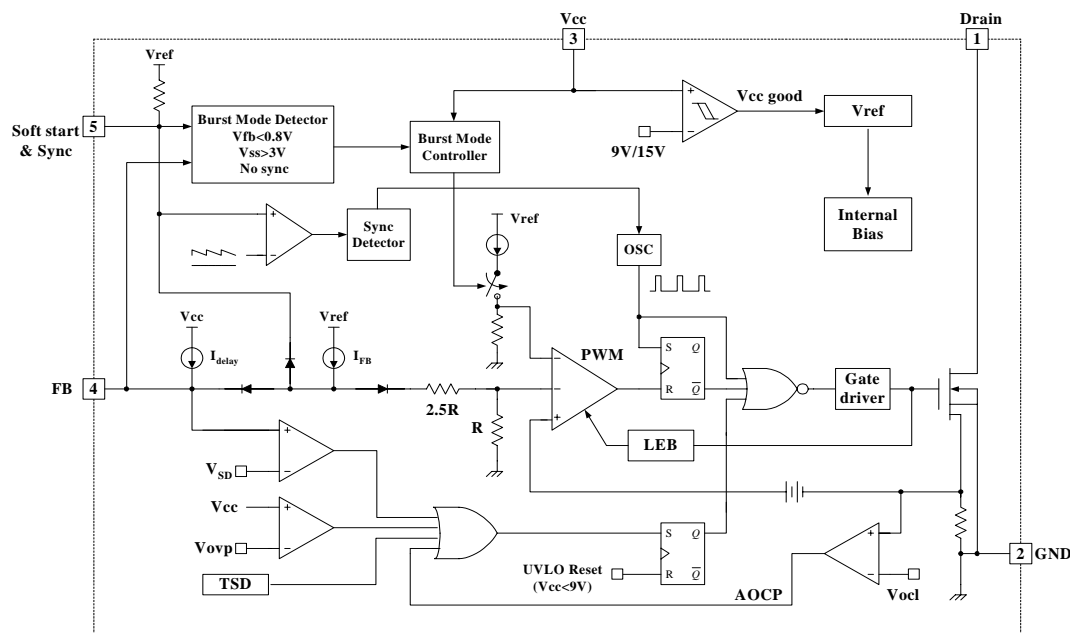
- Monitor SMPS

Description

FS8S0765RCB is a Fairchild Power Switch (FPS) that is specially designed for off-line SMPS of CRT monitor with minimal external components. This device is a current mode PWM controller combined with a high voltage power SenseFET in a single package. The PWM controller features integrated oscillator to be synchronized with the external sync signal, under voltage lockout, optimized gate driver and temperature compensated precise current sources for the loop compensation. This device also includes various fault protection circuits such as over voltage protection, over load protection, abnormal over current protection and over temperature protection. Compared with discrete MOSFET and PWM controller solution, FPS can reduce total cost, component count, size and weight simultaneously increasing efficiency, productivity and system reliability. This device is well suited for the cost effective monitor power supply.



Internal Block Diagram



Rev.1.0.1

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	Drain	High voltage power SenseFET drain connection. This pin is designed to drive the transformer directly.
2	GND	This pin is the control ground and the SenseFET source.
3	Vcc	This pin is the positive supply input. This pin provides internal operating current for both start-up and steady-state operation.
4	Feedback	This pin is internally connected to the inverting input of the PWM comparator. For stable operation, a capacitor should be placed between this pin and GND. If the voltage of this pin reaches 7.5V, the over load protection is activated resulting in shutdown of FPS.
5	Soft Start & Sync	This pin is for soft start and synchronization to the external sync signal.

Absolute Maximum Ratings

(Ta=25°C, unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-Gate Voltage (RGS=1MΩ)	VDGR	650	V
Gate-Source (GND) Voltage	VGS	±30	V
Drain Current Pulsed ⁽²⁾	IDM	28	ADC
Single Pulsed Avalanche Energy ⁽³⁾	EAS	370	mJ
Single Pulsed Avalanche Current ⁽⁴⁾	IAS	17	A
Continuous Drain Current (Tc = 25°C)	ID	7	ADC
Continuous Drain Current (TC=100°C)	ID	4.5	ADC
Supply Voltage	VCC	35	V
Input Voltage Range	VFB	-0.3 to Vcc	V
	VS_S	-0.3 to 10	V
Total Power Dissipation	P _D (Watt H/S)	145	W
	Derating	1.16	W/°C
Operating Junction Temperature	T _j	+150	°C
Operating Ambient Temperature	T _A	-25 to +85	°C
Storage Temperature Range	TSTG	-55 to +150	°C

Notes:

1. T_j=25°C to 150°C
2. Repetitive rating: Pulse width limited by maximum junction temperature
3. L=14mH, starting T_j=25°C
4. L=13uH, starting T_j=25°C

Electrical Characteristics (SenseFET part)

(Ta=25°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	650	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =650V, V _{GS} =0V	-	-	200	μA
		V _{DS} =520V V _{GS} =0V, T _C =125°C	-	-	300	μA
Static Drain Source On Resistance ⁽¹⁾	R _{DS(ON)}	V _{GS} =10V, I _D =3.5A	-	1.4	1.6	Ω
Forward Transconductance	g _{fs}	V _{DS} =40V, I _D =3.5A	-	8	-	mho
Input Capacitance	C _{iss}	V _{GS} =0V, V _{DS} =25V, f = 1MHz	-	1415	-	pF
Output Capacitance	C _{oss}		-	100	-	
Reverse Transfer Capacitance	C _{rss}		-	15	-	
Turn On Delay Time	t _{d(on)}	V _{DD} =325V, I _D =6.5A (MOSFET switching time is essentially independent of operating temperature)	-	25	-	nS
Rise Time	t _r		-	60	-	
Turn Off Delay Time	t _{d(off)}		-	115	-	
Fall Time	t _f		-	65	-	
Total Gate Charge (Gate-Source+Gate-Drain)	Q _g	V _{GS} =10V, I _D =6.5A, V _{DS} =325V (MOSFET switching time is essentially independent of operating temperature)	-	40	-	nC
Gate-Source Charge	Q _{gs}		-	7	-	
Gate-Drain (Miller) Charge	Q _{gd}		-	12	-	

Note:

(1) Pulse test : Pulse width ≤ 300μS, duty 2%

Electrical Characteristics (Continued)

(Ta=25°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
UVLO SECTION						
Start Threshold Voltage	VSTART	VFB=GND	14	15	16	V
Stop Threshold Voltage	VSTOP	VFB=GND	8	9	10	V
OSCILLATOR SECTION						
Initial Frequency	FOSC	-	18	20	22	kHz
Voltage Stability	FSTABLE	12V ≤ Vcc ≤ 23V	0	1	3	%
Temperature Stability (1)	ΔFOSC	-25°C ≤ Ta ≤ 85°C	0	±5	±10	%
Maximum Duty Cycle	DMAX	-	92	95	98	%
Minimum Duty Cycle	DMIN	-	-	-	0	%
FEEDBACK SECTION						
Feedback Source Current	IFBSO	VFB=GND	0.7	0.9	1.1	mA
Feedback Sink Current	IFBSI	VFB=4V, VCC=19V	2.4	3.0	3.6	mA
Shutdown Feedback Voltage	VSD	Vfb ≥ 6.9V	6.9	7.5	8.1	V
Shutdown Delay Current	Idelay	VFB=5V	1.6	2.0	2.4	μA
PROTECTION SECTION						
Over Voltage Protection	VOVP	Vcc ≥ 27V	34	37	-	V
Over Current Latch Voltage (2)	VOCL	-	0.95	1.0	1.05	V
Thermal Shutdown Temp.(1)	TSD	-	140	160	-	°C
SYNC & SOFTSTART SECTION						
Softstart Vortage	VSS	Vfb=2	4.7	5.0	5.3	V
Softstart Current	ISS	Vss=0V	0.8	1.0	1.2	mA
Sync High Threshold Voltage	VSH	Vcc=16V, Vfb=5V	6.7	7.2	7.9	V
Sync Low Threshold Voltage	VSL	Vcc=16V, Vfb=5V	5.4	5.8	6.2	V

Note:

1. These parameters, although guaranteed at the design, are not tested in mass production.
2. These parameters, although guaranteed, are tested in EDS(wafer test) process.

Electrical Characteristics(Continued)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
BURST MODESECTION(DPMS MODE)						
Burst Mode High Threshold Voltage	VBUH	Vfb=0V	11.6	12	12.6	V
Burst Mode Low Threshold Voltage	VBUL	Vfb=0V	10.6	11	11.6	V
Burst Mode Enable FB Voltage	VBUFB	Vcc=10.5V	0.9	1.0	1.1	V
Burst Mode Enable S_S Voltage	VBUSS	Vcc=10.5V,Vfb=0V	2.5	3.0	3.5	V
Burst Mode Enable Delay Time	TBUDT	Vcc=10.5V,Vfb=0V	-	0.5	-	ms
Burst Mode Frequency	FBU	Vcc=10.5V,Vfb=0V	32	40	48	kHz
CURRENT LIMIT(SELF-PROTECTION)SECTION						
Peak Current Limit(1)	I _{OVER}	-	3.52	4.0	4.48	A
Burst Mode Peak Current Limit	I _{BU_PK}	-	0.45	0.6	0.75	A
TOTAL DEVICE SECTION						
Start Up Current	I _{START}	VCC=Vstart-0.1V	-	40	80	uA
Operating Supply Current (2)	I _{OP}	Vfb=GND, VCC=16V	-	9	15	mA
	I _{OP(MIN)}	Vfb=GND, VCC=12V				
	I _{OP(MAX)}	Vfb=GND, VCC=27V				

Note:

1. These parameters indicate inductor current.
2. These parameters are the current flowing in the control IC.

Typical Performance Characteristics

(These characteristic graphs are normalized at $T_a = 25^\circ\text{C}$)

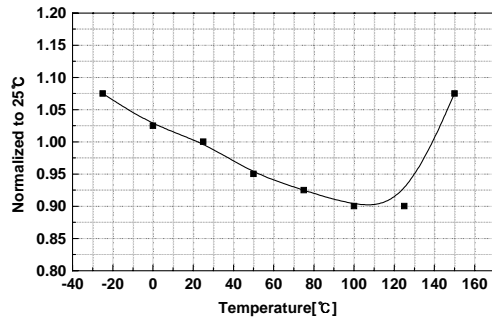


Figure 1. Start Up Current vs. Temp.

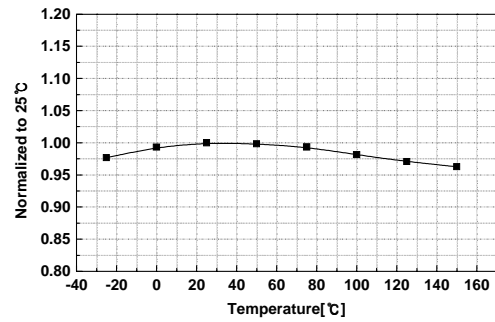


Figure 2. Operating Supply Current vs. Temp.

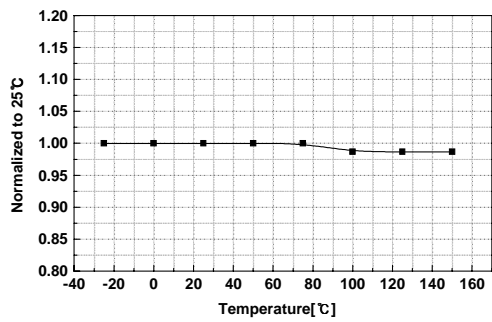


Figure 3. Start Threshold Voltage vs. Temp.

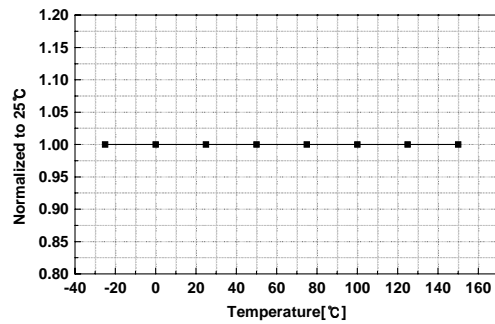


Figure 4. Stop Threshold Voltage vs. Temp.

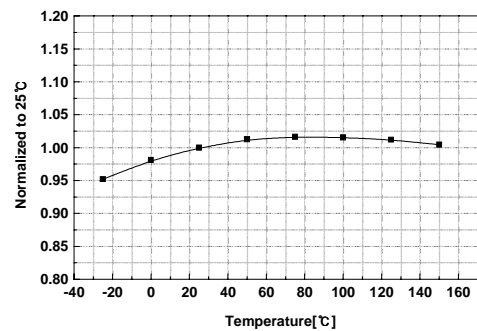


Figure 5. Initial Frequency vs. Temp.

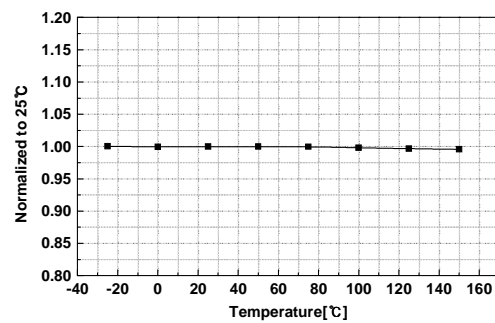


Figure 6. Maximum Duty Cycle vs. Temp.

Typical Performance Characteristics (Continued)

(These characteristic graphs are normalized at $T_a = 25^\circ\text{C}$)

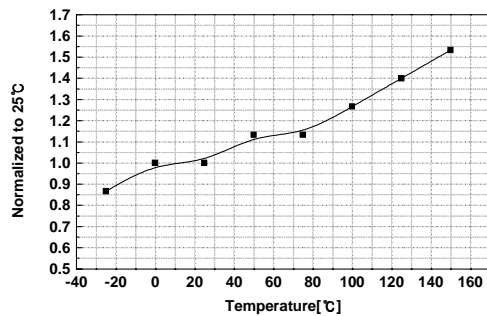


Figure 7. Feedback Offset Voltage vs. Temp.

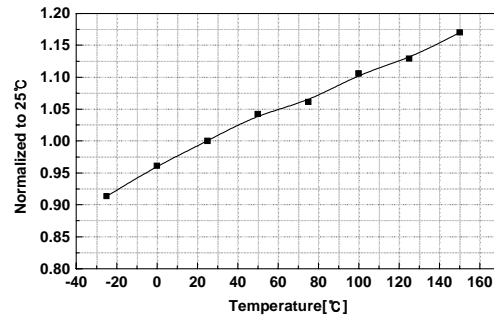


Figure 8. Feedback Sink Current vs. Temp.

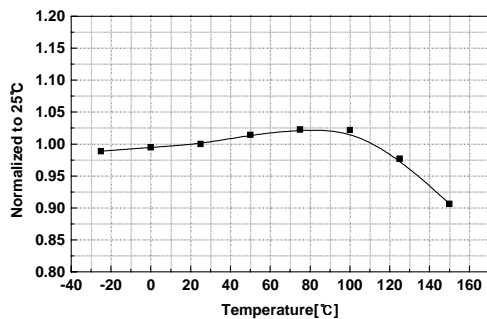


Figure 9. Shutdown Delay Current vs. Temp.

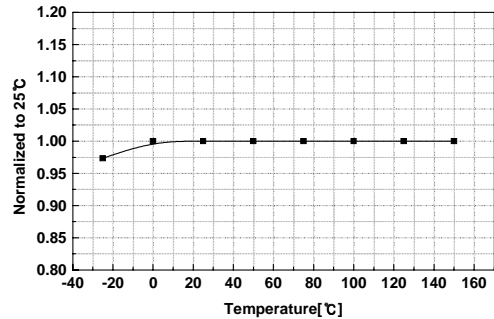


Figure 10. Shutdown Feedback Voltage vs. Temp.

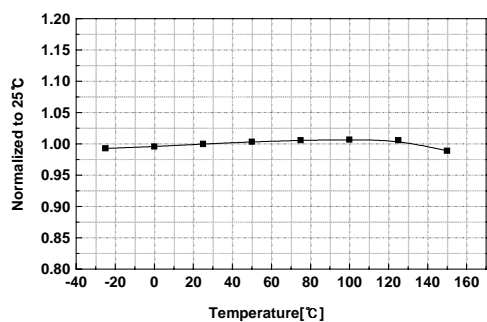


Figure 11. Soft Start Voltage vs. Temp.

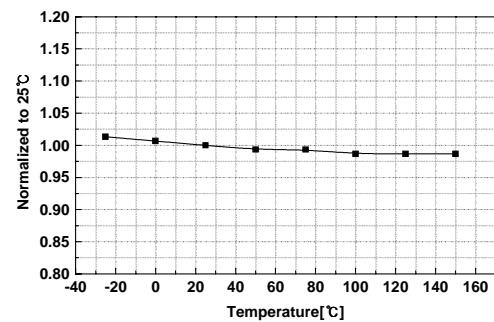


Figure 12. Over Voltage Protection vs. Temp.

Typical Performance Characteristics(Continued)

(These characteristic graphs are normalized at Ta= 25°C)

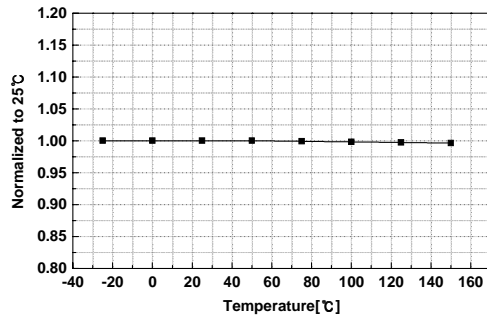


Figure 13. Normal Mode Regulation Voltage vs. Temp.

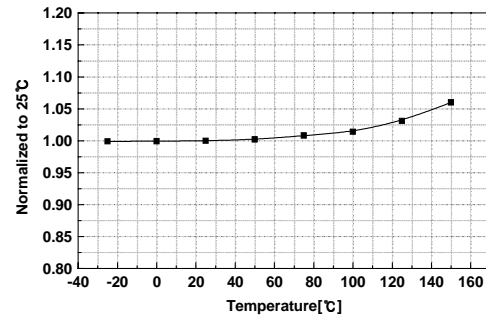


Figure 14. Peak Current vs. Temp.

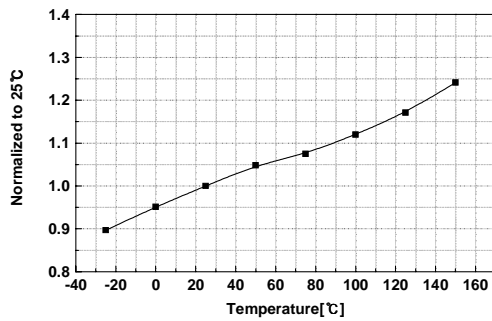


Figure 15. Feedback Sink Current vs. Temp.

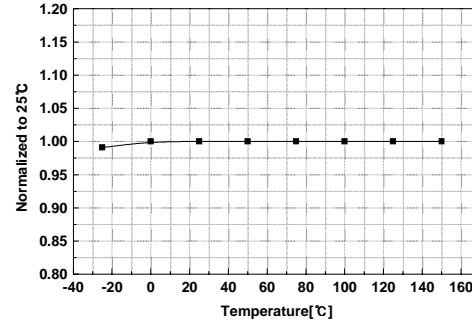


Figure 16. Burst Mode Low Threshold Voltage vs. Temp.

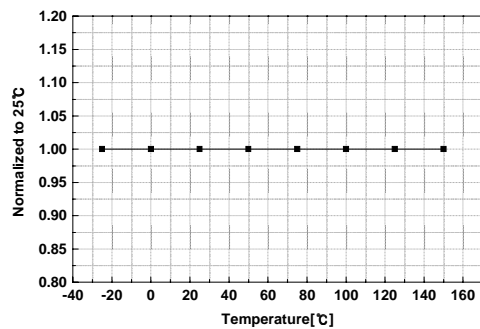


Figure 17. Burst Mode High Threshold Voltage vs. Temp.

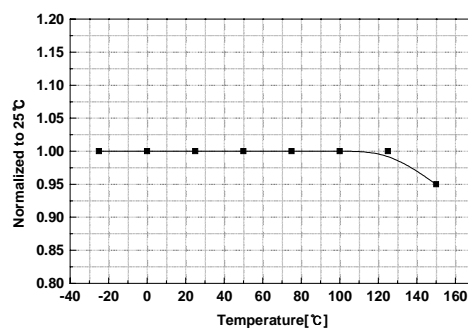


Figure 18. Burst Mode Enable Voltage vs. Temp.

Typical Performance Characteristics (Continued)

(These characteristic graphs are normalized at $T_a = 25^\circ\text{C}$)

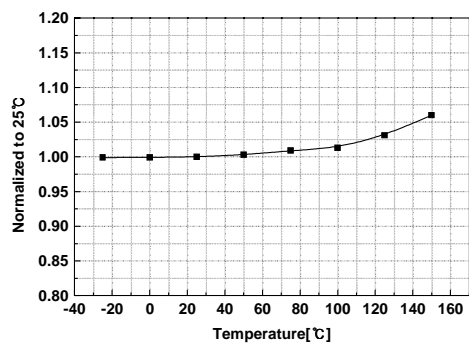


Figure 19. Burst Mode Peak Current vs. Temp.

Functional Description

1. Start up : To guarantee stable operation of the control IC, FS8S0765RCB has UVLO circuit with 6V hysteresis band. Figure 1 shows the relation between the supply current (I_{cc}) and the supply voltage (V_{cc}). Before V_{cc} reaches 15V, the FPS consumes only startup current of 80 μ A, which is usually provided by the DC link through start-up resistor. When V_{cc} reaches 15V, the FPS begins operation and the operating current increases to 15mA as shown. Once the control IC starts operation, it continues its normal operation until V_{cc} goes below the stop voltage of 9V

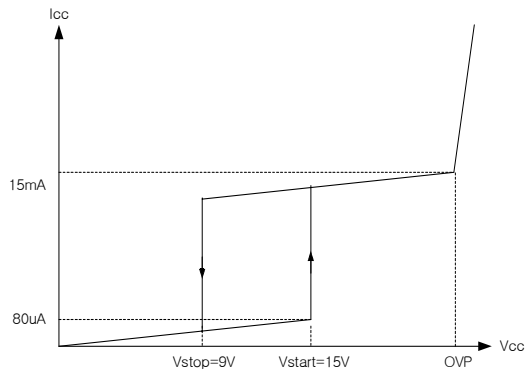


Figure 1. Strat up with hysteresis

2. Feedback Control : FS8S0765RCB employs primary side regulation, which permits elimination of feedback circuit components in the secondary side such as opto coupler and TL431. Figure 2 shows the primary side control circuit. The primary side regulation voltage (V_{psr}) is controlled to the breakdown voltage of zener diode (D_z). Because current mode control is employed, the drain current of the power MOSFET is limited by the inverting input of PWM comparator (V_{fb}^*). When MOSFET turns on, usually there exists high current spike in the MOSFET current caused by primary-side capacitance and secondary-side rectifier reverse recovery. In order to prevent premature termination of the switching pulse due to the current spike, the FPS employs leading edge blanking (LEB). The leading edge blanking circuit inhibits the PWM comparator for a short time after the MOSFET is turned on.

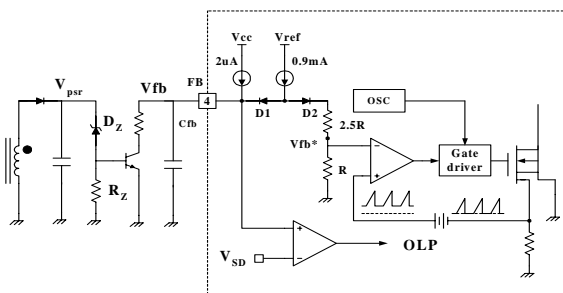


Figure 2. Primary side control circuit

3. Protection function : FS8S0765RCB has 4 self protective functions such as abnormal over current protection (AOCP), over load protection (OLP), over voltage protection (OVP) and thermal shutdown (TSD). Because these protection circuits are fully integrated into the IC without external components, the reliability can be improved without cost increase. In the event of these fault conditions, the FPS enters into auto-restart operation. Once the fault condition occurs, switching operation is terminated and MOSFET remains off, which forces V_{cc} to be reduced. When V_{cc} reaches 9V, the protection is reset and the supply current reduces to 80 μ A. Then, V_{cc} begin to increase with the current provided through the start-up resistor. When V_{cc} reaches 15V, the FPS resumes its normal operation if the fault condition is removed. In this manner, the auto-restart alternately enables and disables the switching of the power MOSFET until the fault condition is eliminated as illustrated in figure 3.

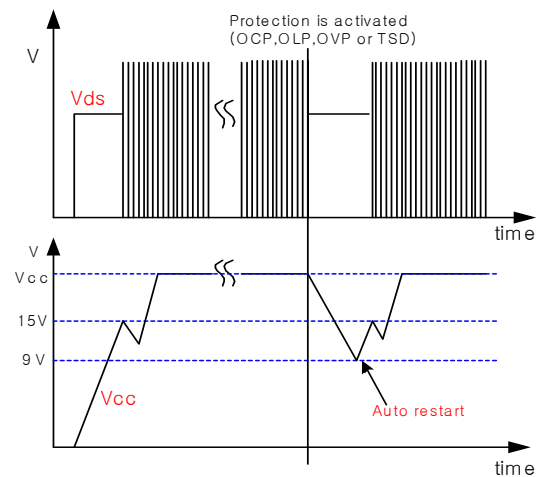


Figure 3. Auto restart operation after protection

3.1 Abnormal Over Current Protection (AOCP) : When the secondary rectifying diodes or the transformer pins are shorted, a steep current with extremely high di/dt can flow during the LEB time. Therefore, the abnormal over current protection (AOCP) block is added to ensure the reliability as shown in figure 4. It turns off the SenseFET within 300ns after the abnormal over current condition is sensed.

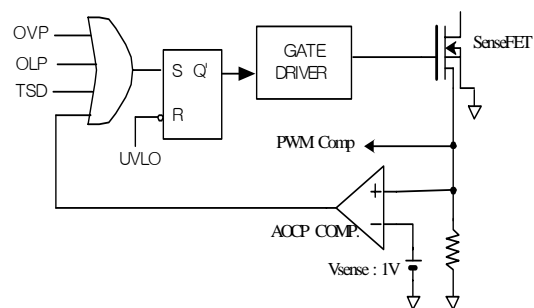


Figure 4. AOCP block

3.2 Over Load Protection (OLP) : When the load current exceeds a pre-set level for longer than pre-determined time, protection circuit should be activated in order to protect the SMPS. Because of the pulse-by-pulse current limit capability, the maximum peak current through the SMPS is limited, and therefore the maximum input power is restricted with a given input voltage. If the output consumes beyond this maximum power, the output voltage together with primary side regulation voltage decrease below the set voltage. This reduces the current through primary side regulation transistor, which increases feedback voltage (Vfb). If Vfb exceeds 2.7V, D1 is blocked and the 2uA current source starts to charge Cfb slowly compared to when the 0.9mA current source charges Cfb. In this condition, Vfb continues increasing until it reaches 7.5V, and the switching operation is terminated at that time as shown in figure 6. The delay time for shutdown is the time required to charge Cfb from 2.7V to 7.5V with 2uA.

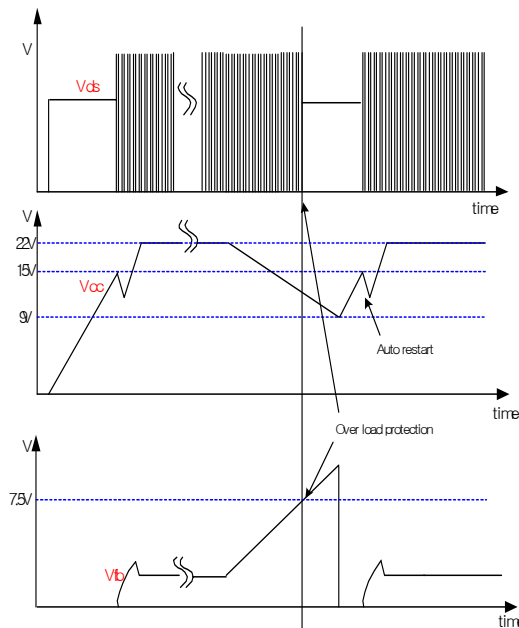


Figure 5. The waveforms at the OLP and auto restart

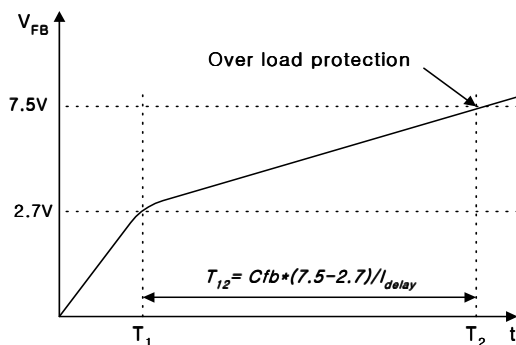


Figure 6. Over load protection

3.3 Over Voltage Protection (OVP) : In case of malfunction in the primary side feedback circuit, or feedback loop open caused by a defect of solder, the current through primary side control transistor becomes almost zero. Then, Vfb climbs up in a similar manner to the over load situation, forcing the preset maximum current to be supplied to the secondary side until the over load protection is activated. Because energy more than required is provided to the output, the output voltage may exceed the rated voltage before the over load protection is activated, resulting in the breakdown of the devices in the secondary side. In order to prevent this situation, an over voltage protection (OVP) circuit is employed. When the Vcc voltage touches 37V, the OVP block is activated.

3.4 Thermal Shutdown (TSD) : The SenseFET and the control IC are built in one package. This makes it easy for the control IC to detect the heat generation from the SenseFET. When the temperature exceeds approximately 160°C, the thermal shutdown is activated.

4. Soft Start : Figure 7 shows the soft start circuit. During the initial start up, the 0.9 mA current source leaks out through C_{ss} and R_{ss}. As C_{ss} is charged, the leakage current decreases. Therefore, by choosing much bigger C_{ss} than C_{fb}, it is possible to increase the feedback voltage slowly forcing the SenseFET current to increase slowly. After C_{ss} reaches its steady state value, D3 is blocked and the soft switching circuit is decoupled from the feedback circuit. If the value of C_{ss} is too large, there is possibility that Vfb increases to 7.5V activating the over load protection during soft start time. In order to avoid this situation, it is recommended that the value of C_{ss} should not exceed 100 times of C_{fb}.

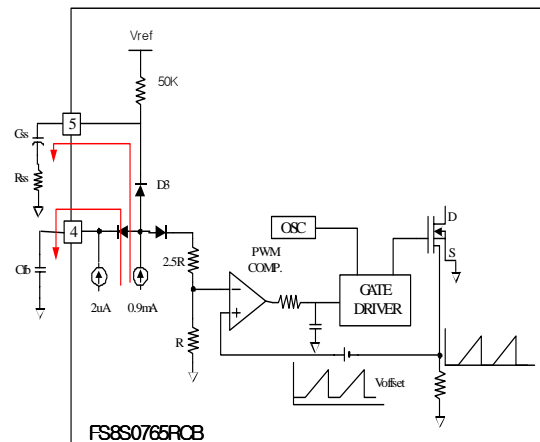
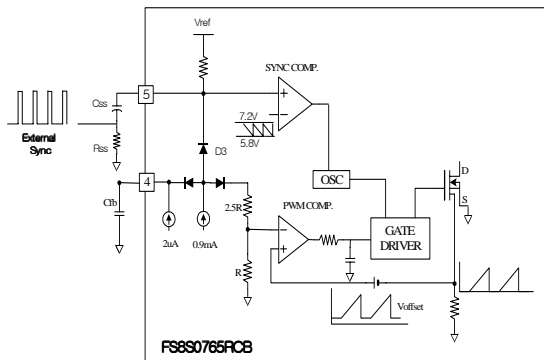
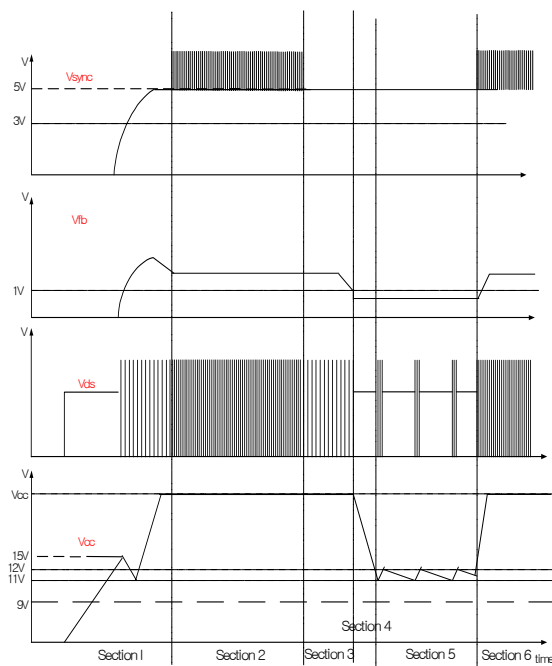


Figure 7. The circuit for the soft start

5. Synchronization : In order to reduce the effect of switching noise on the screen, the SMPS for monitor synchronizes its switching frequency to an external signal, typically the horizontal sync flyback signal. The switching frequency of the FPS can vary from 20 kHz to 150 kHz according to the

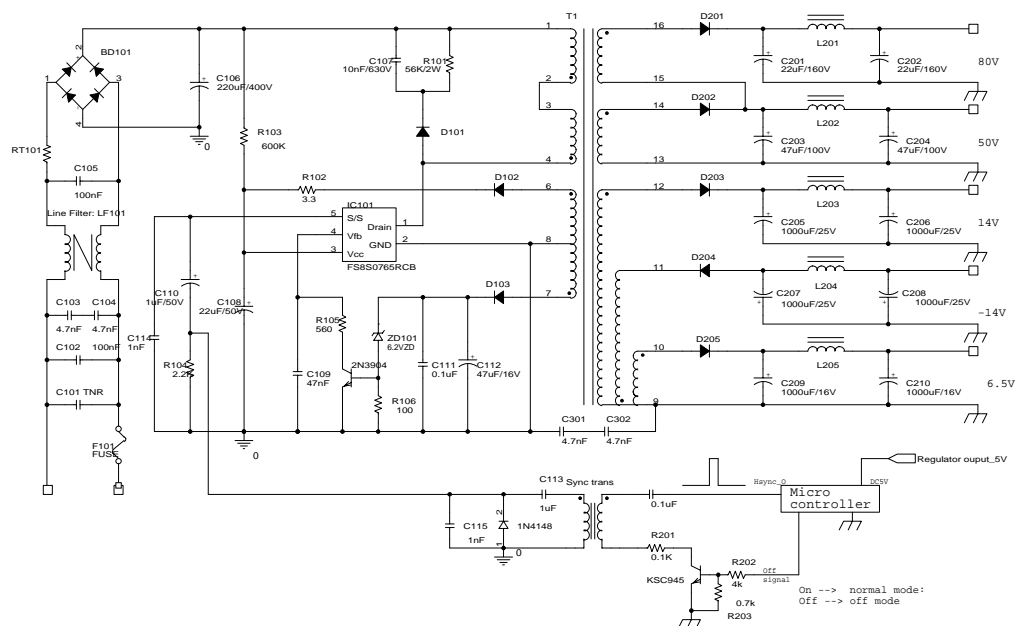


sumption in standby mode, it is recommended to set the value of Vcc during normal operation as high as possible (about 29V).

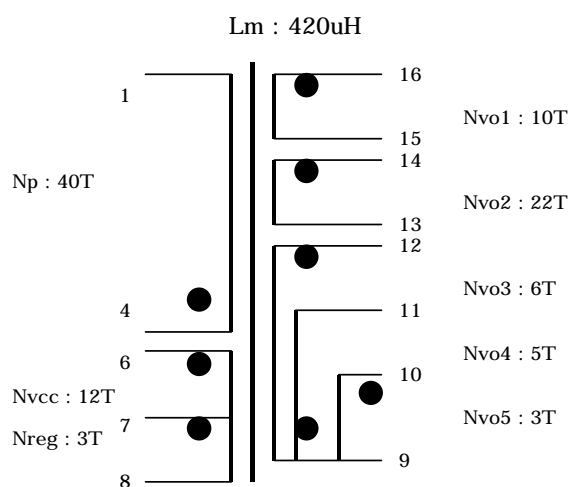


6. Burst mode operation : In order to minimize the power dissipation at standby mode, FS8S0765RCB has a burst mode operation. In burst mode, the FPS reduces the effective switching frequency and output voltage. The FPS enters into burst mode when the voltage of the soft start pin is higher than 3V, no sync signal is applied and the feedback voltage is lower than 1V. During the burst mode operation, V_{cc} is hysteresis controlled between 11V and 12V. Once the FPS enters into burst mode, it stops switching operation until V_{cc} drops to 11V. When V_{cc} reaches 11V, the FPS starts switching with switching frequency of 40kHz and peak MOSFET current of 0.6 A until V_{cc} reaches 12V. When V_{cc} reaches 12V, the switching operation is terminated again until V_{cc} reduces to 11V. Figure 9 shows operating waveforms. The soft start during the initial start-up is shown in the section 1. During this period, there is no external sync signal and the switching frequency is 20kHz. The section 2 represents the normal mode operation. The switching frequency is synchronized with the external sync signal. In the section 3, the external sync signal is removed. However, the load still exists and thus the feedback voltage (V_{fb}) is higher than 1V. In this period, the FPS does the normal switching operation with switching frequency of 20kHz. The section 4 and 5 show the burst mode operation. At the end of the section 3, the load is eliminated and the feedback voltage (V_{fb}) drops below 1V forcing the FPS to stop switching operation. During the section 4, V_{cc} goes down to 11V. During section 5, V_{cc} is hysteresis controlled between 11V and 12V. When the external sync signal is applied on the pin 5, the FPS resumes its normal operation. In order to minimize the power con-

1. 80W Universal Input Power Supply For CRT Monitor



2. Transformer Schematic Diagram



3.Winding Specification

No	Pin (s→f)	Wire	Turns	Winding Method
Np1	4 → 1	$0.3^{\phi} \times 1$	40	Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
Nvo1	16 → 15	$0.3^{\phi} \times 1$	10	Center Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
Nreg	7 → 8	$0.2^{\phi} \times 1$	3	Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
Nvo2	14 → 13	$0.3^{\phi} \times 3$	22	Center Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
Np2	4 → 1	$0.3^{\phi} \times 1$	40	Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
Nvo3	12 → 9	$0.3^{\phi} \times 2$	6	Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
Nvo4	9 → 11	$0.3^{\phi} \times 1$	5	Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
Nvo5	10 → 9	$0.3^{\phi} \times 2$	3	Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
Nvcc	6 → 8	$0.2^{\phi} \times 1$	12	Solenoid Winding
Outer Insulation: Polyester Tape t = 0.050mm, 2Layers				

4.Electrical Charateristics

	Pin	Specification	Remarks
Inductance	1 - 4	420uH \pm 10%	300kHz, 1V
Leakage Inductance	1 - 4	5uH Max	2 nd all short

5. Core & Bobbin

Core : EER 3540

Bobbin : EER3540

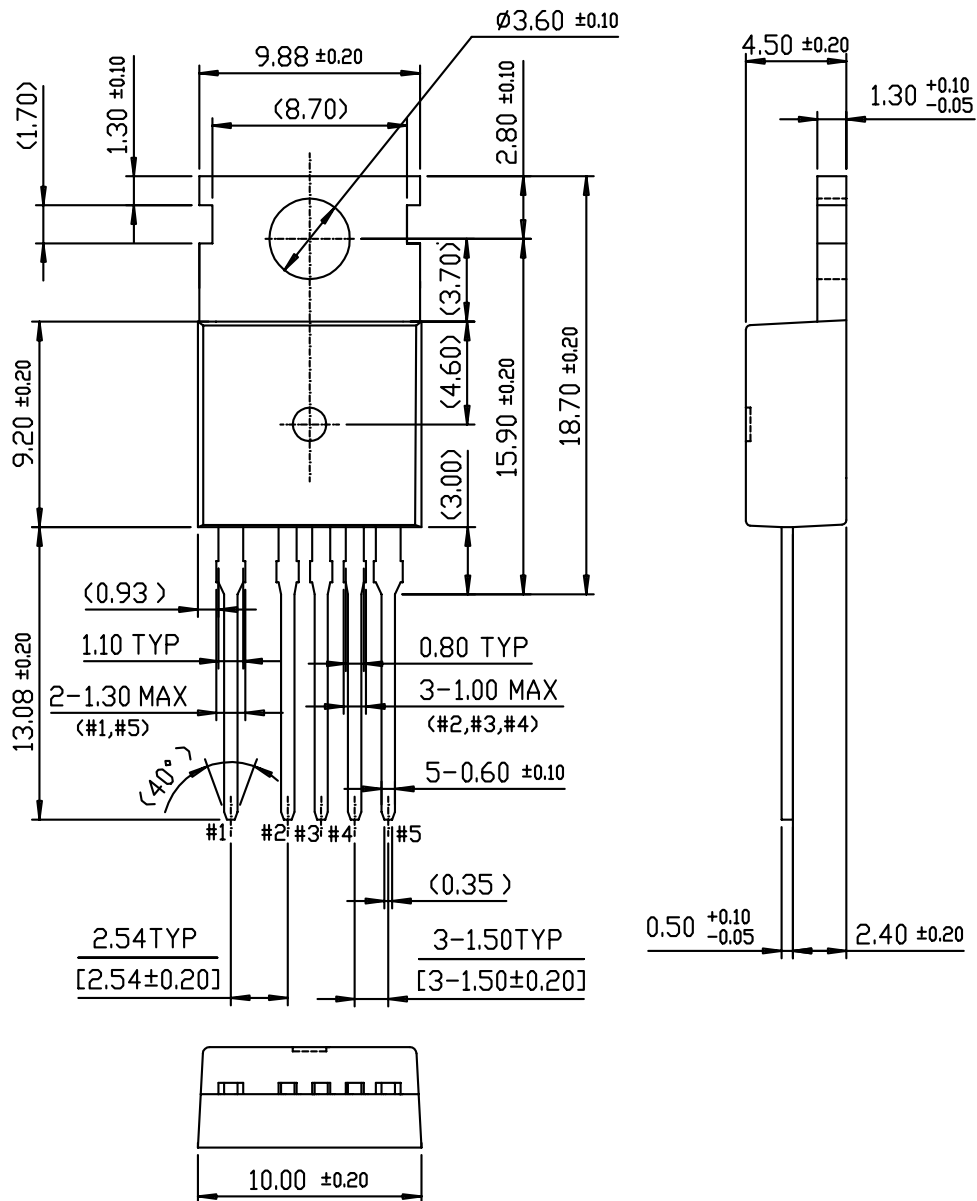
Ae(mm²) : 107

6.Demo Circuit Part List

Part	Value	Note	Part	Value	Note
Fuse			C201	22nF/160V	Electorlytic Capacitor
F101	3A/250V	-	C202	22nF/160V	Electorlytic Capacitor
NTC			C203	47nF/100V	Electorlytic Capacitor
RT101	10D-9	-	C204	47nF/100V	Electorlytic Capacitor
Resistor			C205	1000nF/25V	Electorlytic Capacitor
R101	56K	2W	C206	1000nF/25V	Electorlytic Capacitor
R102	3.3	1/4W	C207	1000nF/25V	Electorlytic Capacitor
R103	600K	1W	C208	1000nF/25V	Electorlytic Capacitor
R104	2.2K	1/4W	C209	1000nF/25V	Electorlytic Capacitor
R105	0.56K	1/4W	C210	1000nF/25V	Electorlytic Capacitor
R106	0.1K	1/4W	C211	0.1uF/50V	Ceramic Capacitor
R201	0.1K	1/4W	C301	4.7nF	AC Filter Capacitor
R202	4K	1/4W	C302	4.7nF	AC Filter Capacitor
R203	0.7K	1/4W			
			Sync trans	22mH	
Inductor					
L201 ~ L205	13uH				
			Diode		
			D101	UF4007	
Capacitor			D102	TVR10G	
C101	471D10	TNR	D103	TVR10G	
C102	100nF	Box Capacitor	D201	UF4007	
C103	4.7nF	AC Filter Capacitor	D202	UF5404	
C104	4.7nF	AC Filter Capacitor	D203	UF5402	
C105	100nF	Box Capacitor	D204	UF5402	
C106	220uF/400V	Electorlytic Capacitor	D205	UF5401	
C107	10nF/630V	Caramic Capacitor			
C108	22uF/50V	Electorlytic Capacitor	BD101	KBL406	Bridge Diode
C109	47nF/50V	Caramic Capacitor	Line Filter		
C110	1uF/50V	Electorlytic Capacitor	LF101	24mH	
C111	0.1uF/50V	Caramic Capacitor	IC		
C112	47uF/50V	Electorlytic Capacitor	IC101	FS8S0765RC	(7A, 650V)
C113	1uF/50v	Electorlytic Capacitor	IC201	KSC945	NPN Transistor
C114	1nF/50V	Caramic Capacitor			
C115	1nF/50V	Caramic Capacitor			

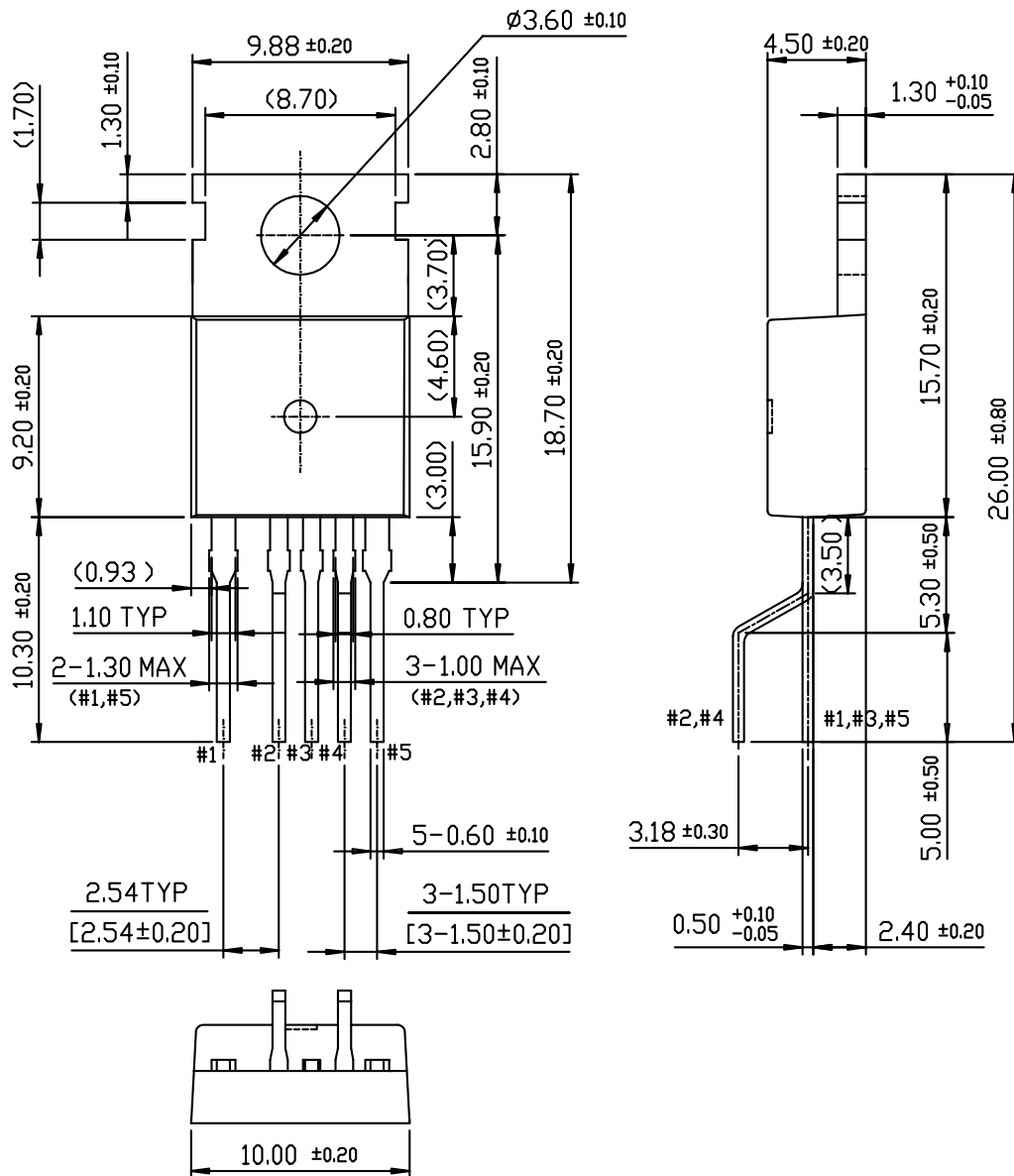
Package Dimensions

TO-220-5L



Package Dimensions (Continued)

TO-220-5L(Forming)



Ordering Information

Product Number	Package	Marking Code	BVdss	Rds(on)Max.
FS8S0765RCBTU	TO-220-5L	8S0765RCB	650V	1.6
FS8S0765RCBYDTU	TO-220-5L(Forming)			

TU : Non Forming Type

YDTU : Forming Type

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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