64K × 64 BURST PIPELINED HIGH-SPEED CMOS STATIC RAM

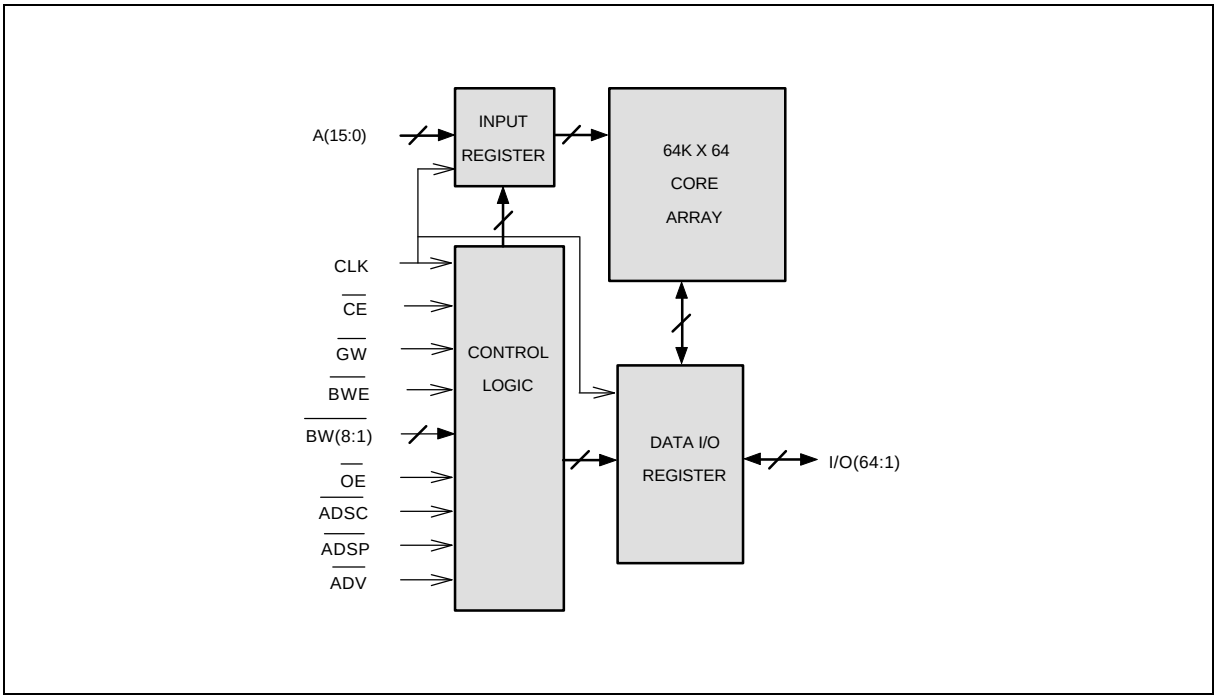
GENERAL DESCRIPTION

The W25P240A is a high-speed, low-power, synchronous-burst pipelined CMOS static RAM organized as 65,536 × 64 bits that operates on a single 3.3-volt power supply. A built-in two-bit burst address counter supports Pentium™ burst mode.

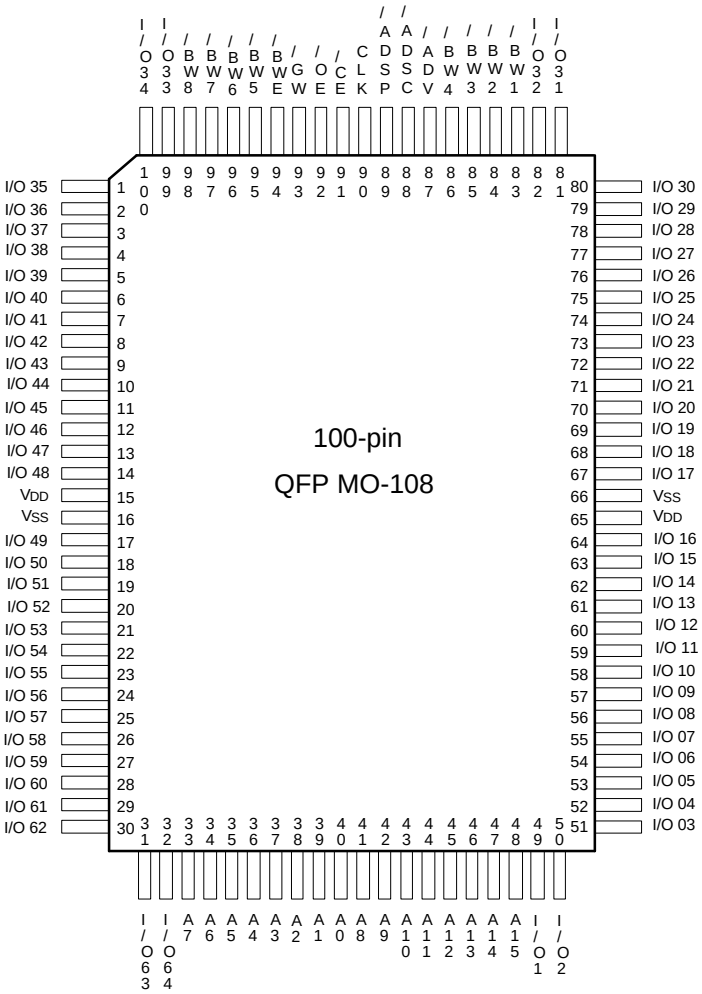
FEATURES

- Synchronous operation
- Support 66/75 MHz bus speed
- Single +3.3V power supply
- Individual byte write capability
- 3.3V LVTTL compatible I/O
- Clock-controlled and registered input
- Asynchronous output enable
- Internal burst counter supports Intel burst mode
- Packaged in 100-pin QFP

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	TYPE	DESCRIPTION
A0–A15	Input, Synchronous	Host Address
I/O1–I/O64	I/O, Synchronous	Data Inputs/Outputs
CLK	Input, Clock	Processor Host Bus Clock
$\overline{CE}$	Input, Synchronous	Chip Enables
$\overline{GW}$	Input, Synchronous	Global Write
$\overline{BWE}$	Input, Synchronous	Byte Write Enable from Cache Controller
$\overline{BW1} - \overline{BW8}$	Input, Synchronous	Host Bus Byte Enables used with $\overline{BWE}$
$\overline{OE}$	Input, Asynchronous	Output Enable Input
$\overline{ADV}$	Input, Synchronous	Internal Burst Address Counter Advance
$\overline{ADSC}$	Input, Synchronous	Address Status from chip set
$\overline{ADSP}$	Input, Synchronous	Address Status from CPU
V_{DD}		Power Supply
V_{SS}		Ground

FUNCTIONAL DESCRIPTION

The W25P240A is a synchronous-burst pipelined SRAM designed for use in high-end personal computers. It supports only one burst address sequence for Intel™ systems. The burst cycles are initiated by $\overline{ADSP}$ or $\overline{ADSC}$ and the burst counter is incremented whenever $\overline{ADV}$ is sampled low.

Burst Address Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
External Start Address	00	01	10	11
Second Address	01	00	11	10
Third Address	10	11	00	01
Fourth Address	11	10	01	00

The device supports several types of write mode operations. $\overline{BWE}$ and $\overline{BW}$ [8:1] support individual byte writes. The $\overline{BE}$ [7:0] signals can be directly connected to the SRAM $\overline{BW}$ [8:1]. The $\overline{GW}$ signal is used to override the byte enable signals and allows the cache controller to write all bytes to the SRAM, no matter what the byte write enable signals are. The various write modes are indicated in the Write Table below. Note that in pipelined mode, the byte write enable signals are not latched by the SRAM with addresses but with data. In pipelined mode, the cache controller must ensure the SRAM latches both data and valid byte enable signals from the processor.

TRUTH TABLE

CYCLE	ADDRESS USED	$\overline{CE}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{OE}$	DATA	WRITE*
Unselected	No	1	X	0	X	X	Hi-Z	X
Begin Read	External	0	0	X	X	X	Hi-Z	X
Begin Read	External	0	1	0	X	X	Hi-Z	Read
Continue Read	Next	X	1	1	0	1	Hi-Z	Read
Continue Read	Next	X	1	1	0	0	D-Out	Read
Continue Read	Next	1	X	1	0	1	Hi-Z	Read
Continue Read	Next	1	X	1	0	0	D-Out	Read
Suspend Read	Current	X	1	1	1	1	Hi-Z	Read
Suspend Read	Current	X	1	1	1	0	D-Out	Read
Suspend Read	Current	1	X	1	1	1	Hi-Z	Read
Suspend Read	Current	1	X	1	1	0	D-Out	Read
Begin Write	Current	X	1	1	1	X	Hi-Z	Write
Begin Write	Current	1	X	1	1	X	Hi-Z	Write
Begin Write	External	0	1	0	X	X	Hi-Z	Write
Continue Write	Next	X	1	1	0	X	Hi-Z	Write
Continue Write	Next	1	X	1	0	X	Hi-Z	Write
Suspend Write	Current	X	1	1	1	X	Hi-Z	Write
Suspend Write	Current	1	X	1	1	X	Hi-Z	Write

Notes:

1. For a detailed definition of read/write, see the Write Table below.
2. An "X" means don't care, "1" means logic high, and "0" means logic low.
3. The $\overline{OE}$ pin enables the data output but is not synchronous with the clock. All signals of the SRAM are sampled synchronous to the bus clock except for the $\overline{OE}$ pin.
4. On a write cycle that follows a read cycle, $\overline{OE}$ must be inactive prior to the start of the write cycle to allow write data to set up the SRAM. $\overline{OE}$ must also disable the output buffer prior to the end of a write cycle to ensure the SRAM data hold timings are met.

WRITE TABLE

READ/WRITE FUNCTION	$\overline{GW}$	$\overline{BWE}$	$\overline{BW8}$	$\overline{BW7}$	$\overline{BW6}$	$\overline{BW5}$	$\overline{BW4}$	$\overline{BW3}$	$\overline{BW2}$	$\overline{BW1}$
Read	1	1	X	X	X	X	X	X	X	X
Read	1	0	1	1	1	1	1	1	1	1
Write byte 1 I/O1–I/O8	1	0	1	1	1	1	1	1	1	0
Write byte 2 I/O9–I/O16	1	0	1	1	1	1	1	1	0	1
Write byte 2, byte 1	1	0	1	1	1	1	1	1	0	0

Write Table, continued

READ/WRITE FUNCTION	$\overline{GW}$	$\overline{BWE}$	$\overline{BW8}$	$\overline{BW7}$	$\overline{BW6}$	$\overline{BW5}$	$\overline{BW4}$	$\overline{BW3}$	$\overline{BW2}$	$\overline{BW1}$
Write byte 3 I/O17–I/O24	1	0	1	1	1	1	1	0	1	1
Write byte 3, byte 1	1	0	1	1	1	1	1	0	1	0
Write byte 3, byte 2	1	0	1	1	1	1	1	0	0	1
Write byte 3, byte 2, byte 1	1	0	1	1	1	1	1	0	0	0
Write byte 4, I/O25–I/O32	1	0	1	1	1	1	0	1	1	1
Write byte 4, byte 1	1	0	1	1	1	1	0	1	1	0
Write byte 4, byte 2	1	0	1	1	1	1	0	1	0	1
Write byte 4, byte 2, byte 1	1	0	1	1	1	1	0	1	0	0
Write byte 4, byte 3	1	0	1	1	1	1	0	0	1	1
Write byte 4, byte 3, byte 1	1	0	1	1	1	1	0	0	1	0
Write byte 4, byte 3, byte 2	1	0	1	1	1	1	0	0	0	1
Write byte 4, byte 3, byte 2, byte 1	1	0	1	1	1	1	0	0	0	0
Write byte 5, I/O33–I/O40	1	0	1	1	1	0	1	1	1	1
Write byte 5, byte 1	1	0	1	1	1	0	1	1	1	0
Write byte 5, byte 2	1	0	1	1	1	0	1	1	0	1
Write byte 5, byte 2, byte 1	1	0	1	1	1	0	1	1	0	0
Write byte 5, byte 3	1	0	1	1	1	0	1	0	1	1
Write byte 5, byte 3, byte 1	1	0	1	1	1	0	1	0	1	0
Write byte 5, byte 3, byte 2	1	0	1	1	1	0	1	0	0	1
Write byte 5, byte 3, byte 2, byte 1	1	0	1	1	1	0	1	0	0	0
Write byte 5, byte 4	1	0	1	1	1	0	0	1	1	1
Write byte 5, byte 4, byte 1	1	0	1	1	1	0	0	1	1	0
Write byte 5, byte 4, byte 2	1	0	1	1	1	0	0	1	0	1
Write byte 5, byte 4, byte 2, byte 1	1	0	1	1	1	0	0	1	0	0
Write byte 5, byte 4, byte 3	1	0	1	1	1	0	0	0	1	1
Write byte 5, byte 4, byte 3, byte1	1	0	1	1	1	0	0	0	1	0
Write byte 5, byte 4, byte 3, byte2	1	0	1	1	1	0	0	0	0	1
Write byte 5, byte 4, byte 3, byte 2, byte 1	1	0	1	1	1	0	0	0	0	0
Write byte 6	1	0	1	1	0	1	1	1	1	1
Write byte 6, byte1	1	0	1	1	0	1	1	1	1	0
Write byte 6, byte2	1	0	1	1	0	1	1	1	0	1
Write byte 6, byte2, byte1	1	0	1	1	0	1	1	1	0	0
..... and so on	...	...	...	...	...	...	...	...	...	...
Write byte 8, byte 7, byte 6, byte 5, byte 4, byte 2, byte 1	1	0	0	0	0	0	0	1	0	0

Write Table, continued

READ/WRITE FUNCTION	$\overline{GW}$	$\overline{BWE}$	$\overline{BW8}$	$\overline{BW7}$	$\overline{BW6}$	$\overline{BW5}$	$\overline{BW4}$	$\overline{BW3}$	$\overline{BW2}$	$\overline{BW1}$
Write byte 8, byte 7, byte 6, byte 5, byte 4, byte 3	1	0	0	0	0	0	0	0	1	1
Write byte 8, byte 7, byte 6, byte 5, byte 4, byte 3, byte 1	1	0	0	0	0	0	0	0	1	0
Write byte 8, byte 7, byte 6, byte 5, byte 4, byte 3, byte 2	1	0	0	0	0	0	0	0	0	1
Write all bytes	1	0	0	0	0	0	0	0	0	0
Write all bytes	0	x	x	x	x	x	x	x	x	x

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to Vss	-0.5 to 4.6	V
Input/Output to V_{SS} Potential	V_{SS} -0.5 to V_{DD} +0.5	V
Allowable Power Dissipation	1.5	W
Storage Temperature	-65 to 150	°C
Operating Temperature	0 to +55	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(V_{DD} = 3.15V to 3.6V, V_{SS} = 0V, T_A = 0 to 55° C)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Low Voltage	V_{IL}	-	-0.5	-	+0.8	V
Input High Voltage	V_{IH}	-	+2.0	-	V_{DD} +0.3	V
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{DD}	-10	-	+10	µA
Output Leakage Current	I_{LO}	$V_{I/O}$ = V_{SS} to V_{DD}, and data I/O pins in high-Z state defined in truth table	-10	-	+ 10	µA
Output Low Voltage	V_{OL}	I_{OL} = +8.0 mA	-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0 mA	2.4	-	-	V
Operating Current	I_{DD}	$T_{CYC} \geq$ min., I/O = 0 mA	-	-	350	mA
Standby Current	I_{SB}	Unselected mode defined in truth table, V_{IN}, V_{IO} = V_{IH} (min.) /V_{IL} (max.) $T_{CYC} \geq$ min.	-	-	80	mA

Note: Typical characteristics are measured at V_{DD} = 3.3V, T_A = 25° C.

CAPACITANCE

(V_{DD} = 3.3V, T_A = 25° C, f = 1 MHz)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0V	8	pF

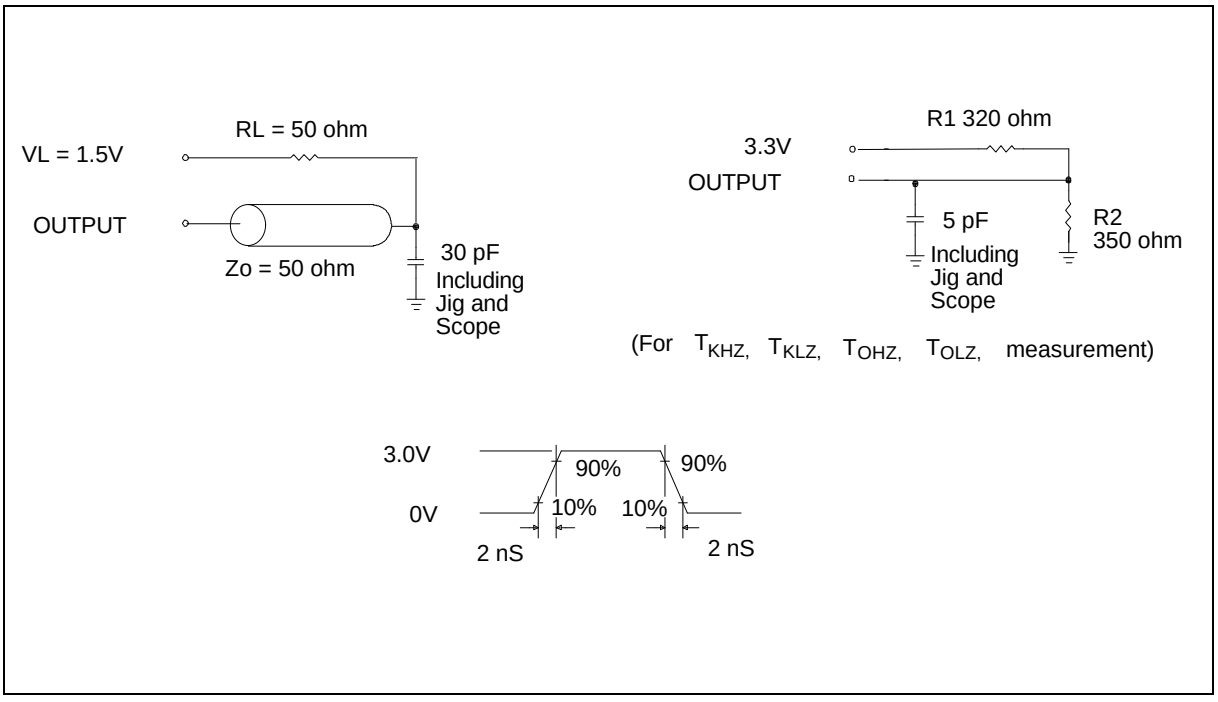
Note: These parameters are sampled but not 100% tested.

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	2 nS
Input and Output Timing Reference Level	1.5V
Output Load	C_L = 30 pF, I_{OH}/I_{OL} = -4 mA/8 mA

AC Test Loads and Waveform



AC Timing Characteristics

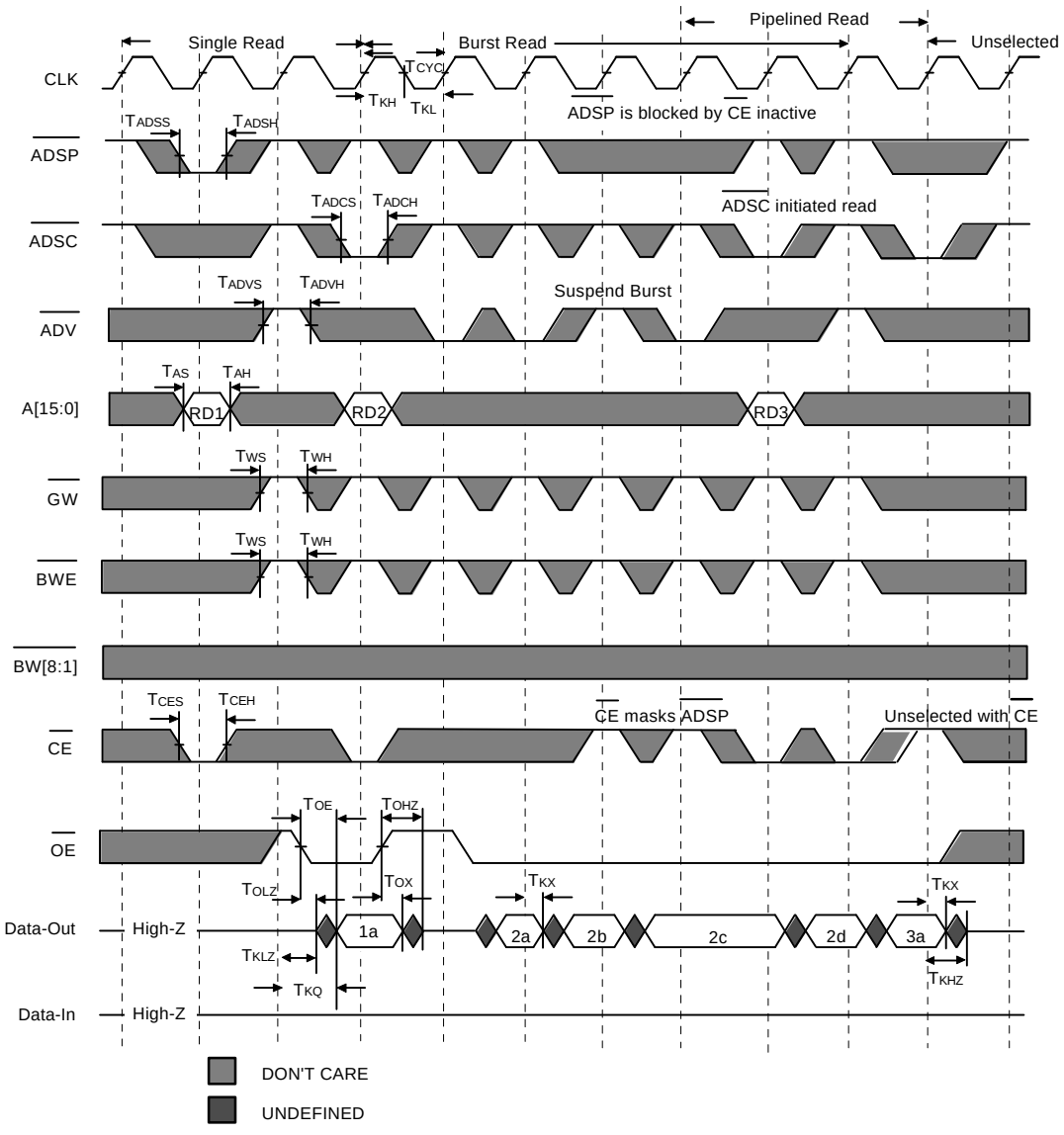
(V_{DD} = 3.15V to 3.6V, V_{SS} = 0V, T_A = 0 to 55° C)

PARAMETER	SYMBOL	W25P240A-6		W25P240A-6A		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Add. Setup Time	TAS	1.5	-	1.5	-	nS	
Add. Hold Time	TAH	1.5	-	1.5	-	nS	
Write Data Setup Time	TDS	2.5	-	2.5	-	nS	
Write Data Hold Time	TDH	0.5	-	0.5	-	nS	
$\overline{ADV}$ Setup Time	TADVS	2.5	-	2.5	-	nS	
$\overline{ADV}$ Hold Time	TADVH	0.5	-	0.5	-	nS	
$\overline{ADSP}$ Setup Time	TADSS	2.5	-	2.5	-	nS	
$\overline{ADSP}$ Hold Time	TADSH	0.5	-	0.5	-	nS	
$\overline{ADSC}$ Setup Time	TADCS	2.5	-	2.5	-	nS	
$\overline{ADSC}$ Hold Time	TADCH	0.5	-	0.5	-	nS	
$\overline{CE}$, Setup Time	TCES	2.5	-	2.5	-	nS	
$\overline{CE}$, Hold Time	TCEH	0.5	-	0.5	-	nS	
$\overline{GW}$, $\overline{BWE}$ X Setup Time	TWS	2.0	-	2.0	-	nS	
$\overline{GW}$, $\overline{BWE}$ X Hold Time	TWH	1.0	-	1.0	-	nS	
Clock Cycle Time	TCYC	13.3	-	15	-	nS	
Clock High Pulse Width	TKH	5	-	6	-	nS	
Clock Low Pulse Width	TKL	5	-	6	-	nS	
Clock to Output Valid	TKQ	-	6	-	7	nS	
Clock to Output High-Z	TKHZ	2	13.3	2	15	nS	Note
Clock to Output Low-Z	TKLZ	0	-	0	-	nS	Note
Clock to Output Invalid	TKX	2	-	2	-	nS	Note
Output Enable to Output Valid	TOE	-	6	-	7	nS	
Output Enable to Output High-Z	TOHZ	-	6	-	7	nS	Note
Output Enable to Output Low-Z	TOLZ	0	-	0	-	nS	Note
Output Enable to Output Invalid	TOX	0	-	0	-	nS	

Note: These parameters are sampled but not 100% tested.

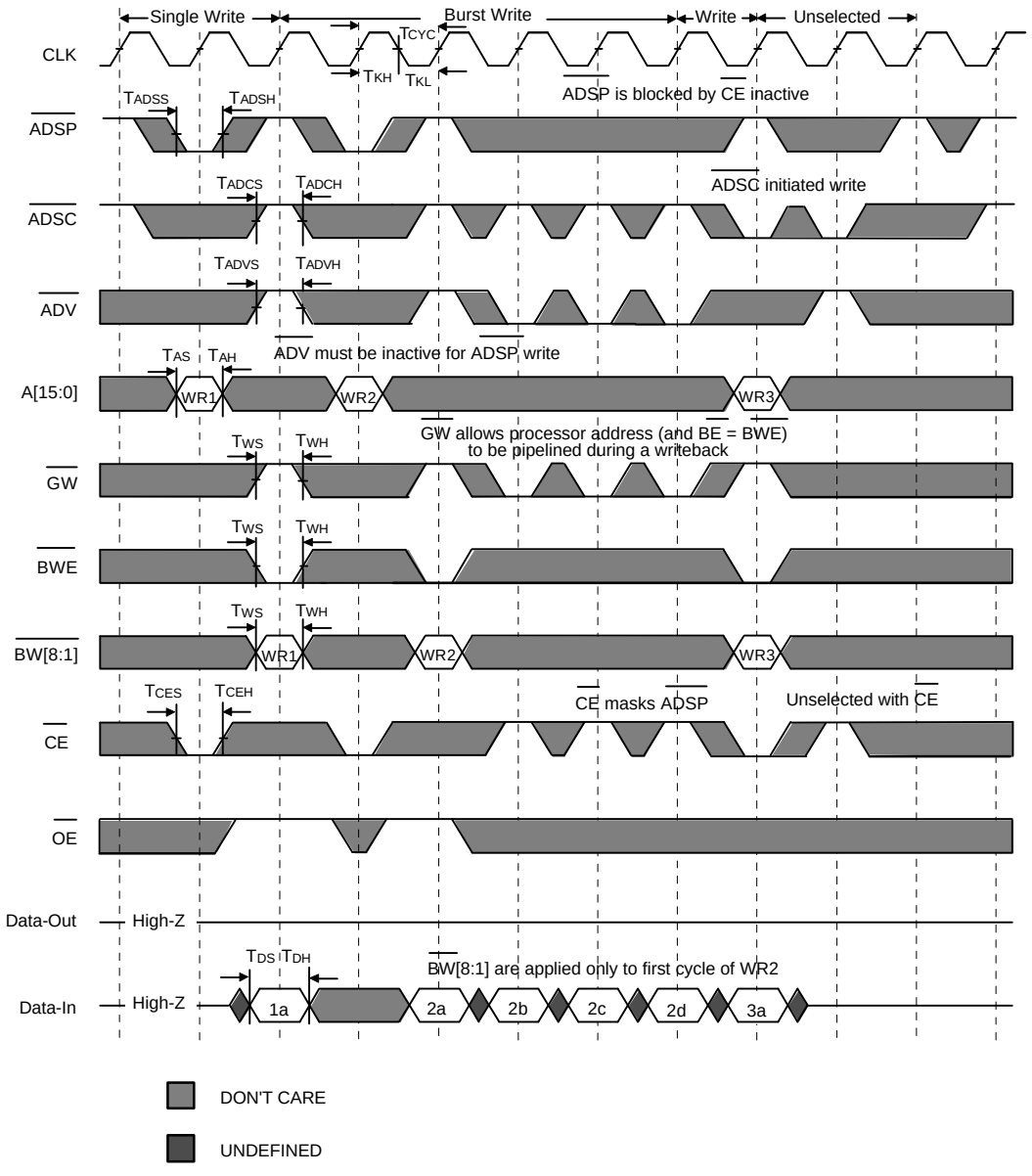
TIMING WAVEFORMS

Read Cycle Timing



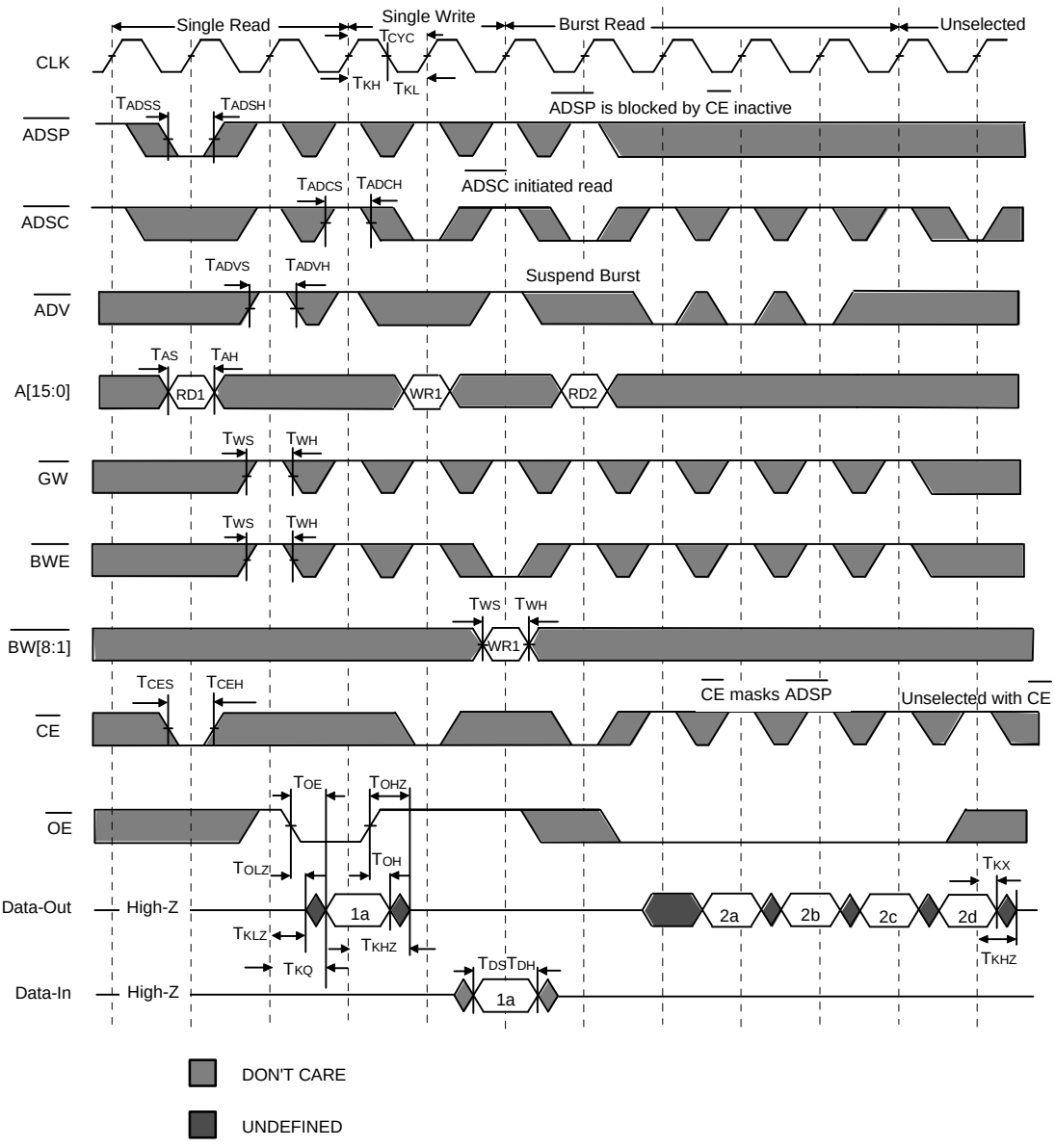
Timing Waveforms, continued

Write Cycle Timing



Timing Waveforms, continued

Read/Write Cycle Timing



ORDERING INFORMATION

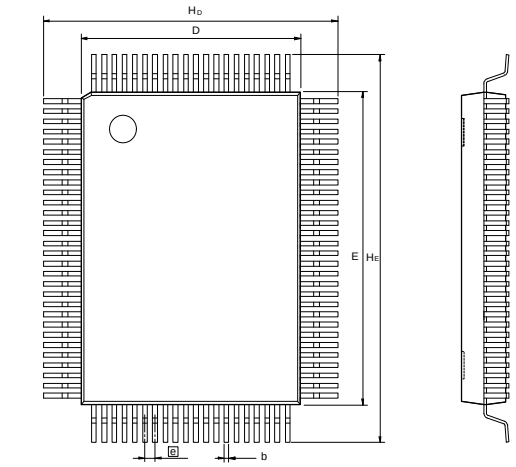
PART NO.	SUPPORTABLE BUS SPEED (MHz)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (mA)	PACKAGE
W25P240AF-6	75	350	80	100-pin QFP
W25P240AF-6A	66	350	80	100-pin QFP

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

PACKAGE DIMENSIONS

100-pin QFP



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	—	—	—	—
A_1	0.01	0.014	0.018	0.25	0.35	0.45
A_2	0.101	0.107	0.113	2.57	2.72	2.87
b	0.008	0.012	0.016	0.20	0.30	0.40
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.555	13.90	14.00	14.10
E	0.783	0.787	0.791	19.90	20.00	20.10
e	0.020	0.026	0.032	0.498	0.65	0.802
H_D	0.669	0.677	0.685	17.00	17.20	17.40
H_E	0.905	0.913	0.921	23.00	23.20	23.40
L	0.025	0.031	0.037	0.65	0.80	0.95
L_1		0.063			1.60	
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

Notes:
1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.

VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Dec. 1996		Initial Issued
A2	Mar. 1997	1, 8, 12	Change part no. from W25P240A-75/66 to W25P240A-6/7
A3	Aug. 1997	8	A.C. Timing Characteristics: TAS from 2.5 to 1.5 TAH from 0.5 to 1.5 TWS from 2.5 to 2.0 TWH from 0.5 to 1.0
		6, 8	Working temperature range from 70–0° C to 55–0° C
A4	Feb. 1998	8, 12	Part no. W25P240AX-"7" change to "6A"

Headquarters
No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5796096
http://www.winbond.com.tw/
Voice & Fax-on-demand: 886-2-27197006

Taipei Office
11F, No. 115, Sec. 3, Min-Sheng East Rd.,
Taipei, Taiwan
TEL: 886-2-27190505
FAX: 886-2-27197502

Winbond Electronics (H.K.) Ltd.
Rm. 803, World Trade Square, Tower II,
123 Hoi Bun Rd., Kwun Tong,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064

Winbond Electronics North America Corp.
Winbond Memory Lab.
Winbond Microelectronics Corp.
Winbond Systems Lab.
2727 N. First Street, San Jose,
CA 95134, U.S.A.
TEL: 408-9436666
FAX: 408-5441798