

# LH5168

## CMOS 64K (8K × 8) Static Ram

### FEATURES

- 8,192 × 8 bit organization
- Access times: 80/100 ns (MAX.)
- Low-power consumption:
  - Operating:
    - 303 mW (MAX.) LH5168/D/N @ 80 ns
    - 248 mW (MAX.) LH5168/D/N/T/TR @ 100 ns
    - 275 mW (MAX.) LH5168H/HD/HN @ 100 ns
  - Standby:
    - 5.5 μW (MAX.) LH5168/D/N/T/TR
    - 16.5 μW (MAX.) LH5168H/HD/HN
- Fully-static operation
- Three-state outputs
- Single +5 V power supply
- TTL compatible I/O
- Pin compatible to 64K bit EPROM
- Wide temp. range available
  - LH5168: -10 to +70°C
  - LH5168H: -40 to +85°C
- Packages:
  - 28-pin, 600-mil DIP
  - 28-pin, 300-mil SK-DIP
  - 28-pin, 450-mil SOP
  - 28-pin, 8 × 13 mm<sup>2</sup> TSOP (Type I)

### DESCRIPTION

The LH5168 is a static RAM organized as 8,192 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

The LH5168H is designed for wide temperature range from -40 to +85°C.

### PIN CONNECTIONS

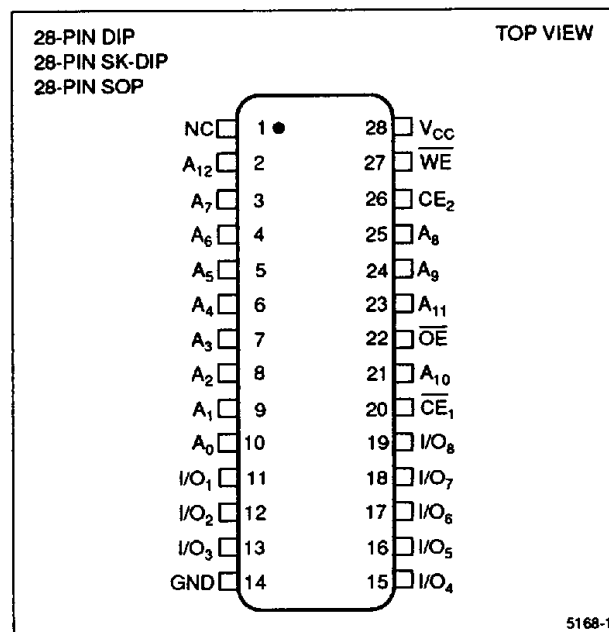


Figure 1. Pin Connections for DIP, SK-DIP, and SOP Packages

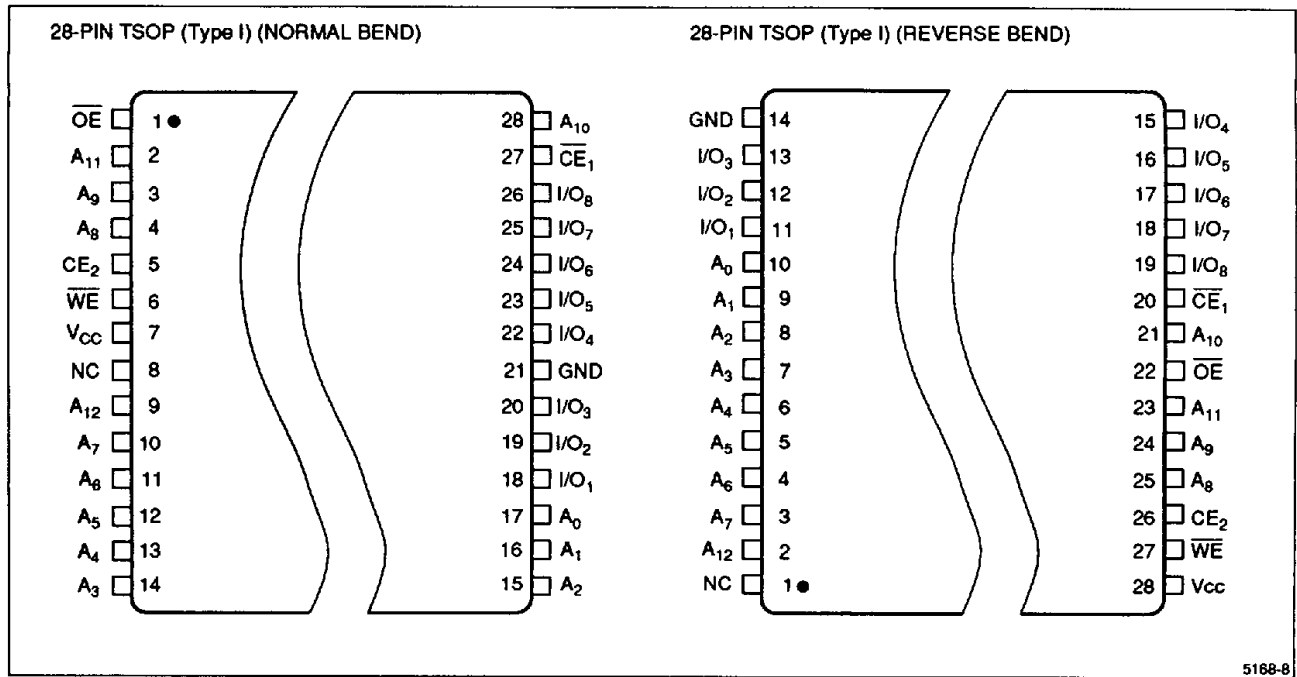
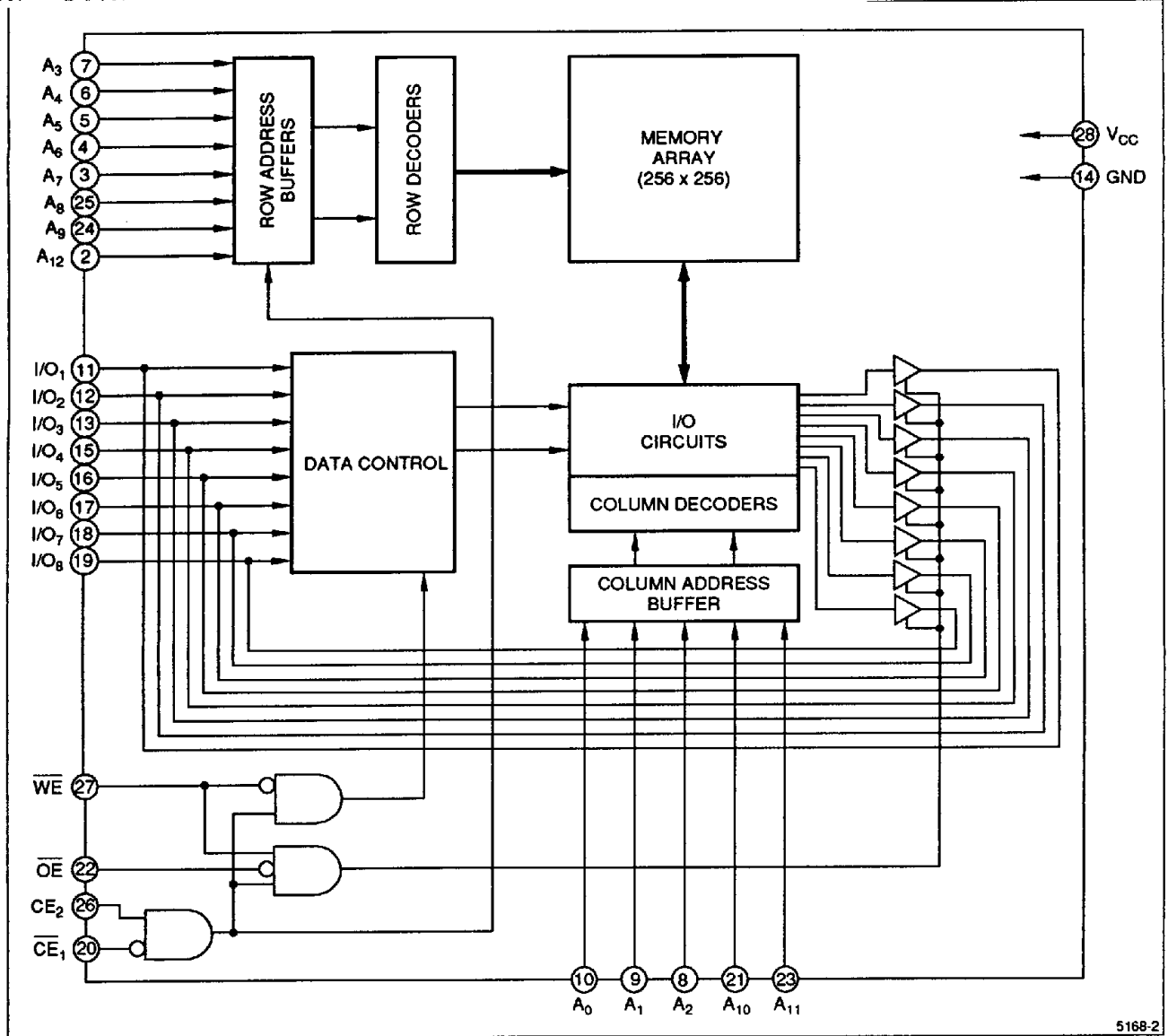


Figure 2. Pin Connections for TSOP Packages

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5168-2

Figure 3. LH5168 Block Diagram

**PIN DESCRIPTION**

SIGNAL	PIN NAME
A <sub>0</sub> - A <sub>12</sub>	Address inputs
$\overline{CE}_1$ - $\overline{CE}_2$	Chip Enable input
$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input

SIGNAL	PIN NAME
I/O <sub>1</sub> - I/O <sub>8</sub>	Data inputs and outputs
V <sub>cc</sub>	Power supply
GND	Ground
NC	Non-connection

## TRUTH TABLE

$\overline{CE}_1$	$CE_2$	$\overline{WE}$	$\overline{OE}$	MODE	I/O <sub>1</sub> - I/O <sub>8</sub>	SUPPLY CURRENT	NOTE
H	X	X	X	Deselect	High-Z	Standby (I <sub>SB</sub> )	1
X	L	X	X	Deselect	High-Z	Standby (I <sub>SB</sub> )	1
L	H	L	X	Write	D <sub>IN</sub>	Operating (I <sub>CC</sub> )	
L	H	H	L	Read	D <sub>OUT</sub>	Operating (I <sub>CC</sub> )	
L	H	H	H	Output disable	High-Z	Operating (I <sub>CC</sub> )	

## NOTE:

- X = H or L

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	80 ns	100 ns	UNIT	NOTE
		RATING	RATING		
Supply voltage	V <sub>CC</sub>	-0.3 to +7.0	-0.3 to +7.0	V	1
Input voltage	V <sub>IN</sub>	-0.5 to V <sub>CC</sub> + 0.5	-0.3 to V <sub>CC</sub> + 0.3	V	1
Operating temperature	T <sub>opr</sub>	-10 to +70	-10 to +70	°C	2
			-40 to +85	°C	3
Storage temperature	T <sub>stg</sub>	-55 to +150	-55 to +150	°C	

## NOTES:

- The maximum applicable voltage on any pin with respect to GND.
- LH5168/D/N
- LH5168H/HD/HN

## RECOMMENDED OPERATING CONDITIONS (Note 1)

PARAMETER	SYMBOL	80 ns			100 ns			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	4.5	5.0	5.5	V
Input voltage	V <sub>IH</sub>	2.2		V <sub>CC</sub> + 0.5	2.2		V <sub>CC</sub> + 0.3	V
	V <sub>IL</sub>	-0.5		0.8	-0.3		0.8	V

## NOTE:

- T<sub>A</sub> = -10 to +70°C (LH5168/D/N), T<sub>A</sub> = -40 to +85°C (LH5168H/HD/HN).

DC CHARACTERISTICS<sup>1</sup> (V<sub>CC</sub> = 5 V ± 10%)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = 0 to V <sub>CC</sub>		1.0	μA	
Output leakage current	I <sub>LO</sub>	$\overline{CE}_1 = V_{IH}$ or $CE_2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ V <sub>I/O</sub> = 0 to V <sub>CC</sub>		1.0	μA	
Operating current	I <sub>CC</sub>	$\overline{CE}_1 = V_{IL}$ , V <sub>IN</sub> = V <sub>IL</sub> to V <sub>IH</sub> CE <sub>2</sub> = V <sub>IH</sub> , Outputs open	t <sub>CYCLE</sub> = 80 ns	55	mA	
		$\overline{CE}_1 = V_{IL}$ , V <sub>IN</sub> = V <sub>IL</sub> to V <sub>IH</sub> CE <sub>2</sub> = V <sub>IH</sub> , Outputs open	t <sub>CYCLE</sub> = 100 ns	45		2
		$\overline{CE}_1 = V_{IL}$ , V <sub>IN</sub> = 0.2 V to V <sub>CC</sub> - 0.2 V CE <sub>2</sub> = V <sub>IH</sub> , Outputs open	t <sub>CYCLE</sub> = 1.0 μs	50		3
Standby current	I <sub>SB1</sub>	$\overline{CE}_1 = V_{IH}$ or CE <sub>2</sub> = V <sub>IL</sub>		10	mA	
	I <sub>SB</sub>	CE <sub>2</sub> ≤ 0.2 V or CE <sub>1</sub> , CE <sub>2</sub> ≥ V <sub>CC</sub> - 0.2 V	T <sub>A</sub> ≤ 70°C T <sub>A</sub> ≤ 85°C	1.0	μA	2
Output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1 mA		0.4	V	
	V <sub>OH</sub>	I <sub>OH</sub> = -1 mA	2.4		V	

## NOTES:

- T<sub>A</sub> = -10 to 70°C (LH5168/D/N/T/TR), T<sub>A</sub> = -40 to +85°C (LH5168H/HD/HN)
- LH5168/D/N/T/TR
- LH5168H/HD/HN

## AC CHARACTERISTICS <sup>1</sup>

### (1) READ CYCLE ( $V_{CC} = 5 V \pm 10\%$ )

PARAMETER	SYMBOL	80 ns		100 ns		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Read cycle	$t_{RC}$	80		100		ns	
Address access time	$t_{AA}$		80		100	ns	
Chip enable access time	$(\overline{CE}_1)$ $t_{ACE1}$		80		100	ns	
	$(CE_2)$ $t_{ACE2}$		80		100	ns	
Output enable access time	$t_{OE}$		40		40	ns	
Output hold time	$t_{OH}$	10		10		ns	
Chip enable to output in Low-Z	$(\overline{CE}_1)$ $t_{LZ1}$	10		10		ns	2
	$(CE_2)$ $t_{LZ2}$	10		10		ns	2
Output enable to output in Low-Z	$t_{OLZ}$	5		5		ns	2
Chip enable to output in High-Z	$(\overline{CE}_1)$ $t_{HZ1}$	0	30	0	30	ns	2
	$(CE_2)$ $t_{HZ2}$	0	30	0	30	ns	2
Output disable to output in High-Z	$t_{OHZ}$	0	20	0	20	ns	2

**NOTES:**

- $T_A = -10$  to  $+70^\circ C$  (LH5168/D/N/T/TR),  $T_A = -40$  to  $+85^\circ C$  (LH5168H/HD/HN)
- Active output to high-impedance and high-impedance to output active tests specified for a  $\pm 500$  mV transition from steady state levels into the test load.  $C_{LOAD} = 5$  pF.

### (2) WRITE CYCLE ( $V_{CC} = 5 V \pm 10\%$ )

PARAMETER	SYMBOL	80 ns		100 ns		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Write cycle time	$t_{WC}$	80		100		ns	
Chip enable to end of write	$t_{CW}$	70		80		ns	
Address valid to end of write	$t_{AW}$	70		80		ns	
Address setup time	$t_{AS}$	0		0		ns	
Write pulse width	$t_{WP}$	60		60		ns	
Write recovery time	$t_{WR}$	0		0		ns	
Data valid to end of write	$t_{DW}$	40		40		ns	
Data hold time	$t_{DH}$	0		0		ns	
Output active from end of write	$t_{OW}$	10		10		ns	1
$\overline{WE}$ to output in High-Z	$t_{WZ}$	0	30	0	30	ns	1
$\overline{OE}$ to output in High-Z	$t_{OHZ}$	0	20	0	20	ns	1

**NOTE:**

- Active output to high-impedance and high-impedance to output active tests specified for a  $\pm 500$  mV transition from steady state levels into the test load.  $C_{LOAD} = 5$  pF.

## AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.6 to 2.4 V
Input rise/fall time	10 ns
Timing reference level	1.5 V
Output load conditions	(1TTL + $C_L = 100$ pF)

CAPACITANCE<sup>1</sup> (T<sub>A</sub> = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0 V			7	pF
Input/output capacitance	C <sub>VO</sub>	V <sub>VO</sub> = 0 V			10	pF

NOTE:

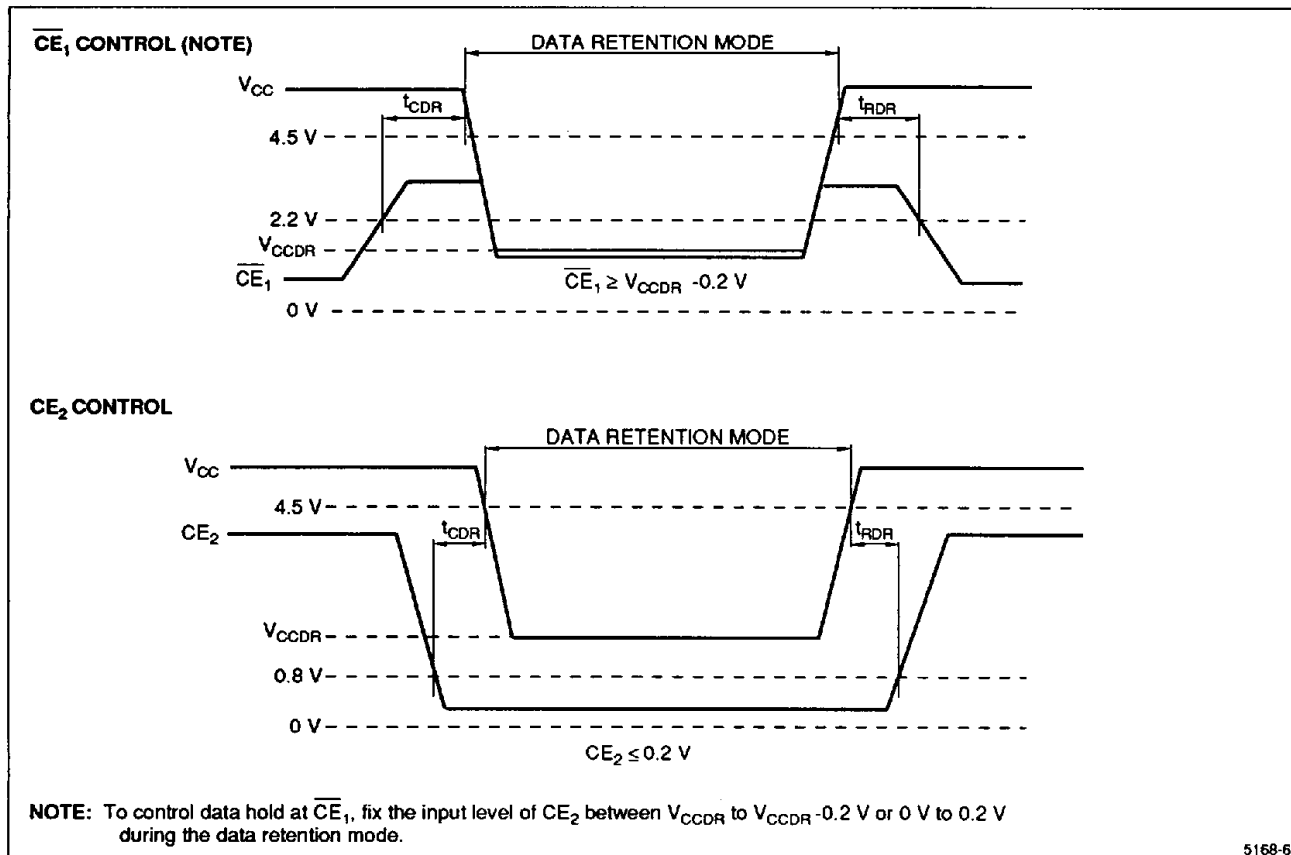
1. This parameter is sampled and not production tested.

DATA RETENTION CHARACTERISTICS<sup>1</sup>

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Data retention voltage	V <sub>CCDR</sub>	CE <sub>2</sub> ≤ 0.2 V or CE <sub>1</sub> , CE <sub>2</sub> ≥ V <sub>CC</sub> - 0.2 V	2.0		V	
Data retention current	I <sub>CCDR</sub>	V <sub>CCDR</sub> = 3 V, CE <sub>2</sub> ≤ 0.2 V or CE <sub>1</sub> , CE <sub>2</sub> ≥ V <sub>CCDR</sub> - 0.2 V		0.6	μA	2
				1.5	μA	3
Chip disable to data retention	t <sub>CDR</sub>		0		ns	
Recovery time	t <sub>RDR</sub>		t <sub>RC</sub>		ns	4

NOTES:

1. T<sub>A</sub> = -10 to +70°C (LH5168/D/N/T/TR), T<sub>A</sub> = -40 to +85°C (LH5168H/HD/HN)
2. LH5168/D/N/T/TR at T<sub>A</sub> ≤ 70°C
3. LH5168H/HD/HN at T<sub>A</sub> ≤ 85°C
4. t<sub>RC</sub> = Read cycle time



5168-6

Figure 4. Low Voltage Data Retention

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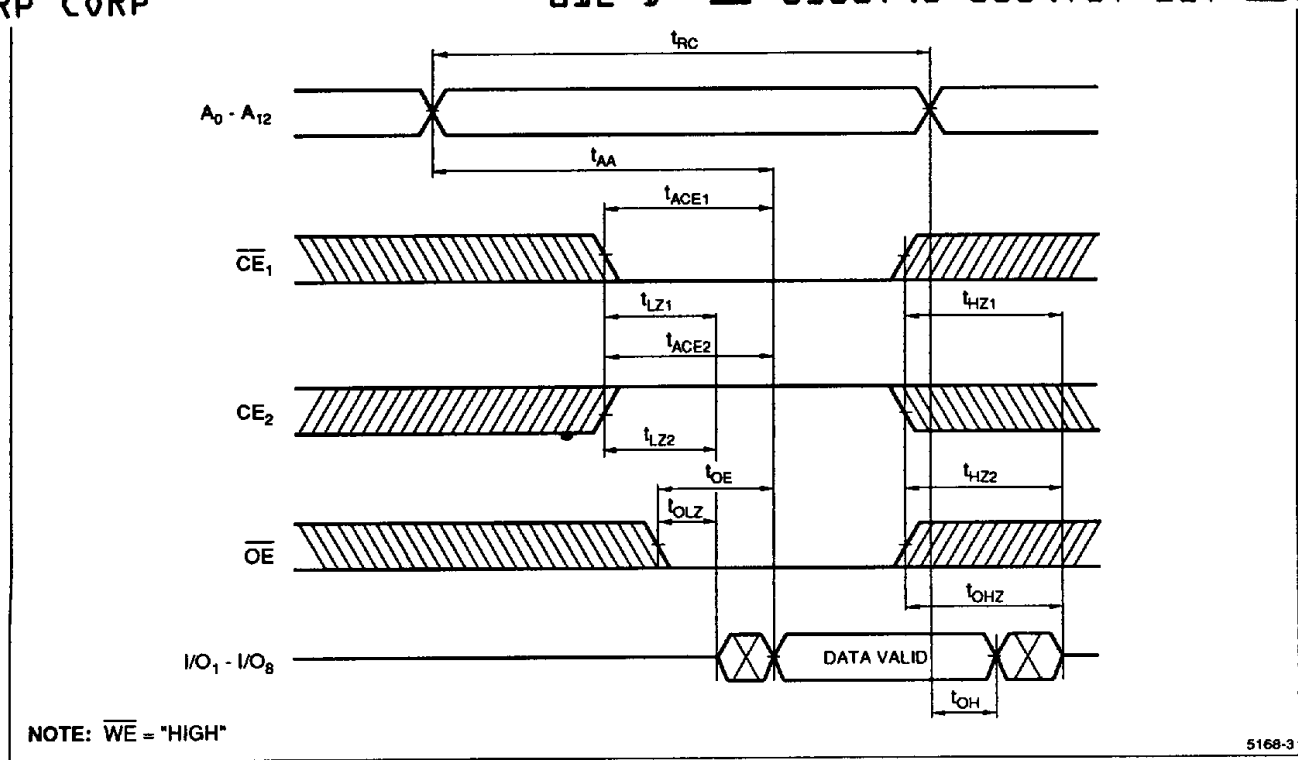
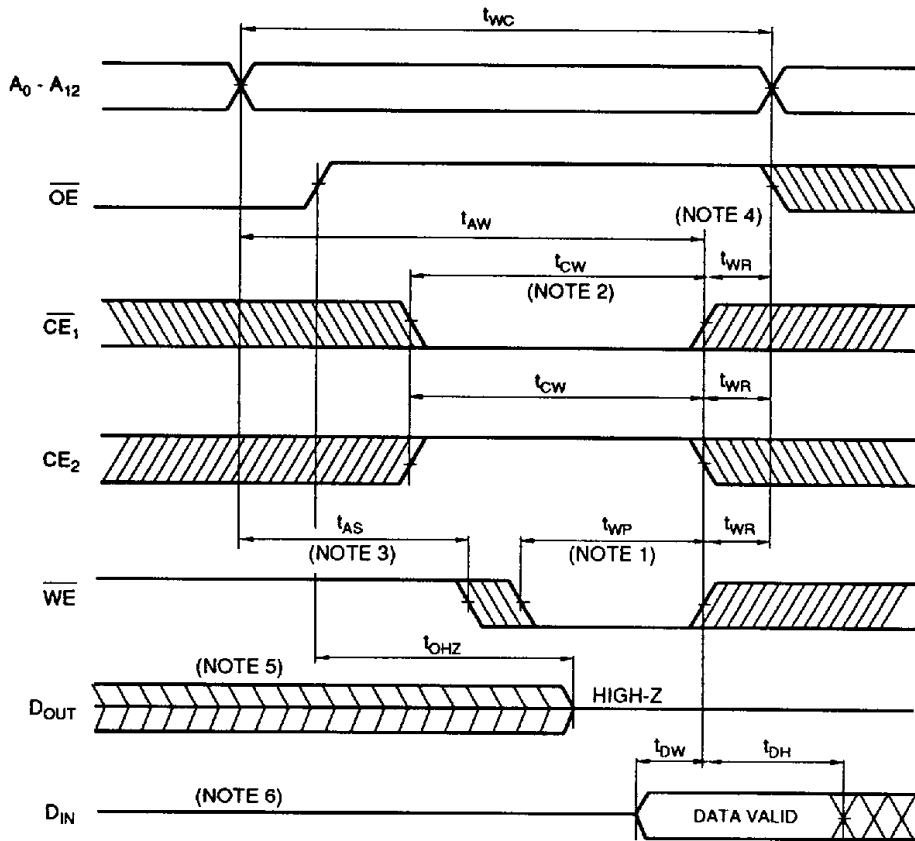


Figure 5. Read Cycle



**NOTES:**

1. The writing occurs during the overlap ( $t_{WP}$ ) of  $\overline{CE}_1 = \text{"LOW"}$ ,  $CE_2 = \text{"HIGH"}$ , and  $\overline{WE} = \text{"LOW"}$ .
2.  $t_{CW}$  is defined as the time from the last occurring transition, either  $\overline{CE}_1$  LOW transition or  $CE_2$  HIGH transition, to the time when the writing is finished.
3.  $t_{AS}$  is defined as the time from address change to writing start.
4.  $t_{WR}$  is defined as the time from writing finish to address change.
5. If  $\overline{CE}_1$  LOW transition or  $CE_2$  HIGH transition occurs at the same time or after  $\overline{WE}$  LOW transition, the output will remain high-impedance.
6. While the I/O pins are in the output state, input signals with the opposite logic level must not be applied.

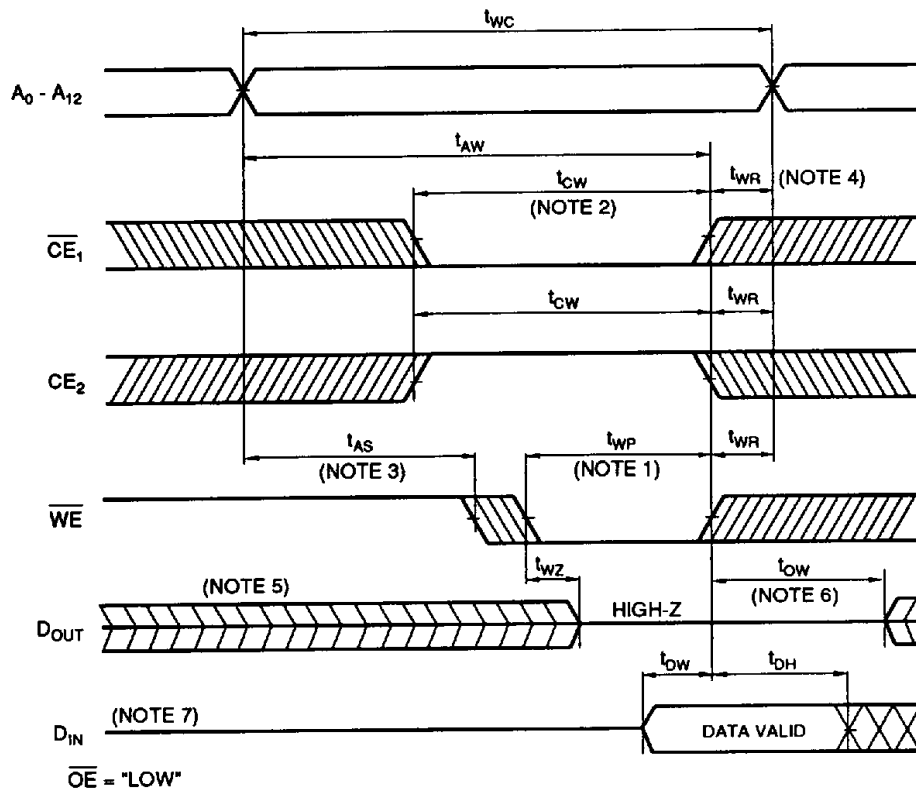
5168-4

**Figure 6. Write Cycle 1**



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NOTES:

1. The writing occurs during the overlap ( $t_{WP}$ ) of  $\overline{CE}_1 = \text{"LOW"}$ ,  $CE_2 = \text{"HIGH"}$ , and  $\overline{WE} = \text{"LOW"}$ .
2.  $t_{CW}$  is defined as the time from the last occurring transition, either  $\overline{CE}_1$  LOW transition or  $CE_2$  HIGH transition, to the time when the writing is finished.
3.  $t_{AS}$  is defined as the time from address change to writing start.
4.  $t_{WR}$  is defined as the time from writing finish to address change.
5. If  $\overline{CE}_1$  LOW transition or  $CE_2$  HIGH transition occurs at the same time or after  $\overline{WE}$  LOW transition, the output will remain high-impedance.
6. If  $\overline{CE}_1$  HIGH transition or  $CE_2$  LOW transition occurs at the same time or before  $\overline{WE}$  HIGH transition, the output will remain high-impedance.
7. While the I/O pins are in the output state, input signals with the opposite logic level must not be applied.

5168-5

Figure 7. Write Cycle 2

ORDERING INFORMATION

LH5168 Device Type	X Operating Temperature	X Package	- ## Speed
			{ 10L 100 80L 80 Access Time (ns)
			{ Blank 28 pin, 600-mil DIP (DIP 28-P-600) D 28-pin, 300-mil SK-DIP (SK-DIP28-P-300) N 28-pin, 450-mil SOP (SOP28-P-450) T 28-pin, 8 x 13 mm <sup>2</sup> TSOP (Type I) (TSOP28-P-0813) TR 28-pin, 8 x 13 mm <sup>2</sup> TSOP (Type I) Reverse Bend (TSOP28-P-0813)
			{ Blank -10 to 70°C H -40 to +85°C
CMOS 64K (8K x 8) Static RAM			
<b>Example:</b> LH5168D-10L (CMOS 64K (8K x 8) Static RAM, 100 ns, 28-pin, 300-mil SK-DIP)			

5168-7