LH52B256

CMOS 256K (32K × 8) Static RAM

FEATURES

- Access Times: 70/90/100 ns
- Automatic Power Down During Long Read Cycles
- Low-Power Standby When Deselected
- TTL Compatible I/O
- Single +5 V Power Supply
- Fully-Static Operation
- 2 V Data Retention
- Packages:
  - 28-Pin, 600-mil DIP
  - 28-Pin, 300-mil SK-DIP
  - 28-Pin, 450-mil SOP
  - 28-Pin, 8 × 13 mm^2 TSOP (Type I)

FUNCTIONAL DESCRIPTION

The LH52B256 is a high-density 262,144 bit static RAM organized as 32K × 8. An efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enable ($\overline{CE}$) control permits Read and Write operations when active (LOW) or places the RAM in a low-power standby mode when inactive (HIGH). Standby power (I_{SB1}) drops to its lowest level if $\overline{CE}$ is raised to within 0.2 V of V_{CC}.

Write cycles occur when both Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) are LOW. Data is transferred from the I/O pins to the memory location specified by the 15 address lines. The proper use of the Output Enable control ($\overline{OE}$) can prevent bus contention.

When $\overline{CE}$ is LOW and $\overline{WE}$ is HIGH, a static Read will occur at the memory location specified by the address lines. $\overline{OE}$ must be brought LOW to enable the outputs. Since the device is fully static in operation, new Read cycles can be performed by simply changing the address. An Automatic Power Down feature decreases current consumption when Read cycles extend beyond their minimum cycle time.

High-frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

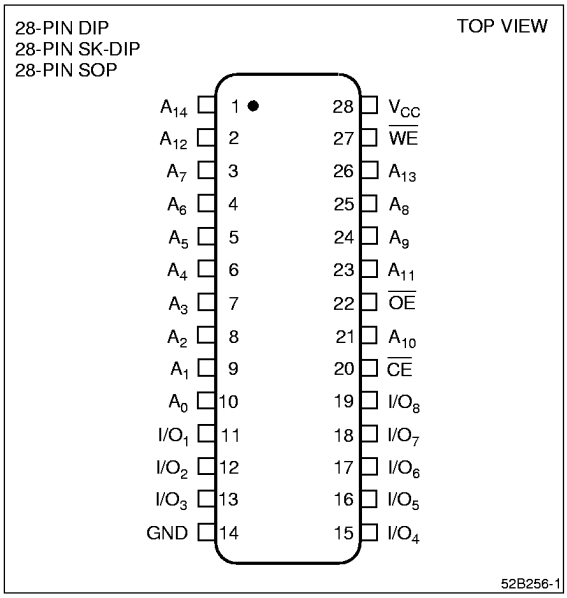


Figure 1. Pin Connections for DIP and SOP Packages

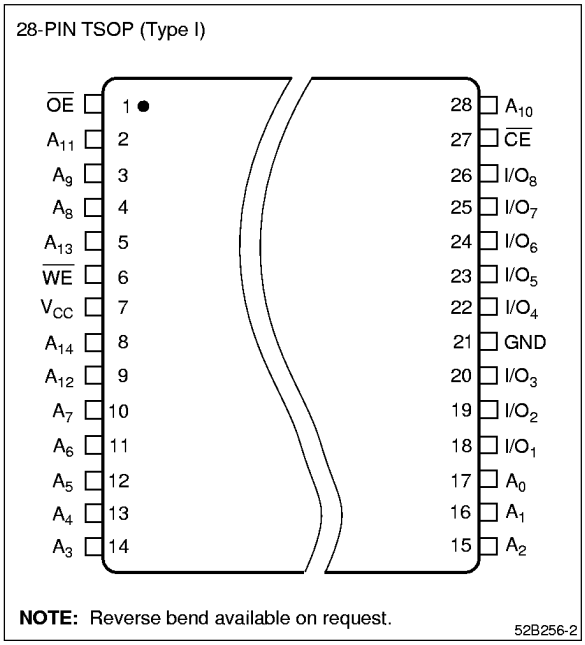


Figure 2. Pin Connections for TSOP Package

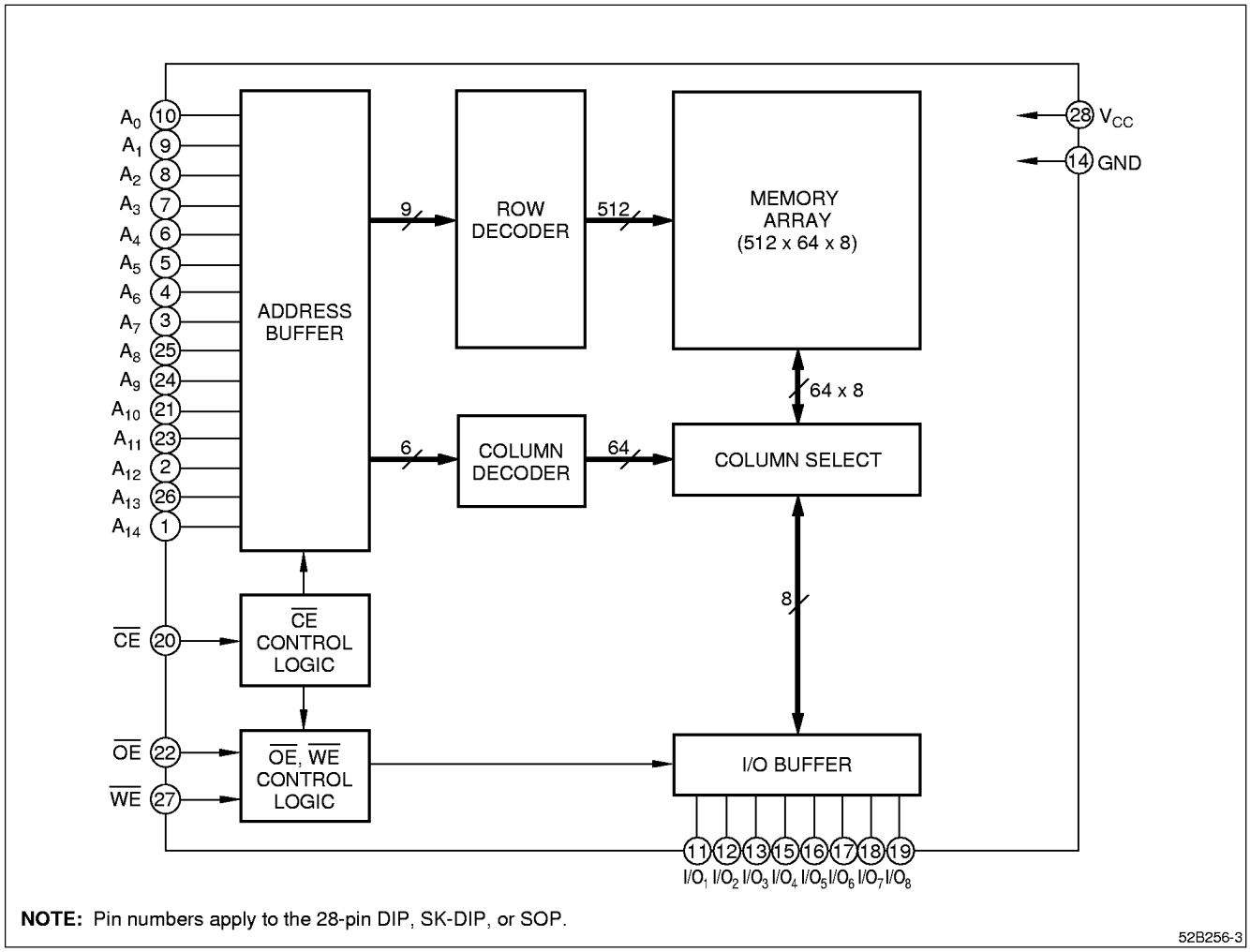


Figure 3. LH52B256 Block Diagram

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{14}$	Address Inputs
$\overline{CE}$	Chip Enable input
$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input

PIN	DESCRIPTION
$I/O_1 - I/O_8$	Data Input/Output
V_{CC}	Power Supply
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	MODE	$I/O_1 - I/O_8$	SUPPLY CURRENT	NOTE
H	X	X	Deselect	High-Z	Standby (I_{SB})	1
L	L	X	Write	D_{IN}	Operating (I_{CC})	1
L	H	L	Read	D_{OUT}	Operating (I_{CC})	
L	H	H	Output Disable	High-Z	Operating (I_{CC})	

NOTE:
1. X = H or L.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply Voltage	V_{CC}	−0.5 to +7.0	V	1
Input Voltage	V_{IN}	−0.5 to V_{CC} + 0.5	V	1, 2
Operating Temperature	Topr	0 to +70	°C	
Storage Temperature	Tstg	−65 to +150	°C	

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
2. V_{IN} (MIN.) = −3.0 V for pulse width ≤50 ns.

RECOMMENDED OPERATING CONDITIONS (T_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input Voltage	V_{IH}	2.2		V_{CC} + 0.5	V	
	V_{IL}	−0.5		0.8	V	1

NOTE:
1. V_{IN} (MIN.) = −3.0 V for pulse width ≤50 ns.

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0°C to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}	−1		1	µA
Output Leakage Current	I_{LO}	$\overline{CE}$ or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0 to V_{CC}	−1		1	µA
Operating Current	I_{CC}	Minimum Cycle, V_{IN} = V_{IL} or V_{IH}, $I_{I/O}$ = 0 mA, $\overline{CE}$ = V_{IL}			70	mA
		t_{RC}, t_{WC} = 1 µs, V_{IN} = V_{IL} or V_{IH}, $I_{I/O}$ = 0 mA, $\overline{CE}$ = V_{IL}		15	30	mA
Standby Current	I_{SB1}	$\overline{CE}$ = V_{IH}			3.0	mA
	I_{SB}	$\overline{CE}$ ≥ V_{CC} − 0.2 V			40	µA
Output Voltage	V_{OL}	IOL = 2.1 mA			0.4	V
	V_{OH}	IOH = −1.0 mA	2.4			V

AC CHARACTERISTICS

(1) READ CYCLE (V_{CC} = 5 V ±10%, T_A = 0°C to +70°C)

DESCRIPTION	SYMBOL	LH52B256-70		LH52B256-90		LH52B256-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read Cycle Time	t_{RC}	70		90		100		ns	
Address Access Time	t_{AA}		70		90		100	ns	
Chip Enable Access Time	t_{ACE}		70		90		100	ns	
Output Enable Access Time	t_{OE}		40		50		50	ns	
Output Hold Time	t_{OH}	10		10		10		ns	
$\overline{CE}$ Low to Output in Low-Z	t_{LZ}	10		10		10		ns	1
$\overline{OE}$ Low to Output in Low-Z	t_{OLZ}	5		5		5		ns	1
$\overline{CE}$ High to Output in High-Z	t_{HZ}	0	35	0	40	0	40	ns	1
$\overline{OE}$ High to Output High-Z	t_{OHZ}	0	35	0	40	0	40	ns	1

(2) WRITE CYCLE (V_{CC} = 5 V ±10%, T_A = 0°C to +70°C)

DESCRIPTION	SYMBOL	LH52B256-70		LH52B256-90		LH52B256-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write Cycle Time	t_{WC}	70		90		100		ns	
$\overline{CE}$ Low to End of Write	t_{CW}	60		70		80		ns	
Address Valid to End of Write	t_{AW}	60		70		80		ns	
Address Setup Time	t_{AS}	0		0		0		ns	
Write Pulse Width	t_{WP}	55		65		75		ns	
Write Recovery Time	t_{WR}	0		0		0		ns	
Input Data Setup Time	t_{DW}	30		35		40		ns	
Input Data Hold Time	t_{DH}	0		0		0		ns	
$\overline{WE}$ High to Output in High-Z	t_{OW}	5		5		5		ns	1
$\overline{WE}$ Low to Output in High-Z	t_{WZ}	0	40	0	40	0	40	ns	1
$\overline{OE}$ High to Output in High-Z	t_{OHZ}	0	35	0	40	0	40	ns	1

NOTE:

1. Active output to high-impedance and high-impedance to output active tests specified for a ±200 mV transition from steady state levels into the test load.

AC TEST CONDITIONS

PARAMETER	RATING	NOTE
Input Voltage Amplitude	0.6 to 2.4 V	
Input Rise/Fall Time	10 ns	
Timing Reference Level	1.5 V	
Output Load Conditions	1TTL + CL (100 pF)	1

NOTE:
1. Includes scope and jig capacitance.

CAPACITANCE [1] (T_A = 25°C, f = 1 MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Capacitance	C_{IN}	VIN = 0 V			9	pF
Input/Output Capacitance	$C_{I/O}$	VI/O = 0 V			10	pF

NOTE:
1. This parameter is sampled and not production tested.

DATA RETENTION CHARACTERISTICS (T_A = 0°C to +70°C)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	NOTE
Data Retention Voltage	V_{CCDR}	$\overline{CE} \geq V_{CCDR} - 0.2$ V		2.0		5.5	V	
Data Retention Current	I_{CCDR}	V_{CCDR} = 3.0 V $\overline{CE} \geq V_{CCDR} - 0.2$ V	T_A = 25°C			1	µA	
			T_A = 0 to 40°C			3		
						20		
$\overline{CE}$ Setup Time	t_{CDR}			0			ns	
$\overline{CE}$ Hold Time	t_R			t_{RC}			ns	1

NOTE:
1. t_{RC} = Read cycle time

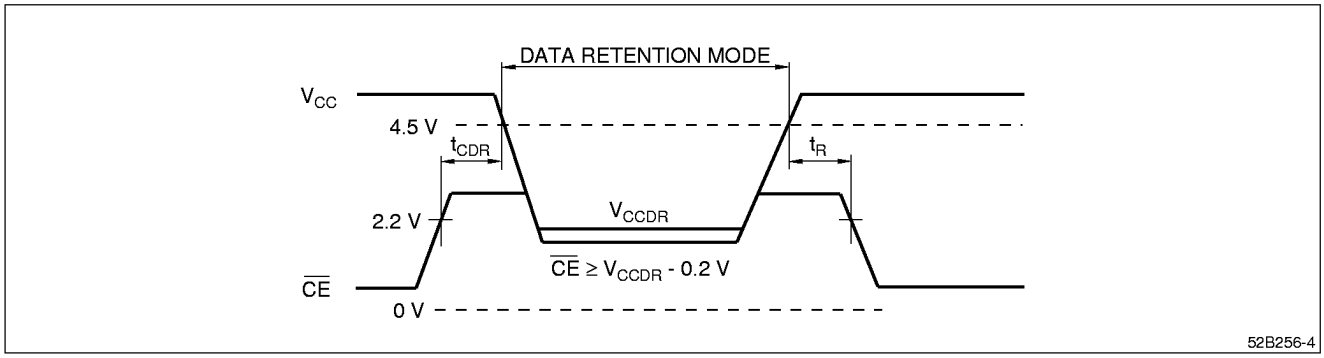


Figure 4. Data Retention Characteristics

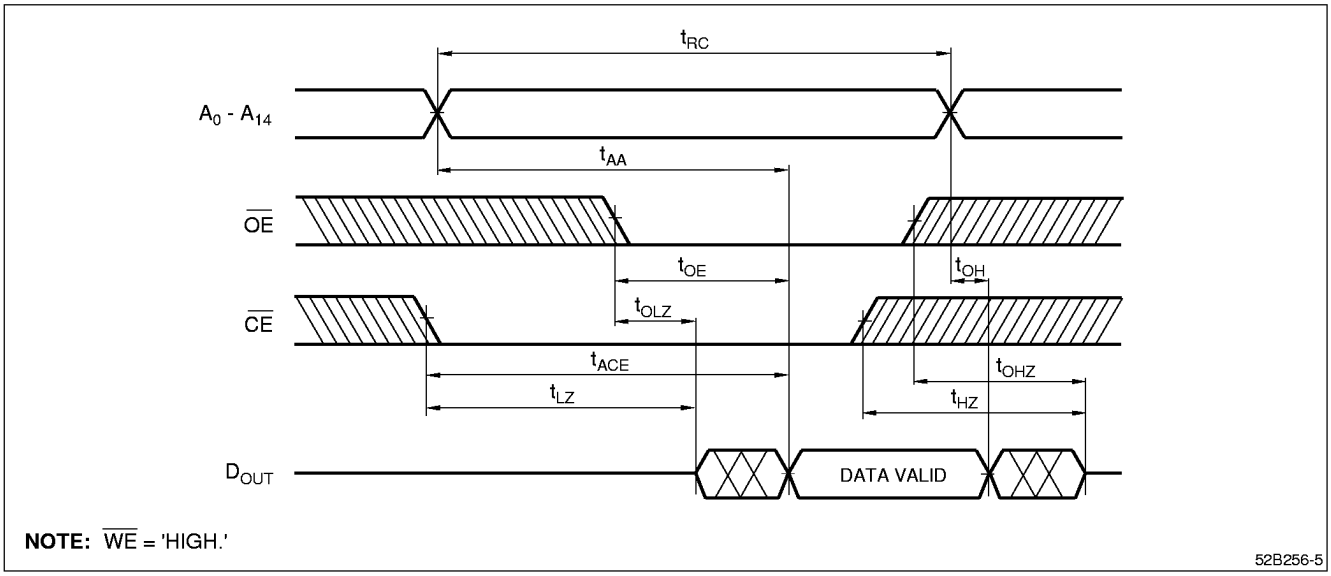
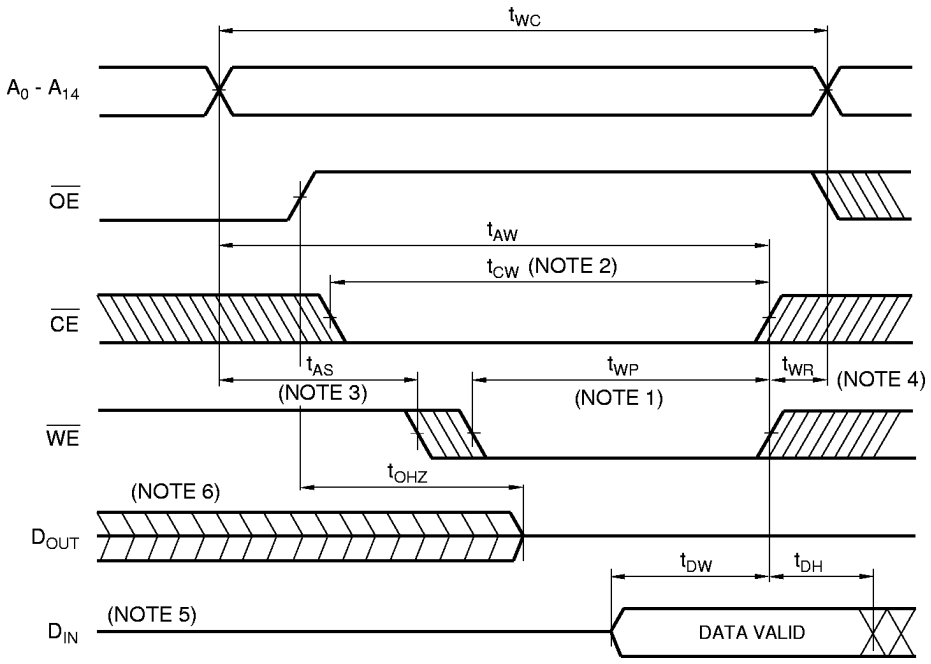


Figure 5. Read Cycle



NOTES:

1. The writing occurs during an overlapping period of $\overline{CE}$ = 'LOW' and $\overline{WE}$ = 'LOW' (t_{WP}).
2. t_{CW} is defined as the time from $\overline{CE}$ LOW transition to the end of writing.
3. t_{AS} is defined as the time from address change to the start of writing.
4. t_{WR} is defined as the time from the end of writing to the address change.
5. When I/O pins are in the output state, input signals with the opposite logic level must not be applied.
6. If $\overline{CE}$ LOW transition occurs at the same time or after $\overline{WE}$ LOW transition, the outputs will remain high-impedance.

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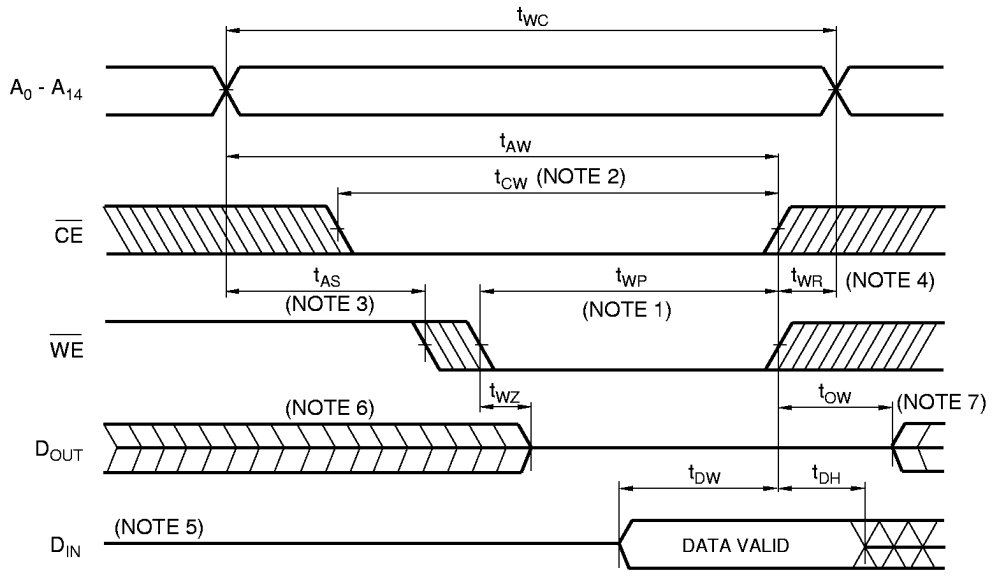
Figure 6. Write Cycle 1 ($\overline{OE}$ Controlled)



NOTES:

1. The writing occurs during an overlapping period of $\overline{CE}$ = 'LOW' and $\overline{WE}$ = 'LOW' (t_{WP}).
2. t_{CW} is defined as the time from $\overline{CE}$ LOW transition to the end of writing.
3. t_{AS} is defined as the time from address change to the start of writing.
4. t_{WR} is defined as the time from the end of writing to address change.
5. When I/O pins are in the output state, input signals with the opposite logic level must not be applied.
6. If $\overline{CE}$ LOW transition occurs at the same time or after $\overline{WE}$ LOW transition, the output will remain high-impedance.
7. If $\overline{CE}$ HIGH transition occurs at the same time or before $\overline{WE}$ HIGH transition, the output will remain high-impedance.

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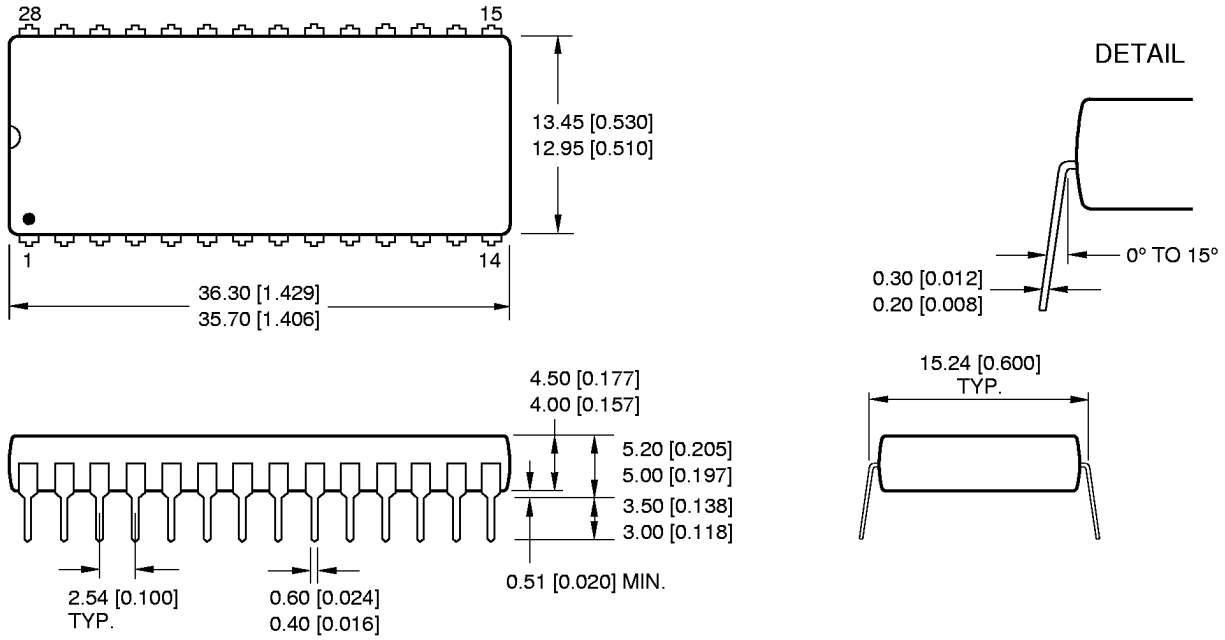
Figure 7. Write Cycle No. 2 ($\overline{OE}$ Low Fixed)

PACKAGE DIAGRAMS

28DIP (DIP028-P-0600)

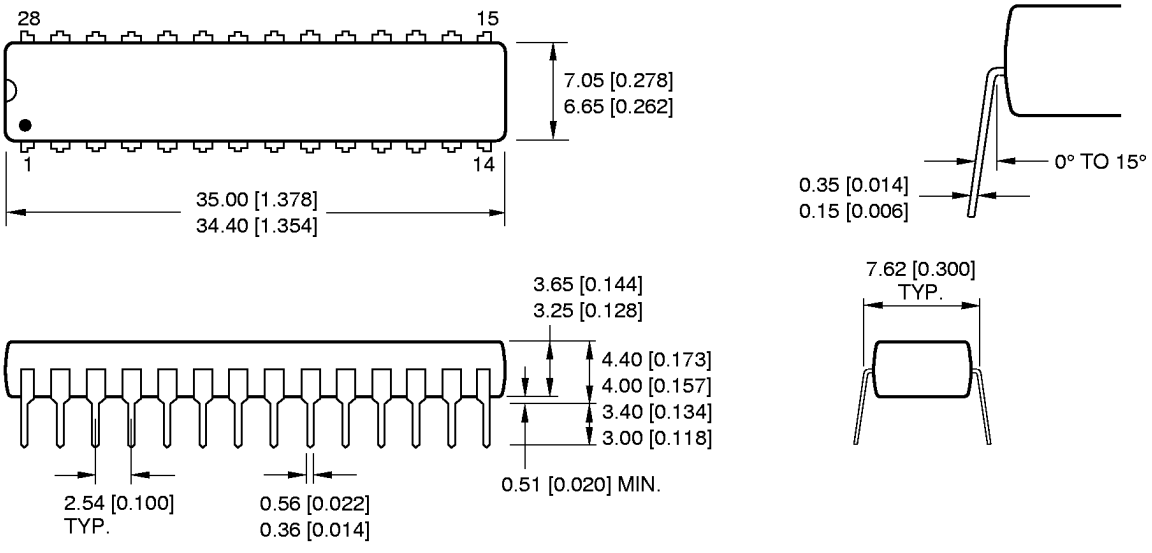


DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28DIP-2

28-pin, 600-mil DIP

28SK-DIP (DIP028-P-0300)

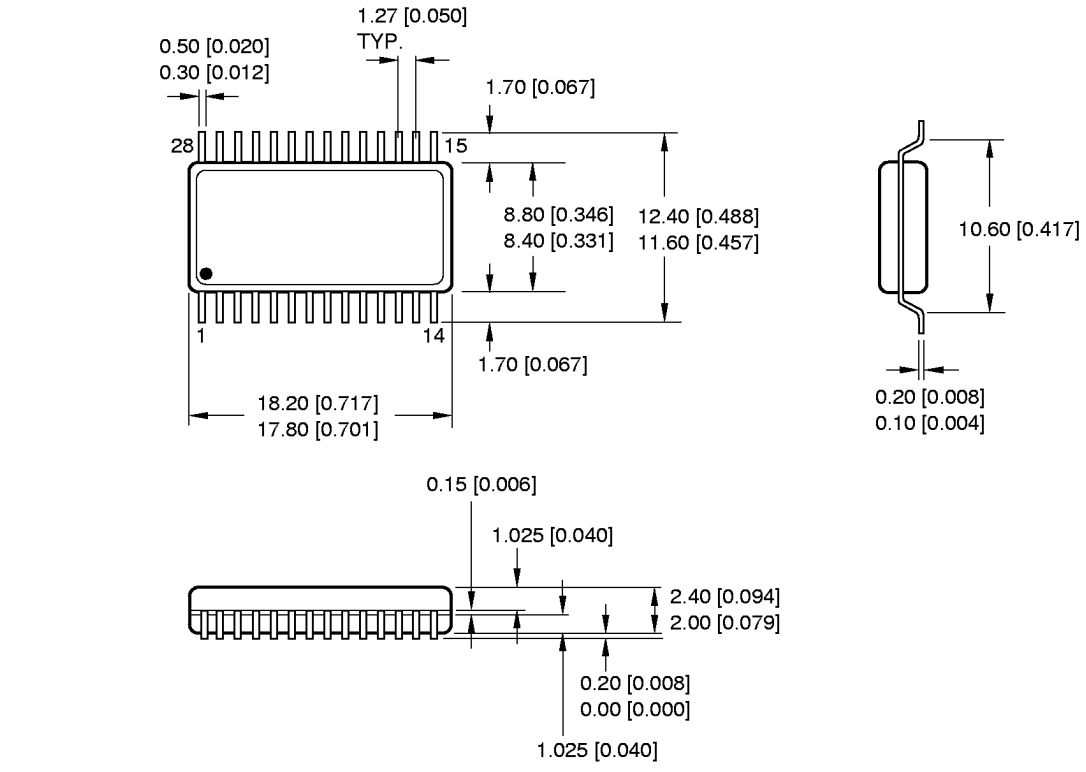


DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28DIP-1

28-pin, 300-mil DIP

28SOP (SOP028-P-0450)

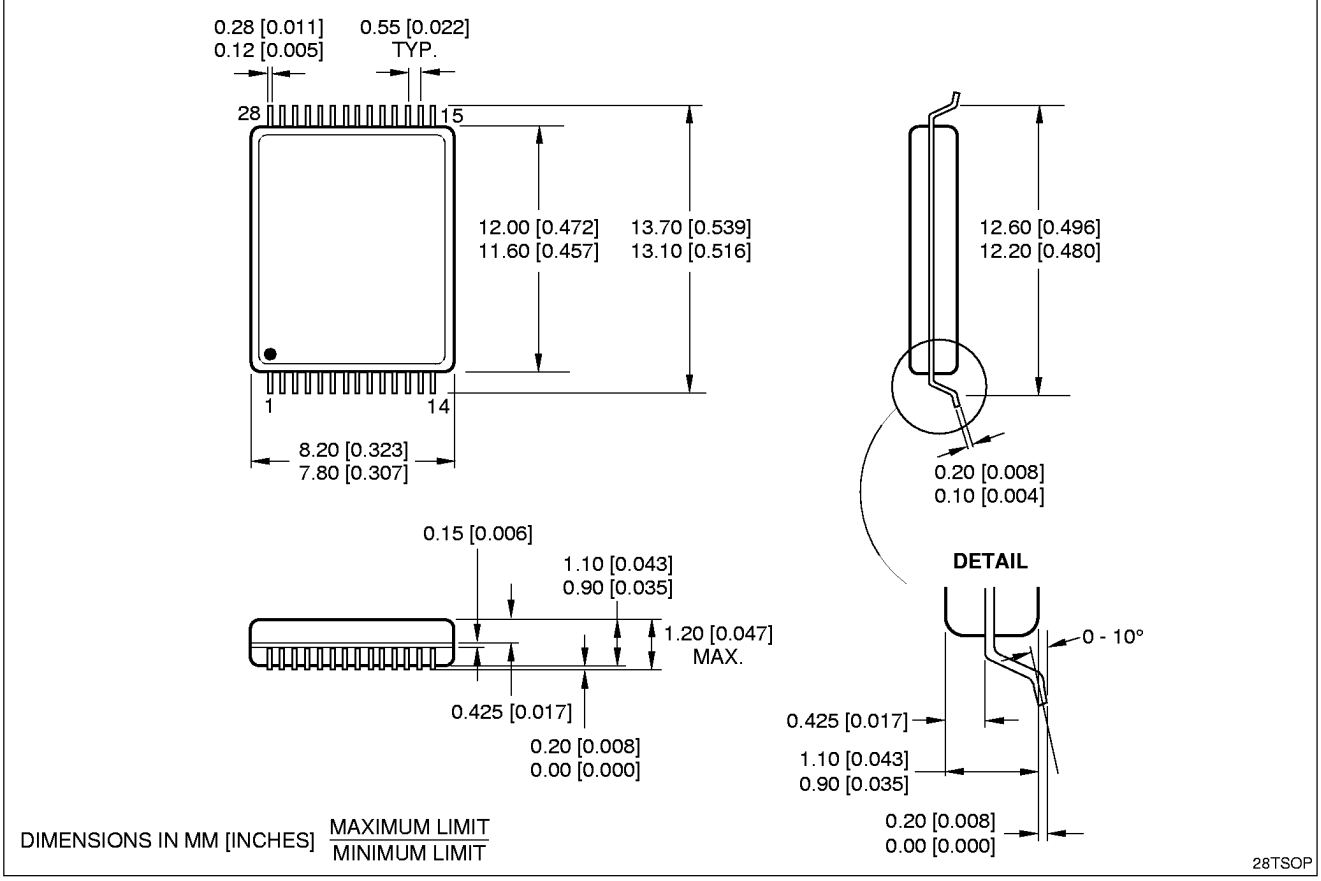


DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28SOP

28-pin, 450-mil SOP

28TSOP (TSOP028-P-0813)



28-pin, 8 × 13 mm² TSOP (Type I)

ORDERING INFORMATION