STK14CA8

128K x 8 *AutoStore*™ nvSRAM
QuantumTrap™ CMOS
Nonvolatile Static RAM

FEATURES

- **25ns, 35ns and 45ns Access Times**
- **"Hands-off" Automatic *STORE* on Power Down with only a small capacitor**
- ***STORE* to *QuantumTrap*™ Nonvolatile Elements is Initiated by Software , device pin or *AutoStore*™ on Power Down**
- ***RECALL* to SRAM Initiated by Software or Power Up**
- **Unlimited *READ, WRITE* and *RECALL* Cycles**
- **5mA Typical I_{CC} at 200ns Cycle Time**
- **1,000,000 *STORE* Cycles to *QuantumTrap*™**
- **100-Year Data Retention to *QuantumTrap*™**
- **Single 3V +20%, -10% Operation**
- **Commercial and Industrial Temperatures**
- **SOIC, SSOP and DIP Packages**
- **RoHS Compliance**

DESCRIPTION

The Simtek STK14CA8 is a fast static RAM with a nonvolatile element in each memory cell. The embedded nonvolatile elements incorporate Simtek's *QuantumTrap*™ technology producing the world's most reliable nonvolatile memory. The SRAM provides unlimited read and write cycles, while independent, nonvolatile data resides in the highly reliable *QuantumTrap*™ cell. Data transfers from the SRAM to the nonvolatile elements (the *STORE* operation) takes place automatically at power down. On power up, data is restored to the SRAM (the *RECALL* operation) from the nonvolatile memory. Both the *STORE* and *RECALL* operations are also available under software control.

BLOCK DIAGRAM

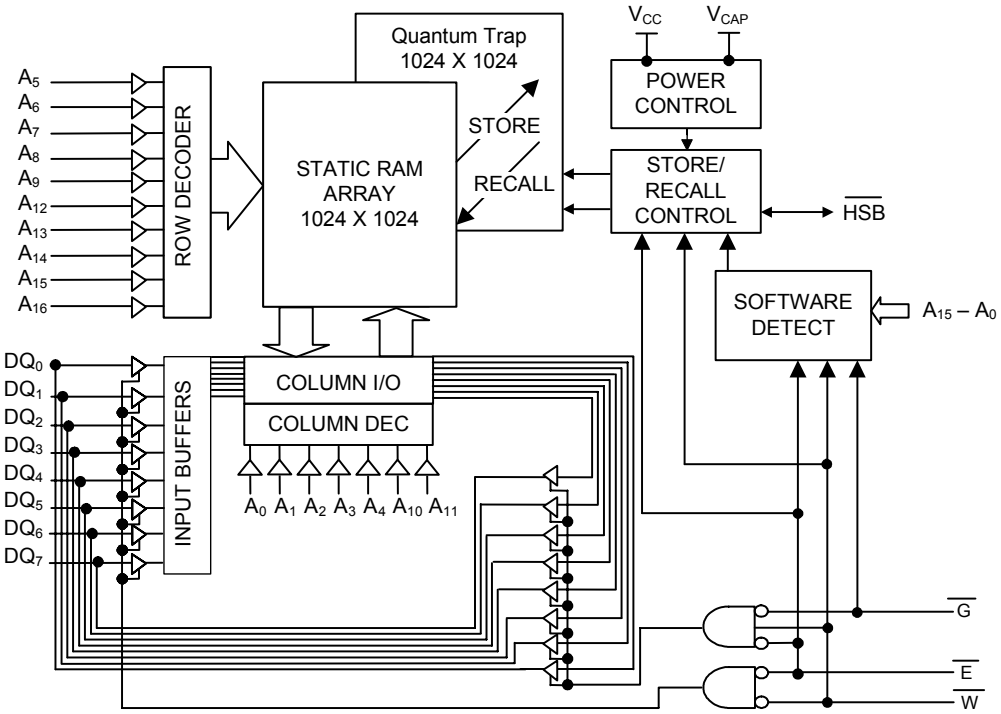
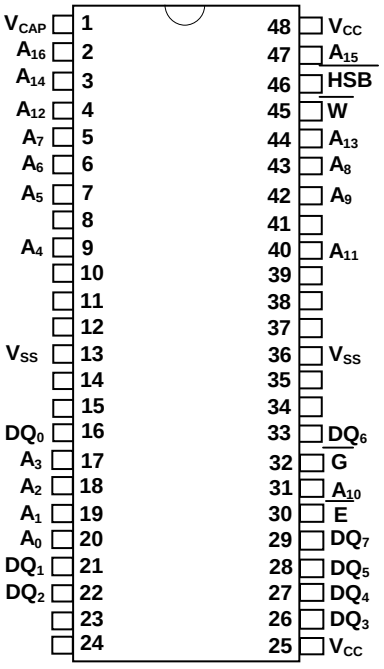
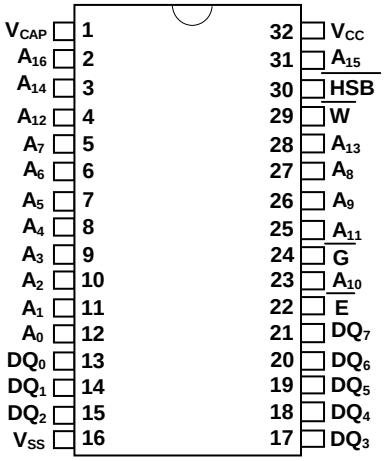


Figure 1. Block Diagram

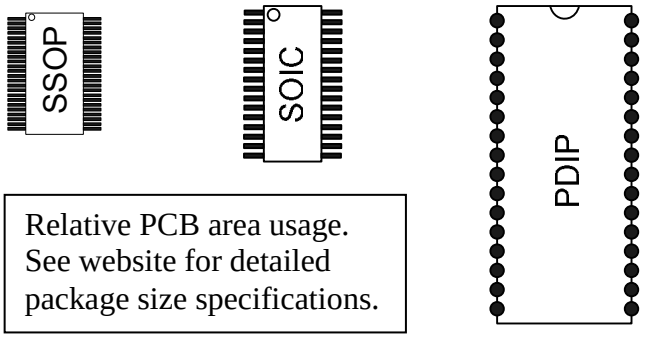
PACKAGES



48 Pin SSOP



32 Pin
SOIC or **PDIP**



Relative PCB area usage.
See website for detailed package size specifications.

PIN DESCRIPTIONS

Pin Name	I/O	Description
$A_{16} – A_0$	Input	Address: The 17 address inputs select one of 131,072 bytes in the nvSRAM array.
$DQ_7 – DQ_0$	I/O	Data: Bi-directional 8-bit data bus for accessing the nvSRAM.
$\overline{E}$	Input	Chip Enable: The active low $\overline{E}$ input selects the device.
$\overline{W}$	Input	Write Enable: The active low $\overline{W}$ enables data on the DQ pins to be written to the address location latched by the falling edge of $\overline{E}$.
$\overline{G}$	Input	Output Enable: The active low $\overline{G}$ input enables the data output buffers during read cycles. De-asserting $\overline{G}$ high causes the DQ pins to tri-state.
V_{CC}	Power Supply	Power 3.0V +20%, -10%
$\overline{HSB}$	I/O	Hardware Store Busy: When low this output indicates a Hardware Store is in progress. When pulled low external to the chip it will initiate a nonvolatile STORE operation. A weak internal pull up resistor keeps this pin high if not connected. (Connection Optional)
V_{CAP}	Power Supply	*Autostore* Capacitor: Supplies power to nvSRAM during power loss to store data from SRAM to nonvolatile elements.
V_{SS}	Power Supply	Ground
(Blank)	No Connect	Unlabeled pins have no internal connection.

ABSOLUTE MAXIMUM RATINGS[a]

Power Supply Voltage	-0.5V to +4.1V
Voltage on Input Relative to V_{SS}	-0.5V to (V_{CC} + 0.5V)
Voltage on Outputs	-0.5V to (V_{CC} + 0.5V)
Temperature under Bias	–55°C to 125°C
Junction Temperature	–55°C to 140°C
Storage Temperature	–65°C to 150°C
Power Dissipation	1W
DC Output Current (1 output at a time, 1s duration)	15mA

Notes

a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Package Thermal Characteristics see website: http://www.simtek.com/

DC CHARACTERISTICS

Symbol	Parameter	Commercial		Industrial		Units	Notes
		MIN	MAX	MIN	MAX		
I_{CC1}	Average V_{CC} Current		65 55 50		70 60 55	mA mA mA	t_{AVAV} = 25ns t_{AVAV} = 35ns t_{AVAV} = 45ns Dependent on output loading and cycle rate. Values obtained without output loads.
I_{CC2}	Average V_{CC} Current during STORE		3		3	mA	All Inputs Don't Care, V_{CC} = max Average current for duration of *STORE* cycle (t_{STORE}).
I_{CC3}	Average V_{CC} Current at t_{AVAV} = 200ns 3V, 25°C, Typical		5		5	mA	$\overline{W}$ ≥ (V_{CC} – 0.2V) All Others Inputs Cycling, at CMOS Levels. Dependent on output loading and cycle rate. Values obtained without output loads.
I_{CC4}	Average V_{CAP} Current during *AutoStore*™ Cycle		3		3	mA	All Inputs Don't Care Average current for duration of *STORE* cycle (t_{STORE}).
I_{SB}	V_{CC} Standby Current (Standby, Stable CMOS Input Levels)		2		2	mA	$\overline{E}$ ≥ (V_{CC} – 0.2V) All Others V_{IN} ≤ 0.2V or ≥ (V_{CC} – 0.2V) Standby current level after nonvolatile cycle is complete.
I_{ILK}	Input Leakage Current		±1		±1	µA	V_{CC} = max V_{IN} = V_{SS} to V_{CC}
I_{OLK}	Off-State Output Leakage Current		±1		±1	µA	V_{CC} = max V_{IN} = V_{SS} to V_{CC}, $\overline{E}$ or $\overline{G}$ ≥ V_{IH}
V_{IH}	Input Logic "1" Voltage	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V	All Inputs
V_{IL}	Input Logic "0" Voltage	V_{SS} – 0.5	0.8	V_{SS} – 0.5	0.8	V	All Inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	I_{OUT} = –2mA
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	I_{OUT} = 4mA
T_A	Operating Temperature	0	70	–40	85	°C	
V_{CC}	Operating Voltage	2.7	3.6	2.7	3.6	V	3.0V +20%, -10%
V_{CAP}	Storage Capacitor	17	57	17	57	µF	Between Vcap pin and Vss, 5V rated.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	≤ 5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figure 2 and Figure 3

CAPACITANCE[b] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	7	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Notes
b: These parameters are guaranteed but not tested

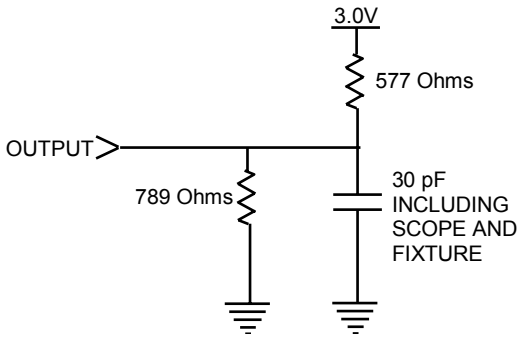


Figure 2. AC Output Loading

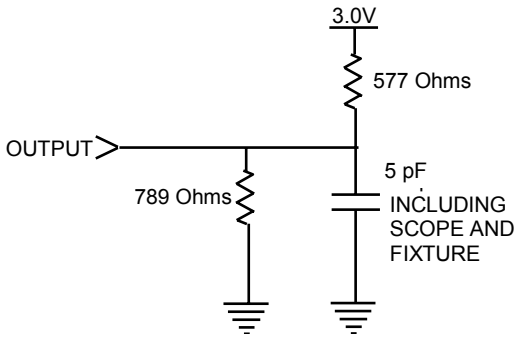


Figure 3. AC Output Loading, for tristate specs (t_{HZ}, t_{LZ}, t_{WLQZ}, t_{WHQZ}, t_{GLQX}, t_{GHQZ})

SRAM READ CYCLES #1 & #2

NO.	SYMBOLS			PARAMETER	STK14CA8-25		STK14CA8-35		STK14CA8-45		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
1		t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		35		45	ns
2	t_{AVAV}[c]	t_{AVAV}[c]	t_{RC}	Read Cycle Time	25		35		45		ns
3	t_{AVQV}[d]		t_{AA}	Address Access Time		25		35		45	ns
4		t_{GLQV}	t_{OE}	Output Enable to Data Valid		12		15		20	ns
5	t_{AXQX}[d]		t_{OH}	Output Hold after Address Change	3		3		3		ns
6		t_{ELQX}	t_{LZ}	Chip Enable to Output Active	3		3		3		ns
7		t_{EHQZ}[e]	t_{HZ}	Chip Disable to Output Inactive		10		13		15	ns
8		t_{GLQX}	t_{OLZ}	Output Enable to Output Active	0		0		0		ns
9		t_{GHQZ}[e]	t_{OHZ}	Output Disable to Output Inactive		10		13		15	ns
10		t_{ELICC}[b]	t_{PA}	Chip Enable to Power Active	0		0		0		ns
11		t_{EHICC}[b]	t_{PS}	Chip Disable to Power Standby		25		35		45	ns

Notes

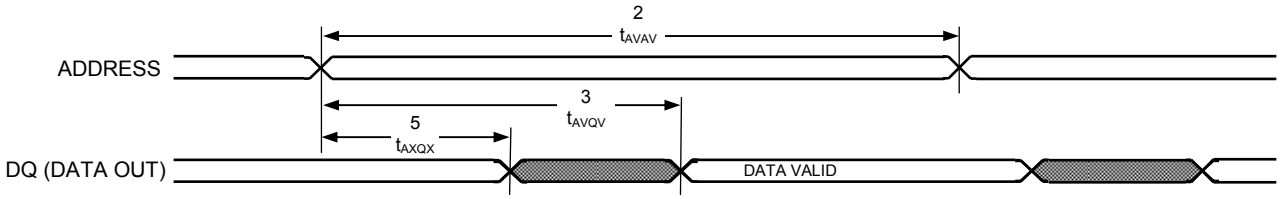
c: $\overline{W}$ must be high during SRAM READ cycles

d: Device is continuously selected with $\overline{E}$ and $\overline{G}$ both low

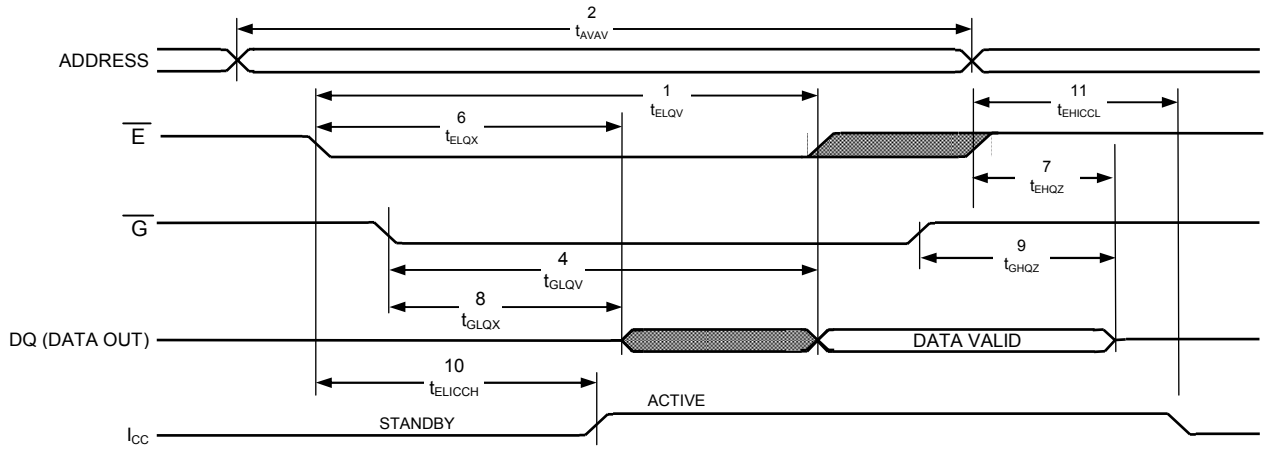
e: Measured ± 200mV from steady state output voltage

f: $\overline{HSB}$ must remain high during READ and WRITE cycles.

SRAM READ CYCLE #1: Address Controlled[c,d,f]



SRAM READ CYCLE #2: $\overline{E}$ Controlled[c,f]



SRAM WRITE CYCLES #1 & #2

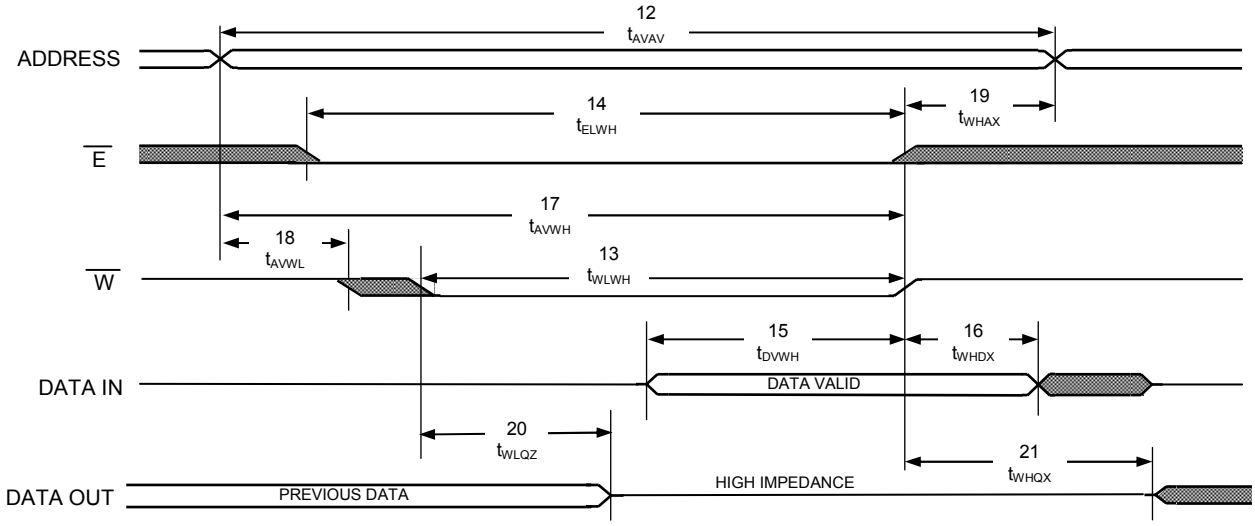
NO.	SYMBOLS			PARAMETER	STK14CA8-25		STK14CA8-35		STK14CA8-45		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	20		25		30		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		25		30		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	10		12		15		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold after End of Write	0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		25		30		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold after End of Write	0		0		0		ns
20	t_{WLQZ}[e,g]		t_{WZ}	Write Enable to Output Disable		10		13		15	ns
21	t_{WHQX}		t_{OW}	Output Active after End of Write	3		3		3		ns

Notes

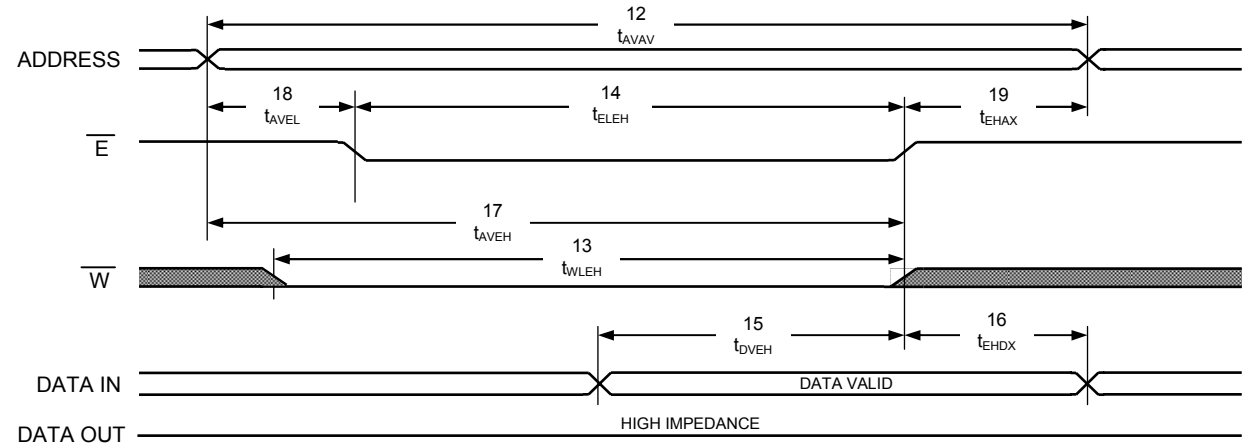
g: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high-impedance state.

h: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.

SRAM WRITE CYCLE #1: $\overline{W}$ Controlled[h,f]



SRAM WRITE CYCLE #2: $\overline{E}$ Controlled[h,f]



MODE SELECTION

$\overline{E}$	$\overline{W}$	$\overline{G}$	A_{15} - A_0	MODE	I/O	POWER	NOTES
H	X	X	X	Not Selected	Output High Z	Standby	
L	H	L	X	Read SRAM	Output Data	Active	
L	L	X	X	Write SRAM	Input Data	Active	
L	H	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8B45	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Autostore Disable	Output Data Output Data Output Data Output Data Output Data Output Data	Active	**i**, **j**, **k**
L	H	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4B46	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Autostore Enable	Output Data Output Data Output Data Output Data Output Data Output Data	Active	**i**, **j**, **k**
L	H	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Store	Output Data Output Data Output Data Output Data Output Data Output High Z	Active ICC2	**i**, **j**, **k**
L	H	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Recall	Output Data Output Data Output Data Output Data Output Data Output High Z	Active	**i**, **j**, **k**

Notes

i: The six consecutive addresses must be in the order listed. $\overline{W}$ must be high during all six consecutive cycles to enable a nonvolatile cycle.

j: While there are 17 addresses on the STK14CA8, only the lower 16 are used to control software modes

k: I/O state depends on the state of $\overline{G}$. The I/O table shown assumes $\overline{G}$ low.

*AutoStore™ /*POWER-UP *RECALL*

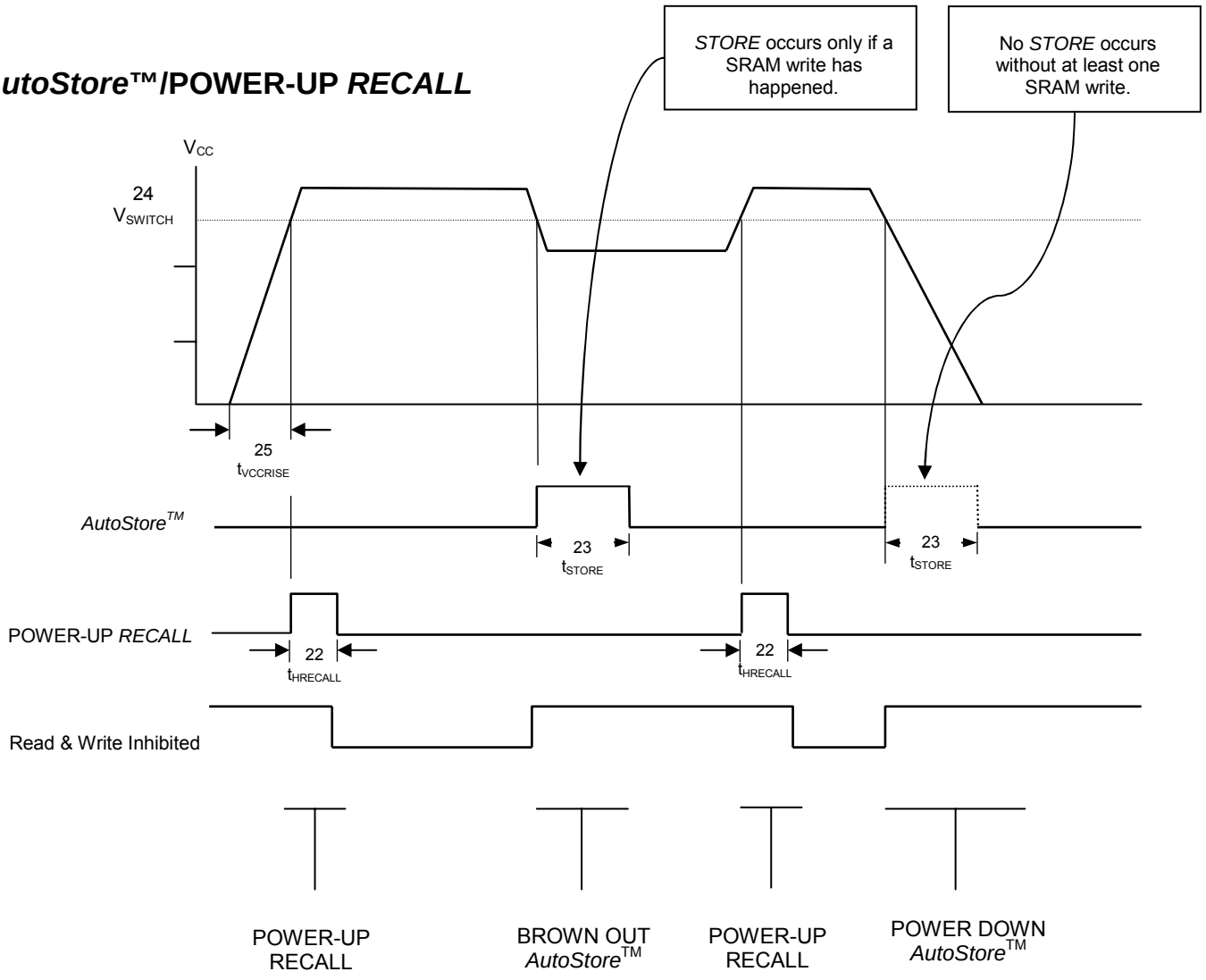
NO.	SYMBOLS		PARAMETER	STK14CA8		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
22	$t_{HRECALL}$		Power-up RECALL Duration		20	ms	**l**
23	t_{STORE}	t_{HLHZ}	STORE Cycle Duration		12.5	ms	**m**
24	V_{SWITCH}		Low Voltage Trigger Level	2.55	2.65	V	
25	$t_{VCCRISE}$		V_{CC} Rise Time	150		µs	

Notes

l: $t_{HRECALL}$ starts from the time V_{CC} rises above V_{SWITCH}

m: If an SRAM WRITE has not taken place since the last nonvolatile cycle, no *STORE* will take place

*AutoStore™ /*POWER-UP *RECALL*



Note: Read and Write cycles will be ignored during *STORE*, *RECALL* and while V_{CC} is below V_{SWITCH}.

SOFTWARE-CONTROLLED *STORE/RECALL* CYCLE[n,o]

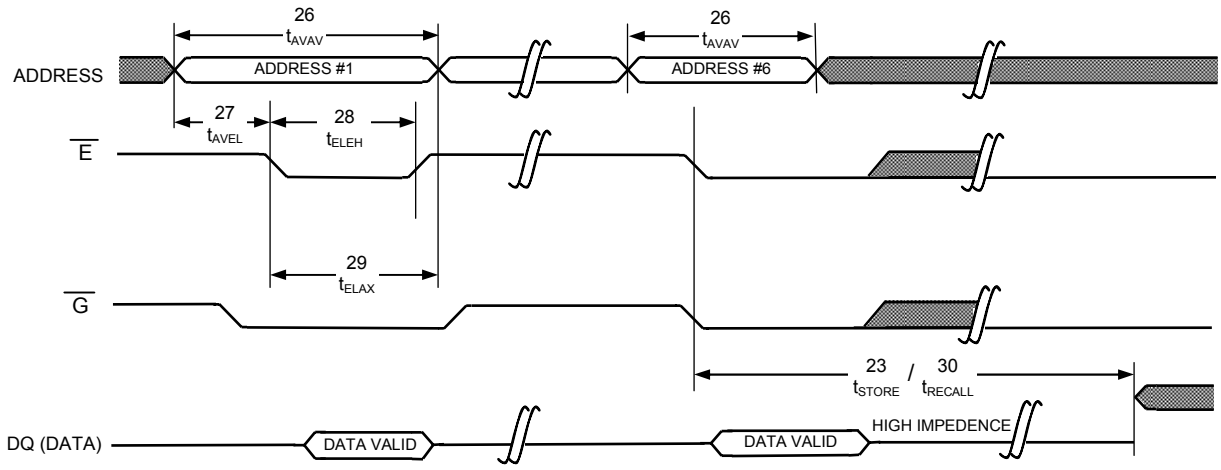
NO.	SYMBOLS			PARAMETER	STK14CA8-25		STK14CA8-35		STK14CA8-45		UNITS	NOTES
	$\overline{E}$ cont	$\overline{G}$ cont	Alt.		MIN	MAX	MIN	MAX	MIN	MAX		
26	t_{AVAV}	t_{AVAV}	t_{RC}	*STORE/RECALL* Initiation Cycle Time	25		35		45		ns	o
27	t_{AVEL}	t_{AVGL}	t_{AS}	Address Set-up Time	0		0		0		ns	
28	t_{ELEH}	t_{GLGH}	t_{CW}	Clock Pulse Width	20		25		30		ns	
29	t_{ELAX}	t_{GLAX}		Address Hold Time	20		20		20		ns	
30	t_{RECALL}	t_{RECALL}		*RECALL* Duration		40		40		40	µs	

Notes

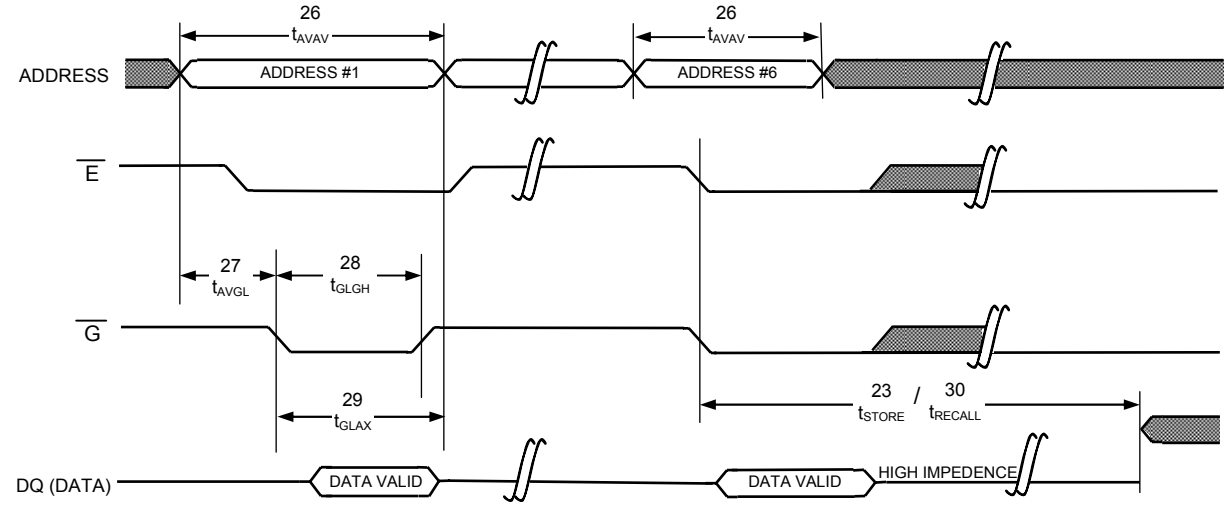
n: The software sequence is clocked with $\overline{E}$ controlled READs or $\overline{G}$ controlled READs.

o: The six consecutive addresses must be read in the order listed in the Mode Selection Table. $\overline{W}$ must be high during all six consecutive cycles.

SOFTWARE *STORE/RECALL* CYCLE: $\overline{E}$ Controlled[o]



SOFTWARE *STORE/RECALL* CYCLE: $\overline{G}$ Controlled[o]



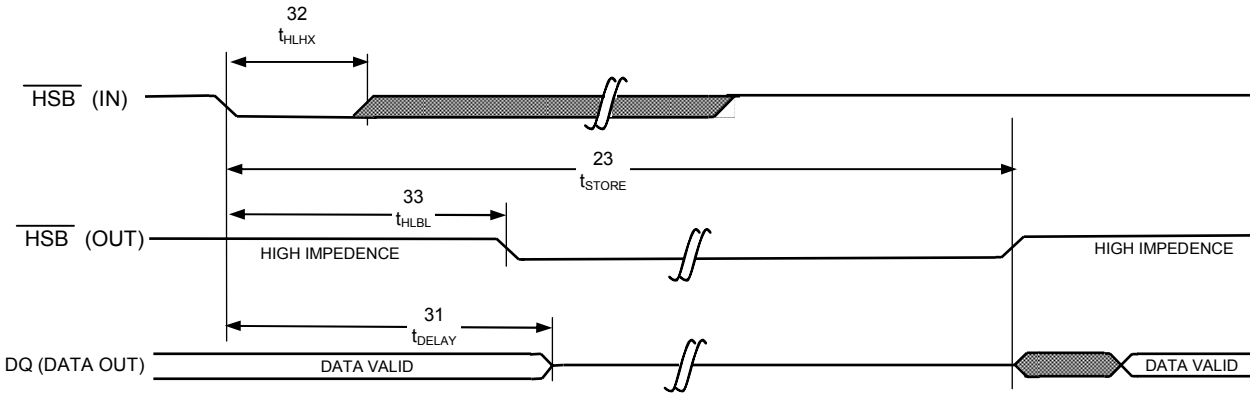
HARDWARE *STORE* CYCLE

NO.	SYMBOLS		PARAMETER	STK14CA8		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
31	t_{DELAY}	t_{HLQZ}	Time Allowed to Complete SRAM Cycle	1		µs	p
32	t_{HLHX}		Hardware *STORE* Pulse Width	15		ns	
33	t_{HLBL}		Hardware *STORE* Low to *STORE* Busy		300	ns	

Notes

p: Read and Write cycles in progress before $\overline{HSB}$ is asserted are given this amount of time to complete.

HARDWARE *STORE* CYCLE



DEVICE OPERATION

nvSRAM

The STK14CA8 nvSRAM is made up of two functional components paired in the same physical cell. These are a SRAM memory cell and a nonvolatile *QuantumTrap*™ cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM can be transferred to the nonvolatile cell (the *STORE* operation), or from the nonvolatile cell to SRAM (the *RECALL* operation). This unique architecture allows all cells to be stored and recalled in parallel. During the *STORE* and *RECALL* operations SRAM READ and WRITE operations are inhibited. The STK14CA8 supports unlimited reads and writes just like a typical SRAM. In addition, it provides unlimited *RECALL* operations from the nonvolatile cells and up to 1 million *STORE* operations.

SRAM READ

The STK14CA8 performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are low while $\overline{W}$ and $\overline{HSB}$ are high. The address specified on pins A_{16-0} determines which of the 131,072 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ cycle #1). If the READ is initiated by $\overline{E}$ or $\overline{G}$, the outputs will be valid at t_{ELQV} or at t_{GLQV}, whichever is later (READ cycle #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought high, or $\overline{W}$ or $\overline{HSB}$ is brought low.

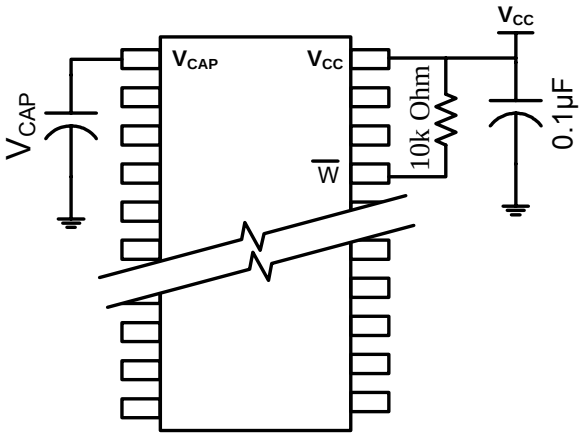


Figure 4: *AutoStore*™ Mode

SRAM WRITE

A WRITE cycle is performed whenever $\overline{E}$ and $\overline{W}$ are low and $\overline{HSB}$ is high. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ goes high at the end of the cycle. The data on the common I/O pins DQ_{0-7} will be written into the memory if it is valid t_{DVWH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} before the end of an $\overline{E}$ controlled WRITE.

It is recommended that $\overline{G}$ be kept high during the entire WRITE cycle to avoid data bus contention on common I/O lines. If $\overline{G}$ is left low, internal circuitry will turn off the output buffers t_{WLQZ} after $\overline{W}$ goes low.

AutoStore™ OPERATION

The STK14CA8 stores data to nvSRAM using one of three storage operations. These three operations are Hardware Store, activated by $\overline{HSB}$, Software Store, actived by an address sequence, and *AutoStore*™, on device power down.

AutoStore™ operation is a unique feature of Simtek *QuantumTrap*™ technology and is enabled by default on the STK14CA8.

During normal operation, the device will draw current from Vcc to charge a capacitor connected to the Vcap pin. This stored charge will be used by the chip to perform a single STORE operation. If the voltage on the Vcc pin drops below Vswitch, the part will automatically disconnect the Vcap pin from Vcc. A STORE operation will be initiated with power provided by the Vcap capacitor.

Figure 4 shows the proper connection of the storage capacitor (Vcap) for automatic store operation. Refer to the DC CHARACTERISTICS table for the size of Vcap. The voltage on the Vcap pin is driven to 5V by a charge pump internal to the chip. A pull up should be placed on $\overline{W}$ to hold it inactive during power up.

To reduce unneeded nonvolatile stores, *AutoStore*™ and Hardware Store operations will be ignored unless at least one WRITE operation has taken place since the most recent *STORE* or *RECALL* cycle. Software initiated *STORE* cycles are performed regardless of whether a WRITE operation has taken place. The $\overline{HSB}$ signal can be monitored by the system to detect an *AutoStore*™ cycle is in progress.

HARDWARE *STORE* ($\overline{\text{HSB}}$) OPERATION

The STK14CA8 provides the $\overline{\text{HSB}}$ pin for controlling and acknowledging the *STORE* operations. The HSB pin can be used to request a hardware *STORE* cycle. When the $\overline{\text{HSB}}$ pin is driven low, the STK14CA8 will conditionally initiate a *STORE* operation after t_{DELAY}. An actual *STORE* cycle will only begin if a WRITE to the SRAM took place since the last *STORE* or *RECALL* cycle. The $\overline{\text{HSB}}$ pin also acts as an open drain driver that is internally driven low to indicate a busy condition while the *STORE* (initiated by any means) is in progress.

SRAM READ and WRITE operations that are in progress when $\overline{\text{HSB}}$ is driven low by any means are given time to complete before the *STORE* operation is initiated. After $\overline{\text{HSB}}$ goes low, the STK14CA8 will continue SRAM operations for t_{DELAY}. During t_{DELAY}, multiple SRAM READ operations may take place. If a WRITE is in progress when $\overline{\text{HSB}}$ is pulled low it will be allowed a time, t_{DELAY}, to complete. However, any SRAM WRITE cycles requested after $\overline{\text{HSB}}$ goes low will be inhibited until $\overline{\text{HSB}}$ returns high.

During any *STORE* operation, regardless of how it was initiated, the STK14CA8 will continue to drive the $\overline{\text{HSB}}$ pin low, releasing it only when the *STORE* is complete. Upon completion of the *STORE* operation the STK14CA8 will remain disabled until the $\overline{\text{HSB}}$ pin returns high.

If $\overline{\text{HSB}}$ is not used, it should be left unconnected.

HARDWARE *RECALL* (POWER-UP)

During power up, or after any low-power condition (V_{CC} < V_{SWITCH}), an internal *RECALL* request will be latched. When V_{CC} once again exceeds the sense voltage of V_{SWITCH}, a *RECALL* cycle will automatically be initiated and will take $t_{HRECALL}$ to complete.

SOFTWARE *STORE*

Data can be transferred from the SRAM to the nonvolatile memory by a software address sequence. The STK14CA8 software *STORE* cycle is initiated by executing sequential $\overline{\text{E}}$ controlled READ cycles from six specific address locations in exact order. During the *STORE* cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. Once a *STORE* cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for *STORE* initiation, it is important that no other READ or WRITE accesses intervene in the sequence, or the sequence will be aborted and no *STORE* or *RECALL* will take place.

To initiate the software *STORE* cycle, the following READ sequence must be performed:

1.	Read address	0x4E38	Valid READ
2.	Read address	0xB1C7	Valid READ
3.	Read address	0x83E0	Valid READ
4.	Read address	0x7C1F	Valid READ
5.	Read address	0x703F	Valid READ
6.	Read address	0x8FC0	Initiate *STORE* cycle

The software sequence may be clocked with $\overline{\text{E}}$ controlled READs or $\overline{\text{G}}$ controlled READs.

Once the sixth address in the sequence has been entered, the *STORE* cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that $\overline{\text{G}}$ be low for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

SOFTWARE *RECALL*

Data can be transferred from the nonvolatile memory to the SRAM by a software address sequence. A software *RECALL* cycle is initiated with a sequence of READ operations in a manner similar to the software *STORE* initiation. To initiate the *RECALL* cycle, the following sequence of $\overline{\text{E}}$ controlled READ operations must be performed:

1.	Read address	0x4E38	Valid READ
2.	Read address	0xB1C7	Valid READ
3.	Read address	0x83E0	Valid READ
4.	Read address	0x7C1F	Valid READ
5.	Read address	0x703F	Valid READ
6.	Read address	0x4C63	Initiate *RECALL* cycle

Internally, *RECALL* is a two-step procedure. First, the SRAM data is cleared, and second, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time the SRAM will once again be ready for READ and WRITE operations. The *RECALL* operation in no way alters the data in the nonvolatile elements.

PREVENTING *AUTOSTORE*™

The *AutoStore*™ function can be disabled by initiating an *AutoStore Disable* sequence. A sequence of read operations is performed in a manner similar to the software *STORE* initiation. To initiate the *AutoStore Disable* sequence, the following sequence of $\overline{E}$ controlled read operations must be performed:

1.	Read address	0x4E38	Valid READ
2.	Read address	0xB1C7	Valid READ
3.	Read address	0x83E0	Valid READ
4.	Read address	0x7C1F	Valid READ
5.	Read address	0x703F	Valid READ
6.	Read address	0x8B45	*AutoStore Disable*

The *AutoStore*™ can be re-enabled by initiating an *AutoStore Enable* sequence. A sequence of read operations is performed in a manner similar to the software RECALL initiation. To initiate the *AutoStore Enable* sequence, the following sequence of $\overline{E}$ controlled read operations must be performed:

1.	Read address	0x4E38	Valid READ
2.	Read address	0xB1C7	Valid READ
3.	Read address	0x83E0	Valid READ
4.	Read address	0x7C1F	Valid READ
5.	Read address	0x703F	Valid READ
6.	Read address	0x4B46	*AutoStore Enable*

If the *AutoStore*™ function is disabled or re-enabled a manual *STORE* operation (Hardware or Software) needs to be issued to save the *AutoStore* state through subsequent power down cycles. The part comes from the factory with *AutoStore*™ enabled.

DATA PROTECTION

The STK14CA8 protects data from corruption during low-voltage conditions by inhibiting all externally initiated STORE and WRITE operations. The low-voltage condition is detected when $V_{CC} < V_{SWITCH}$.

If the STK14CA8 is in a WRITE mode (both $\overline{E}$ and $\overline{W}$ low) at power-up, after a *RECALL*, or after a STORE, the WRITE will be inhibited until a negative transition on $\overline{E}$ or $\overline{W}$ is detected. This protects against inadvertent writes during power up or brown out conditions.

NOISE CONSIDERATIONS

The STK14CA8 is a high-speed memory and so must have a high-frequency bypass capacitor of approximately 0.1μF connected between V_{CC} and V_{SS}, using leads and traces that are as short as possible. As with all high-speed CMOS ICs, careful routing of power, ground and signals will reduce circuit noise.

LOW AVERAGE ACTIVE POWER

CMOS technology provides the STK14CA8 this the benefit of drawing significantly less current when it is cycled at times longer than 50ns. Figure 5 shows the relationship between I_{CC} and READ/WRITE cycle time. Worst-case current consumption is shown for commercial temperature range, V_{CC} = 3.6V, and chip enable at maximum frequency. Only standby current is drawn when the chip is disabled. The overall average current drawn by the STK14CA8 depends on the following items:

1. The duty cycle of chip enable.
2. The overall cycle rate for accesses.
3. The ratio of READs to WRITEs.
4. The operating temperature.
5. The V_{CC} level.
6. I/O loading.

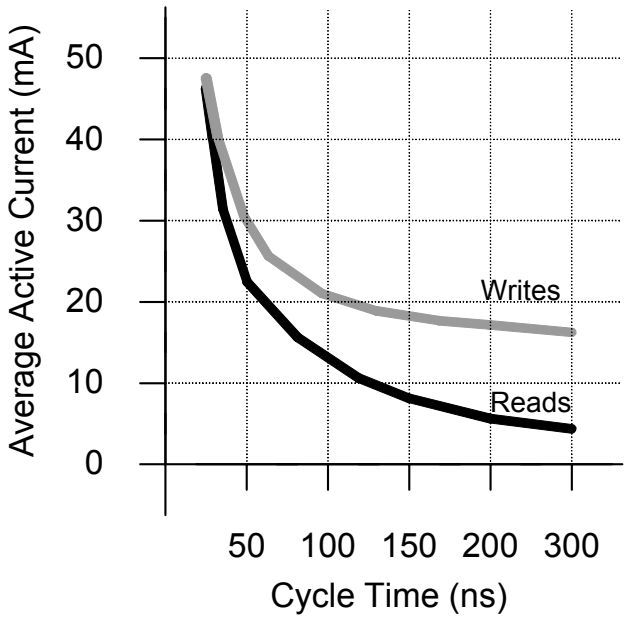
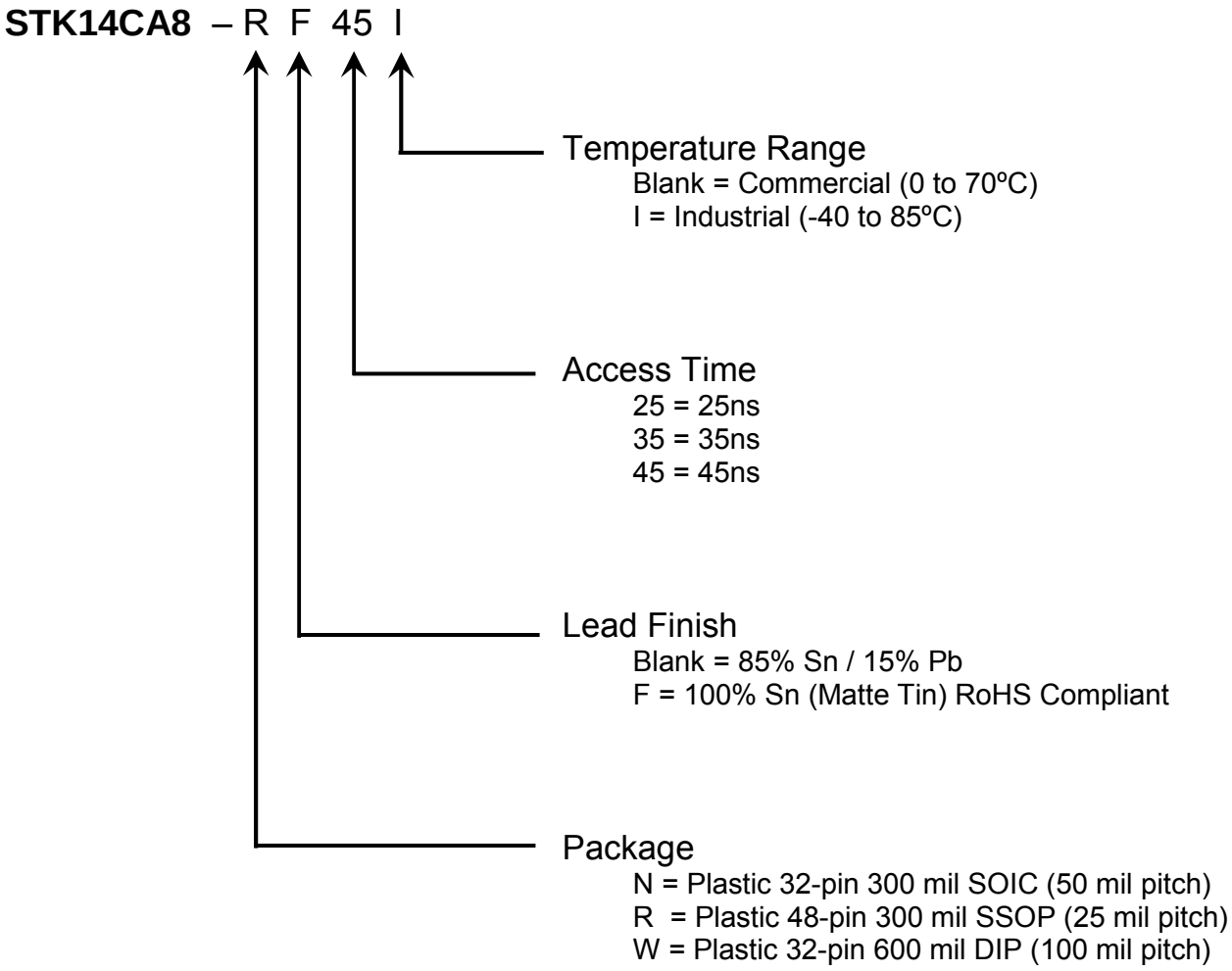


Figure 5 Current vs. Cycle time

ORDERING INFORMATION



Document Revision History

<table>
<tr><th>Revision</th><th>Date</th><th>Summary</th></tr>
<tr><td>0.0</td><td>January 2003</td><td>Publish new datasheet</td></tr>
<tr><td>0.1</td><td>May 2003</td><td>Add 48 pin SSOP, Modify AutoStore drawing (Figure 2), Update Mode Selection Table and Absolute Maximum Ratings, Added $\overline{G}$ control software store</td></tr>
<tr><td>0.2</td><td>September 2003</td><td>Added lead-free lead finish</td></tr>
<tr><td>1.0</td><td>December 2004</td><td>
<table>
<tr><th>Parameter</th><th>Old Value</th><th>New Value</th><th>Notes</th></tr>
<tr><td>Vcap Min</td><td>10µF</td><td>17 µF</td><td></td></tr>
<tr><td>$t_{VCCRISE}$</td><td>NA</td><td>150 µs</td><td>New Spec</td></tr>
<tr><td>I_{CC1} Max Com.</td><td>35 mA</td><td>50 mA</td><td>@ 45ns access</td></tr>
<tr><td>I_{CC1} Max Com.</td><td>40 mA</td><td>55 mA</td><td>@ 35ns access</td></tr>
<tr><td>I_{CC1} Max Com.</td><td>50 mA</td><td>65 mA</td><td>@ 25ns access</td></tr>
<tr><td>I_{CC1} Max Ind.</td><td>35 mA</td><td>55 mA</td><td>@ 45ns access</td></tr>
<tr><td>I_{CC1} Max Ind.</td><td>45 mA</td><td>60 mA</td><td>@ 35ns access</td></tr>
<tr><td>I_{CC1} Max Ind.</td><td>55 mA</td><td>70 mA</td><td>@ 25ns access</td></tr>
<tr><td>I_{CC2} Max</td><td>1.5 mA</td><td>3.0 mA</td><td>Com. & Ind.</td></tr>
<tr><td>I_{CC4} Max</td><td>0.5 mA</td><td>3 mA</td><td>Com & Ind.</td></tr>
<tr><td>$t_{HRECALL}$</td><td>5 ms</td><td>20 ms</td><td></td></tr>
<tr><td>t_{STORE}</td><td>10 ms</td><td>12.5 ms</td><td></td></tr>
<tr><td>t_{RECALL}</td><td>20µs</td><td>40µs</td><td></td></tr>
<tr><td>t_{GLQV}</td><td>10ns</td><td>12ns</td><td>25 ns device</td></tr>
</table>
</td></tr>
</table>