HM-6642

March 1997

512 x 8 CMOS PROM

Features

- **Low Power Standby and Operating Power**
  - **ICCSB 100µA**
  - **ICCOP . . . . . .20mA at 1MHz**
- **Fast Access Time. 120/200ns**
- **Industry Standard Pinout**
- **Single 5.0V Supply**
- **CMOS/TTL Compatible Inputs**
- **Field Programmable**
- **Synchronous Operation**
- **On-Chip Address Latches**
- **Separate Output Enable**

Description

The HM-6642 is a 512 x 8 CMOS NiCr fusible link Programmable Read Only Memory in the popular 24 pin, byte wide pinout. Synchronous circuit design techniques combine with CMOS processing to give this device high speed performance with very low power dissipation.

On-chip address latches are provided, allowing easy interfacing with recent generation microprocessors that use multiplexed address/data bus structures, such as the 8085. The output enable controls, both active low and active high, further simplify microprocessor system interfacing by allowing output data bus control independent of the chip enable control. The data output latches allow the use of the HM-6642 in high speed pipelined architecture systems, and also in synchronous logic replacement functions.

Applications for the HM-6642 CMOS PROM include low power handheld microprocessor based instrumentation and communications systems, remote data acquisition and processing systems, processor control store, and synchronous logic replacement.

All bits are manufactured storing a logical “0” and can be selectively programmed for a logical “1” at any bit location.

Ordering Information

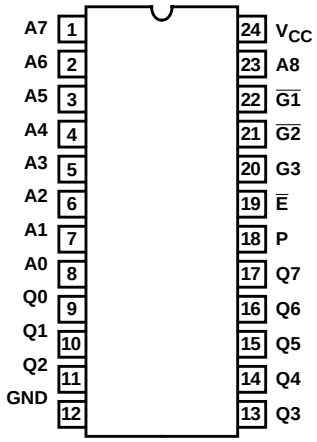
PACKAGE	TEMPERATURE RANGE	120ns	200ns	PKG. NO.
SBDIP	-40^{o}C to +85^{o}C	HM1-6642B-9	HM1-6642-9	D24.6
SMD#	-55^{o}C to +125^{o}C	5962-8869002JA	5962-8869001JA	D24.6
SLIM SBDIP	-40^{o}C to +85^{o}C	HM6-6642B-9	HM6-6642-9	D24.3
SMD#	-55^{o}C to +125^{o}C	5962-8869002LA	5962-8869001LA	D24.3
CLCC	-40^{o}C to +85^{o}C	-	HM4-6642-9	J28.A
SMD#	-55^{o}C to +125^{o}C	5962-88690023A	5962-88690013A	J28.A

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

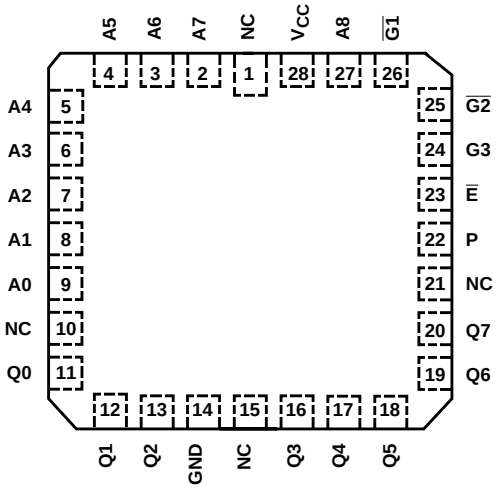
File Number **3012.1**

Pinouts

HM-6642 (SBDIP)
TOP VIEW



HM-6642 (CLCC)
TOP VIEW

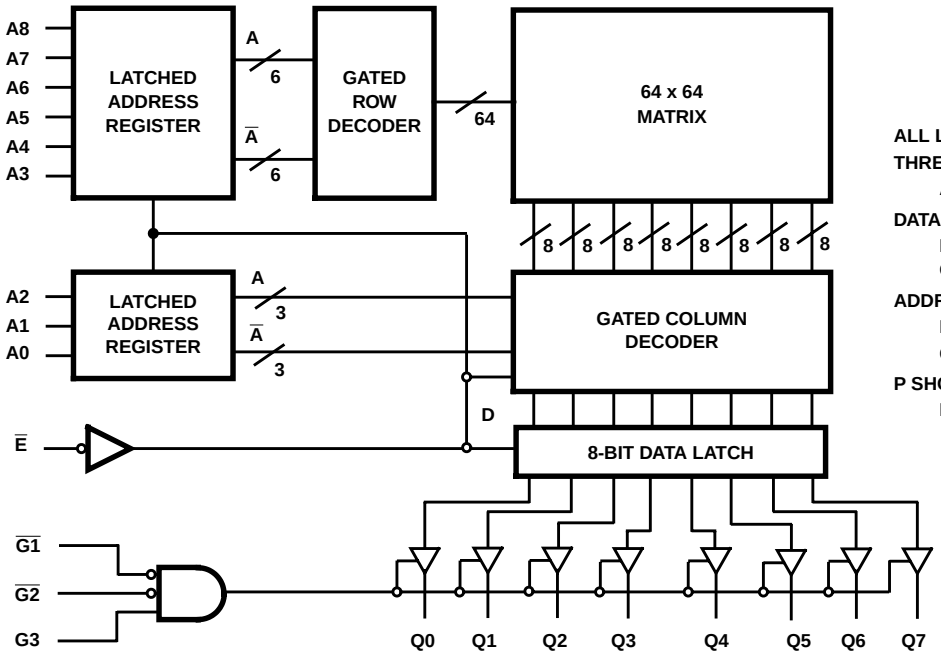


PIN DESCRIPTION

PIN	DESCRIPTION
NC	No Connect
A0-A8	Address Inputs
$\overline{E}$	Chip Enable
Q	Data Output
V_{CC}	Power (+5V)
$\overline{G1}$, $\overline{G2}$, G3	Output Enable
P (Note)	Program Enable

NOTE: P should be hardwired to GND except during programming.

Functional Diagram



ALL LINES POSITIVE LOGIC - ACTIVE HIGH
THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE
DATA LATCHES:
L HIGH → Q = D
Q LATCHES ON RISING EDGE OF $\overline{E}$
ADDRESS LATCHES AND GATED DECODERS:
LATCH ON FALLING EDGE OF $\overline{E}$
GATE ON FALLING EDGE OF $\overline{E}$
P SHOULD BE HARDWIRED TO GND EXCEPT DURING PROGRAMMING

Programming

Introduction

The HM-6642 is a 512 word by 8-bit field Programmable Read Only Memory utilizing nicrome fusible links as programmable memory elements. Selected memory locations are permanently changed from their manufactured state, of all low (V_{OL}) to a logical high (V_{OH}), by the controlled application of programming potentials and pulses. Careful adherence to the following programming specifications will result in high programming yield. Both high V_{CC} (6.0V) and low V_{CC} (4.0V) verify cycles are specified to assure the integrity of the programmed fuse. This programming specification, although complete, does not preclude rapid programming. The worst case programming time required is 37.4 seconds, and typical programming time can be approximately 4 seconds per device.

The chip ($\overline{E}$) and output enable ($\overline{G}$) are used during the programming procedure. On PROMs which have more than one output enable control G3 is to be used. The other output enables must be held in the active, or enabled, state throughout the entire programming sequence. The programmer designer is advised that all pins of the programmer's socket should be at ground potential when the PROM is inserted into the socket. V_{CC} must be applied to the PROM before any input or output pin is allowed to rise (See Note).

Overall Programming Procedure

1. The address of the first bit to be programmed is presented, and latched by the chip enable ($\overline{E}$) falling edge. The output is disabled by taking the output enable $\overline{G}$ Low: The programming pin is enabled by taking (P) high.
2. V_{CC} is raised to the programming voltage level, 12.5V.
3. All data output pins are pulled up to V_{CC} program. Then the data output pin corresponding to the bit to be programmed is pulled low for 100ms. Only one bit should be programmed at a time.
4. The data output pin is returned to V_{CC}, and the V_{CC} pin is returned to 6.0V.
5. The address of the bit is again presented, and latched by a second chip enable falling edge.
6. The data outputs are enabled, and read, to verify that the bit was successfully programmed.
   a). If verified, the next bit to be programmed is addressed and programmed.
   b). If not verified, the programs verify sequence is repeated up to 8 times total.
7. After all bits to be programmed have been verified at 6.0V, the V_{CC} is lowered to 4.0V and all bits are verified.
   a). If all bits verify, the device is properly programmed.
   b). If any bit fails to verify, the device is rejected.

Programming System Requirements

1. The power supply for the device to be programmed must be able to be set to three voltages: 4.0V, 6.0V, 12.5V. This supply must be able to supply 500mA average, and 1A dynamic, currents to the PROM during programming. The power supply rise fall times when switching between voltages must be no quicker than 1ms.
2. The address drivers must be able to supply a V_{IH} of 4.0V and 6.0V and V_{IL} when the system is at programming voltages. (See Note)
3. The control input buffers must be able to maintain input voltage levels of ≥ 70% and ≤ 20% V_{CC} for V_{IH} and V_{IL} levels, respectively. Notice that chip enable ($\overline{E}$) and $\overline{G}$ does not require a pull up to programming voltage levels. The program control (P) must switch from ground to VIH and from V_{IH} to the V_{CC} PGM level. (See Note)
4. The data input buffers must be able to sink up to 3mA from the PROM's output pins without rising more than 0.7V above ground, be able to hold the other outputs high with a current source capability of 0.5mA to 2.0mA, and not interfere with the reading and verifying of the data output of the PROM. Notice that a bit to be programmed is changed from a low state (V_{OL}) to high (V_{OH}) by pulling low on the output pin. A suggested implementation is open collector TTL buffers (or inverters) with 4.7kΩ pull up resistors to V_{CC}. (See Note)

NOTE: Never allow any input or output pin to rise more than 0.3V above V_{CC}, or fall more than 0.3V below ground.

Background Information HM-6642 Programming

PROGRAMMING SPECIFICATIONS

SYMBOL	PARAMETER	LIMITS			UNITS
		MIN	TYP	MAX	
VCC PROG	Programming VCC	12.0	12.0	12.5	V
VCCN	Operating VCC	4.5	5.5	5.5	V
VCC LV	Special Verify VCC	4.0	-	6.0	V
ICC	System ICC Capability	500	-	-	mA
ICC Peak	Transient ICC Capability	1.0	-	-	A
PROM INPUT PINS					
VOL	Output Low Voltage (To PROM)	-0.3	GND	20% VCC	V
VOH	Output High Voltage (To PROM)	70% VCC	VCC	VCC +0.3	V
IOL	Output Sink Current (At VOL)	0.01	-	-	mA
IOH	Output Source Current (At VOH)	0.01	-	-	mA
PROM DATA OUTPUT PINS					
VOL	Output Low Voltage (To PROM)	-0.3	GND	0.7	V
VOH	Output High Voltage (To PROM)	70% VCC	VCC	VCC +0.3	V
IOL	Output Sink Current (At VOL)	3.0	-	-	mA
IOH	Output Source Current (At VOH)	0.5	1.0	2.0	mA
tD	Delay Time	1.0	1.0	-	µs
tR	Rise Time	1.0	10.0	10.0	µs
tF	Fall Time	1.0	10.0	10.0	µs
TEHEL	Chip Enable Pulse Width	500	-	-	ns
TAVEL	Address Valid to Chip Enable Low Time	500	-	-	ns
TELQV	Chip Enable Low to Output Valid Time	-	-	500	ns
tpw	Programming Pulse Width	90	100	110	µs
tIP	Input Leakage at VCC = VCC PROG	-10	+1.0	10	µA
TA	Ambient Temperature	-	25	-	^{o}C

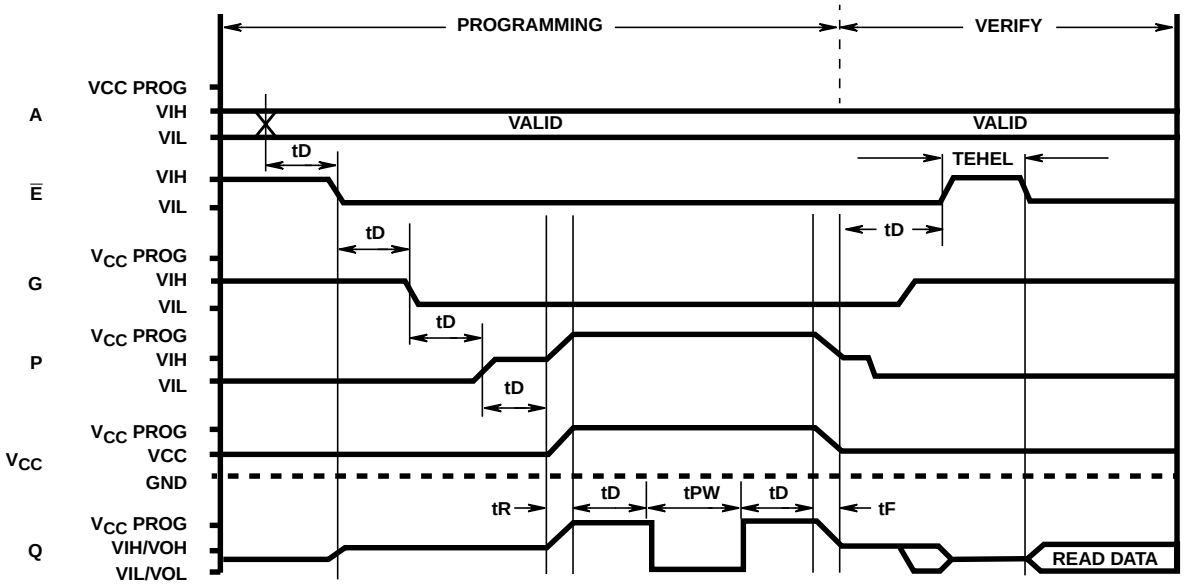


FIGURE 1. HM-6642 PROGRAMMING CYCLE

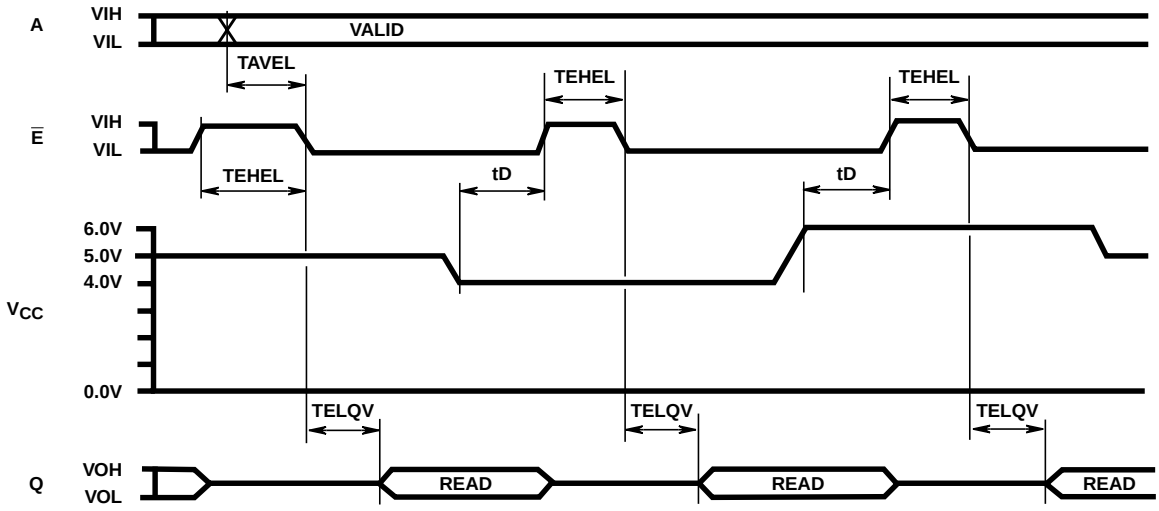


FIGURE 2. HM-6642 POST PROGRAMMING VERIFY CYCLE

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.3V to V_{CC} +0.3V
Typical Derating Factor . . . . . 5mA/MHz Increase in ICCOP
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range
HM-6642B-9, HM-6642-9 . . . . . -40^oC to $+85^oC$

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
SBDIP Package	$52^oC/W$	$14^oC/W$
Slim SBDIP	$70^oC/W$	$19^oC/W$
CLCC Package	$58^oC/W$	$14^oC/W$

Maximum Storage Temperature Range . . . . . -65^oC to $+150^oC$
Maximum Junction Temperature . . . . . $+175^oC$
Maximum Lead Temperature (Soldering 10s) $+300^oC$

Die Characteristics

Gate Count . . . . . 1680 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

V_{CC} = 5V ± 10%; T_A = -40^oC to $+85^oC$ (HM-6642B-9, HM-6642-9)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	100	µA	IO = 0, VI = VCC or GND, VCC = 5.5V
ICCOP	Operating Supply Current (Note 3)	-	20	mA	f = 1MHz, IO = 0, VI = VCC or GND, VCC = 5.5V
II	Input Leakage Current	-1.0	+1.0	µA	GND ≤ VI ≤ VCC, VCC = 5.5V
IOZ	Output Leakage Current	-1.0	+1.0	µA	GND ≤ VO ≤ VCC, VCC = 5.5V
VIL	Input Low Voltage	-0.3	0.8	V	VCC = 4.5V
VIH	Input High Voltage	2.4	VCC + 0.3	V	VCC = 5.5V
VOL	Output Low Voltage	-	0.4	V	IOL = 3.2mA, VCC = 4.5V
VOH1	Output High Voltage	2.4	-	V	IOH = -1.0mA, VCC = 4.5V
VOH2	Output High Voltage (Note 2)	VCC - 1.0	-	V	IOH = -100µA, VCC = 4.5V

AC Electrical Specifications

SYMBOL	PARAMETER	LIMITS HM-6642B-9 MIN	LIMITS HM-6642B-9 MAX	LIMITS HM-6642-9 MIN	LIMITS HM-6642-9 MAX	UNITS	TEST CONDITIONS
(1) TELQV	Chip Enable Access Time	-	120	-	200	ns	Notes 1, 4
(2) TAVQV	Address Access Time (TAVQV = TELQV + TAVEL)	-	140	-	220	ns	Notes 1, 4
(3) TGVQV	Output Enable Access Time	-	50	-	150	ns	Notes 1, 4
(4) TGVQX	Output Enable Time	5	50	5	150	ns	Notes 2, 4
(5) TGXQZ	Output Disable Time	-	50	-	150	ns	Notes 2, 4
(6) TELEH	Chip Enable Pulse Negative Width	120	-	200	-	ns	Notes 1, 4
(7) TELEL	Read Cycle Time	160	-	350	-	ns	Notes 1, 4
(8) TEHEL	Chip Enable Pulse Positive Width	40	-	150	-	ns	Notes 1, 4
(9) TAVEL	Address Setup Time	20	-	20	-	ns	Notes 1, 4
(10) TELAX	Address Hold Time	25	-	60	-	ns	Notes 1, 4

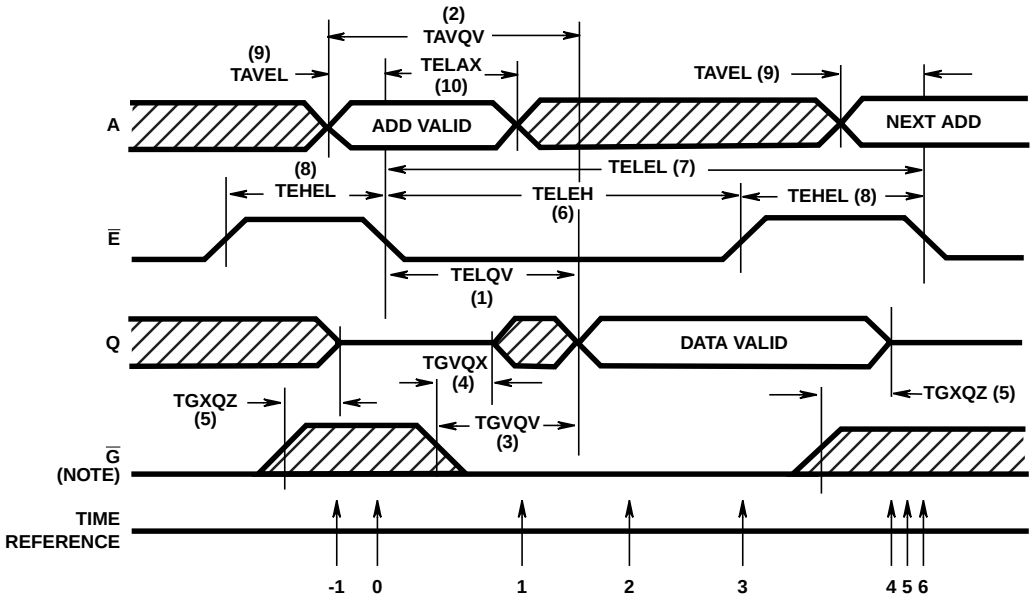
Capacitance $T_A = +25^oC$

SYMBOL	PARAMETER	LIMITS		UNITS	TEST CONDITIONS
		MIN	MAX		
CI	Input Capacitance (Note 2)	-	10.0	pF	f = 1MHz, All Measurements Reference Device Ground
CO	Output Capacitance (Note 2)	-	12.0	pF	

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent C_L = 50pF (min) - for C_L greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. V_{CC} = 4.5V and 5.5V.

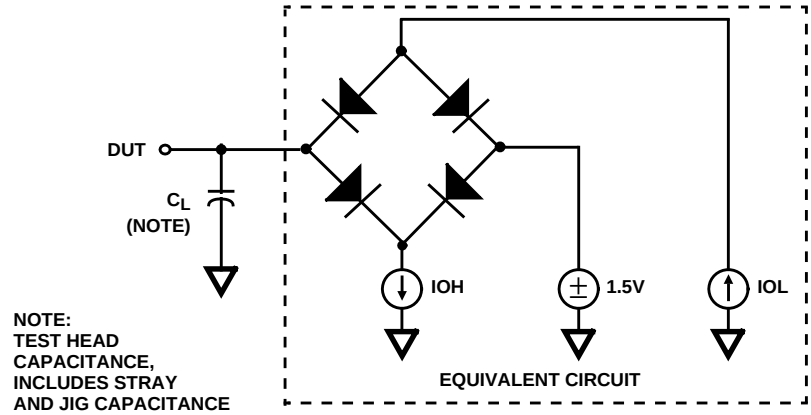
Switching Waveform



NOTE: G has the same timing as $\overline{G}$ except signal is inverted.

FIGURE 3. READ CYCLE

Test Load Circuit



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Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
Taiwan Limited
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029