

### Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low Power Standby and Operating Power
  - ICCSB .....100 $\mu$ A
  - ICCOP .....20mA at 1MHz
- Fast Access Time..... 90/120ns
- Industry Standard Pinout
- Single 5.0V Supply
- CMOS/TTL Compatible Inputs
- High Output Drive ..... 12 LSTTL Loads
- Synchronous Operation
- On-Chip Address Latches
- Separate Output Enable
- Operating Temperature Range ..... -55 $^{\circ}$ C to +125 $^{\circ}$ C

### Description

The HM-6617/883 is a 16,384-bit fuse link CMOS PROM in a 2K word by 8-bit/word format with "Three-State" outputs. This PROM is available in the standard 0.600 inch wide 24 pin SBDIP, the 0.300 inch wide slim SBDIP, and the JEDEC standard 32 pad CLCC.

The HM-6617/883 utilizes a synchronous design technique. This includes on-chip address latches and a separate output enable control which makes this device ideal for applications utilizing recent generation microprocessors. This design technique, combined with the Intersil advanced self-aligned silicon gate CMOS process technology offers ultra-low standby current. Low ICCSB is ideal for battery applications or other systems with low power requirements.

The Intersil NiCr fuse link technology is utilized on this and other Intersil CMOS PROMs. This gives the user a PROM with permanent, stable storage characteristics over the full industrial and military temperature voltage ranges. NiCr fuse technology combined with the low power characteristics of CMOS provides an excellent alternative to standard bipolar PROMs or NMOS EPROMs.

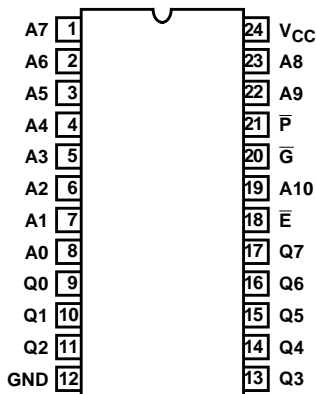
All bits are manufactured storing a logical "0" and can be selectively programmed for a logical "1" at any bit location.

### Ordering Information

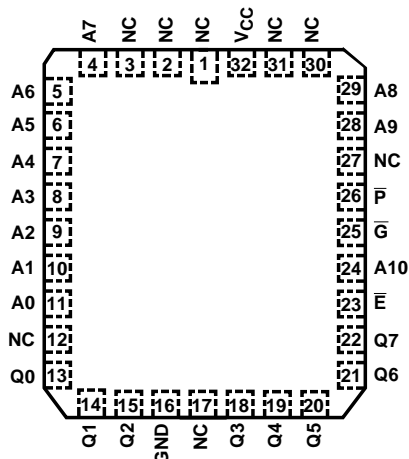
PACKAGE	TEMPERATURE RANGE	90ns	120ns	PACKAGE NO.
SBDIP	-55 $^{\circ}$ C to +125 $^{\circ}$ C	HM1-6617B/883	HM1-6617B/883	D24.6
SLIM SBDIP	-55 $^{\circ}$ C to +125 $^{\circ}$ C	HM6-6617B/883	HM6-6617B/883	D24.3
CLCC	-55 $^{\circ}$ C to +125 $^{\circ}$ C	HM4-6617B/883	HM4-6617B/883	J32.A

### Pinouts

HM-6617/883 (SBDIP)  
TOP VIEW



HM-6617/883 (CLCC)  
TOP VIEW

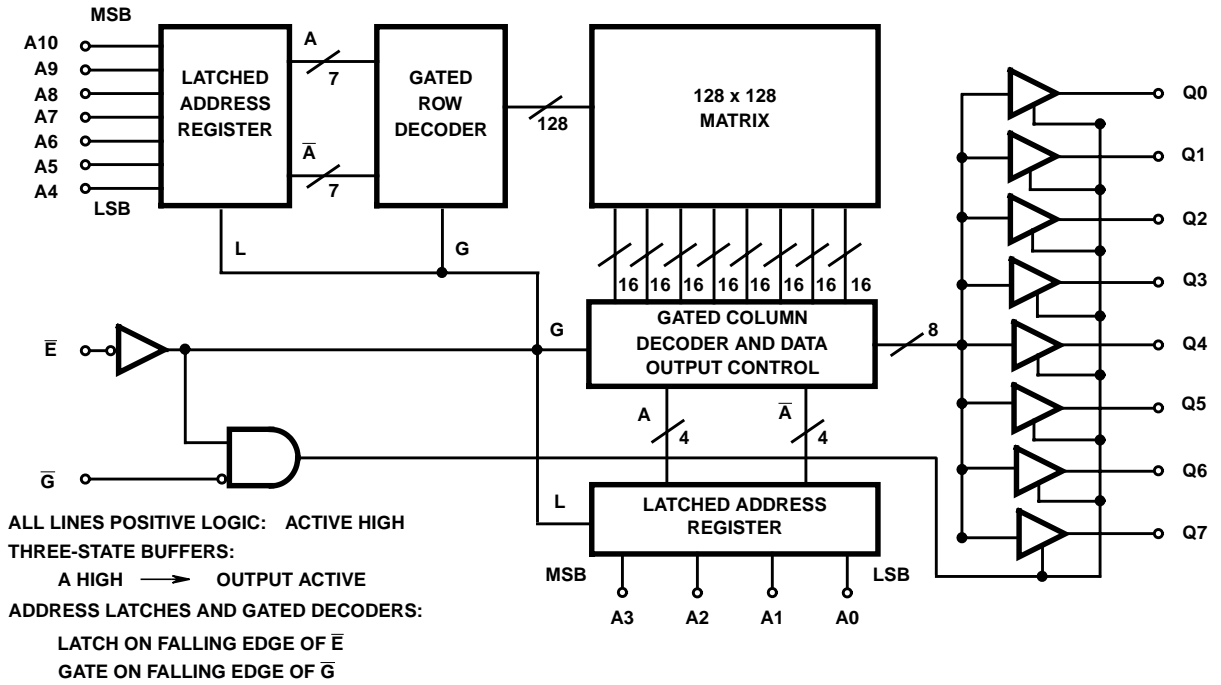


### PIN DESCRIPTION

PIN	DESCRIPTION
NC	No Connect
A0-A10	Address Inputs
$\bar{E}$	Chip Enable
Q	Data Output
VCC	Power (+5V)
$\bar{G}$	Output Enable
$\bar{P}$ (Note)	Program Enable

NOTE:  $\bar{P}$  should be hardwired to VCC except during programming.

**Functional Diagram**



**Absolute Maximum Ratings**

Supply Voltage . . . . . +7.0V  
 Input, Output or I/O Voltage . . . . . GND -0.3V to VCC +0.3V  
 Typical Derating Factor . . . . . 5mA/MHz Increase in ICCOP  
 ESD Classification . . . . . Class 1

**Operating Conditions**

Operating Voltage Range . . . . . +4.5V to +5.5V  
 Operating Temperature Range . . . . . -55°C to +125°C  
 Input Low Voltage . . . . . -0.3V to +0.8V  
 Input High Voltage . . . . . +2.4V to VCC +0.3V

**Thermal Information**

Thermal Resistance  $\theta_{JA}$   $\theta_{JC}$   
 SBDIP Package . . . . . 48°C/W 9°C/W  
 Slim SBDIP . . . . . 65°C/W 14°C/W  
 CLCC Package . . . . . 58°C/W 19°C/W  
 Maximum Storage Temperature Range . . . . . -65°C to +150°C  
 Maximum Junction Temperature . . . . . +175°C  
 Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

**Die Characteristics**

Gate Count . . . . . 5473 Gates

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

**TABLE 1. HM-6617/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS**

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 4) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
High Level Output Voltage	VOH1	VCC = 4.5V, IO = -2.0mA	1, 2, 3	-55°C ≤ TA ≤ +125°C	2.4	-	V
Low Level Output Voltage	VOL	VCC = 4.5V, IO = +4.8mA	1, 2, 3	-55°C ≤ TA ≤ +125°C	-	0.4	V
High Impedance Output Leakage Current	IIOZ	VCC = 5.5V, $\bar{G}$ = 5.5V, VI/O = GND or VCC	1, 2, 3	-55°C ≤ TA ≤ +125°C	-1.0	1.0	μA
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC, $\bar{P}$ Not Tested	1, 2, 3	-55°C ≤ TA ≤ +125°C	-1.0	1.0	μA
Standby Supply Current	ICCSB	VI = VCC or GND, VCC = 5.5V, IO = 0mA	1, 2, 3	-55°C ≤ TA ≤ +125°C	-	100	μA
Operating Supply Current	ICCOP	VCC = 5.5V, $\bar{G}$ = GND, (Note 3), f = 1MHz, IO = 0mA, VI = VCC or GND	1, 2, 3	-55°C ≤ TA ≤ +125°C	-	20	mA
Functional Test	FT	VCC = 4.5V (Note 6)	7, 8A, 8B	-55°C ≤ TA ≤ +125°C	-	-	

**TABLE 2. HM-6617/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS**

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2, 4) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS HM-6617B/883		LIMITS HM-6617/883		UNITS
					MIN	MAX	MIN	MAX	
Address Access Time	TAVQV	VCC = 4.5V and 5.5V (Note 5)	9, 10, 11	-55°C ≤ TA ≤ +125°C	-	105	-	140	ns
Output Enable Access Time	TGLQV	VCC = 4.5V and 5.5V	9, 10, 11	-55°C ≤ TA ≤ +125°C	-	40	-	50	ns
Chip Enable Access Time	TELQV	VCC = 4.5V and 5.5V	9, 10, 11	-55°C ≤ TA ≤ +125°C	-	90	-	120	ns
Address Setup Time	TAVEL	VCC = 4.5V and 5.5V	9, 10, 11	-55°C ≤ TA ≤ +125°C	15	-	20	-	ns
Address Hold Time	TELAX	VCC = 4.5V and 5.5V	9, 10, 11	-55°C ≤ TA ≤ +125°C	20	-	25	-	ns
Chip Enable Low Width	TELEH	VCC = 4.5V and 5.5V	9, 10, 11	-55°C ≤ TA ≤ +125°C	95	-	120	-	ns
Chip Enable High Width	TEHEL	VCC = 4.5V and 5.5V	9, 10, 11	-55°C ≤ TA ≤ +125°C	40	-	40	-	ns

## HM-6617/883

**TABLE 2. HM-6617/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)**

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2, 4) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS HM-6617B/883		LIMITS HM-6617/883		UNITS
					MIN	MAX	MIN	MAX	
Read Cycle Time	TELEL	VCC = 4.5V and 5.5V	9, 10, 11	-55°C ≤ TA ≤ +125°C	136	-	160	-	ns

NOTES:

1. All voltages referenced to Device GND.
2. AC measurements assume transition time ≤ 5ns; input levels = 0.0V to 3.0V; timing reference levels = 1.5V; output load = 1TTL equivalent load and CL ≅ 50pF.
3. Typical derating = 5mA/MHz increase in ICCOP.
4. All tests performed with  $\bar{P}$  hardwired to VCC.
5. TAVQV = TELQV + TAVEL.
6. Tested as follows: f = 1MHz, VIH = 2.4V, VIL = 0.8V, IOH = -1mA, IOL = +1mA, VOH ≥ 1.5V, VOL ≤ 1.5V.

**TABLE 3. HM-6617/883 AC AND DC ELECTRICAL PERFORMANCE SPECIFICATIONS**

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	NOTES	TEMPERATURE	LIMITS HM-6617B/883		LIMITS HM-6617/883		UNITS
					MIN	MAX	MIN	MAX	
Input Capacitance	CIN	VCC = Open, f = 1MHz, All Measurements Referenced to Device GND	2, 3	+25°C	-	10	-	10	pF
		VCC = Open, f = 1MHz, All Measurements Referenced to Device GND	2, 4	+25°C	-	12	-	12	pF
			2, 5	+25°C	-	10	-	10	pF
I/O Capacitance	CI/O	VCC = Open, f = 1MHz, All Measurements Referenced to Device GND	2, 3	+25°C	-	12	-	12	pF
		VCC = Open, f = 1MHz, All Measurements Referenced to Device GND	2, 4	+25°C	-	14	-	14	pF
			2, 5	+25°C	-	12	-	12	pF
Chip Enable Time	TELQX	VCC = 4.5V and 5.5V	2	-55°C ≤ TA ≤ +125°C	5	-	5	-	ns
Output Enable Time	TGLQX	VCC = 4.5V and 5.5V	2	-55°C ≤ TA ≤ +125°C	5	-	5	-	ns
Chip Disable Time	TEHQZ	VCC = 4.5V and 5.5V	2	-55°C ≤ TA ≤ +125°C	-	45	-	50	ns
Output Disable Time	TGHQZ	VCC = 4.5V and 5.5V	2	-55°C ≤ TA ≤ +125°C	-	40	-	50	ns
Output High Voltage	VOH2	VCC = 4.5V, IO = 100μA	2	-55°C ≤ TA ≤ +125°C	VCC-1V	-	VCC-1V	-	V

NOTES:

1. All tests performed with  $\bar{P}$  hardwired to VCC.
2. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design changes which would affect these characteristics.
3. Applies to 0.600 inch SBDIP device types only.
4. Applies to 0.300 inch SBDIP device types only.
5. Applies to Ceramic Leadless Chip Carrier (CLCC) device types only.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Switching Waveforms

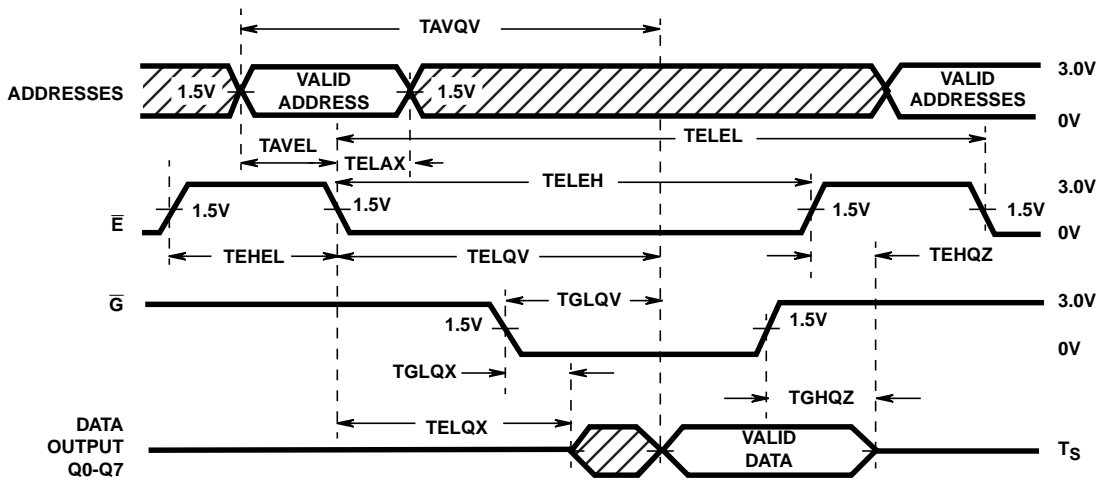


FIGURE 1. READ CYCLE

Test Circuit

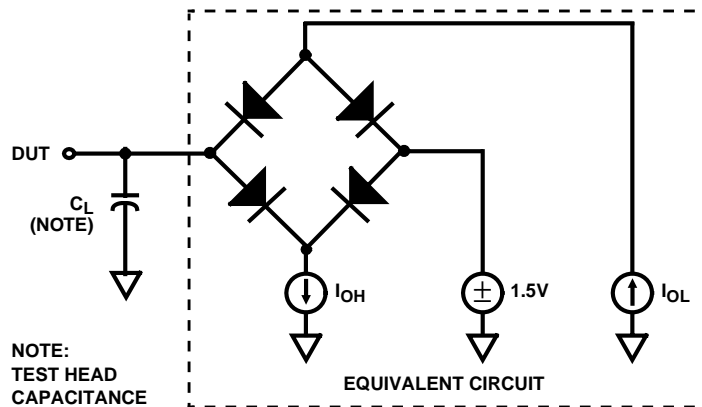
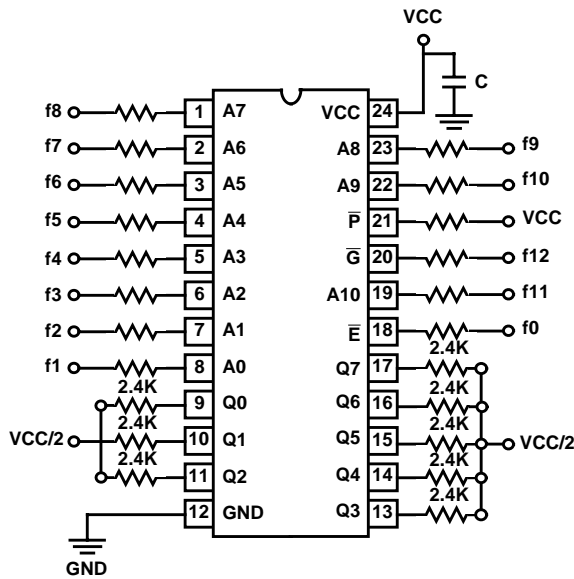


FIGURE 2. TEST CIRCUIT

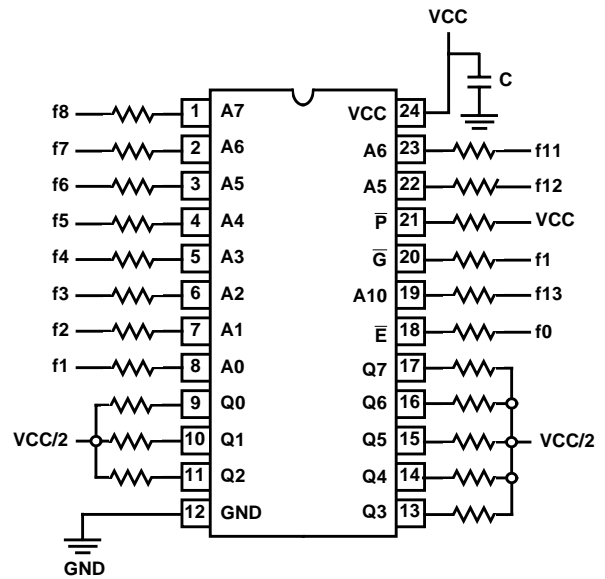
# HM-6617/883

## Burn-In Circuits

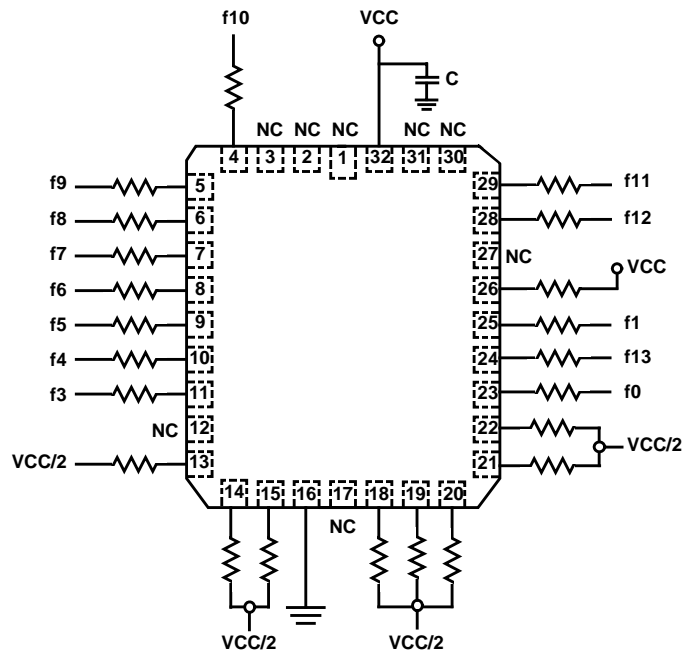
HM-6617/883 (.300 INCH) SBDIP



HM-6617/883 (.600 INCH) SBDIP



HM-6617/883 CLCC



**NOTES:**

f0 = 100KHz ± 10%.

All resistors = 47kΩ Unless Otherwise Noted.

VCC = 5.5V ± 0.05V.

C = 0.01 μF min.

## HM-6617/883

### Die Characteristics

#### DIE DIMENSIONS:

140 x 232 x 19 ± 1mils

#### METALLIZATION:

Type: Si - Al

Thickness: 11kÅ ± 15kÅ

#### GLASSIVATION:

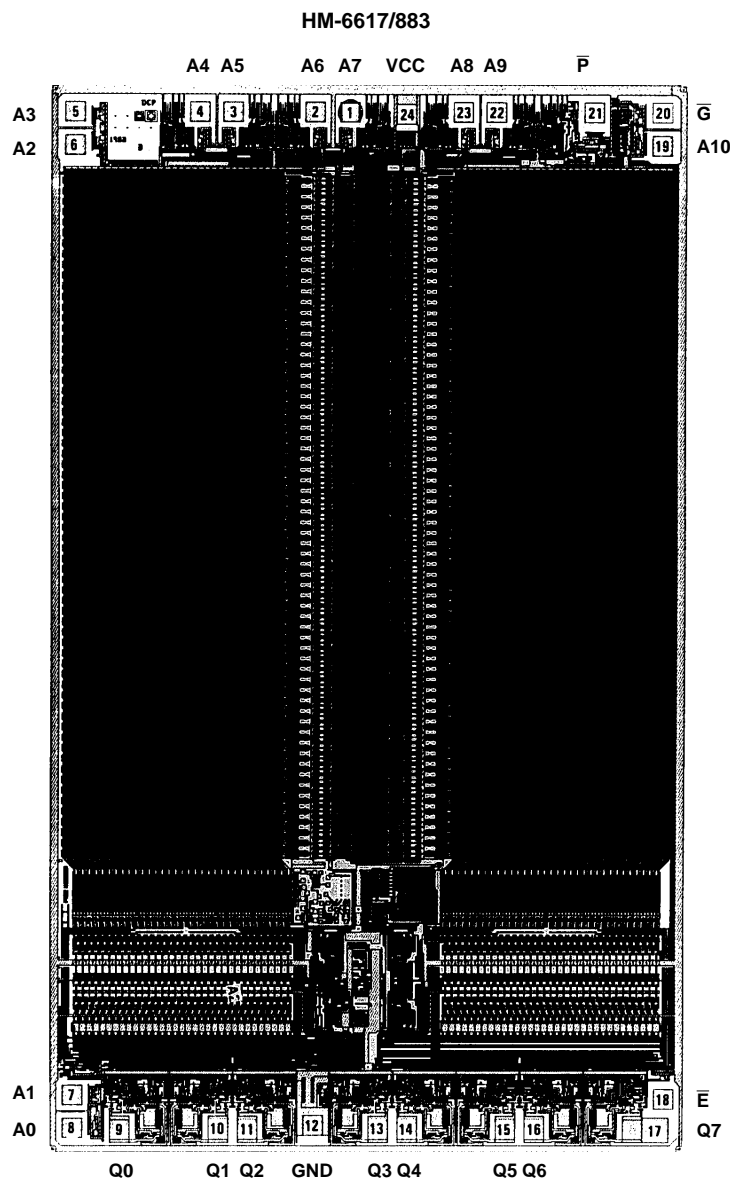
Type: SiO<sub>2</sub>

Thickness: 7kÅ ± 9kÅ

#### WORST CASE CURRENT DENSITY:

1.7 x 10<sup>5</sup> A/cm<sup>2</sup>

### Metallization Mask Layout



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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