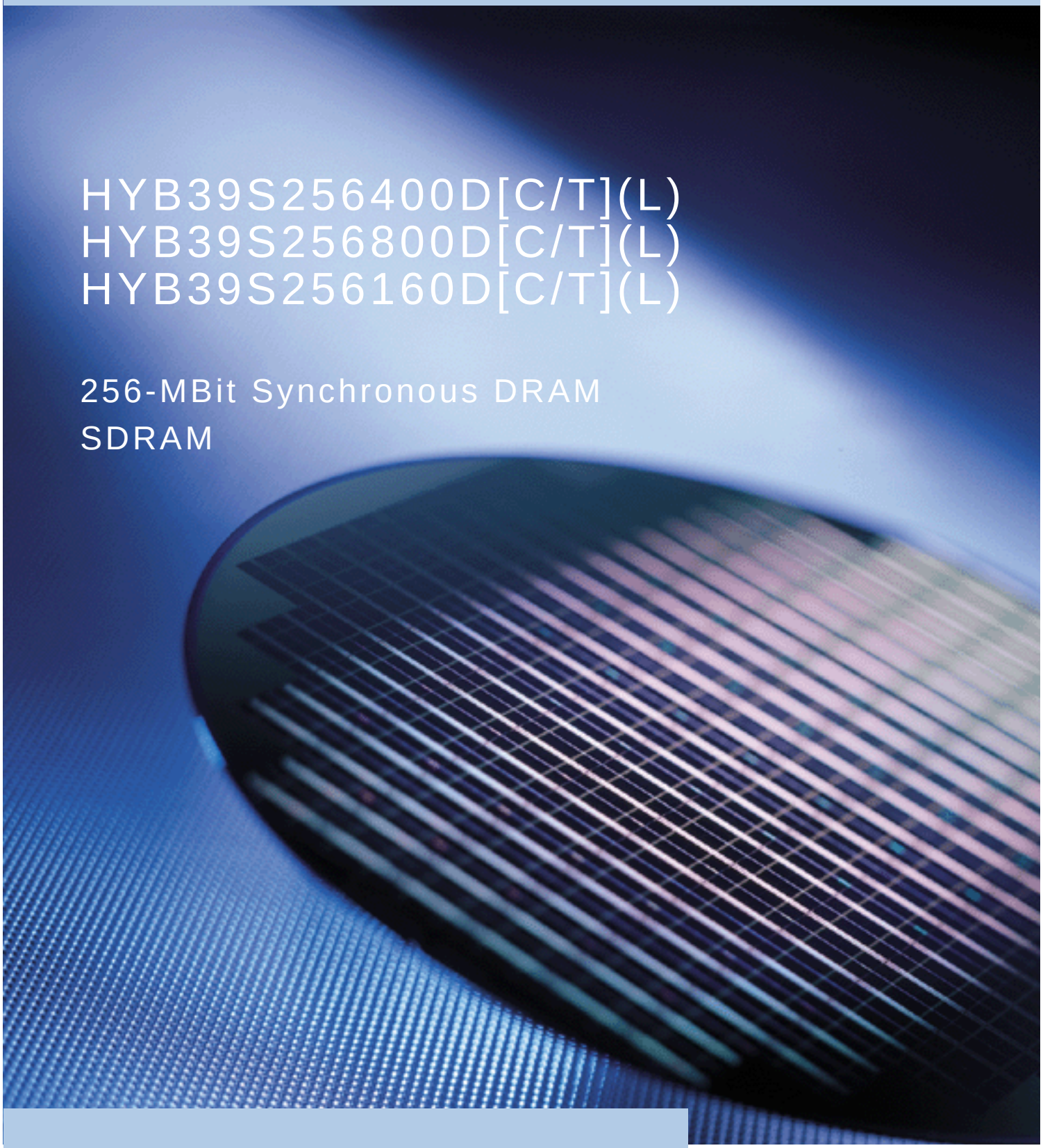
Data Sheet, Rev. 1.02, Feb. 2004

# HYB39S256400D[C/T](L)
# HYB39S256800D[C/T](L)
# HYB39S256160D[C/T](L)

## 256-MBit Synchronous DRAM
## SDRAM



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Data Sheet, Rev. 1.02, Feb. 2004

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| **Revision History:** | **Rev. 1.02** | **2004-02** |
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| Page | Subjects (major changes since last revision) | |
| 17 | Corrected Mode Register Definition in chapter 3 | |
| all | Various layout and editorial changes | |
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| all | Various layout and editorial changes | |
| Previous Version: | Rev. 1.0 | 2002-06 |

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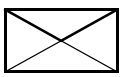

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# 1 Overview

## 1.1 Features

- Fully Synchronous to Positive Clock Edge
- 0 to 70 °C operating temperature
- Four Banks controlled by BA0 & BA1
- Programmable $\overline{\text{CAS}}$ Latency: 2 & 3
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length: 1, 2, 4, 8 and full page
- Multiple Burst Read with Single Write Operation
- Automatic and Controlled Precharge Command
- Data Mask for Read / Write control (x4, x8)
- Data Mask for byte control (x16)
- Auto Refresh (CBR) and Self Refresh
- Power Down and Clock Suspend Mode
- 8192 refresh cycles / 64 ms (7,8 µs)
- Random Column Address every CLK (1-N Rule)
- Single 3.3 V ± 0.3 V Power Supply
- LVTTL Interface versions
- Plastic Packages: P–TSOPII–54 400mil width (x4, x8, x16)
- Chipsize Packages: P–TFBGA–54 (12 mm x 8 mm)

**Table 1 Performance**

| Part Number Speed Code | | | –6 | –7 | -7.5 | –8 | Unit |
|---|---|---|---|---|---|---|---|
| Speed Grade | | | PC166 3–3–3 | PC133 2–2–2 | PC133 3–3–3 | PC100 2–2–2 | — |
| max. Clock Frequency | @CL3 | $f_{CK3}$ | 166 | 143 | 133 | 125 | MHz |
| | | $t_{CK3}$ | 6 | 7 | 7.5 | 8 | ns |
| | | $t_{AC3}$ | 5 | 5.4 | 5.4 | 6 | ns |
| | @CL2 | $t_{CK2}$ | 7.5 | 7.5 | 10 | 10 | ns |
| | | $t_{AC2}$ | 5.4 | 5.4 | 6 | 6 | ns |

## 1.2 Description

The HYB39S256[40/80/16]0D[C/T](L) are four bank Synchronous DRAM's organized as 4 banks x 16 MBit x4, 4 banks x 8 MBit x8 and 4 banks x 4 Mbit x16 respectively. These synchronous devices achieve high speed data transfer rates for $\overline{\text{CAS}}$-latencies by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock. The chip is fabricated with INFINEON's advanced 0.14 µm 256-MBit DRAM process technology.

The device is designed to comply with all industry standards set for synchronous DRAM products, both electrically and mechanically. All of the control, address, data input and output circuits are synchronized with the positive edge of an externally supplied clock.

Operating the four memory banks in an interleave fashion allows random access operation to occur at a higher rate than is possible with standard DRAMs. A sequential and gapless data rate is possible depending on burst length, $\overline{\text{CAS}}$ latency and speed grade of the device.

Auto Refresh (CBR) and Self Refresh operation are supported. These devices operate with a single 3.3 V ± 0.3 V power supply. All 256-Mbit components are available in P–TSOPII–54 and P–TFBGA–54 packages.

**Table 2 Ordering Information**

| Type | Speed Grade | Package | Description |
|---|---|---|---|
| HYB 39S256400DT-6 | PC166-333-520 | P-TSOP-54-2 (400mil) | 166MHz 4B x 16M x 4 SDRAM |
| HYB 39S256400DT-7 | PC133-222-520 | P-TSOP-54-2 (400mil) | 143MHz 4B x 16M x 4 SDRAM |
| HYB 39S256400DT-7.5 | PC133-333-520 | P-TSOP-54-2 (400mil) | 133MHz 4B x 16M x 4 SDRAM |
| HYB 39S256400DT-8 | PC100-222-620 | P-TSOP-54-2 (400mil) | 125MHz 4B x 16M x 4 SDRAM |
| HYB 39S256800DT-6 | PC166-333-520 | P-TSOP-54-2 (400mil) | 166MHz 4B x 8M x 8 SDRAM |
| HYB 39S256800DT-7 | PC133-222-520 | P-TSOP-54-2 (400mil) | 143MHz 4B x 8M x 8 SDRAM |
| HYB 39S256800DT-7.5 | PC133-333-520 | P-TSOP-54-2 (400mil) | 133MHz 4B x 8M x 8 SDRAM |
| HYB 39S256800DT-8 | PC100-222-620 | P-TSOP-54-2 (400mil) | 125MHz 4B x 8M x 8 SDRAM |
| HYB 39S256160DT-6 | PC166-333-520 | P-TSOP-54-2 (400mil) | 166MHz 4B x 4M x 16 SDRAM |
| HYB 39S256160DT-7 | PC133-222-520 | P-TSOP-54-2 (400mil) | 143MHz 4B x 4M x 16 SDRAM |
| HYB 39S256160DT-7.5 | PC133-333-520 | P-TSOP-54-2 (400mil) | 133MHz 4B x 4M x 16 SDRAM |
| HYB 39S256160DT-8 | PC100-222-620 | P-TSOP-54-2 (400mil) | 125MHz 4B x 4M x 16 SDRAM |
| HYB39S256400DTL-x | – | P-TSOP-54-2 (400mil) | 4B x 16M x 4 SDRAM Low Power Versions (on request) |
| HYB39S256800DTL-x | – | P-TSOP-54-2 (400mil) | 4B x 8M x 8 SDRAM Low Power Versions (on request) |
| HYB39S256160DTL-x | – | P-TSOP-54-2 (400mil) | 4B x 4M x 16 SDRAM Low Power Versions (on request) |
| HYB39S256xx0DC(L)-x | – | P-TFBGA-54 | (on request) |

# 2 Pin Configuration

## 2.1 Signal Pin Description

**Table 3 Signal Pin Description**

| Pin | Type | Signal | Polarity | Function |
|---|---|---|---|---|
| CLK | Input | Pulse | Positive Edge | **Clock Input**<br>The system clock input. All of the SDRAM inputs are sampled on the rising edge of the clock. |
| CKE | Input | Level | Active High | **Clock Enable**<br>Activates the CLK signal when high and deactivates the CLK signal when low, thereby initiating either the Power Down mode, Suspend mode, or the Self Refresh mode. |
| $\overline{CS}$ | Input | Pulse | Active Low | **Chip Select**<br>$\overline{CS}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. |
| $\overline{RAS}$<br>$\overline{CAS}$<br>$\overline{WE}$ | Input | Pulse | Active Low | **Command Signals**<br>When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the command to be executed by the SDRAM. |
| A0 - A12 | Input | Level | – | **Address Inputs**<br>During a Bank Activate command cycle, A0-A12 define the row address (RA0-RA12) when sampled at the rising clock edge.<br>During a Read or Write command cycle, A0-An define the column address (CA0-CAn) when sampled at the rising clock edge. CAn depends upon the SDRAM organization:<br>64M x4 SDRAM CAn = CA9, CA11 (Page Length = 2048 bits)<br>32M x8 SDRAM CAn = CA9 (Page Length = 1024 bits)<br>16M x16 SDRAM CAn = CA8 (Page Length = 512 bits)<br>In addition to the column address, A10 (= AP) is used to invoke the autoprecharge operation at the end of the burst read or write cycle. If A10 is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If A10 is low, autoprecharge is disabled.<br>During a Precharge command cycle, A10 (= AP) is used in conjunction with BA0 and BA1 to control which bank(s) to precharge. If A10 is high, all four banks will be precharged regardless of the state of BA0 and BA1. If A10 is low, then BA0 and BA1 are used to define which bank to precharge. |
| BA0, BA1 | Input | Level | – | **Bank Select**<br>Bank Select Inputs. Bank address inputs selects which of the four banks a command applies to. |
| DQx | Input Output | Level | – | **Data Input/Output**<br>Data Input/Output pins operate in the same manner as on EDO or FPM DRAMs. |
| DQM<br>LDQM<br>UDQM | Input | Pulse | Active High | **Data Mask**<br>The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. In Write mode, DQM has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the write operation if DQM is high. One DQM input is present in x4 and x8 SDRAMs, LDQM and UDQM controls the lower and upper bytes in x16 SDRAMs. |

**Table 3 Signal Pin Description**

| Pin | Type | Signal | Polarity | Function |
|---|---|---|---|---|
| $V_{DD}$ $V_{SS}$ | Supply | – | – | **Power and Ground**<br>Power and ground for the input buffers and the core logic (3.3 V) |
| $V_{DDQ}$ $V_{SSQ}$ | Supply | – | – | **Power and Ground for DQs**<br>Isolated power supply and ground for the output buffers to provide improved noise immunity. |
| NC | – | – | – | **Not Connected**<br>No internal electrical connection is present. |

## 2.2 Package P–TSOPII–54

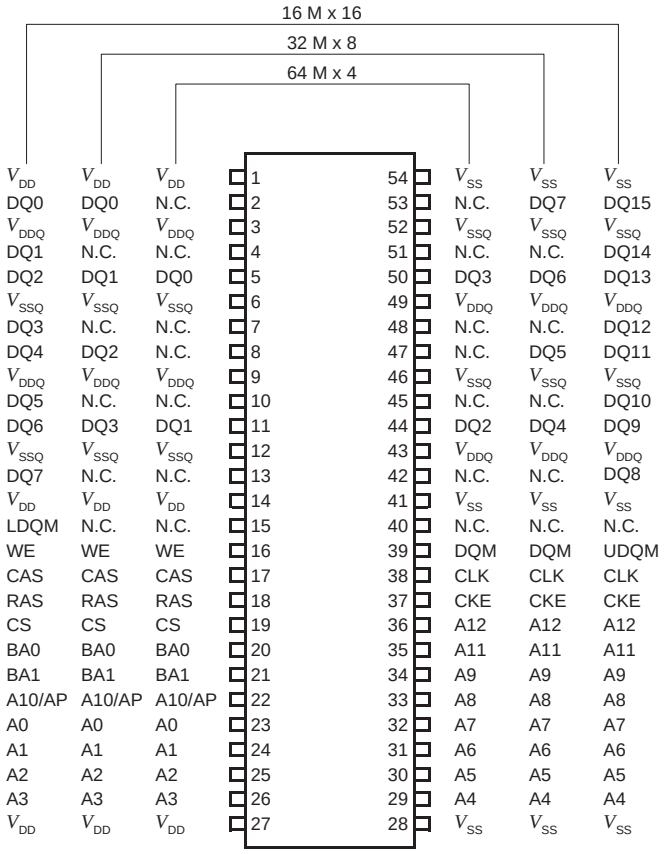



**Figure 1 Pinouts P–TSOPII–54**

## 2.3 Package P–TFBGA–54

**Table 4 Pin Configuration for x16 devices**

| 1 | 2 | 3 | | 7 | 8 | 9 |
|---|---|---|---|---|---|---|
| $V_{SS}$ | DQ15 | $V_{SSQ}$ | A | $V_{DDQ}$ | DQ0 | $V_{DD}$ |
| DQ14 | DQ13 | $V_{DDQ}$ | B | $V_{SSQ}$ | DQ2 | DQ1 |
| DQ12 | DQ11 | $V_{SSQ}$ | C | $V_{DDQ}$ | DQ4 | DQ3 |
| DQ10 | DQ9 | $V_{DDQ}$ | D | $V_{SSQ}$ | DQ6 | DQ5 |
| DQ8 | NC | $V_{SS}$ | E | NC | $V_{DDQ}$ | NC |
| $V_{REF}$ | | DM | F | $\overline{CAS}$ | $\overline{RAS}$ | $\overline{WE}$ |
| A12 | A11 | A9 | G | BA0 | BA1 | $\overline{CS}$ |
| A8 | A7 | A6 | H | A0 | A1 | A10 |
| $V_{SS}$ | A5 | A4 | J | A3 | A2 | $V_{DD}$ |

**Table 5 Pin Configuration for x8 devices**

| 1 | 2 | 3 | | 7 | 8 | 9 |
|---|---|---|---|---|---|---|
| $V_{SS}$ | DQ7 | $V_{SSQ}$ | A | $V_{DDQ}$ | DQ0 | $V_{DD}$ |
| NC | DQ6 | $V_{DDQ}$ | B | $V_{SSQ}$ | DQ2 | NC |
| NC | DQ5 | $V_{SSQ}$ | C | $V_{DDQ}$ | DQ3 | NC |
| NC | DQ4 | $V_{DDQ}$ | D | $V_{SSQ}$ | DQ6 | NC |
| NC | NC | $V_{SS}$ | E | $V_{DD}$ | NC | NC |
| DQM | CLK | CKE | F | $\overline{CAS}$ | $\overline{RAS}$ | $\overline{WE}$ |
| A12 | A11 | A9 | G | BA0 | BA1 | $\overline{CS}$ |
| A8 | A7 | A6 | H | A0 | A1 | A10 |
| $V_{SS}$ | A5 | A4 | J | A3 | A2 | $V_{DD}$ |

**Table 6 Pin Configuration for x4 devices**

| 1 | 2 | 3 | | 7 | 8 | 9 |
|---|---|---|---|---|---|---|
| $V_{SS}$ | NC | $V_{SSQ}$ | A | $V_{DDQ}$ | NC | $V_{DD}$ |
| NC | DQ3 | $V_{DDQ}$ | B | $V_{SSQ}$ | DQ0 | NC |
| NC | NC | $V_{SSQ}$ | C | $V_{DDQ}$ | NC | NC |
| NC | DQ2 | $V_{DDQ}$ | D | $V_{SSQ}$ | DQ1 | NC |
| NC | NC | $V_{SS}$ | E | $V_{DD}$ | NC | NC |
| DQM | CLK | CKE | F | $\overline{CAS}$ | $\overline{RAS}$ | $\overline{WE}$ |
| A12 | A11 | A9 | G | BA0 | BA1 | $\overline{CS}$ |
| A8 | A7 | A6 | H | A0 | A1 | A10 |
| $V_{SS}$ | A5 | A4 | J | A3 | A2 | $V_{DD}$ |

## 2.4 Block Diagrams

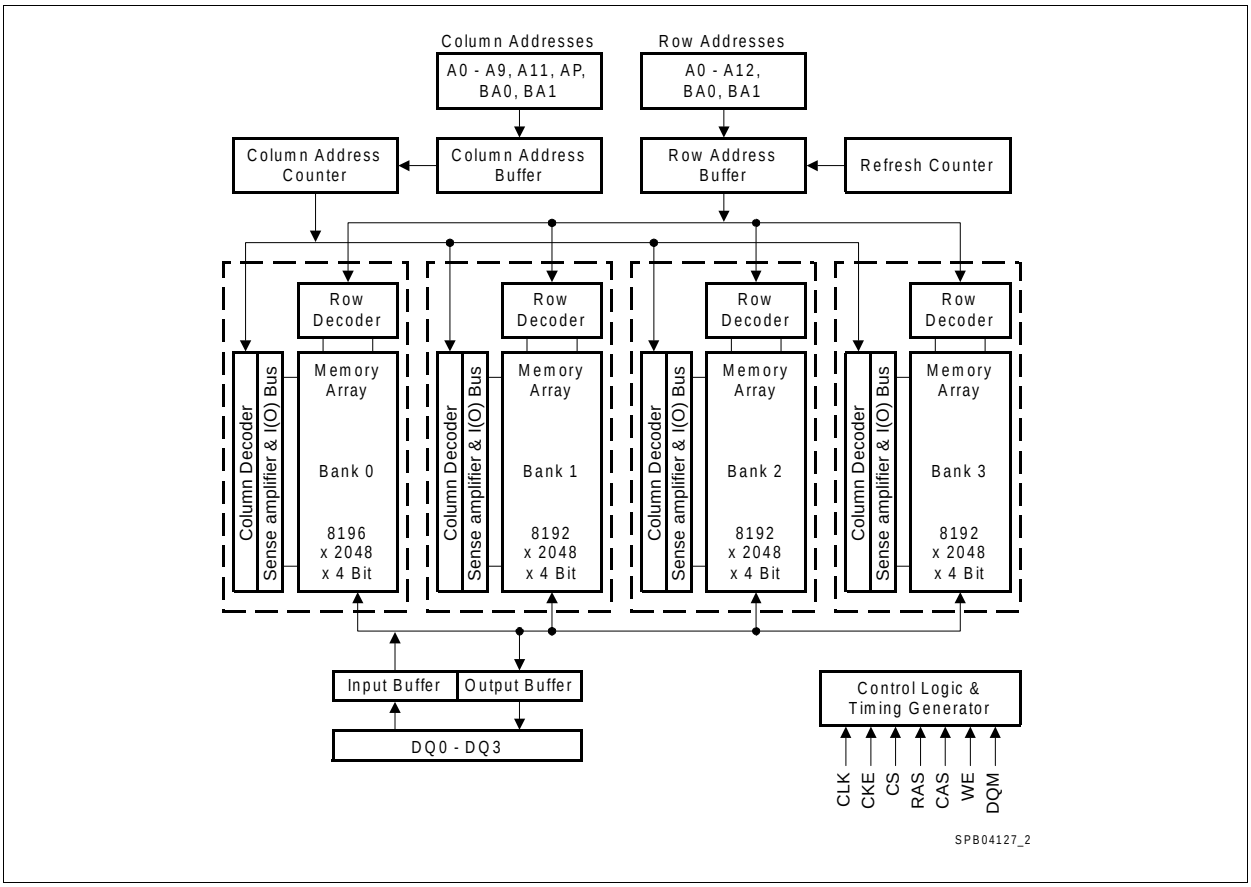



**Figure 2 Block Diagram for 64M x 4 SDRAM (13/11/2 addressing)**

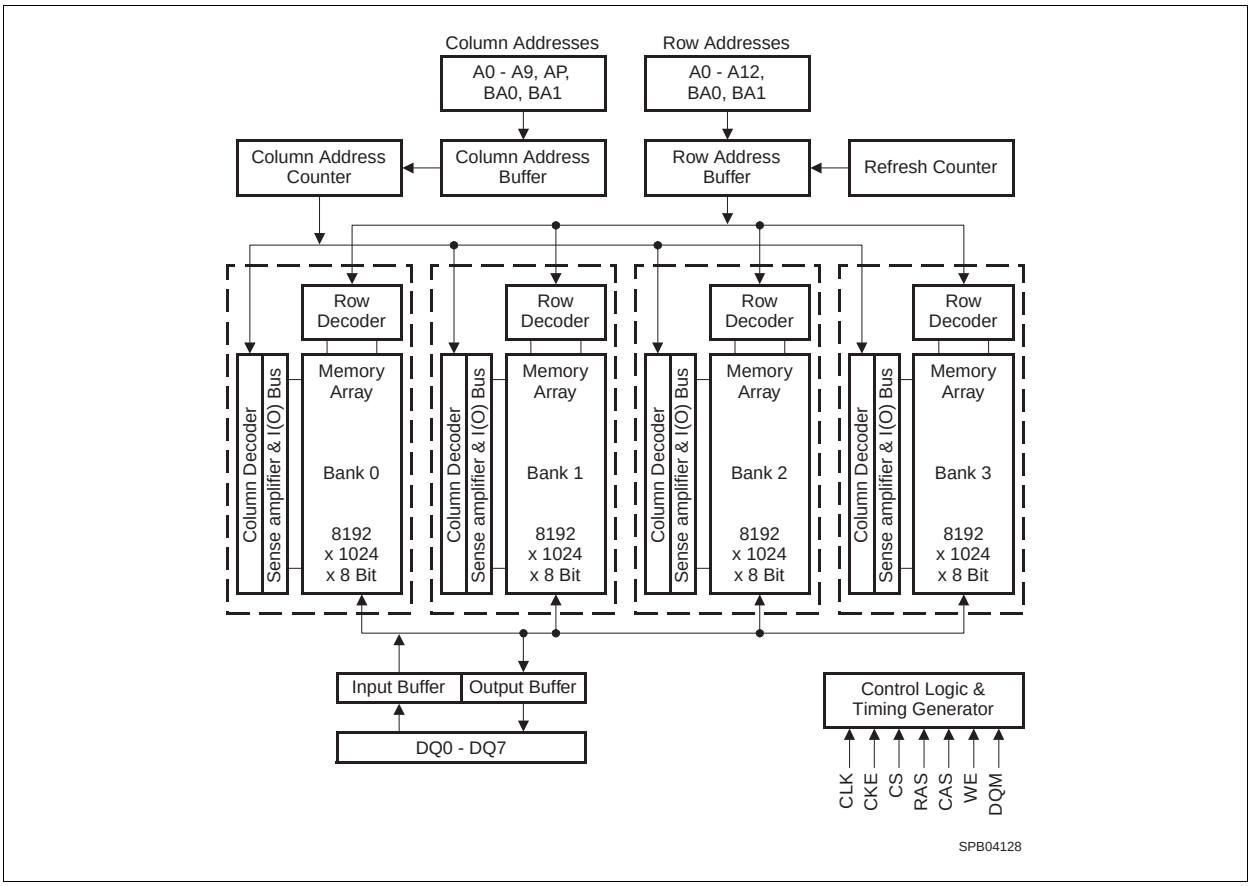



**Figure 3 Block Diagram for 32M x 8 SDRAM (13/10/2 addressing)**

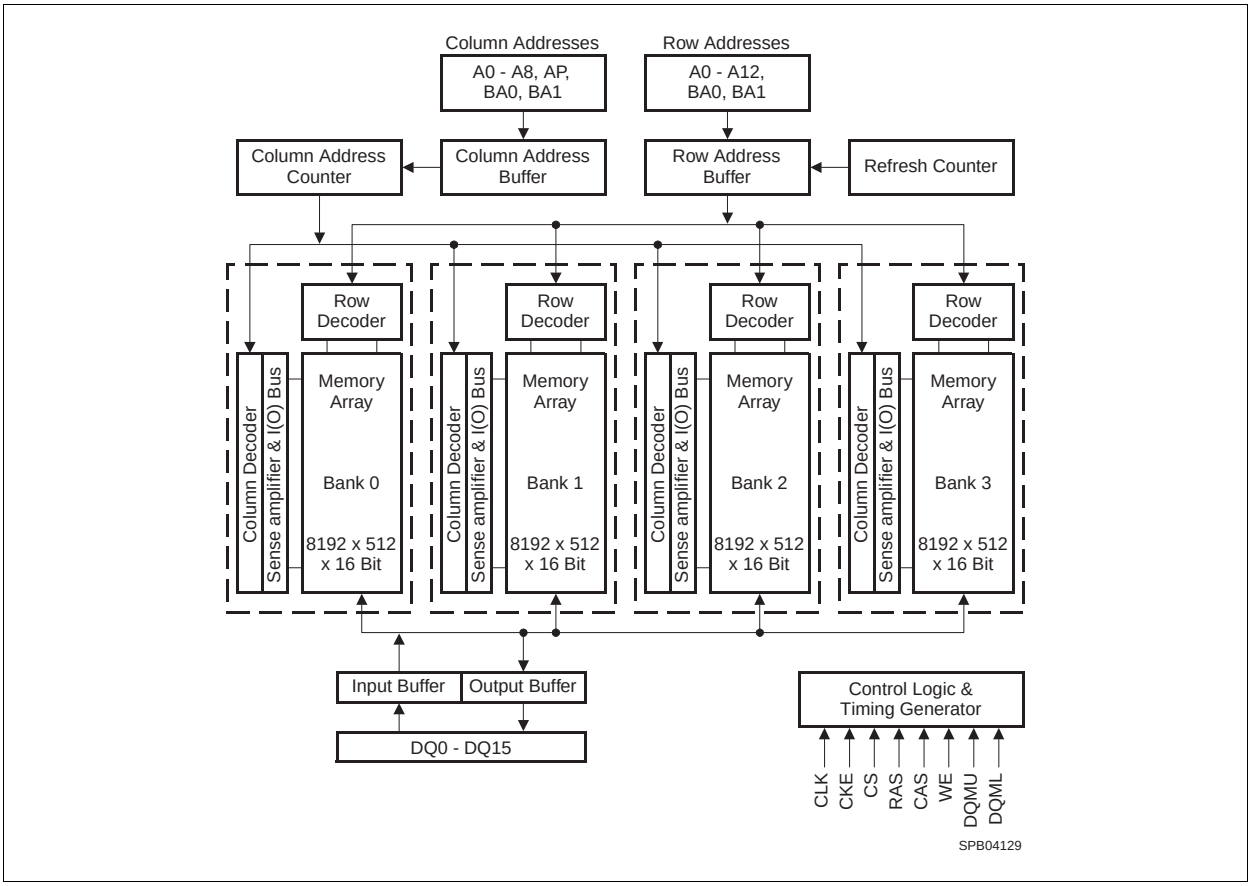



**Figure 4 Block Diagram for 16M x 16 SDRAM (13/9/2 addressing)**

# 3 Functional Description

## 3.1 Operation Definition

All of SDRAM operations are defined by states of control signals $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and DQM at the positive edge of the clock. The following list shows the truth table for the operation commands.

**Table 7 Truth Table: Operation Command**

| Operation | Device State | CKE n-1[1)2)] | CKE n[1)2)] | DQM [1)2)] | BA0 BA1[1)2)] | AP= A10[1)2)] | Addr. [1)2)] | $\overline{CS}$ [1)2)] | $\overline{RAS}$ [1)2)] | $\overline{CAS}$ [1)2)] | $\overline{WE}$ [1)2)] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Bank Active | Idle[3)] | H | X | X | V | V | V | L | L | H | H |
| Bank Precharge | Any | H | X | X | V | L | X | L | L | H | L |
| Precharge All | Any | H | X | X | X | H | X | L | L | H | L |
| Write | Active[3)] | H | X | X | V | L | V | L | H | L | L |
| Write with Autoprecharge | Active[3)] | H | X | X | V | H | V | L | H | L | L |
| Read | Active[3)] | H | X | X | V | L | V | L | H | L | H |
| Read with Autoprecharge | Active[3)] | H | X | X | V | H | V | L | H | L | H |
| Mode Register Set | Idle | H | X | X | V | V | V | L | L | L | L |
| No Operation | Any | H | X | X | X | X | X | L | H | H | H |
| Burst Stop | Active | H | X | X | X | X | X | L | H | H | L |
| Device Deselect | Any | H | X | X | X | X | X | H | X | X | X |
| Auto Refresh | Idle | H | H | X | X | X | X | L | L | L | H |
| Self Refresh Entry | Idle | H | L | X | X | X | X | L | L | L | H |
| Self Refresh Exit | Idle (Self Refr.) | L | H | X | X | X | X | H | X | X | X |
| | | | | | | | | L | H | H | X |
| Clock Suspend Entry | Active | H | L | X | X | X | X | X | X | X | X |
| Power Down Entry (Precharge or active standby) | Idle | H | L | X | X | X | X | H | X | X | X |
| | Active | | | | | | | L | H | H | H |
| Clock Suspend Exit | Active[4)] | L | H | X | X | X | X | X | X | X | X |
| Power Down Exit | Any (Power Down) | L | H | X | X | X | X | H | X | X | X |
| | | | | | | | | L | H | H | L |
| Data Write/Output Enable | Active | H | X | L | X | X | X | X | X | X | X |
| Data Write/Output Disable | Active | H | X | H | X | X | X | X | X | X | X |

1) V = Valid, x = Don't Care, L = Low Level, H = High Level

2) CKEn signal is input level when commands are provided, CKEn-1 signal is input level one clock before the commands are provided.

3) This is the state of the banks designated by BA0, BA1 signals.

4) Power Down Mode can not be entered in a burst cycle. When this command asserted in the burst mode cycle device is in clock suspend mode.

## 3.2 Initialization

The default power on state of the mode register is supplier specific and may be undefined. The following power on and initialization sequence guarantees the device is preconditioned to each users specific needs. Like a conventional DRAM, the Synchronous DRAM must be powered up and initialized in a predefined manner. During power on, all $V_{DD}$ and $V_{DDQ}$ pins must be built up simultaneously to the specified voltage when the input signals are held in the “NOP” state. The power on voltage must not exceed $V_{DD}$+0.3V on any of the input pins or $V_{DD}$ supplies. The CLK signal must be started at the same time. After power on, an initial pause of 200 ms is required followed by a precharge of all banks using the precharge command. To prevent data contention on the DQ bus during power on, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. A minimum of eight Auto Refresh cycles (CBR) are also required.These may be done before or after programming the Mode Register. Failure to follow these steps may lead to unpredictable start-up modes.

## 3.3 Mode Register Definition

The Mode register designates the operation mode at the read or write cycle. This register is divided into four fields. First, a Burst Length Field which sets the length of the burst, Second, an Addressing Selection bit which programs the column access sequence in a burst cycle (interleaved or sequential). Third, a $\overline{\text{CAS}}$ Latency Field to set the access time at clock cycle. Fourth, an Operation mode field to differentiate between normal operation (Burst read and burst Write) and a special Burst Read and Single Write mode. After the initial power up, the mode set operation must be done before any activate command. Any content of the mode register can be altered by re-executing the mode set command. All banks must be in precharged state and CKE must be high at least one clock before the mode set operation. After the mode register is set, a Standby or NOP command is required. Low signals of $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WE}}$ at the positive edge of the clock activate the mode set operation. Address input data at this timing defines parameters to be set as shown in the previous table.

**MR**
**Mode Register Definition** **(BA[1:0] = $00_B$)**

| BA1 | BA0 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **MODE** | | | | | | **CL** | | | **BT** | **BL** | | |
| reg. addr | | w | | | | | | w | | | w | w | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| **BL** | [2:0] | w | **Burst Length**<br>Number of sequential bits per DQ related to one read/write command, see **Chapter 3.3.1**<br>*Note: All other bit combinations are RESERVED*<br>000 1<br>001 2<br>010 4<br>011 8<br>111 Full Page (Sequential burst type only) |
| **BT** | 3 | w | **Burst Type**<br>See **Table 8** for internal address sequence of low order address bits.<br>0 Sequential<br>1 Interleaved |
| **CL** | [6:4] | w | **CAS Latency**<br>Number of full clocks from read command to first data valid window.<br>*Note: All other bit combinations are RESERVED.*<br>010 2<br>011 3 |
| **Operating Mode** | [13:7] | w | **Operating Mode**<br>*Note: All other bit combinations are RESERVED.*<br>0 burst read/burst write<br>1 burst read/single write |

### 3.3.1 Burst Length

**Table 8 Burst Length and Sequence**

| Burst Length | Starting Column Address | | | Order of Accesses within a Burst | |
|---|---|---|---|---|---|
| | A2 | A1 | A0 | Type=Sequential | Type=Interleaved |
| 2 | | | 0 | 0–1 | 0–1 |
| | | | 1 | 1–0 | 1–0 |
| 4 | | 0 | 0 | 0–1–2–3 | 0–1–2–3 |
| | | 0 | 1 | 1–2–3–0 | 1–0–3–2 |
| | | 1 | 0 | 2–3–0–1 | 2–3–0–1 |
| | | 1 | 1 | 3–0–1–2 | 3–2–1–0 |
| 8 | 0 | 0 | 0 | 0–1–2–3–4–5–6–7 | 0–1–2–3–4–5–6–7 |
| | 0 | 0 | 1 | 1–2–3–4–5–6–7–0 | 1–0–3–2–5–4–7–6 |
| | 0 | 1 | 0 | 2–3–4–5–6–7–0–1 | 2–3–0–1–6–7–4–5 |
| | 0 | 1 | 1 | 3–4–5–6–7–0–1–2 | 3–2–1–0–7–6–5–4 |
| | 1 | 0 | 0 | 4–5–6–7–0–1–2–3 | 4–5–6–7–0–1–2–3 |
| | 1 | 0 | 1 | 5–6–7–0–1–2–3–4 | 5–4–7–6–1–0–3–2 |
| | 1 | 1 | 0 | 6–7–0–1–2–3–4–5 | 6–7–4–5–2–3–0–1 |
| | 1 | 1 | 1 | 7–0–1–2–3–4–5–6 | 7–6–5–4–3–2–1–0 |
| FullPage | n | | | Cn, Cn+1, Cn+2 .... | not supported |

*Note:*

1. *For a burst length of two, A1-Ai selects the two-data-element block; A0 selects the first access within the block.*
2. *For a burst length of four, A2-Ai selects the four-data-element block; A0-A1 selects the first access within the block.*
3. *For a burst length of eight, A3-Ai selects the eight-data- element block; A0-A2 selects the first access withinthe block.*
4. *Whenever a boundary of the block is reached within a given sequence above, the following access wrapswithin the block.*

## 3.4 Commands

**Refresh Mode**

SDRAM has two refresh modes, Auto Refresh and Self Refresh. Auto Refresh is similar to the $\overline{CAS}$ -before-$\overline{RAS}$ refresh of conventional DRAMs. All banks must be precharged before applying any refresh mode. An on-chip address counter increments the word and the bank addresses and no bank information is required for both refresh modes.

The chip enters the Auto Refresh mode, when $\overline{RAS}$ and $\overline{CAS}$ are held low and CKE and $\overline{WE}$ are held high at aclock timing. The mode restores word line after the refresh and no external precharge command is necessary. Aminimum tRC time is required between two automatic refreshes in a burst refresh mode. The same rule applies toany access command after the automatic refresh operation.

The chip has an on-chip timer and the Self Refresh mode is available. The mode restores the word lines after $\overline{RAS}$, $\overline{CAS}$, and CKE are low and $\overline{WE}$ is high at a clock timing. All of external control signals including the clock aredisabled. Returning CKE to high enables the clock and initiates the refresh exit operation. After the exit command,at least one $t_{RC}$ delay is required prior to any access command.

### Auto Precharge

Two methods are available to precharge SDRAMs. In an automatic precharge mode, the $\overline{CAS}$ timing accepts one extra address, CA10, to determine whether the chip restores or not after the operation. If CA10 is high when a Read Command is issued, the Read with Auto-Precharge function is initiated. If CA10 is high when a Write Command is issued, the Write with Auto-Precharge function is initiated. The SDRAM automatically enters the precharge operation a time delay equal to $t_{WR}$ (“write recovery time”) after the last data in. A burst operation with Auto-Precharge may only be interrupted by a burst start to another bank. It must not be interrupted by a precharge or a burst stop command.

### Precharge Command

There is also a separate precharge command available. When $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at a clock timing, it triggers the precharge operation. Three address bits, BA0, BA1 and A10 are used to define banks as shown in the following list. The precharge command can be imposed one clock before the last data out for $\overline{CAS}$ latency = 2 and two clocks before the last data out for $\overline{CAS}$ latency = 3. Writes require a time delay twr (“write recovery time”) of 2 clocks minimum from the last data out to apply the precharge command.

**Table 9 Bank Selection by Address Bits**

| A10 | BA0 | BA1 | |
|---|---|---|---|
| 0 | 0 | 0 | Bank 0 |
| 0 | 0 | 1 | Bank 1 |
| 0 | 1 | 0 | Bank 2 |
| 0 | 1 | 1 | Bank 3 |
| 1 | 1 | X | all Banks |

### Burst Termination

Once a burst read or write operation has been initiated, there are several methods in which to terminate the burst operation prematurely. These methods include using another Read or Write Command to interrupt an existing burst operation, use a Precharge Command to interrupt a burst cycle and close the active bank, or using the Burst Stop Command to terminate the existing burst operation but leave the bank open for future Read or Write Commands to the same page of the active bank. When interrupting a burst with another Read or Write Command care must be taken to avoid DQ contention. The Burst Stop Command, however, has the fewest restrictions making it the easiest method to use when terminating a burst operation before it has been completed. If a Burst Stop command is issued during a burst write operation, then any residual data from the burst write cycle will be ignored. Data that is presented on the DQ pins before the Burst Stop Command is registered will be written to the memory.

## 3.5 Operations

### 3.5.1 Read and Write

When $\overline{RAS}$ is low and both $\overline{CAS}$ and $\overline{WE}$ are high at the positive edge of the clock, a $\overline{RAS}$ cycle starts. According to address data, a word line of the selected bank is activated and all of sense amplifiers associated to the wordline are set. A $\overline{CAS}$ cycle is triggered by setting $\overline{RAS}$ high and $\overline{CAS}$ low at a clock timing after a necessary delay, $t_{RCD}$ from the $\overline{RAS}$ timing. $\overline{WE}$ is used to define either a read ($\overline{WE}$ = H) or a write ($\overline{WE}$ = L) at this stage.

SDRAM provides a wide variety of fast access modes. In a single $\overline{CAS}$ cycle, serial data read or write operations are allowed at up to a 166 MHz data rate. The numbers of serial data bits are the burst length programmed at the mode set operation, i.e., one of 1, 2, 4 and 8 and full page. Column addresses are segmented by the burst length and serial data accesses are done within this boundary. The first column address to be accessed is supplied at the $\overline{CAS}$ timing and the subsequent addresses are generated automatically by the programmed burst length and its sequence. For example, in a burst length of 8 with interleave sequence, if the first address is ‘2’, then the rest of the burst sequence is 3, 0, 1, 6, 7, 4, and 5.

Full page burst operation is only possible using the sequential burst type and page length is a function of the I/O organization and column addressing. Full page burst operation does not self terminate once the burst length has been reached. In other words, unlike burst lengths of 2, 4 and 8, fulll page burst continues until it is terminated using another command.

Similar to the page mode of conventional DRAMs, burst read or write accesses on any column address are possible once the $\overline{RAS}$ cycle latches the sense amplifiers. The maximum $t_{RAS}$ or the refresh interval time limits the number of random column accesses. A new burst access can be done even before the previous burst ends. The interrupt operation at every clock cycle is supported. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. An interrupt which accompanies an operation change from a read to a write is possible by exploiting DQM to avoid bus contention.

When two or more banks are activated sequentially, interleaved bank read or write operations are possible. With the programmed burst length, alternate access and precharge operations on two or more banks can realize fast serial data access modes among many different pages. Once two or more banks are activated, column to column interleave operation can be performed between different pages.

### 3.5.2 DQM Function

DQM has two functions for data I/O read and write operations. During reads, when it turns to “high“ at a clock timing, data outputs are disabled and become high impedance after two clock delay (DQM Data Disable Latency $t_{DQZ}$). It also provides a data mask function for writes. When DQM is activated, the write operation at the next clock is prohibited (DQM Write Mask Latency $t_{DQW}$ = zero clocks).

### 3.5.3 Suspend Mode

During normal access mode, CKE is held high enabling the clock. When CKE is low, it freezes the internal clock and extends data read and write operations. One clock delay is required for mode entry and exit (Clock Suspend Latency $t_{CSL}$).

### 3.5.4 Power Down

In order to reduce standby power consumption, a power down mode is available. All banks must be precharged and the necessary Precharge delay ($t_{RP}$) must occur before the SDRAM can enter the Power Down mode. Once the Power Down mode is initiated by holding CKE low, all of the receiver circuits except CLK and CKE are gated off. The Power Down mode does not perform any refresh operations, therefore the device can’t remain in Power Down mode longer than the Refresh period *(*$t_{REF}$) of the device. Exit from this mode is performed by taking CKE “high“. One clock delay is required for Power Down mode entry and exit.

# 4 Electrical Characteristics

## 4.1 Operating Conditions

**Table 10 Absolute Maximum Ratings**

| Parameter | Symbol | Limit Values | | Unit | Note/ Test Condition |
|---|---|---|---|---|---|
| | | min. | max. | | |
| Input / Output voltage relative to $V_{SS}$ | $V_{IN,}$ $V_{OUT}$ | – 1.0 | +4.6 | V | – |
| Voltage on $V_{DD}$ supply relative to $V_{SS}$ | $V_{DD}$ | – 1.0 | +4.6 | V | – |
| Voltage on $V_{DDQ}$ supply relative to $V_{SS}$ | $V_{DDQ}$ | – 1.0 | +4.6 | V | – |
| Operating Temperature | $T_A$ | 0 | +70 | °C | – |
| Storage temperature range | $T_{STG}$ | -55 | +150 | °C | – |
| Power dissipation per SDRAM component | $P_D$ | – | 1 | W | – |
| Data out current (short circuit) | $I_{OUT}$ | – | 50 | mA | – |

***Attention: Permanent device damage may occur if "Absolute Maximum Ratings" are exceeded.Functional operation should be restricted to recommended operation conditions. Exposure to higher than recommended voltage for extended periods of time affect device reliability***

**Table 11 DC Characteristics[1)]**

| Parameter | Symbol | Values | | Unit | Note/ Test Condition |
|---|---|---|---|---|---|
| | | min. | max. | | |
| Supply Voltage | $V_{DD}$ | 3.0 | 3.6 | V | 2) |
| I/O Supply Voltage | $V_{DDQ}$ | 3.0 | 3.6 | V | 2) |
| Input high voltage | $V_{IH}$ | 2.0 | $V_{DDQ}$+0.3 | V | 2)3) |
| Input low voltage | $V_{IL}$ | – 0.3 | +0.8 | V | 2)3) |
| Output high voltage ($I_{OUT}$ = – 4.0 mA) | $V_{OH}$ | 2.4 | – | V | 2) |
| Output low voltage ($I_{OUT}$ = 4.0 mA) | $V_{OL}$ | – | 0.4 | V | 2) |
| Input leakage current, any input (0 V < $V_{IN}$ < $V_{DD}$, all other inputs = 0 V) | $I_{IL}$ | – 5 | +5 | mA | – |
| Output leakage current (DQs are disabled, 0 V < $V_{OUT}$ < $V_{DDQ}$) | $I_{OL}$ | – 5 | +5 | mA | – |

1) $T_A$ = 0 to 70 °C

2) All voltages are referenced to $V_{SS}$

3) $V_{IH}$ may overshoot to $V_{DDQ}$ + 2.0 V for pulse width of < 4ns with 3.3V. $V_{IL}$ may undershoot to -2.0 V for pulse width < 4.0 ns with 3.3V. Pulse width measured at 50% points with amplitude measured peak to DC reference.

**Table 12 Input and Output Capacitances[1)]**

| Parameter | Symbol | Values[2)] | | Unit |
|---|---|---|---|---|
| | | min. | max. | |
| Input Capacitances: CK, $\overline{CK}$ | $C_{I1}$ | 2.5 | 3.5 | pF |
| Input Capacitance (A0-A12, BA0, BA1, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, DQM) | $C_{I2}$ | 2.5 | 3.8 | pF |
| Input/Output Capacitance (DQ) | $C_{I0}$ | 4.0 | 6.0 | pF |

1) TA = 0 to 70 °C; VDD,VDDQ = 3.3 V ± 0.3 V, f = 1 MHz

2) Capacitance values are shown for TSOP-54 packages. Capacitance values for TFBGA packages are lower by 0.5 pF

**Table 13 $I_{DD}$ Conditions**

| Parameter | Symbol |
|---|---|
| **Operating Current** One bank active, Burst length = 1 | $I_{DD1}$ |
| **Precharge Standby Current in Power Down Mode** | $I_{DD2P}$ |
| **Precharge Standby Current in Non-Power Down Mode** | $I_{DD2N}$ |
| **No Operating Current** active state ( max. 4 banks) | $I_{DD3N}$ |
| | $I_{DD3P}$ |
| **Burst Operating Current** Read command cycling | $I_{DD4}$ |
| **Auto Refresh Current** Auto Refresh command cycling | $I_{DD5}$ |
| **Self Refresh Current (standard components)** Self Refresh Mode, CKE=0.2V, $t_{CK}$=infinity | $I_{DD6}$ |
| **Self Refresh Current (low power components)** Self Refresh Mode, CKE=0.2V, $t_{CK}$=infinity | |

**Table 14 $I_{DD}$ Specifications and Conditions[1)]**

| Symbol | | | -6 | -7 | -7.5 | -8 | Unit | Note/ Test Condition |
|---|---|---|---|---|---|---|---|---|
| | | | max. | | | | | |
| $I_{DD1}$ | $t_{RC} = t_{RC(min)}$, $I_O$ = 0 mA | | 100 | 80 | 80 | 80 | mA | 2)3) |
| $I_{DD2P}$ | $\overline{CS}$ =$V_{IH\ (min.)}$, CKE ≤$V_{IL(max)}$ | | 2 | 2 | 2 | 2 | mA | 2) |
| $I_{DD2N}$ | $\overline{CS}$ =$V_{IH\ (min.)}$, CKE≥ $V_{IH(min)}$ | | 35 | 30 | 30 | 25 | mA | 2) |
| $I_{DD3N}$ | $\overline{CS}$ = $V_{IH(min)}$, CKE ≥$V_{IH(min.)}$ | | 40 | 35 | 35 | 30 | mA | 2) |
| $I_{DD3P}$ | $\overline{CS}$ = $V_{IH(min)}$, CKE ≤ $V_{IL(max.)}$ | | 5 | 5 | 5 | 5 | mA | 2) |
| $I_{DD4}$ | | | 110 | 90 | 90 | 70 | mA | 2)3) |
| $I_{DD5}$ | $t_{RFC}$= $t_{RFC(min)}$ | | 220 | 190 | 190 | 160 | mA | 4) |
| | $t_{RFC}$= 7.8 µs | | 3 | 3 | 3 | 3 | mA | |
| $I_{DD6}$ | x4, x8, x16 | standard components | 3<br>1.5 | 3<br>1.5 | 3<br>1.5 | 3<br>1.5 | mA<br>mA | |
| | | low power components | 0.85 | 0.85 | 0.85 | 0.85 | mA | |

1) $T_A$ = 0 to 70 °C; $V_{SS}$ = 0 V; $V_{DD}$, $V_{DDQ}$ = 3.3 V ± 0.3 V

2) These parameters depend on the cycle rate. All values are measured at 166 MHz for -6, at 133 MHz for -7 and -7.5 and at 100 MHz for -8 components with the outputs open. Input signals are changed once during $t_{CK}$.

3) These parameters are measured with continuous data stream during read access and all DQ toggling. CL=3 and BL=4 is assumed and the $V_{DDQ}$ current is excluded.

4) $t_{RFC}$= $t_{RFC(min)}$ “burst refresh”, $t_{RFC}$= 7.8 µs “distributed refresh”.

## 4.2 AC Characteristics

**Table 15 AC Timing - Absolute Specifications –8/-7.5/–7/-6 [1)2)3)]**

| Parameter | Symbol | –8 | | –7.5 | | –7 | | –6 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | PC100 - 222 | | PC166 - 333 | | PC166 - 222 | | PC166 - 333 | | | |
| | | min. | max. | min. | max. | min. | max. | min. | max. | | |
| **Clock and Clock Enable** | | | | | | | | | | | |
| Clock Cycle Time<br>CAS Latency = 3<br>CAS Latency = 2 | $t_{CK}$ | 8<br>10 | —<br>— | 7.5<br>10 | —<br>— | 7<br>7.5 | —<br>— | 6<br>7.5 | —<br>— | ns<br>ns | |
| Clock Frequency<br>CAS Latency = 3<br>CAS Latency = 2 | $t_{CK}$ | —<br>— | 125<br>100 | —<br>— | 133<br>100 | —<br>— | 143<br>100 | —<br>— | 166<br>133 | MHz<br>MHz | |
| Access Time from Clock<br>CAS Latency = 3<br>CAS Latency = 2 | $t_{AC}$ | —<br>— | 6<br>6 | —<br>— | 5.4<br>6 | —<br>— | 5.4<br>5.4 | —<br>— | 5<br>5.4 | ns<br>ns | 3)4)5) |
| Clock High Pulse Width | $t_{CH}$ | 3 | — | 2.5 | — | 2.5 | — | 2 | — | ns | |
| Clock Low Pulse Width | $t_{CL}$ | 3 | — | 2.5 | — | 2.5 | — | 2 | — | ns | |
| Transition time | $t_{T}$ | 0.5 | 10 | 0.3 | 1.2 | 0.3 | 1.2 | 0.3 | 1.2 | ns | |
| **Setup and Hold Times** | | | | | | | | | | | |
| Input Setup Time | $t_{IS}$ | 2 | — | 1.5 | — | 1.5 | — | 1.5 | — | ns | 6) |
| Input Hold Time | $t_{IH}$ | 1 | — | 0.8 | — | 0.8 | — | 0.8 | — | ns | 6) |
| CKE Setup Time | $t_{CK}$ | 2 | — | 1.5 | — | 1.5 | — | 1.5 | — | ns | 6) |
| CKE Hold Time | $t_{CKH}$ | 1 | — | 0.8 | — | 0.8 | — | 0.8 | — | ns | 6) |
| Mode Register Set-up to Active delay | $t_{RSC}$ | 2 | — | 2 | — | 2 | — | 2 | — | CLK | |
| Power Down Mode Entry Time | $t_{SB}$ | 0 | 8 | 0 | 7.5 | 0 | 7 | 0 | 6 | ns | |
| **Common Parameters** | | | | | | | | | | | |
| Row to Column Delay Time | $t_{RCD}$ | 20 | — | 20 | — | 15 | — | 15 | — | ns | 7) |
| Row Precharge Time | $t_{RP}$ | 20 | — | 20 | — | 15 | — | 15 | — | ns | 7) |
| Row Active Time | $t_{RAS}$ | 48 | 100k | 45 | 100k | 37 | 100k | 36 | 100k | ns | 7) |
| Row Cycle Time | $t_{RC}$ | 70 | — | 67 | — | 60 | — | 60 | — | ns | 7) |
| Row Cycle Time during Auto Refresh | $t_{RFC}$ | 70 | — | 67 | — | 63 | — | 60 | — | ns | |
| Activate(a) to Activate(b) Command period | $t_{RRD}$ | 16 | — | 15 | — | 14 | — | 12 | — | ns | 7) |
| CAS(a) to CAS(b) Command period | $t_{CCD}$ | 1 | — | 1 | — | 1 | — | 1 | — | CLK | |
| **Refresh Cycle** | | | | | | | | | | | |

**Table 15 AC Timing - Absolute Specifications –8/-7.5/–7/-6** (cont'd)[1)2)3)]

| Parameter | Symbol | –8 | | –7.5 | | –7 | | –6 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | PC100 - 222 | | PC166 - 333 | | PC166 - 222 | | PC166 - 333 | | | |
| | | min. | max. | min. | max. | min. | max. | min. | max. | | |
| **Refresh Cycle** | | | | | | | | | | | |
| Refresh Period (8192 cycles) | $t_{REF}$ | – | 64 | – | 64 | – | 64 | – | 64 | ms | |
| Self Refresh Exit Time | $t_{SREX}$ | 1 | — | 1 | — | 1 | — | 1 | — | CLK | |
| Data Out Hold Time | $t_{OH}$ | 3 | — | 3 | — | 3 | — | 2.5 | — | ns | 3)5) |
| **Read Cycle** | | | | | | | | | | | |
| Data Out to Low Impedance Time | $t_{LZ}$ | 0 | — | 0 | — | 0 | — | 0 | — | ns | |
| Data Out to High Impedance Time | $t_{HZ}$ | 3 | 8 | 3 | 7 | 3 | 7 | 3 | 6 | ns | |
| DQM Data Out Disable Latency | $t_{DQZ}$ | — | 2 | — | 2 | — | 2 | — | 2 | CLK | |
| **Write Cycle** | | | | | | | | | | | |
| Last Data Input to Precharge (Write without AutoPrecharge) | $t_{WR}$ | 15 | — | 15 | — | 14 | — | 12 | — | ns | 8) |
| Last Data Input to Activate (Write with AutoPrecharge) | $t_{DAL(min.)}$ | $(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})$ | | | | | | | | CLK | 9) |
| DQM Write Mask Latency | $t_{DQW}$ | 0 | — | 0 | — | 0 | — | 0 | — | CLK | |

1) $T_A$ = 0 to 70 °C; $V_{SS}$ = 0 V; $V_{DD}$, $V_{DDQ}$ = 3.3 V ± 0.3 V, $t_T$ = 1 ns

2) For proper power-up see the operation section of this data sheet.

3) AC timing tests for LV-TTL versions have $V_{IL}$ = 0.4 V and $V_{IH}$ = 2.4 V with the timing referenced to the 1.4 V crossover point. The transition time is measured between $V_{IH}$ and $V_{IL}$. All AC measurements assume $t_T$ = 1 ns with the AC output load circuit shown in figure below. Specified $t_{AC}$ and $t_{OH}$ parameters are measured with a 50 pF only, without any resistive termination and with an input signal of 1V / ns edge rate between 0.8 V and 2.0 V.

4) If clock rising time is longer than 1 ns, a time ($t_T$/2 - 0.5) ns has to be added to this parameter.

5) Access time from clock $t_{AC}$ is 4.6 ns for PC133 components with no termination and 0 pF load,
Data out hold time $t_{OH}$ is 1.8 ns for PC133 components with no termination and 0 pF load.

6) If $t_T$ is longer than 1 ns, a time ($t_T$ - 1) ns has to be added to this parameter.

7) These parameter account for the number of clock cycles and depend on the operating frequency of the clock, as follows: the number of clock cycles = specified value of timing period (counted in fractions as a whole number)

8) It is recommended to use two clock cycles between the last data-in and the precharge command in case of a write command without Auto-Precharge. One clock cycle between the last data-in and the precharge command is also supported, but restricted to cycle times tck greater or equal the specified twr value, where tck is equal to the actual system clock time.

9) When a Write command with AutoPrecharge has been issued, a time of $t_{DAL(min)}$ has be fullfilled before the next Activate Command can be applied. For each of the terms, if not already an integer, round up to the next highest integer. $t_{CK}$ is equal to the actual system clock time.

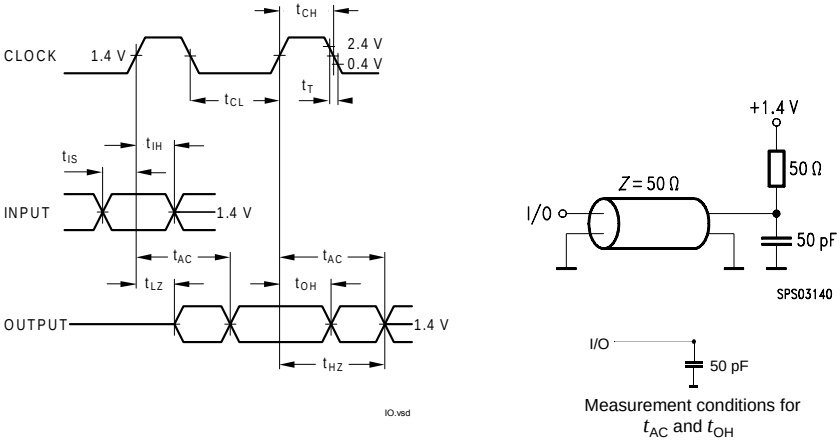
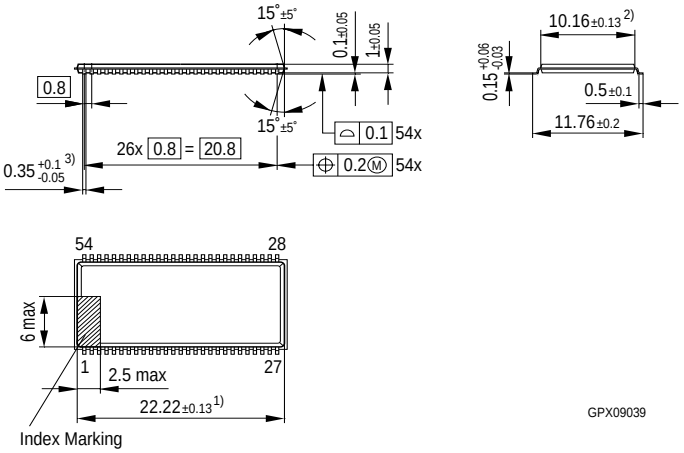



**Figure 5 Measurement conditions for $t_{AC}$ and $t_{OH}$**

# 5 Package Outlines

**Plastic Package P-TSOPII-54**
(400 mil, 0.8 mm lead pitch)
Thin Small Outline Package, SMD




1) Does not include plastic or metal protrusion of 0.15 max per side
2) Does not include plastic protrusion of 0.25 max per side
3) Does not include dambar protrusion of 0.13 max per side

**Figure 6 Package Outline P–TSOPII–54**

**TFBGA-54 package**
(12 mm x 8 mm, 54 balls)

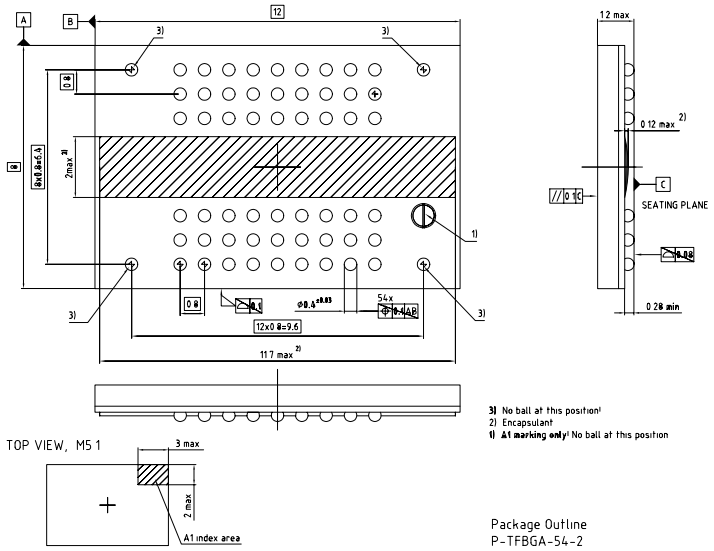



**Figure 7 Package Outline TFBGA-54**

http://www.infineon.com

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