

# SIEMENS

## 4M x 16-Bit Dynamic RAM (4k & 8k Refresh, EDO-version)

HYB 3164165T(L) -50/-60

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### Preliminary Information

- 4 194 304 words by 16-bit organization
- 0 to 70 °C operating temperature
- Fast access and cycle time
  - RAS access time:
    - 50 ns (-50 version)
    - 60 ns (-60 version)
  - Cycle time:
    - 84 ns (-50 version)
    - 104 ns (-60 version)
  - CAS access time:
    - 13 ns (-50 version)
    - 15 ns (-60 version)
- Hyper page mode (EDO) cycle time
  - 20 ns (-50 version)
  - 25 ns (-60 version)
- Single + 3.3 V ( $\pm 0.3V$ ) power supply
- Low power dissipation
  - max. 396 active mW ( HYB 3164165T(L)-50)
  - max. 360 active mW ( HYB 3164165T(L)-60)
  - max. 504 active mW ( HYB 3165165T(L)-50)
  - max. 432 active mW ( HYB 3165165T(L)-60)
  - 7.2 mW standby (TTL)
  - 720 W standby (MOS)
  - 14.4 mW Self Refresh (L-version only)
- Read, write, read-modify-write,  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh (CBR),  $\overline{\text{RAS}}$ -only refresh, hidden refresh and self refresh modes
- Hyper page mode (EDO) capability
- 2 CAS / 1 WE byte control
- 8192 refresh cycles/128 ms , 13 R/ 9C addresses (HYB 3164165T(L))
- 4096 refresh cycles/ 64 ms , 12 R/ 10C addresses (HYB 3165165T(L))
- Plastic Package:
  - P-TSOPII-54-1 500 mil HYB 3164(5)165T(L)

This HYB3164(5)165 is a 64 MBit dynamic RAM organized 4 194 304 x 16 bits. The device is fabricated in SIEMENS/IBM most advanced first generation 64Mbit CMOS silicon gate process technology. The circuit and process design allow this device to achieve high performance and low power dissipation. The HYB3164(5)165 operates with a single 3.3 +/-0.3V power supply and interfaces with either LVTTTL or LVCMOS levels. Multiplexed address inputs permit the HYB3164(5)165 to be packaged in a 500mil wide TSOPII-54 plastic package. These packages provide high system bit densities and are compatible with commonly used automatic testing and insertion equipment. The HYB3164(5)165TL parts have a very low power „sleep mode“ supported by Self Refresh.

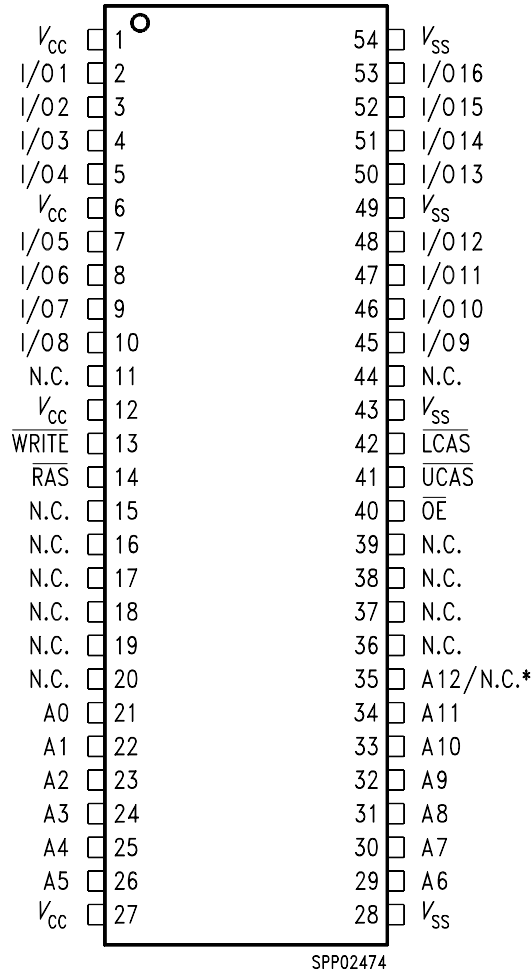
### Ordering Information

Type	Ordering Code	Package	Descriptions
HYB 3164165T-50	on request	P-TSOPII-54-1 500 mil	EDO-DRAM (access time 50 ns)
HYB 3164165T-60	on request	P-TSOPII-54-1 500 mil	EDO-DRAM (access time 60 ns)
HYB 3164165TL-50	on request	P-TSOPII-54-1 500 mil	EDO-DRAM (access time 50 ns)
HYB 3164165TL-60	on request	P-TSOPII-54-1 500 mil	EDO-DRAM (access time 60 ns)
HYB 3165165T-50	on request	P-TSOPII-54-1 500 mil	EDO-DRAM (access time 50 ns)
HYB 3165165T-60	on request	P-TSOPII-54-1 500 mil	EDO-DRAM (access time 60 ns)
HYB 3165165TL-50	on request	P-TSOPII-54-1 500 mil	EDO-DRAM (access time 50 ns)
HYB 3165165TL-60	on request	P-TSOPII-54-1 500 mil	EDO-DRAM (access time 60 ns)

### Pin Names

A0-A12	Address Inputs for HYB 3164165T(L)
A0-A11	Address Inputs for HYB 3165165T(L)
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{OE}}$	Output Enable
I/O1-I/O16	Data Input/Output
$\overline{\text{UCAS}}, \overline{\text{LCAS}}$	Column Address Strobe
$\overline{\text{WRITE}}$	Read/Write Input
Vcc	Power Supply ( + 3.3V)
Vss	Ground

P-TSOPII-54-1 (500 mil)

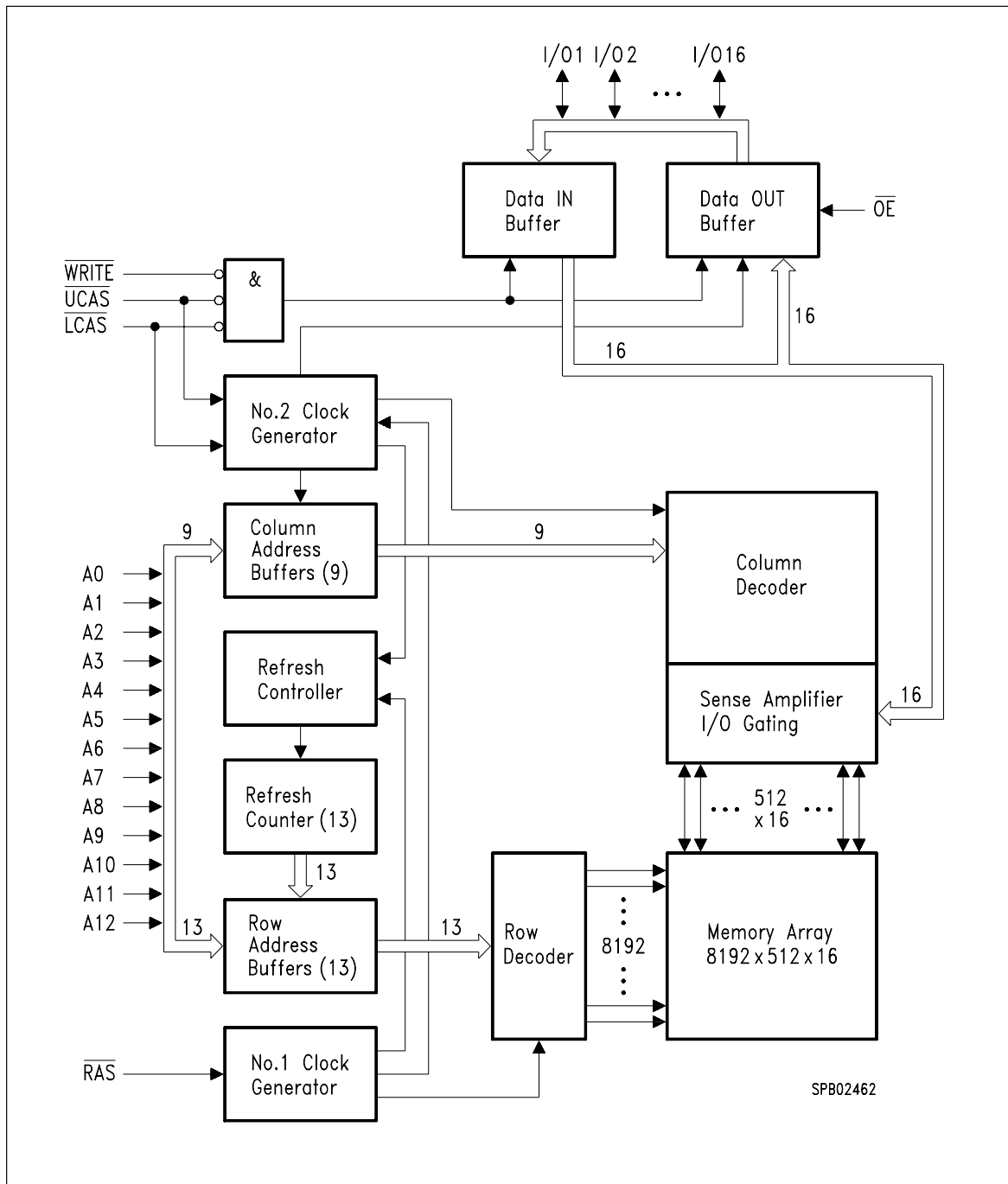


\* Pin 35 is A12 for HYB 3164165T(L) and N.C. for HYB 3165165T(L)

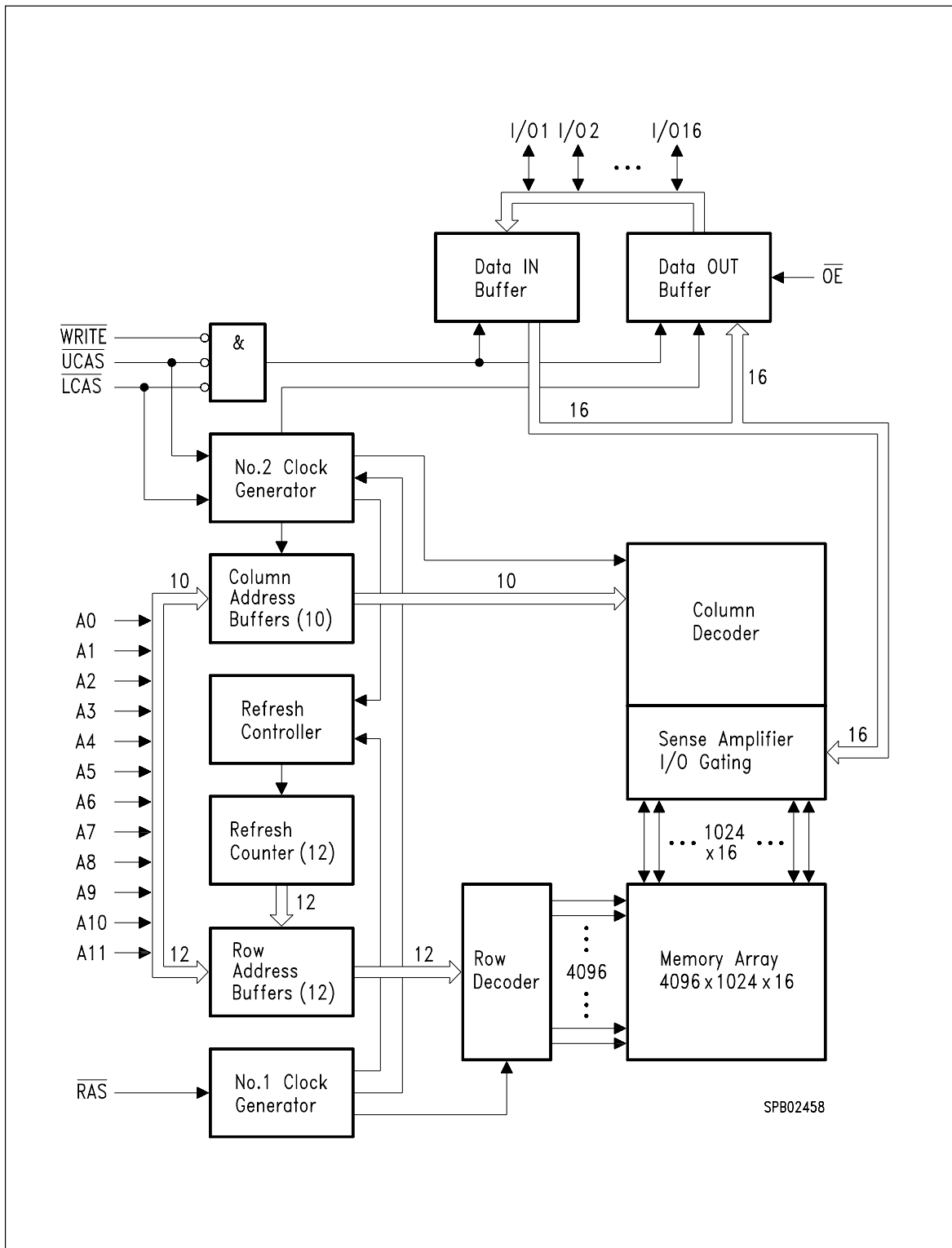
Pin Configuration

### TRUTH TABLE

FUNCTION		RAS	LCAS	UCAS	WRITE	OE	ROW ADD	COL ADD	I/O1-I/O16
Standby		H	H - X	H - X	X	X	X	X	High Impedance
Read:Word		L	L	H	H	L	ROW	COL	Data Out
Read:Lower Byte		L	L	H	H	L	ROW	COL	Lower Byte:Data Out Upper-Byte:High-Z
Read:Upper Byte		L	H	L	H	L	ROW	COL	Lower Byte:High-Z Upper Byte:Data Out
Write:Word (Early-Write)		L	L	L	L	X	ROW	COL	Data In
Write:Lower Byte (Early-Write)		L	L	H	L	X	ROW	COL	Lower Byte:Data Out Upper-Byte:High-Z
Write:Upper Byte (Early Write)		L	H	L	L	X	ROW	COL	Lower Byte:High-Z Upper Byte:Data Out
Read-Modify-Write		L	L	L	H - L	L - H	ROW	COL	Data Out, Data In
Hyper Page Mode Read (Word)	1st Cycle	L	H - L	H - L	H	L	ROW	COL	Data Out
Hyper Page Mode Read (Word)	2nd Cycle	L	H - L	H - L	H	L	n/a	COL	Data Out
Hyper Page Mode Early Write(Word)	1st Cycle	L	H - L	H - L	L	X	ROW	COL	Data In
Hyper Page Mode Early Write(Word)	2nd Cycle	L	H - L	H - L	L	X	n/a	COL	Data In
Hyper Page Mode RMW	1st Cycle	L	H - L	H - L	H - L	L - H	ROW	COL	Data Out, Data In
Hyper Page Mode RMW	2st Cycle	L	H - L	H - L	H - L	L - H	n/a	COL	Data Out, Data In
RAS only refresh		L	H	H	X	X	ROW	n/a	High Impedance
CAS-before-RAS refresh		H - L	L	L	H	X	X	n/a	High Impedance
Test Mode Entry		H - L	L	L	L	X	X	n/a	High Impedance
Hidden Refresh (Read)		L-H-L	L	L	H	L	ROW	COL	Data Out
Hidden Refresh (Write)		L-H-L	L	L	L	X	ROW	COL	Data In
Self Refresh (L-version only)		H-L	L	H	X	X	X	X	High Impedance



Block Diagram for HYB 3164165T(L)



Block Diagram for HYB 3165165T(L)

### Absolute Maximum Ratings

Operating temperature range.....	0 to 70 °C
Storage temperature range.....	- 55 to 150 °C
Input/output voltage.....	-0.5 to min (V <sub>CC</sub> +0.5,4.6) V
Power supply voltage.....	-0.5V to 4.6 V
Power dissipation.....	1.0 W
Data out current (short circuit).....	50 mA

### Note

Stresses above those listed under „Absolute Maximum Ratings“ may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

### DC Characteristics

T<sub>A</sub> = 0 to 70 °C, V<sub>SS</sub> = 0 V, V<sub>CC</sub> = 3.3 V ± 0.3 V, (values in brackets for HYB 3165165J/T)

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Input high voltage	V <sub>IH</sub>	2.0	V <sub>CC</sub> +0.3	V	1)
Input low voltage	V <sub>IL</sub>	- 0.3	0.8	V	1)
Output high voltage (LVTTTL) Output „H“ level voltage (I <sub>out</sub> = -2mA)	V <sub>OH</sub>	2.4	-	V	
Output low voltage (LVTTTL) Output „L“ level voltage (I <sub>out</sub> = +2mA)	V <sub>OL</sub>	-	0.4	V	
Output high voltage (LVCMOS) Output „H“ level voltage (I <sub>out</sub> = -100uA)	V <sub>OH</sub>	V <sub>CC</sub> -0.2	-	V	
Output low voltage (LVCMOS) Output „L“ level voltage (I <sub>out</sub> = +100uA)	V <sub>OL</sub>	-	0.2	V	
Input leakage current,any input (0 V < V <sub>in</sub> < V <sub>CC</sub> , all other pins = 0 V)	I <sub>I(L)</sub>	- 2	2	μA	
Output leakage current (DO is disabled, 0 V < V <sub>out</sub> < V <sub>CC</sub> )	I <sub>O(L)</sub>	- 2	2	μA	
Average V <sub>CC</sub> supply current:  -50 ns version -60 ns version  ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , address cycling: t <sub>RC</sub> = t <sub>RC</sub> min.)	I <sub>CC1</sub>	-	110 (140) 100 (120)	mA mA	2) 3) 4)
Standby V <sub>CC</sub> supply current ( $\overline{\text{RAS}}=\overline{\text{CAS}}=V_{ih}$ )	I <sub>CC2</sub>	-	2	mA	-

### DC Characteristics (cont'd)

$T_A = 0$  to  $70$  °C,  $V_{SS} = 0$  V,  $V_{CC} = 3.3$  V  $\pm$  0.3 V, (values in brackets for HYB 3165165J/T)

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Average Vcc supply current, during RAS-only refresh cycles: -50 ns version -60 ns version  (RAS cycling: CAS = VIH: tRC = tRC min.)	$I_{CC3}$	–	110 (140) 100 (120)	mA mA	2) 4)
Average Vcc supply current, Hyper page mode (EDO): -50 ns version -60 ns version  ( $\overline{RAS} = V_{IL}$ , $\overline{CAS}$ , address cycling: tHPC=tHPC min.)	$I_{CC4}$	–	115 (150) 100 (120)	mA mA	2) 3) 4)
Standby Vcc supply current ( $\overline{RAS}=\overline{CAS}= V_{CC}-0.2V$ )	$I_{CC5}$	–	200	A	–
Average Vcc supply current, during $\overline{CAS}$ -before-RAS refresh mode: -50 ns version -60 ns version  ( $\overline{RAS}$ , $\overline{CAS}$ cycling: tRC = tRC min.)	$I_{CC6}$	–	110 (140) 100 (120)	mA mA	2) 4)
Self Refresh Current (L-version only) Average Power Supply Current during Self Refresh. (CBR cycle with tRAS>TRASSmin, $\overline{CAS}$ held low, WE = Vcc-0.2V, Address and Din=Vcc-0.2V or 0.2V)	$I_{CC7}$	–	400	A	

### Capacitance

$T_A = 0$  to  $70$  °C,  $V_{CC} = 3.3$  V  $\pm$  0.3 V,  $f = 1$  MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A11,A12)	$C_{I1}$	–	5	pF
Input capacitance ( $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WRITE}$ , $\overline{OE}$ )	$C_{I2}$	–	7	pF
I/O capacitance (I/O1-I/O16)	$C_{I0}$	–	7	pF



### AC Characteristics <sup>5)6)</sup>

$T_A = 0$  to  $70$  °C,  $V_{CC} = 3.3$  V  $\pm$  0.3V,  $t_T = 2$  ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		

#### *common parameters*

Random read or write cycle time	$t_{RC}$	84	–	104	–	ns	
RAS precharge time	$t_{RP}$	30	–	40	–	ns	
RAS pulse width	$t_{RAS}$	50	100k	60	100k	ns	
CAS pulse width	$t_{CAS}$	8	10k	10	10k	ns	
Row address setup time	$t_{ASR}$	0	–	0	–	ns	
Row address hold time	$t_{RAH}$	8	–	10	–	ns	
Column address setup time	$t_{ASC}$	0	–	0	–	ns	
Column address hold time	$t_{CAH}$	8	–	10	–	ns	
RAS to CAS delay time	$t_{RCD}$	12	37	14	45	ns	
RAS to column address delay time	$t_{RAD}$	10	25	12	30	ns	
RAS hold time	$t_{RSH}$	8		10	–	ns	
CAS hold time	$t_{CSH}$	45		50	–	ns	
CAS to RAS precharge time	$t_{CRP}$	5	–	5	–	ns	
Transition time (rise and fall)	$t_T$	1	50	1	50	ns	7
Refresh period for HYB3164165	$t_{REF}$	–	128	–	128	ms	
Refresh period for HYB3165165	$t_{REF}$	–	64	–	64	ms	

#### *Read Cycle*

Access time from RAS	$t_{RAC}$	–	50	–	60	ns	8, 9
Access time from CAS	$t_{CAC}$	–	13	–	15	ns	8, 9
Access time from column address	$t_{AA}$	–	25	–	30	ns	8,10
OE access time	$t_{OEA}$	–	13	–	15	ns	
Column address to RAS lead time	$t_{RAL}$	25	–	30	–	ns	
Read command setup time	$t_{RCS}$	0	–	0	–	ns	
Read command hold time	$t_{RCH}$	0	–	0	–	ns	11
Read command hold time referenced to RAS	$t_{RRH}$	0	–	0	–	ns	11
CAS to output in low-Z	$t_{CLZ}$	0	–	0	–	ns	8

### AC Characteristics (cont'd) <sup>5)6)</sup>

$T_A = 0$  to  $70$  °C,  $V_{CC} = 3.3$  V  $\pm$  0.3V,  $t_T = 2$  ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		
Output buffer turn-off delay	$t_{OFF}$	0	13	0	15	ns	12
Output buffer turn-off delay from $\overline{OE}$	$t_{OEZ}$	0	13	0	15	ns	12
Data to $\overline{CAS}$ low delay	$t_{DZC}$	0	–	0	–	ns	13
Data to $\overline{OE}$ low delay	$t_{DZO}$	0	–	0	–	ns	13
$\overline{CAS}$ high to data delay	$t_{CDD}$	13	–	15	–	ns	14
$\overline{OE}$ high to data delay	$t_{ODD}$	13	–	15	–	ns	14

### Write Cycle

Write command hold time	$t_{WCH}$	8	–	10	–	ns	
Write command pulse width	$t_{WP}$	7	–	10	–	ns	
Write command setup time	$t_{WCS}$	0	–	0	–	ns	15
Write command to $\overline{RAS}$ lead time	$t_{RWL}$	8	–	10	–	ns	
Write command to $\overline{CAS}$ lead time	$t_{CWL}$	8	–	10	–	ns	
Data setup time	$t_{DS}$	0	–	0	–	ns	16
Data hold time	$t_{DH}$	7	–	10	–	ns	16

### Read-modify-Write Cycle

Read-write cycle time	$t_{RWC}$	111	–	135	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	$t_{RWD}$	67	–	79	–	ns	15
$\overline{CAS}$ to $\overline{WE}$ delay time	$t_{CWD}$	30	–	34	–	ns	15
Column address to $\overline{WE}$ delay time	$t_{AWD}$	42	–	49	–	ns	15
$\overline{OE}$ command hold time	$t_{OEH}$	7	–	10	–	ns	

### Hyper Page Mode (EDO) Cycle

Hyper page mode (EDO) cycle time	$t_{HPC}$	20	–	25	–	ns	
$\overline{CAS}$ precharge time	$t_{CP}$	8	–	10	–	ns	
Access time from $\overline{CAS}$ precharge	$t_{CPA}$	–	27	–	35	ns	7
Output data hold time	$t_{COH}$	5	–	5	–	ns	
$\overline{RAS}$ pulse width in hyper page mode	$t_{RAS}$	50	200k	60	200k	ns	
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	$t_{RHCP}$	27	–	35	–	ns	

### AC Characteristics (cont'd) <sup>5)6)</sup>

$T_A = 0$  to  $70$  °C,  $V_{CC} = 3.3$  V  $\pm$  0.3V,  $t_T = 2$  ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		
$\overline{OE}$ pulse width	$t_{OEP}$	7	–	10	–	ns	
$\overline{OE}$ hold time from $\overline{CAS}$ high	$t_{OEHC}$	7	–	10	–	ns	
$\overline{WE}$ pulse width to output disable at $\overline{CAS}$ high	$t_{WPZ}$	7	–	10	–	ns	
Output buffer turn-off delay from $\overline{WE}$	$t_{WPZ}$	0	10	0	10	ns	

### Hyper Page Mode (EDO) Read-modify-Write Cycle

Hyper page mode (EDO) read-write cycle time	$t_{PRWC}$	51	–	66	–	ns	
$\overline{CAS}$ precharge to $\overline{WE}$	$t_{CPWD}$	41	–	49	–	ns	

### $\overline{CAS}$ before $\overline{RAS}$ refresh cycle

$\overline{CAS}$ setup time	$t_{CSR}$	5	–	5	–	ns	
$\overline{CAS}$ hold time	$t_{CHR}$	8	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	$t_{RPC}$	5	–	5	–	ns	
Write to $\overline{RAS}$ precharge time	$t_{WRP}$	8	–	10	–	ns	
Write hold time referenced to $\overline{RAS}$	$t_{WRH}$	8	–	10	–	ns	

### CAS-before-RAS counter test cycle

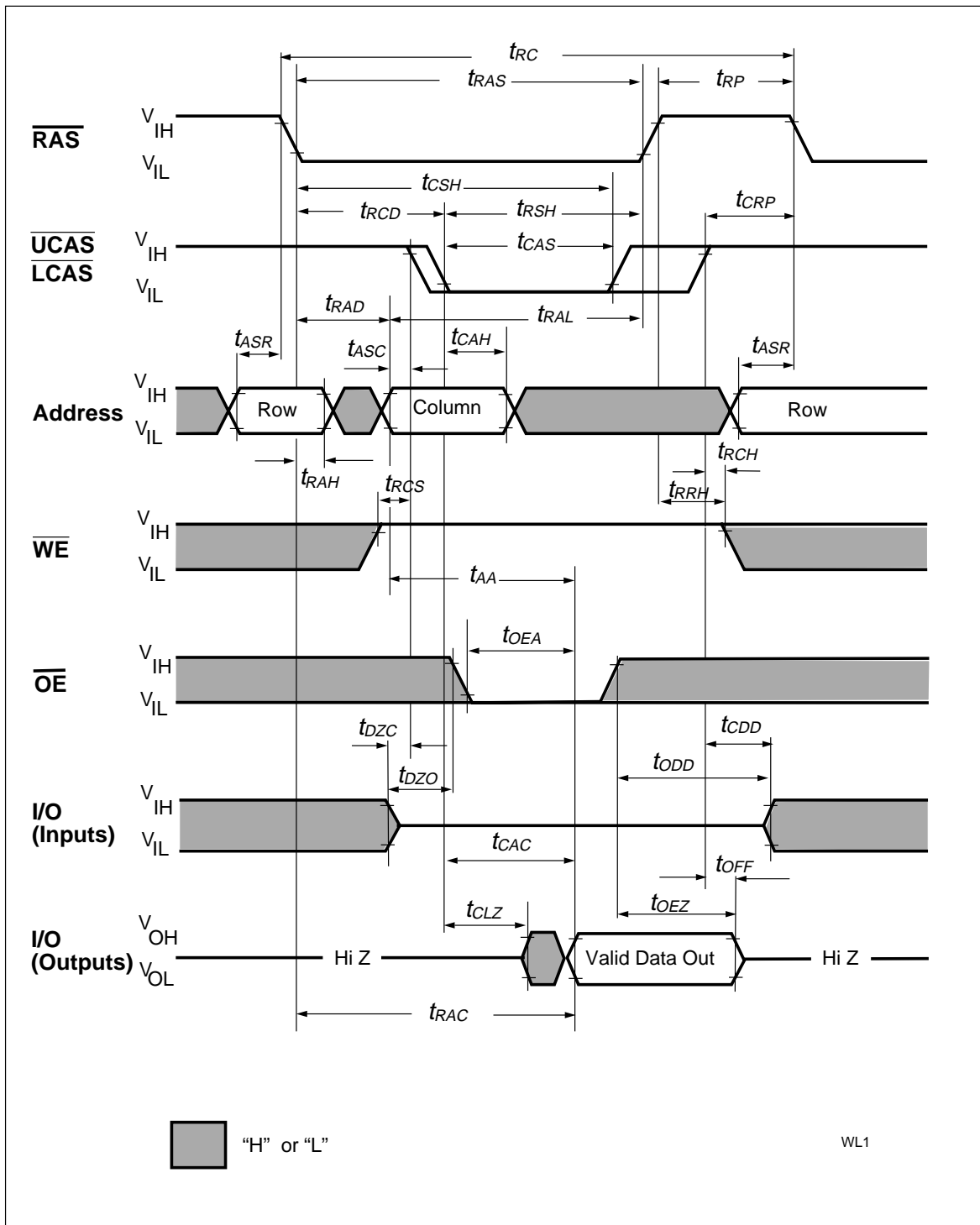
$\overline{CAS}$ precharge time (CAS-before-RAS counter test cycle)	$t_{CPT}$	35	–	40	–	ns	
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### Self Refresh Cycle

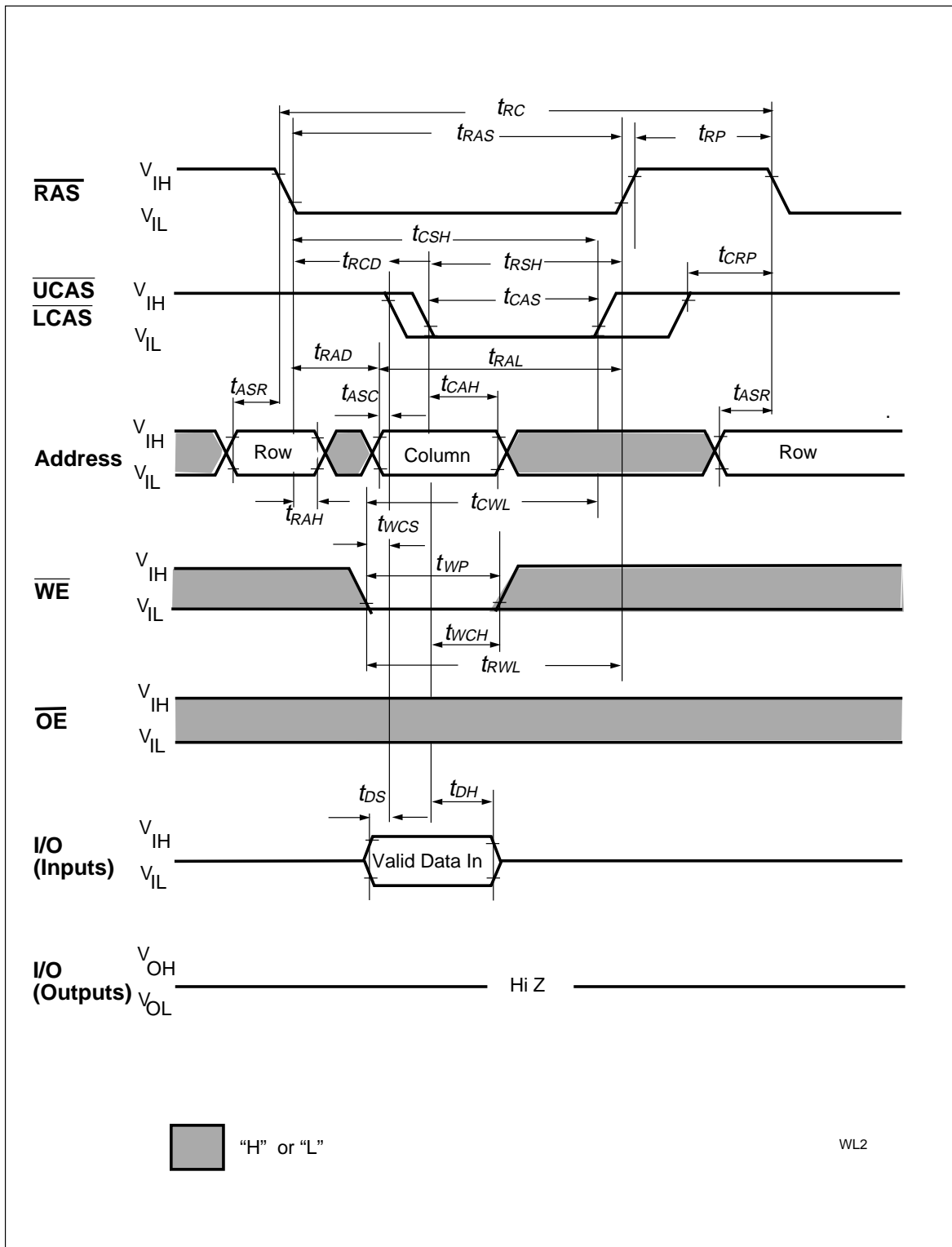
$\overline{RAS}$ pulse width during self refresh	$t_{RASS}$	100k	–	100k	–	ns	17
$\overline{RAS}$ precharge time during self refresh	$t_{RPS}$	84	–	104	–	ns	17
$\overline{CAS}$ hold time during self refresh	$t_{CHS}$	-50	–	-50	–	ns	17

**Notes:**

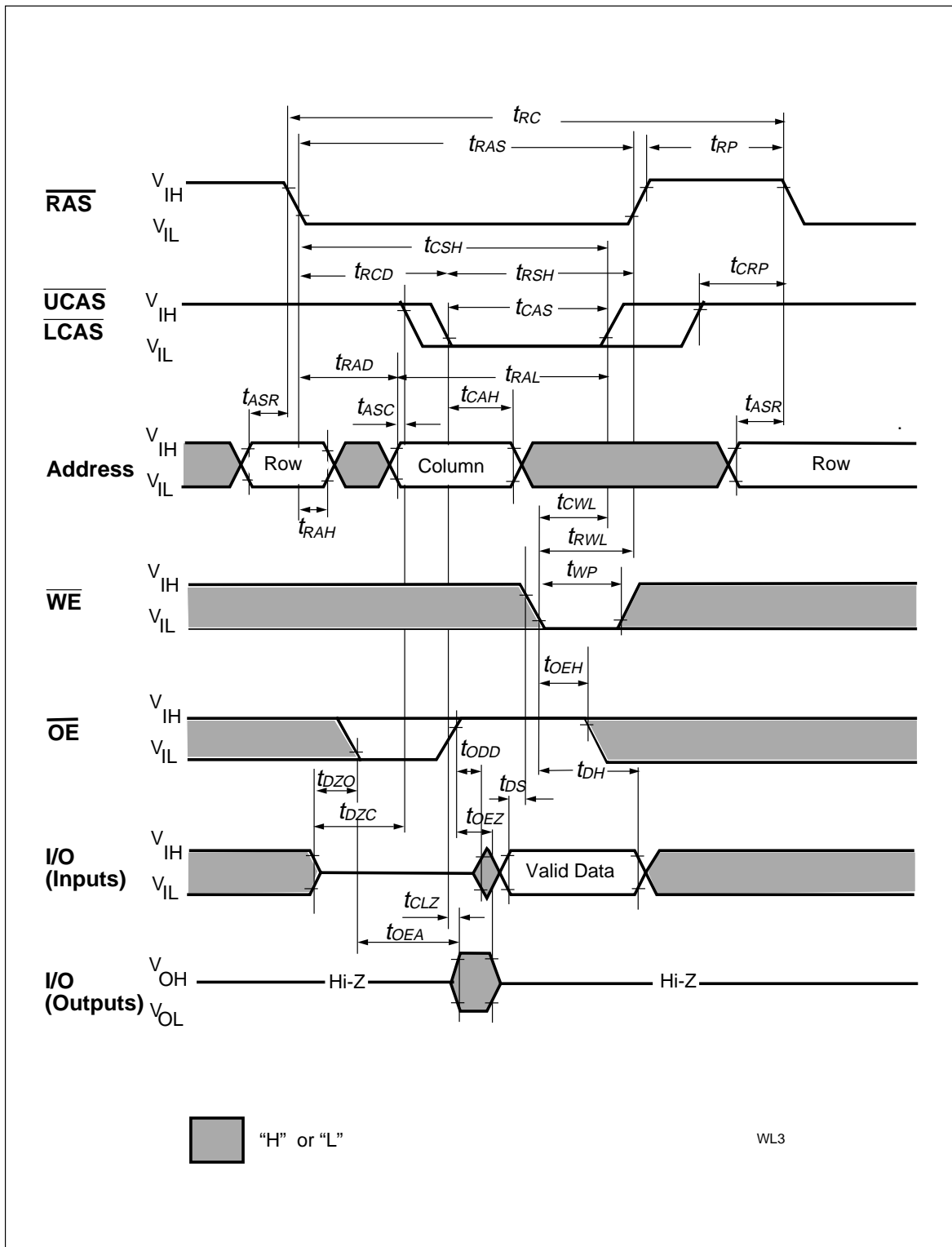
- 1) All voltages are referenced to VSS.  
Vih may overshoot to VV + 0.2V for pulse widths of < 4ns with 3.3V. Vil may undershoot to -2.0V for pulse width < 4.0 ns with 3.3V. Pulse width measured at 50% points with amplitude measured peak to DC reference.
- 2) ICC1, ICC3, ICC4 and ICC6 and ICC7 depend on cycle rate.
- 3) ICC1 and ICC4 depend on output loading. Specified values are measured with the output open.
- 4) Address can be changed once or less while  $\overline{\text{RAS}} = \text{Vil}$ . In the case of ICC4 it can be changed once or less during a Hyper page mode cycle ( thpc).
- 5) An initial pause of 100  $\mu\text{s}$  is required after power-up followed by 8  $\overline{\text{RAS}}$ -only-refresh cycles, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  initialization cycles instead of 8  $\overline{\text{RAS}}$  cycles are required.
- 6) AC measurements assume  $t_T = 2 \text{ ns}$ .
- 7) VIH (min.) and VIL (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between VIH and VIL.
- 8) Measured with the specified current load and 100 pF at Voh = 2.0 V and Vol = 0.8 V.
- 9) Operation within the tRCD (max.) limit ensures that tRAC (max.) can be met. tRCD (max.) is specified as a reference point only: If tRCD is greater than the specified tRCD (max.) limit, then access time is controlled by tCAC.
- 10) Operation within the tRAD (max.) limit ensures that tRAC (max.) can be met. tRAD (max.) is specified as a reference point only: If tRAD is greater than the specified tRAD (max.) limit, then access time is controlled by tAA.
- 11) Either tRCH or tRRH must be satisfied for a read cycle.
- 12) tOFF (max.) and tOEZ (max.) define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.
- 13) Either tDZC or tDZO must be satisfied.
- 14) Either tCDD or tODD must be satisfied.
- 15) tWCS, tRWD, tCWD, tAWD and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS > tWCS (min.), the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if tRWD > tRWD (min.), tCWD > tCWD (min.), tAWD > tAWD (min.) and tCPWD > tCPWD (min.) , the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.
- 16) These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early write cycles and to  $\overline{\text{WRITE}}$  leading edge in Read-Modify-Write cycles.
- 17) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:  
If row addresses are being refresh in an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.  
If row addresses are being refresh in any other manner (ROR - Distributed/Burst or CBR-Burst) over the refresh interval, then a full set of row refreshed must be performed immediately before entry to and immediately after exit from Self Refresh



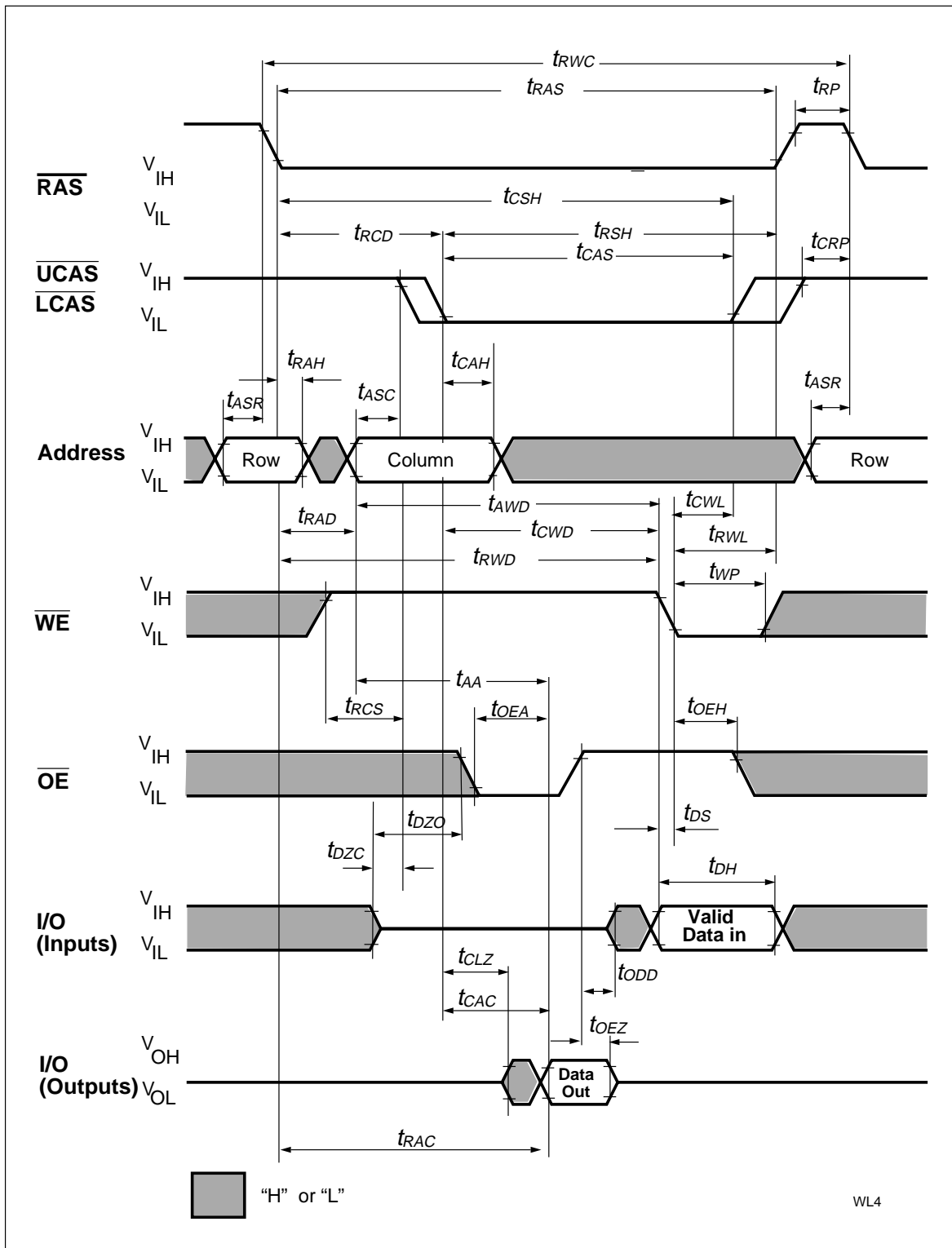
### Read Cycle



**Write Cycle (Early Write)**

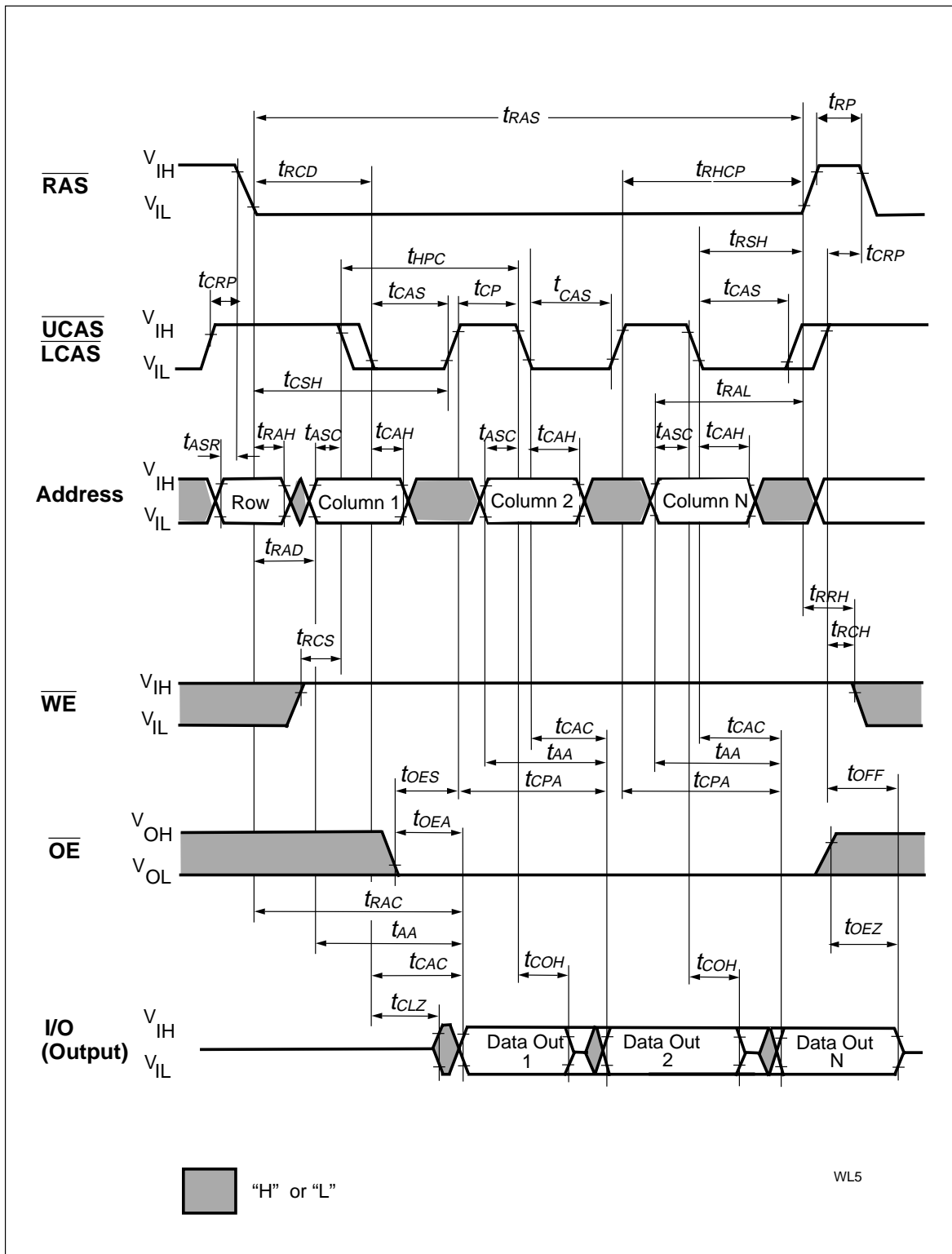


**Write Cycle ( $\overline{OE}$  Controlled Write)**



Read-Write (Read-Modify-Write) Cycle



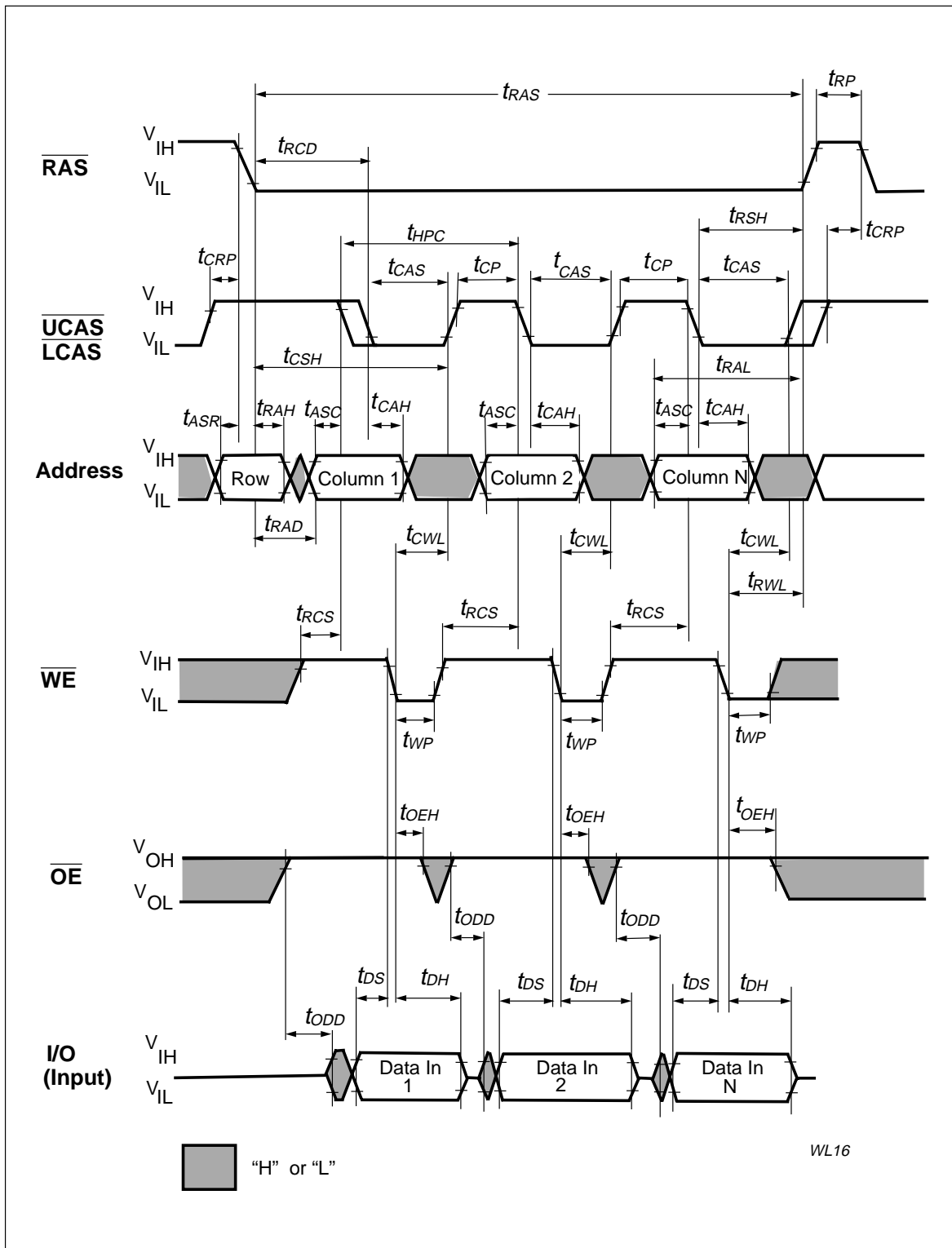


Hyper Page Mode (EDO) Read Cycle



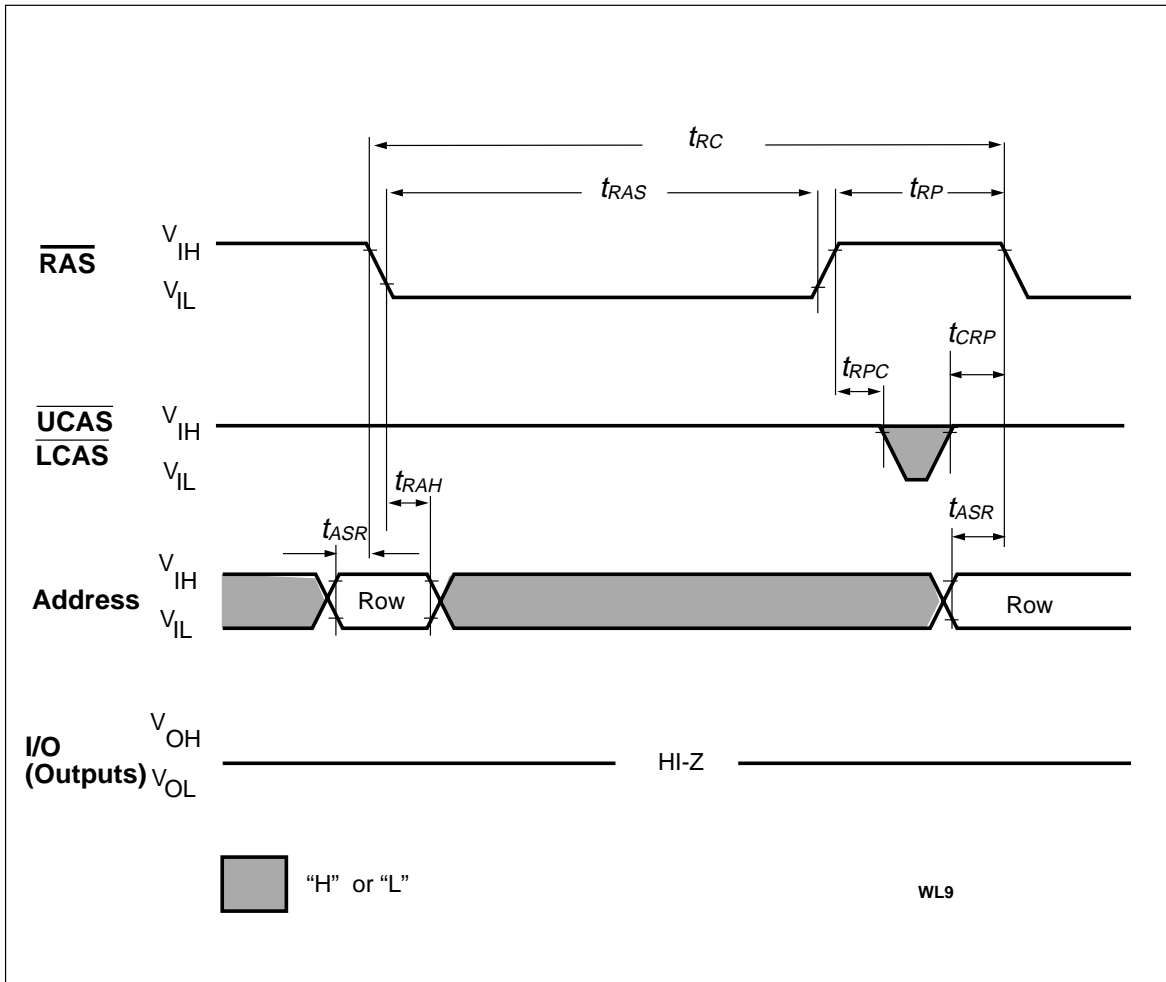




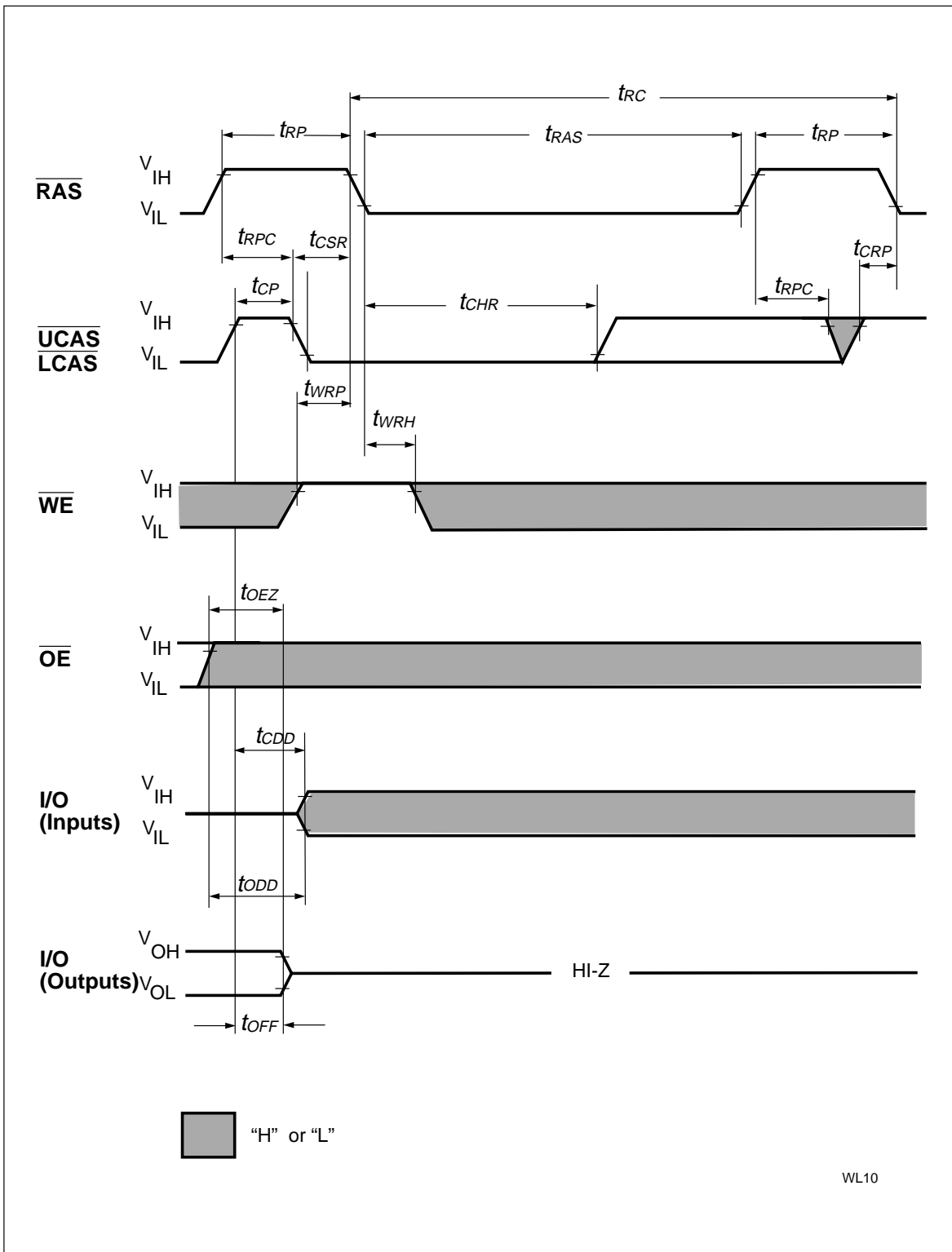


Hyper Page Mode (EDO) Late Write Cycle



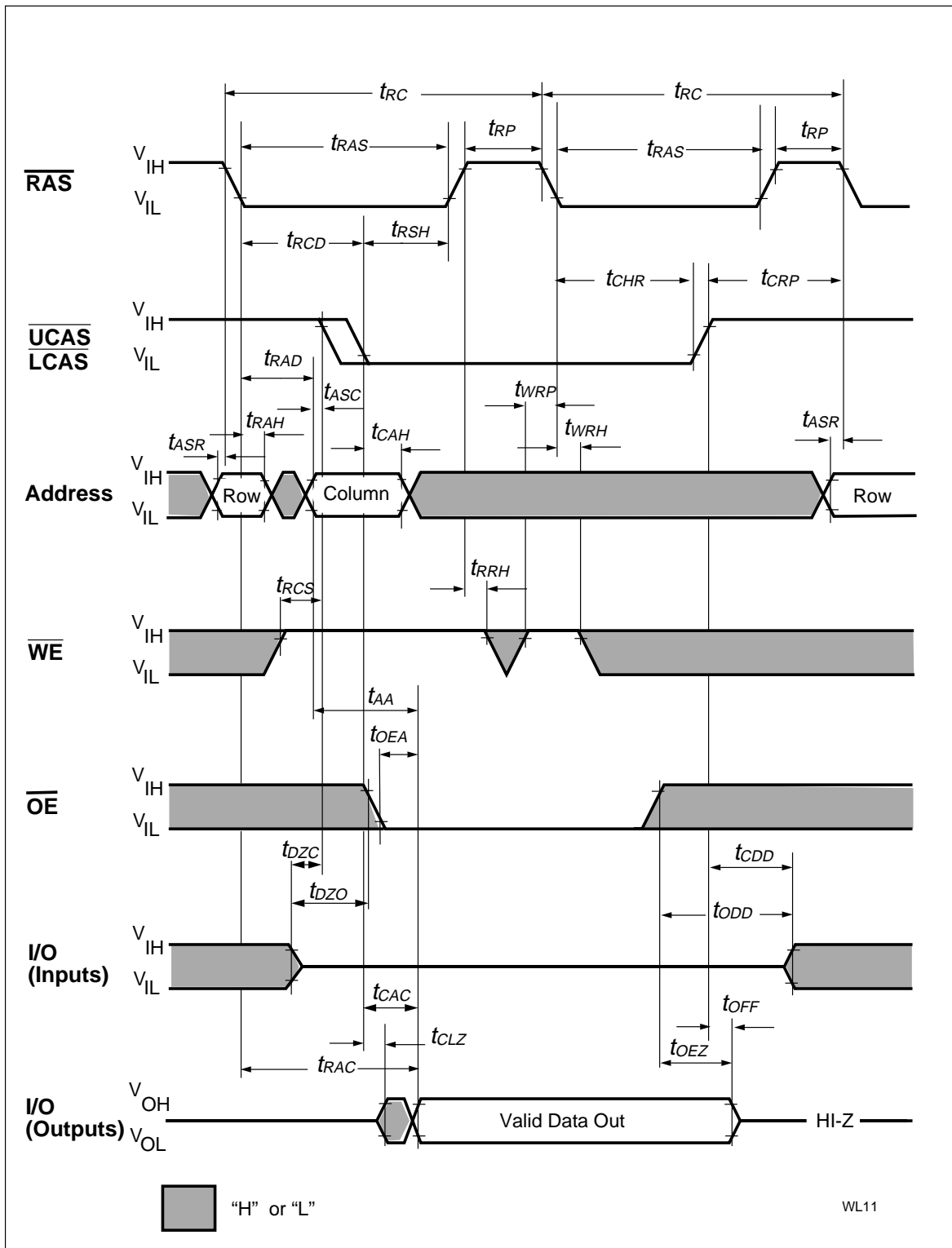


RAS Only Refresh Cycle

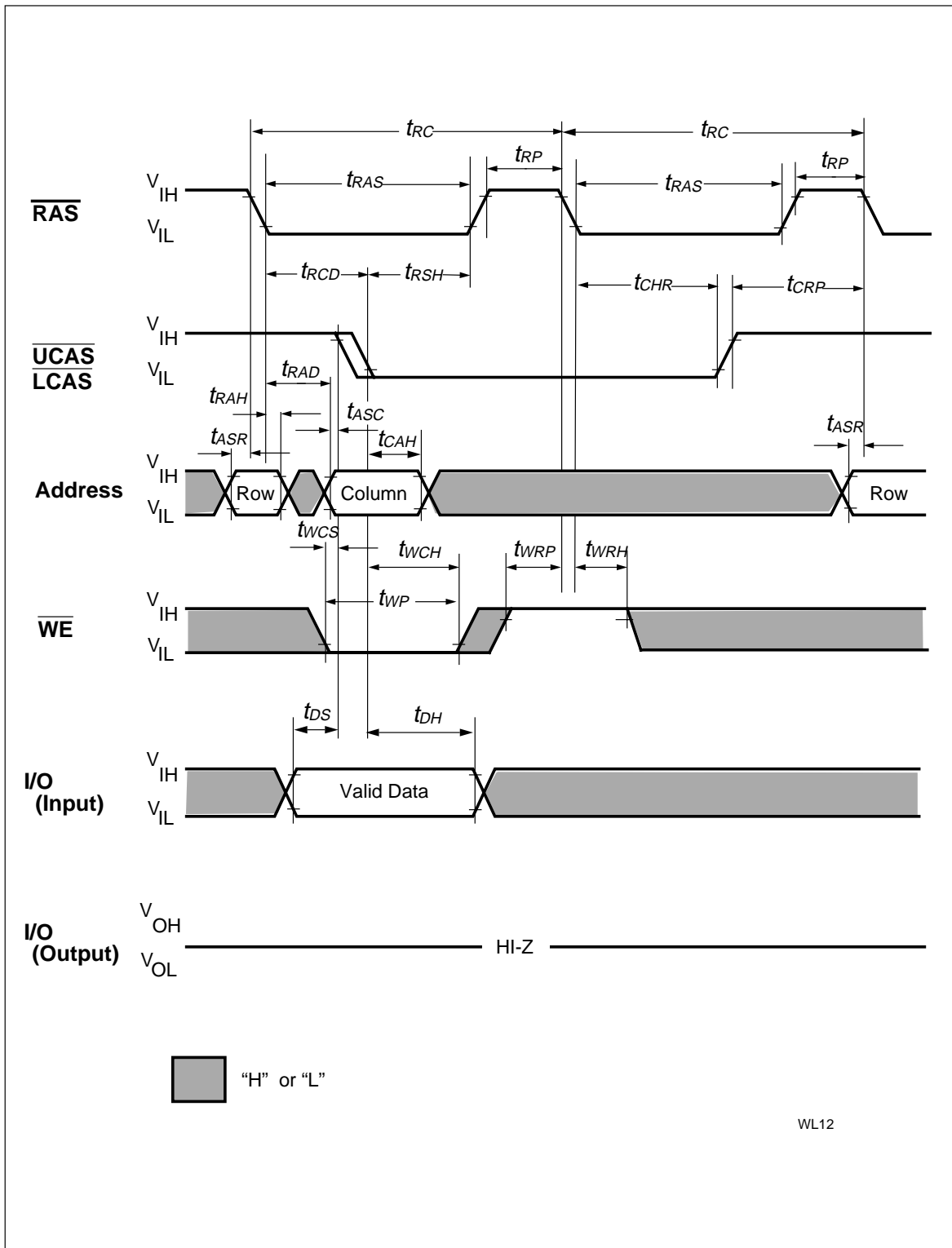


**CAS-before-RAS Refresh Cycle**

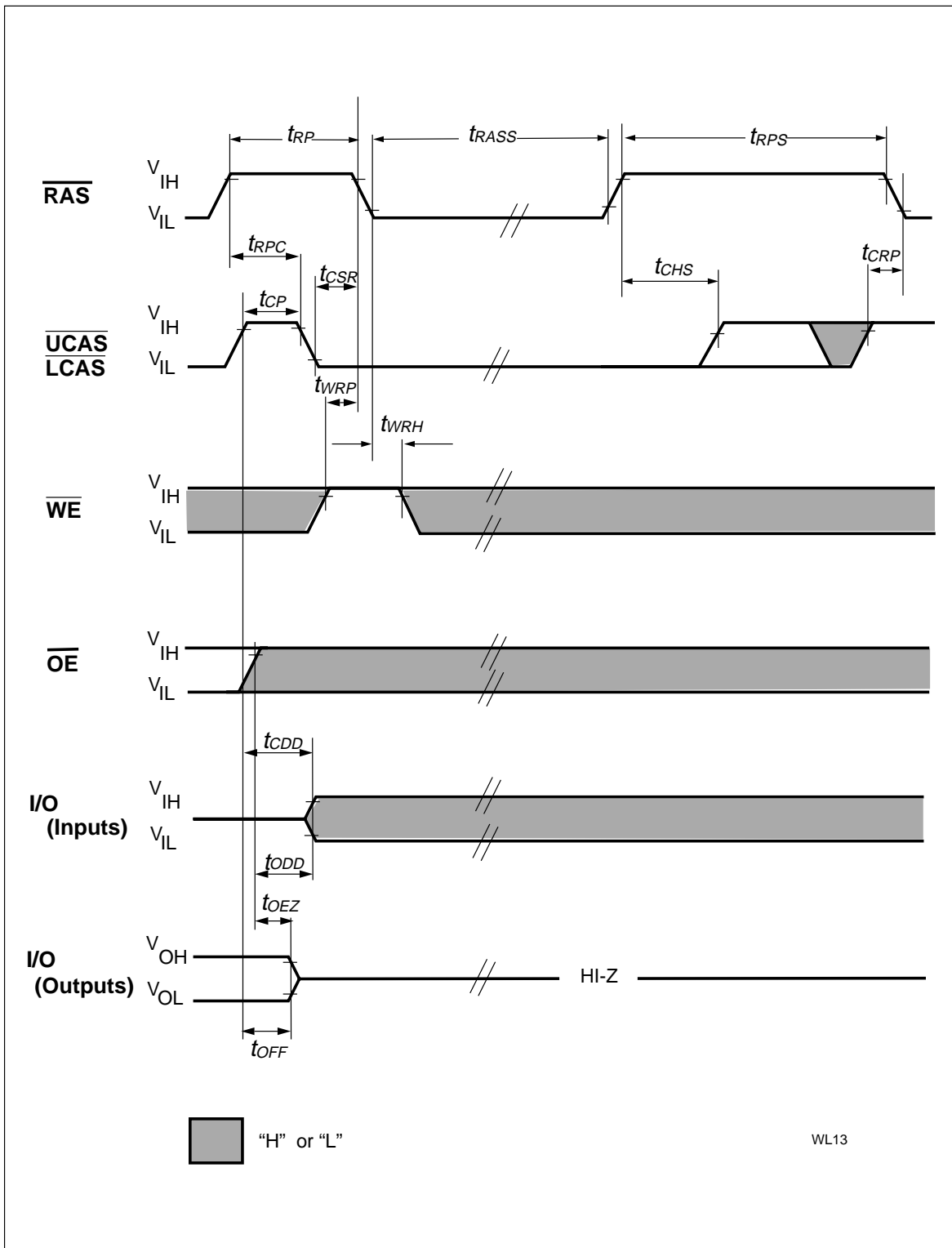




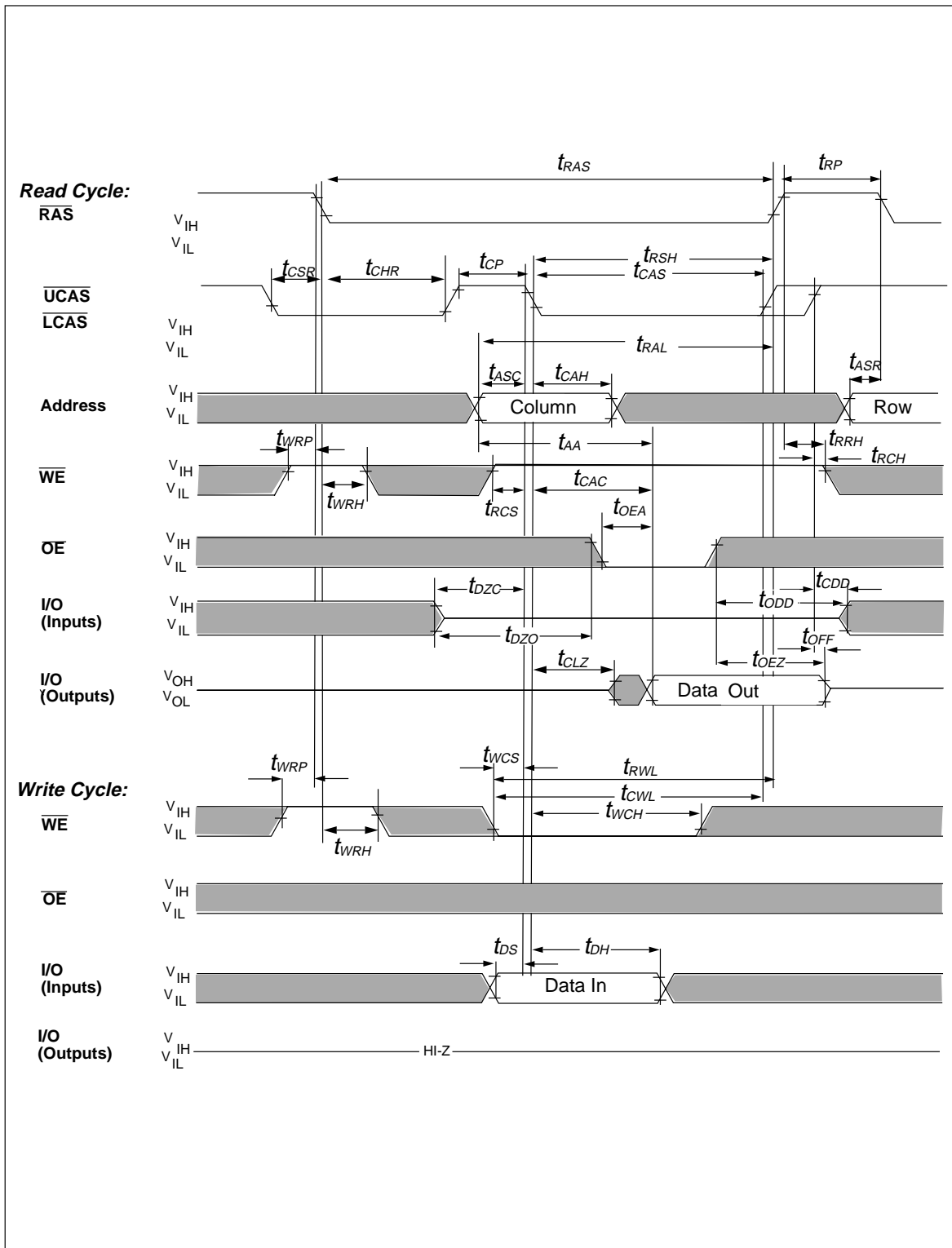
**Hidden Refresh Read Cycle**



Hidden Refresh Early Write Cycle

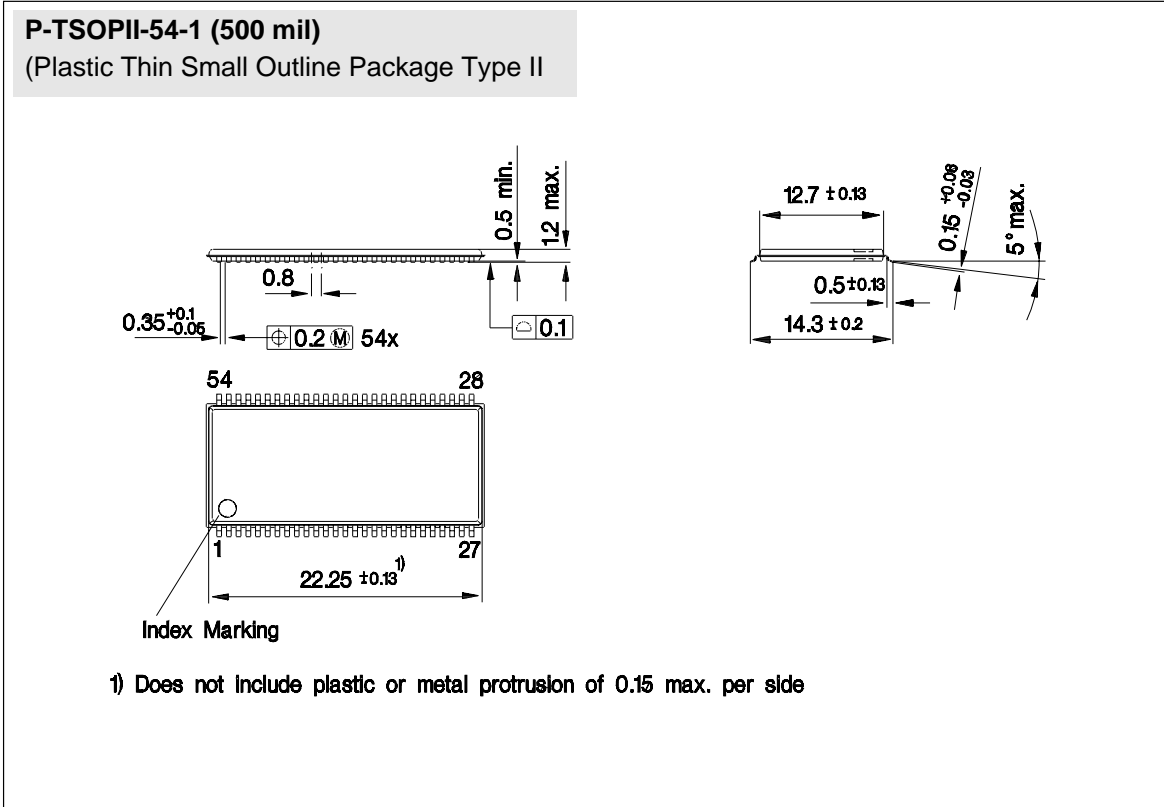


### Self Refresh (Sleep Mode)



CAS-before-RAS Refresh Counter Test Cycle

**Package Outlines**



**Sorts of Packing**

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

VAKAT

((60))