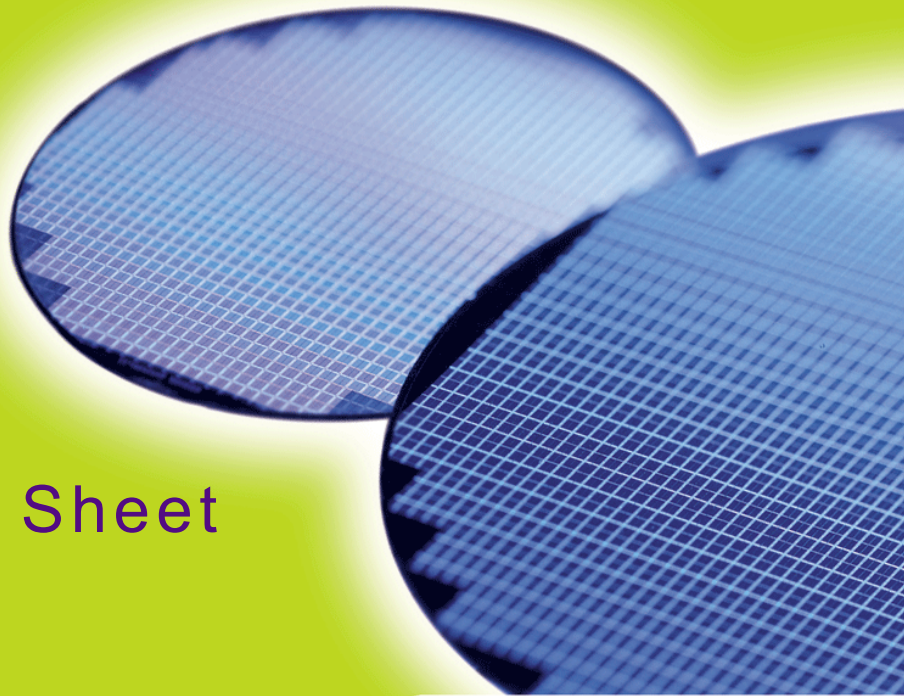


HY[B/I]39S512400A[E/T]  
HY[B/I]39S512800A[E/T]  
HY[B/I]39S512160A[E/T]

*512-Mbit Synchronous DRAM  
SDRAM  
RoHS Compliant Products*



Internet Data Sheet

*Rev. 1.52*

HY[I/B]39S512[40/80/16]0A[E/T]  
512-Mbit Synchronous DRAM

<b>HY[B/I]39S512400A[E/T], HY[B/I]39S512800A[E/T], HY[B/I]39S512160A[E/T]</b>	
<b>Revision History: 2007-06, Rev. 1.52</b>	
<b>Page</b>	<b>Subjects (major changes since last revision)</b>
All	Adapted internet edition
13	Corrected operation command "Power Down / Clock suspend ..." in truth table
<b>Previous Revision: 2007-06, Rev. 1.51</b>	
13	Corrected operation command "Power Down Exit" to X (WE#)
15	Corrected text to "After the mode register is set a NOP command is required" , chapter 3.3
19	Corrected text to "One clock delay is required for mode entry and exit", chapter 3.5
21	Corrected the line "Input Capacitances: CK" in table 10, chapter 4
	Qimonda template
<b>Previous Revision: 2007-05, Rev. 1.5</b>	
All	Added more product types
<b>Previous Revision: 2006-01, Rev. 1.4</b>	

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# 1 Overview

This chapter lists all main features of the product family HY[I/B]39S512[40/80/16]0A[E/T] and the ordering information.

## 1.1 Features

- Fully Synchronous to Positive Clock Edge
- 0 to 70 °C Operating Temperature for HYB...
- -40 to 85 °C Operating Temperature for HYI...
- Four Banks controlled by BA0 & BA1
- Programmable CAS Latency: 2 & 3
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length: 1, 2, 4, 8 and full page
- Multiple Burst Read with Single Write Operation
- Automatic and Controlled Precharge Command
- Data Mask for Read / Write control (x4, x8, x16)
- Data Mask for Byte Control (x16)
- Auto Refresh (CBR) and Self Refresh
- Power Down and Clock Suspend Mode
- 8192 refresh cycles / 64 ms (7.8  $\mu$ s)
- Random Column Address every CLK (1-N Rule)
- Single 3.3 V  $\pm$  0.3 V Power Supply
- LVTTTL Interface
- Plastic Package : P(G)-TSOP11-54
- RoHS compliant product

**TABLE 1**  
Performance

Product Type Speed Code			-7.5	Unit
Speed Grade			PC133-333 <sup>1)</sup>	—
Max. Clock Frequency	@CL3	$f_{CK3}$	133	MHz
		$t_{CK3}$	7.5	ns
		$t_{AC3}$	5.4	ns
	@CL2	$t_{CK2}$	10	ns
		$t_{AC2}$	6	ns

1) Max. Frequency CL/RCD / tRP

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## 1.2 Description

The HY[I/B]39S512[40/80/16]0A[E/T] are four bank Synchronous DRAM's organized as 4 banks × 32MBit × 4, 4 banks × 16MBit × 8 and 4 banks × 8Mbit × 16 respectively. These synchronous devices achieve high speed data transfer rates for CAS latencies by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock. The chip is fabricated with Qimonda advanced 0.14 μm 512-MBit DRAM process technology.

The device is designed to comply with all industry standards set for synchronous DRAM products, both electrically and mechanically. All of the control, address, data input and output circuits are synchronized with the positive edge of an externally supplied clock.

Operating the four memory banks in an interleave fashion allows random access operation to occur at a higher rate than is possible with standard DRAMs. A sequential and gapless data rate is possible depending on burst length, CAS latency and speed grade of the device.

Auto Refresh (CBR) and Self Refresh operation are supported. These devices operate with a single 3.3 V ± 0.3 V power supply. All 512-Mbit components are available in P(G)-TSOPII-54 packages.

**TABLE 2****Ordering Information for RoHS Compliant Products**

Product Type	Speed Grade	Description	Package	Note
<b>Standard Operating Temperature (0 °C - +70 °C)</b>				
HYB39S512400AT-7.5	PC133-333-520	133MHz 4B × 32M × 4 SDRAM	P-TSOPII-54	
HYB39S512800AT-7.5		133MHz 4B × 16M × 8 SDRAM		
HYB39S512160AT-7.5		133MHz 4B × 8M × 16 SDRAM		
HYB39S512400AE-7.5		133MHz 4B × 32M × 4 SDRAM	PG-TSOPII-54	
HYB39S512800AE-7.5		133MHz 4B × 16M × 8 SDRAM		
HYB39S512160AE-7.5		133MHz 4B × 8M × 16 SDRAM		
<b>Industrial Operating Temperature (-40 °C - +85 °C)</b>				
HYI39S512400AT-7.5	PC133-333-520	133MHz 4B × 32M × 4 SDRAM	P-TSOPII-54	
HYI39S512800AT-7.5		133MHz 4B × 16M × 8 SDRAM		
HYI39S512160AT-7.5		133MHz 4B × 8M × 16 SDRAM		
HYI39S512400AE-7.5		133MHz 4B × 32M × 4 SDRAM	PG-TSOPII-54	
HYI39S512800AE-7.5		133MHz 4B × 16M × 8 SDRAM		
HYI39S512160AE-7.5		133MHz 4B × 8M × 16 SDRAM		

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.



## 2 Configuration

This chapter contains the pin configuration table and the TSOP package drawing.

### 2.1 Pin Configuration

Listed below are the pin configurations sections for the various signals of the SDRAM.

**TABLE 3**  
**Ball Configuration of the SDRAM**

Ball No.	Name	Pin Type	Buffer Type	Function
<b>Clock Signals x4/ x8/ x16 Organization</b>				
38	CLK	I	LVTTTL	<b>Clock Signal CLK</b>
37	CKE	I	LVTTTL	<b>Clock Enable</b>
<b>Control Signals x4/ x8/ x16 Organization</b>				
18	$\overline{\text{RAS}}$	I	LVTTTL	<b>Row Address Strobe (RAS), Column Address Strobe (CAS), Write Enable (WE)</b>
17	$\overline{\text{CAS}}$	I	LVTTTL	
16	$\overline{\text{WE}}$	I	LVTTTL	
19	$\overline{\text{CS}}$	I	LVTTTL	<b>Chip Select</b>
<b>Address Signals x4/ x8/ x16 Organization</b>				
20	BA0	I	LVTTTL	<b>Bank Address Signals 1:0</b>
21	BA1	I	LVTTTL	
23	A0	I	LVTTTL	<b>Address Signal 9:0, Address Signal 10/Auto precharge</b>
24	A1	I	LVTTTL	
25	A2	I	LVTTTL	
26	A3	I	LVTTTL	
29	A4	I	LVTTTL	
30	A5	I	LVTTTL	
31	A6	I	LVTTTL	
32	A7	I	LVTTTL	
33	A8	I	LVTTTL	
34	A9	I	LVTTTL	
22	A10	I	LVTTTL	
35	A11	I	LVTTTL	
36	A12	I	LVTTTL	



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Ball No.	Name	Pin Type	Buffer Type	Function
<b>Data Signals x4 Organization</b>				
5	DQ0	I/O	LVTTTL	<b>Data Signal Bus [3:0]</b>
11	DQ1	I/O	LVTTTL	
44	DQ2	I/O	LVTTTL	
50	DQ3	I/O	LVTTTL	
<b>Data Signals x8 Organization</b>				
2	DQ0	I/O	LVTTTL	<b>Data Signal Bus [7:0]</b>
5	DQ1	I/O	LVTTTL	
8	DQ2	I/O	LVTTTL	
11	DQ3	I/O	LVTTTL	
44	DQ4	I/O	LVTTTL	
47	DQ5	I/O	LVTTTL	
50	DQ6	I/O	LVTTTL	
53	DQ7	I/O	LVTTTL	
<b>Data Signals x16 Organization</b>				
2	DQ0	I/O	LVTTTL	<b>Data Signal Bus [15:0]</b>
4	DQ1	I/O	LVTTTL	
5	DQ2	I/O	LVTTTL	
7	DQ3	I/O	LVTTTL	
8	DQ4	I/O	LVTTTL	
10	DQ5	I/O	LVTTTL	
11	DQ6	I/O	LVTTTL	
13	DQ7	I/O	LVTTTL	
42	DQ8	I/O	LVTTTL	
44	DQ9	I/O	LVTTTL	
45	DQ10	I/O	LVTTTL	
47	DQ11	I/O	LVTTTL	
48	DQ12	I/O	LVTTTL	
50	DQ13	I/O	LVTTTL	
51	DQ14	I/O	LVTTTL	
53	DQ15	I/O	LVTTTL	
<b>Data Mask x4 / x8 Organization</b>				
39	DQM	I/O	LVTTTL	<b>Data Mask</b>
<b>Data Mask x16 Organization</b>				
39	UDQM	I/O	LVTTTL	<b>Data Mask Upper Byte</b>
15	LDQM	I/O	LVTTTL	<b>Data Mask Lower Byte</b>
<b>Power Supplies x4 /x8/ x16 Organization</b>				
3, 43, 49	$V_{DDQ}$	PWR	—	<b>Power Supply</b>
1, 14	$V_{DD}$	PWR	—	<b>Power Supply</b>

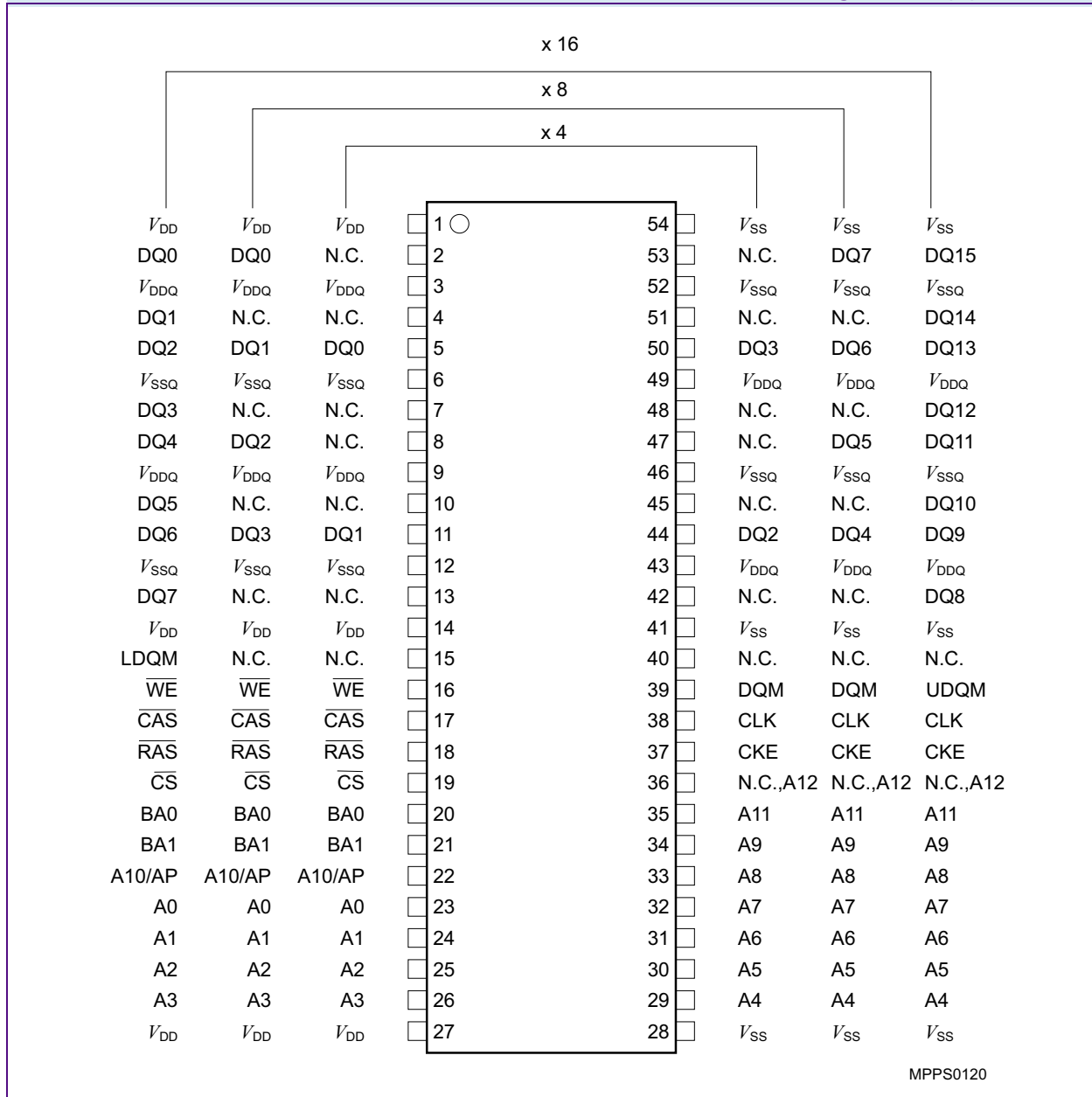
HY[I/B]39S512[40/80/16]0A[E/T]  
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Ball No.	Name	Pin Type	Buffer Type	Function
6, 12, 46, 52	$V_{SSQ}$	PWR	—	Power Supply Ground for DQs
28, 41, 54	$V_{SS}$	PWR	—	Power Supply Ground
<b>Not connected x4 Organization</b>				
2, 4, 7, 8, 10, 13, 15, 40, 42, 45, 47, 48, 51, 53	NC	NC	—	Not connected
<b>Not connected x8 Organization</b>				
4, 7, 10, 13, 15, 40, 42, 45, 48, 51	NC	NC	—	Not connected
<b>Not connected x16 Organization</b>				
40	NC	NC	—	Not connected



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**FIGURE 1**  
**Ball Configuration P(G)-TSOPII-54**







### 3 Functional Description

This chapter lists all defined commands and their usage for this Synchronous DRAM family.

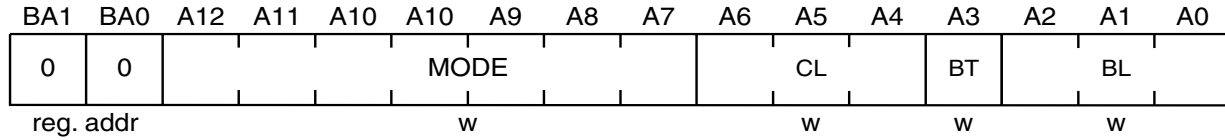
**TABLE 4**  
**Truth Table: Operation Command**

Operation	Device State	CKE n-1 <sup>1)2)</sup>	CKE n <sup>1)2)</sup>	DQM 1)2)	BA0 BA1 <sup>1)2)</sup>	AP= A10 <sup>1)2)</sup>	Addr. 1)2)	CS 1)2)	RAS 1)2)	CAS 1)2)	WE 1)2)
Bank Active	Idle <sup>3)</sup>	H	X	X	V	V	V	L	L	H	H
Bank Precharge	Any	H	X	X	V	L	X	L	L	H	L
Precharge All	Any	H	X	X	X	H	X	L	L	H	L
Write	Active <sup>3)</sup>	H	X	X	V	L	V	L	H	L	L
Write with Auto precharge	Active <sup>3)</sup>	H	X	X	V	H	V	L	H	L	L
Read	Active <sup>3)</sup>	H	X	X	V	L	V	L	H	L	H
Read with Auto precharge	Active <sup>3)</sup>	H	X	X	V	H	V	L	H	L	H
Mode Register Set	Idle	H	X	X	V	V	V	L	L	L	L
No Operation	Any	H	X	X	X	X	X	L	H	H	H
Burst Stop	Active	H	X	X	X	X	X	L	H	H	L
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
Auto Refresh	Idle	H	H	X	X	X	X	L	L	L	H
Self Refresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
Self Refresh Exit	Idle (Self Refr.)	L	H	X	X	X	X	H	X	X	X
								L	H	H	X
Power Down/ Clock Suspend Entry	Active or Idle or Burst	H	L	X	X	X	X	H	X	X	X
								L	H	H	H
Power Down/ Clock Suspend Exit	Active or Idle or Burst	L	H	X	X	X	X	H	X	X	X
								L	H	H	H
Data Write/ Output Enable	Active	H	X	L	X	X	X	X	X	X	X
Data Write/ Output Disable	Active	H	X	H	X	X	X	X	X	X	X

- 1) V = Valid, x = Don't Care, L = Low Level, H = High Level
- 2) CKEn signal is input level when commands are provided, CKEn-1 signal is input level one clock before the commands are provided.
- 3) This is the state of the banks designated by BA0, BA1 signals.



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MPBS0000

**TABLE 5**  
Mode Register Definition (BA[1:0] = 00<sub>B</sub>)

Field	Bits	Type	Description
<b>BL</b>	[2:0]	w	<b>Burst Length</b> Number of sequential bits per DQ related to one read/write command, see <i>Note: All other bit combinations are RESERVED</i>  000 <sub>B</sub> <b>1</b> 001 <sub>B</sub> <b>2</b> 010 <sub>B</sub> <b>4</b> 011 <sub>B</sub> <b>8</b> 111 <sub>B</sub> <b>Full Page (Sequential burst type only)</b>
<b>BT</b>	3	w	<b>Burst Type</b> See <b>Table 6</b> for internal address sequence of low order address bits. 0 <sub>B</sub> <b>Sequential</b> 1 <sub>B</sub> <b>Interleaved</b>
<b>CL</b>	[6:4]	w	<b>CAS Latency</b> Number of full clocks from read command to first data valid window. <i>Note: All other bit combinations are RESERVED.</i>  010 <sub>B</sub> <b>2</b> 011 <sub>B</sub> <b>3</b>
<b>Mode</b>	[12:7]	w	<b>Operation Mode</b> <i>Note: All other bit combinations are RESERVED.</i>  0 <sub>B</sub> <b>Burst read/burst write</b> 1 <sub>B</sub> <b>Burst read/single write</b>



**TABLE 6**  
**Burst Length and Sequence**

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
	A2	A1	A0	Type=Sequential	Type=Interleaved
2			0	0-1	0-1
			1	1-0	1-0
4		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
FullPage	n			Cn, Cn+1, Cn+2 ....	Not supported

**Notes**

1. For a burst length of two, A1-Ai selects the two-data-element block; A0 selects the first access within the block.
2. For a burst length of four, A2-Ai selects the four-data-element block; A0-A1 selects the first access within the block.
3. For a burst length of eight, A3-Ai selects the eight-data- element block; A0-A2 selects the first access with in the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.



## 4 Electrical Characteristics

### 4.1 Operating Conditions

**TABLE 7**  
Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Note/ Test Condition
		Min.	Max.		
Input / Output voltage relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-1.0	+4.6	V	—
Voltage on $V_{DD}$ supply relative to $V_{SS}$	$V_{DD}$	-1.0	+4.6	V	—
Voltage on $V_{DDQ}$ supply relative to $V_{SS}$	$V_{DDQ}$	-1.0	+4.6	V	—
Operating Temperature for HYB...	$T_A$	0	+70	°C	—
Operating Temperature for HYI...	$T_A$	-40	+85	°C	—
Storage temperature range	$T_{STG}$	-55	+150	°C	—
Power dissipation per SDRAM component	$P_D$	—	1	W	—
Data out current (short circuit)	$I_{OUT}$	—	50	mA	—

**Attention:** Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.



**TABLE 8**  
DC Characteristics

Parameter	Symbol	Values		Unit	Note/ Test Condition
		Min.	Max.		
Supply Voltage	$V_{DD}$	3.0	3.6	V	1)
I/O Supply Voltage	$V_{DDQ}$	3.0	3.6	V	1)
Input high voltage	$V_{IH}$	2.0	$V_{DDQ} + 0.3$	V	1)2)
Input low voltage	$V_{IL}$	-0.3	+0.8	V	1)2)
Output high voltage ( $I_{OUT} = -4.0$ mA)	$V_{OH}$	2.4	—	V	1)
Output low voltage ( $I_{OUT} = 4.0$ mA)	$V_{OL}$	—	0.4	V	1)
Input leakage current, any input ( $0 V < V_{IN} < V_{DD}$ , all other inputs = 0 V)	$I_{IL}$	-5	+5	$\mu$ A	—
Output leakage current (DQs are disabled, $0 V < V_{OUT} < V_{DDQ}$ )	$I_{OL}$	-5	+5	$\mu$ A	—

- 1) All voltages are referenced to  $V_{SS}$
- 2)  $V_{IH}$  may overshoot to  $V_{DDQ} + 2.0$  V for pulse width of  $< 4$  ns with 3.3 V.  $V_{IL}$  may undershoot to  $-2.0$  V for pulse width  $< 4.0$  ns with 3.3 V. Pulse width measured at 50% points with amplitude measured peak to DC reference.

**TABLE 9**  
Input and Output Capacitances

Parameter	Symbol	Values		Unit	Note
		Min.	Max.		
Input Capacitances: CK	$C_{I1}$	2.5	3.5	pF	1)2)
Input Capacitance (A0-A12, BA0, BA1, $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ , $\overline{CS}$ , CKE, DQM)	$C_{I2}$	2.5	3.8	pF	1)2)
Input/Output Capacitance (DQ)	$C_{I0}$	4.0	6.0	pF	1)2)

- 1)  $V_{DD}, V_{DDQ} = 3.3$  V  $\pm$  0.3 V,  $f = 1$  MHz,  $T_A$  see **Table 7**
- 2) Capacitance values are shown for TSOP-54 packages. Capacitance values for TFBGA packages are lower by 0.5 pF



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**TABLE 10**  
 **$I_{DD}$  Conditions**

Parameter		Symbol
Operating Current	One bank active, Burst length = 1	$I_{DD1}$
Precharge Standby Current	Power down mode	$I_{DD2P}$
	Non-power down mode	$I_{DD2N}$
No Operating Current	Active state (max. 4 banks)	$I_{DD3N}$
		$I_{DD3P}$
Burst Operating Current	Read command cycling	$I_{DD4}$
Auto Refresh Current	Auto Refresh command cycling	$I_{DD5}$
Self Refresh Current	Self Refresh Mode, $CKE=0.2\text{ V}$ , $t_{CK}=\text{infinity}$	$I_{DD6}$

**TABLE 11**  
 **$I_{DD}$  Specifications and Conditions**

Symbol	Test Condition	-7.5		Unit	Note <sup>1)</sup>
		Typ.	Max.		
$I_{DD1}$	$t_{RC} = t_{RC(\text{min})}$ , $I_O = 0\text{ mA}$	123	145	mA	2 <sup>3)</sup>
$I_{DD2P}$	$\overline{CS} = V_{IH(\text{min.})}$ , $CKE \leq V_{IL(\text{max.})}$	0.6	3	mA	2)
$I_{DD2N}$	$\overline{CS} = V_{IH(\text{min.})}$ , $CKE \geq V_{IH(\text{min.})}$	23	31	mA	2)
$I_{DD3N}$	$\overline{CS} = V_{IH(\text{min.})}$ , $CKE \geq V_{IH(\text{min.})}$	26	35	mA	2)
$I_{DD3P}$	$\overline{CS} = V_{IH(\text{min.})}$ , $CKE \leq V_{IL(\text{max.})}$	2	4	mA	2)
$I_{DD4}$		97	123	mA	2 <sup>3)</sup>
$I_{DD5}$	$t_{RFC} = t_{RFC(\text{min})}$	255	300	mA	4)
	$t_{RFC} = 15.6\ \mu\text{s}$	—	—	mA	—
$I_{DD6}$		2.1	4	mA	—

- 1)  $T_A = 0$  to  $70\text{ }^\circ\text{C}$  for HYB.,  $T_A = -40$  to  $85\text{ }^\circ\text{C}$  for i-temp part (HYI.);  $V_{SS} = 0\text{ V}$ ,  $V_{DD}$ ,  $V_{DDQ} = +3.3\text{ V} \pm 0.3\text{ V}$
- 2) These parameters depend on the cycle rate. All values are measured at 133 MHz for “-7.5” components with the outputs open. Input signals are changed once during  $t_{ck}$ .
- 3) These parameters are measured with continuous data stream during read access and all DQ toggling. CL=3 and BL=4 is assumed and the  $V_{DDQ}$  current is excluded.
- 4)  $t_{RFC} = t_{RFC(\text{min})}$  “burst refresh”,  $t_{RFC} = 15.6\ \mu\text{s}$  “distributed refresh”.



## 4.2 AC Characteristics

**TABLE 12**  
**AC Timing - Absolute Specifications**

Parameter	Symbol	-7.5		Unit	Note <sup>1)2)3)</sup>
		PC133-333			
		Min.	Max.		
<b>Clock and Clock Enable</b>					
Clock Frequency	$t_{CK}$	7.5 10	— —	ns ns	CL3 CL2
Access Time from Clock	$t_{AC}$	— —	5.4 6	ns ns	CL3 CL2 3)4)5)
Clock High Pulse Width	$t_{CH}$	2.5	—	ns	
Clock Low Pulse Width	$t_{CL}$	2.5	—	ns	
Transition time	$t_T$	0.3	1.2	ns	
<b>Setup and Hold Times</b>					
Input Setup Time	$t_{IS}$	1.5	—	ns	6)
Input Hold Time	$t_{IH}$	0.8	—	ns	6)
CKE Setup Time	$t_{CKS}$	1.5	—	ns	6)
CKE Hold Time	$t_{CKH}$	0.8	—	ns	6)
Mode Register Set-up to Active delay	$t_{RSC}$	2	—	$t_{CK}$	
Power Down Mode Entry Time	$t_{SB}$	0	7.5	ns	
<b>Common Parameters</b>					
Row to Column Delay Time	$t_{RCD}$	20	—	ns	7)
Row Precharge Time	$t_{RP}$	20	—	ns	7)
Row Active Time	$t_{RAS}$	45	100k	ns	7)
Row Cycle Time	$t_{RC}$	67	—	ns	7)
Row Cycle Time during Auto Refresh	$t_{RFC}$	67	—	ns	
Activate(a) to Activate(b) Command period	$t_{RRD}$	15	—	ns	7)
CAS(a) to CAS(b) Command period	$t_{CCD}$	1	—	$t_{CK}$	
<b>Refresh Cycle</b>					
Refresh Period (8192 cycles)	$t_{REF}$	—	64	ms	
Self Refresh Exit Time	$t_{SREX}$	1	—	$t_{CK}$	
Data Out Hold Time	$t_{OH}$	3	—	ns	3)5)
<b>Read Cycle</b>					
Data Out to Low Impedance Time	$t_{LZ}$	1	—	ns	
Data Out to High Impedance Time	$t_{HZ}$	3	7	ns	
DQM Data Out Disable Latency	$t_{DQZ}$	—	2	$t_{CK}$	

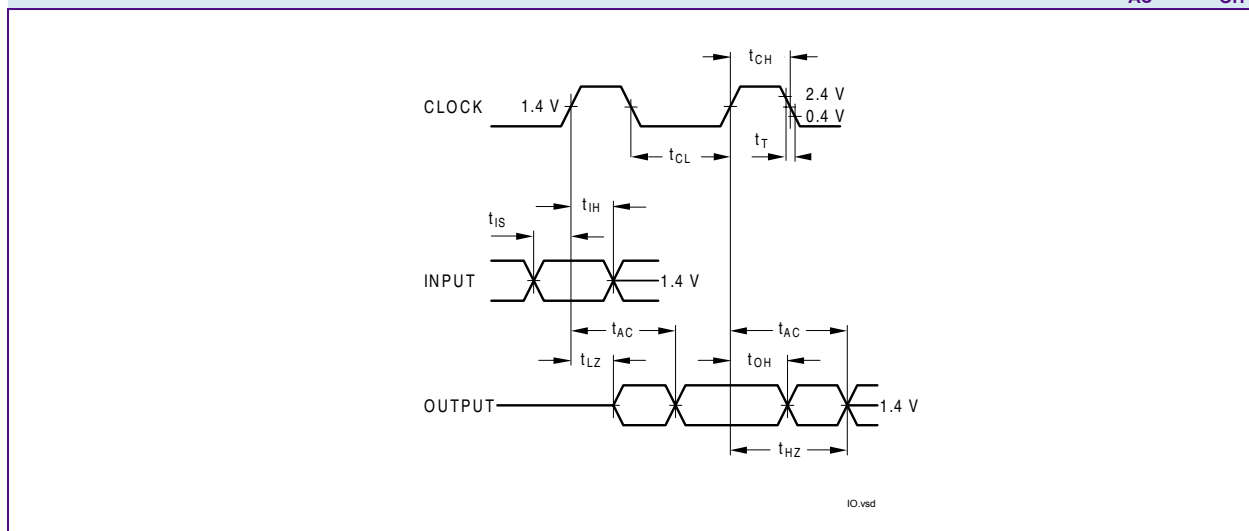


HY[I/B]39S512[40/80/16]0A[E/T]  
512-Mbit Synchronous DRAM

Parameter	Symbol	-7.5		Unit	Note <sup>1)2)3)</sup>
		PC133-333			
		Min.	Max.		
<b>Write Cycle</b>					
Last Data Input to Precharge (Write without Auto Precharge)	$t_{WR}$	15	—	ns	8)
Last Data Input to Activate (Write with Auto Precharge)	$t_{DAL(min.)}$	—	—	$t_{CK}$	9)
DQM Write Mask Latency	$t_{DQW}$	0	—	$t_{CK}$	

- 1)  $T_A = 0$  to  $70$  °C for HYB...,  $T_A = -40$  to  $85$  °C for i-temp part (HYL.);  $V_{SS} = 0$  V,  $V_{DD}, V_{DDQ} = 3.3$  V  $\pm$  0.3 V,  $t_T = 1$  ns
- 2) For proper power-up see the operation section of this data sheet.
- 3) AC timing tests for LV-TTL versions have  $V_{IL} = 0.4$  V and  $V_{IH} = 2.4$  V with the timing referenced to the 1.4 V crossover point. The transition time is measured between  $V_{IH}$  and  $V_{IL}$ . All AC measurements assume  $t_T = 1$  ns with the AC output load circuit shown in figure below. Specified  $t_{AC}$  and  $t_{OH}$  parameters are measured with a 50 pF only, without any resistive termination and with an input signal of 1V / ns edge rate between 0.8 V and 2.0 V.
- 4) If clock rising time is longer than 1 ns, a time  $(t_r/2 - 0.5)$  ns has to be added to this parameter.
- 5) Access time from clock  $t_{ac}$  is 4.6 ns for PC133 components with no termination and 0 pF load, Data out hold time  $t_{oh}$  is 1.8 ns for PC133 components with no termination and 0 pF load.
- 6) If  $t_T$  is longer than 1 ns, a time  $(t_T - 1)$  ns has to be added to this parameter.
- 7) These parameter account for the number of clock cycles and depend on the operating frequency of the clock, as follows:  
the number of clock cycles = specified value of timing period (counted in fractions as a whole number)
- 8) It is recommended to use two clock cycles between the last data-in and the precharge command in case of a write command without Auto-Precharge. One clock cycle between the last data-in and the precharge command is also supported, but restricted to cycle times  $t_{CK}$  greater or equal the specified  $t_{WR}$  value, where  $t_{ck}$  is equal to the actual system clock time.
- 9) When a Write command with Auto Precharge has been issued, a time of  $t_{DAL(min)}$  has to be fulfilled before the next Activate Command can be applied. For each of the terms, if not already an integer, round up to the next highest integer.  $t_{CK}$  is equal to the actual system clock time.

**FIGURE 2**  
Measurement conditions for  $t_{AC}$  and  $t_{OH}$

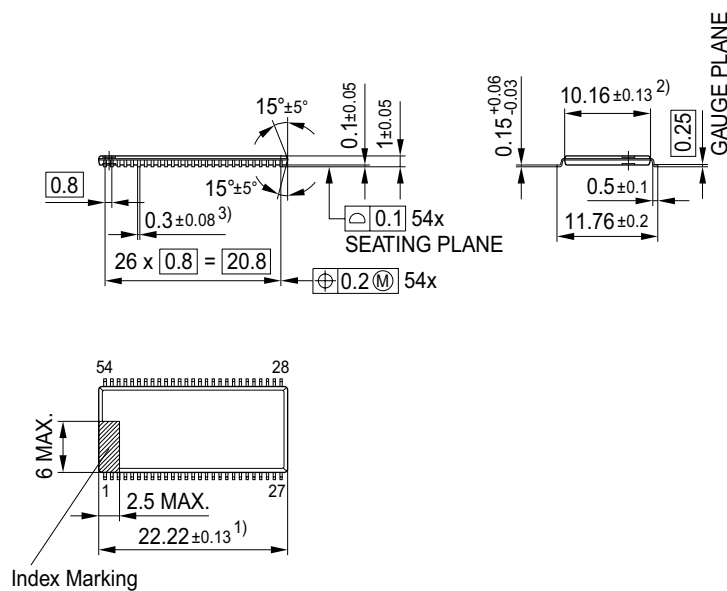




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## 5 Package Outlines

**FIGURE 3**  
Package Outline PG-TSOPII-54 (top view)



- 1) Does not include plastic or metal protrusion of 0.15 max. per side  
2) Does not include plastic protrusion of 0.25 max. per side  
3) Does not include dambar protrusion of 0.13 max. per side

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