

# LH28F160S5-L/S5H-L

## 16 M-bit (2 MB x 8/1 MB x 16) Smart 5 Flash Memories (Fast Programming)

### DESCRIPTION

The LH28F160S5-L/S5H-L flash memories with Smart 5 technology are high-density, low-cost, nonvolatile, read/write storage solution for a wide range of applications, having high programming performance is achieved through highly-optimized page buffer operations. Their symmetrically-blocked architecture, flexible voltage and enhanced cycling capability provide for highly flexible component suitable for resident flash arrays, SIMMs and memory cards. Their enhanced suspend capabilities provide for an ideal solution for code + data storage applications. For secure code storage applications, such as networking, where code is either directly executed out of flash or downloaded to DRAM, the LH28F160S5-L/S5H-L offer three levels of protection : absolute protection with V<sub>PP</sub> at GND, selective hardware block locking, or flexible software block locking. These alternatives give designers ultimate control of their code security needs. The LH28F160S5-L/S5H-L are conformed to the flash Scalable Command Set (SCS) and the Common Flash Interface (CFI) specification which enable universal and upgradable interface, enable the highest system/device data transfer rates and minimize device and system-level implementation costs.

### FEATURES

- Smart 5 technology
  - 5 V V<sub>CC</sub>
  - 5 V V<sub>PP</sub>
- High speed write performance
  - Two 32-byte page buffers
  - 2 μs/byte write transfer rate
- Common Flash Interface (CFI)
  - Universal & upgradable interface
- Scalable Command Set (SCS)
- High performance read access time
  - LH28F160S5-L70
    - 70 ns (5.0±0.25 V)/80 ns (5.0±0.5 V)
  - LH28F160S5H-L70
    - 70 ns (5.0±0.25 V)/90 ns (5.0±0.5 V)
  - LH28F160S5-L10/S5H-L10
    - 100 ns (5.0±0.5 V)
- Enhanced automated suspend options
  - Write suspend to read
  - Block erase suspend to write
  - Block erase suspend to read
- Enhanced data protection features
  - Absolute protection with V<sub>PP</sub> = GND
  - Flexible block locking
  - Erase/write lockout during power transitions
- SRAM-compatible write interface
- User-configurable x8 or x16 operation
- High-density symmetrically-blocked architecture
  - Thirty-two 64 k-byte erasable blocks
- Enhanced cycling capability
  - 100 000 block erase cycles
  - 3.2 million block erase cycles/chip
- Low power management
  - Deep power-down mode
  - Automatic power saving mode decreases I<sub>CC</sub> in static mode
- Automated write and erase
  - Command user interface
  - Status register
- ETOX™\* V nonvolatile flash technology
- Packages
  - 56-pin TSOP Type I (TSOP056-P-1420)  
Normal bend/Reverse bend
  - 56-pin SSOP (SSOP056-P-0600)\*  
[LH28F160S5-L]
  - 64-ball CSP (FBGA064-P-0811)
  - 64-pin SDIP (SDIP064-P-0750)\*

\* ETOX is a trademark of Intel Corporation.

★ Under development

COMPARISON TABLE

VERSIONS	OPERATING TEMPERATURE	ACCESS TIME at 5.0±0.5 V	DC CHARACTERISTICS Vcc deep power-down current (MAX.)	PACKAGE
LH28F160S5-L70/L10	0 to +70°C	80 ns/100 ns	15 µA	56-pin TSOP (I), 56-pin SSOP*, 64-ball CSP, 64-pin SDIP*
LH28F160S5H-L70/L10	-40 to +85°C	90 ns/100 ns	20 µA	56-pin TSOP (I), 64-ball CSP, 64-pin SDIP*

★ Under development

PIN CONNECTIONS

★ Under development

**56-PIN TSOP (Type I)**

NC	1	56	WP#
CE1#	2	55	WE#
NC	3	54	OE#
A20	4	53	STS
A19	5	52	DQ15
A18	6	51	DQ7
A17	7	50	DQ14
A16	8	49	DQ6
VCC	9	48	GND
A15	10	47	DQ13
A14	11	46	DQ5
A13	12	45	DQ12
A12	13	44	DQ4
CE0#	14	43	Vcc
VPP	15	42	GND
RP#	16	41	DQ11
A11	17	40	DQ3
A10	18	39	DQ10
A9	19	38	DQ2
A8	20	37	Vcc
GND	21	36	DQ9
A7	22	35	DQ1
A6	23	34	DQ8
A5	24	33	DQ0
A4	25	32	A0
A3	26	31	BYTE#
A2	27	30	NC
A1	28	29	NC

(TSOP056-P-1420)

**56-PIN SSOP\* [LH28F160S5-L] TOP VIEW**

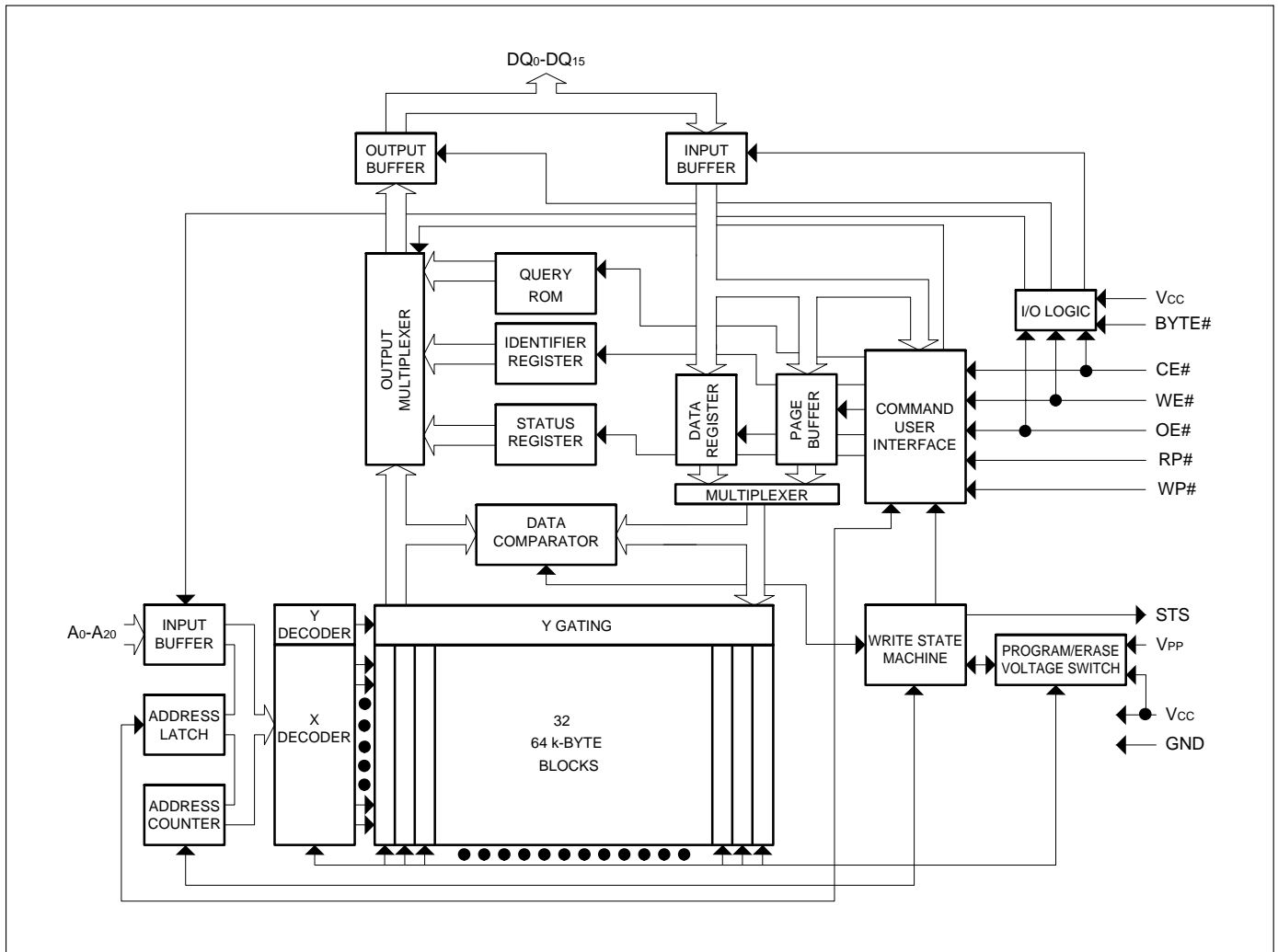
CE0#	1	56	VPP
A12	2	55	RP#
A13	3	54	A11
A14	4	53	A10
A15	5	52	A9
NC	6	51	A1
CE1#	7	50	A2
NC	8	49	A3
A20	9	48	A4
A19	10	47	A5
A18	11	46	A6
A17	12	45	A7
A16	13	44	GND
VCC	14	43	A8
GND	15	42	VCC
DQ6	16	41	DQ9
DQ14	17	40	DQ1
DQ7	18	39	DQ8
DQ15	19	38	DQ0
STS	20	37	A0
OE#	21	36	BYTE#
WE#	22	35	NC
WP#	23	34	NC
DQ13	24	33	DQ2
DQ5	25	32	DQ10
DQ12	26	31	DQ3
DQ4	27	30	DQ11
VCC	28	29	GND

(SSOP056-P-0600)

**NOTE :**  
Reverse bend available on request.



BLOCK DIAGRAM



## PIN DESCRIPTION

SYMBOL	TYPE	NAME AND FUNCTION
A0-A20	INPUT	<b>ADDRESS INPUTS</b> : Inputs for addresses during read and write operations. Addresses are internally latched during a write cycle. A0 : Byte Select Address. Not used in x16 mode (can be floated). A1-A4 : Column Address. Selects 1 of 16-bit lines. A5-A15 : Row Address. Selects 1 of 2 048-word lines. A16-A20 : Block Address.
DQ0-DQ15	INPUT/ OUTPUT	<b>DATA INPUT/OUTPUTS</b> : DQ0-DQ7 : Inputs data and commands during CUI write cycles; outputs data during memory array, status register, query, and identifier code read cycles. Data pins float to high-impedance when the chip is deselected or outputs are disabled. Data is internally latched during a write cycle. DQ8-DQ15 : Inputs data during CUI write cycles in x16 mode; outputs data during memory array read cycles in x16 mode; not used for status register, query and identifier code read mode. Data pins float to high-impedance when the chip is deselected, outputs are disabled, or in x8 mode (BYTE# = V <sub>IL</sub> ). Data is internally latched during a write cycle.
CE0#, CE1#	INPUT	<b>CHIP ENABLE</b> : Activates the device's control logic, input buffers decoders, and sense amplifiers. Either CE0# or CE1# V <sub>IH</sub> deselected the device and reduces power consumption to standby levels. Both CE0# and CE1# must be V <sub>IL</sub> to select the devices.
RP#	INPUT	<b>RESET/DEEP POWER-DOWN</b> : Puts the device in deep power-down mode and resets internal automation. RP# V <sub>IH</sub> enables normal operation. When driven V <sub>IL</sub> , RP# inhibits write operations which provide data protection during power transitions. Exit from deep power-down sets the device to read array mode.
OE#	INPUT	<b>OUTPUT ENABLE</b> : Gates the device's outputs during a read cycle.
WE#	INPUT	<b>WRITE ENABLE</b> : Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of the WE# pulse.
STS	OPEN DRAIN OUTPUT	<b>STS (RY/BY#)</b> : Indicates the status of the internal WSM. When configured in level mode (default mode), it acts as a RY/BY# pin. When low, the WSM is performing an internal operation (block erase, full chip erase, (multi) word/byte write or block lock-bit configuration). STS High Z indicates that the WSM is ready for new commands, block erase is suspended, and (multi) word/byte write is inactive, (multi) word/byte write is suspended or the device is in deep power-down mode. For alternate configurations of the STATUS pin, see the Configuration command ( <b>Table 3</b> and <b>Section 4.14</b> ).
WP#	INPUT	<b>WRITE PROTECT</b> : Master control for block locking. When V <sub>IL</sub> , locked blocks can not be erased and programmed, and block lock-bits can not be set and reset.
BYTE#	INPUT	<b>BYTE ENABLE</b> : BYTE# V <sub>IL</sub> places device in x8 mode. All data are then input or output on DQ0-7, and DQ8-15 float. BYTE# V <sub>IH</sub> places the device in x16 mode, and turns off the A0 input buffer.
V <sub>PP</sub>	SUPPLY	<b>BLOCK ERASE, FULL CHIP ERASE, (MULTI) WORD/BYTE WRITE, BLOCK LOCK-BIT CONFIGURATION POWER SUPPLY</b> : For erasing array blocks, writing bytes or configuring block lock-bits. With V <sub>PP</sub> ≤ V <sub>PLK</sub> , memory contents cannot be altered. Block erase, full chip erase, (multi) word/byte write and block lock-bit configuration with an invalid V <sub>PP</sub> (see <b>Section 6.2.3 "DC CHARACTERISTICS"</b> ) produce spurious results and should not be attempted.
V <sub>CC</sub>	SUPPLY	<b>DEVICE POWER SUPPLY</b> : Internal detection configures the device for 5 V operation. Do not float any power pins. With V <sub>CC</sub> ≤ V <sub>LKO</sub> , all write attempts to the flash memory are inhibited. Device operations at invalid V <sub>CC</sub> voltage (see <b>Section 6.2.3 "DC CHARACTERISTICS"</b> ) produce spurious results and should not be attempted.
GND	SUPPLY	<b>GROUND</b> : Do not float any ground pins.
NC		<b>NO CONNECT</b> : Lead is not internal connected; recommend to be floated.

## 1 INTRODUCTION

This datasheet contains LH28F160S5-L/S5H-L specifications. Section 1 provides a flash memory overview. Sections 2, 3, 4, and 5 describe the memory organization and functionality. Section 6 covers electrical specifications. LH28F160S5-L/S5H-L flash memories documentation also includes ordering information which is referenced in Section 7.

### 1.1 Product Overview

The LH28F160S5-L/S5H-L are high-performance 16 M-bit Smart 5 flash memories organized as 2 MB x 8/1 MB x 16. The 2 MB of data is arranged in thirty-two 64 k-byte blocks which are individually erasable, lockable, and unlockable in-system. The memory map is shown in **Fig.1**.

Smart 5 technology provides a choice of V<sub>CC</sub> and V<sub>PP</sub> combination, as shown in **Table 1**, to meet system performance and power expectations. V<sub>PP</sub> at 5 V eliminates the need for a separate 12 V converter, while V<sub>PP</sub> = 5 V maximizes erase and write performance. In addition to flexible erase and program voltages, the dedicated V<sub>PP</sub> pin gives complete data protection when V<sub>PP</sub> ≤ V<sub>PPLK</sub>.

**Table 1 V<sub>CC</sub> and V<sub>PP</sub> Voltage Combination Offered by Smart 5 Technology**

V <sub>CC</sub> VOLTAGE	V <sub>PP</sub> VOLTAGE
5 V	5 V

Internal V<sub>CC</sub> and V<sub>PP</sub> detection circuitry automatically configures the device for optimized read and write operations.

A Command User Interface (CUI) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase, full chip erase, (multi)

word/byte write and block lock-bit configuration operations.

A block erase operation erases one of the device's 64 k-byte blocks typically within 0.34 second (5 V V<sub>CC</sub>, 5 V V<sub>PP</sub>) independent of other blocks. Each block can be independently erased 100 000 times (3.2 million block erases per device). Block erase suspend mode allows system software to suspend block erase to read data from, or write data to any other block.

A word/byte write is performed in byte increments typically within 9.24 μs (5 V V<sub>CC</sub>, 5 V V<sub>PP</sub>). A multi word/byte write has high speed write performance of 2 μs/byte (5 V V<sub>CC</sub>, 5 V V<sub>PP</sub>). (Multi) word/byte write suspend mode enables the system to read data from, or write data to any other flash memory array location.

Individual block locking uses a combination of bits and WP#, thirty-two block lock-bits, to lock and unlock blocks. Block lock-bits gate block erase, full chip erase and (multi) word/byte write operations. Block lock-bit configuration operations (Set Block Lock-Bit and Clear Block Lock-Bits commands) set and cleared block lock-bits.

The status register indicates when the WSM's block erase, full chip erase, (multi) word/byte write or block lock-bit configuration operation is finished.

The STS output gives an additional indicator of WSM activity by providing both a hardware signal of status (versus software polling) and status masking (interrupt masking for background block erase, for example). Status polling using STS minimizes both CPU overhead and system power consumption. STS pin can be configured to different states using the Configuration command. The STS pin defaults to RY/BY# operation. When low, STS indicates that the WSM is performing a

block erase, full chip erase, (multi) word/byte write or block lock-bit configuration. STS High Z indicates that the WSM is ready for a new command, block erase is suspended and (multi) word/byte write are inactive, (multi) word/byte write are suspended, or the device is in deep power-down mode. The other 3 alternate configurations are all pulse mode for use as a system interrupt.

The access time is 70 ns ( $t_{AVQV}$ ) at the  $V_{CC}$  supply voltage range of 4.75 to 5.25 V over the temperature range, 0 to +70°C (LH28F160S5-L)/-40 to +85°C (LH28F160S5H-L). At 4.5 to 5.5 V  $V_{CC}$ , the access time is 80 ns/100 ns (LH28F160S5-L70/S5-L10) or 90 ns/100 ns (LH28F160S5H-L70/S5H-L10).

The Automatic Power Saving (APS) feature substantially reduces active current when the device is in static mode (addresses not switching). In APS mode, the typical  $I_{CCR}$  current is 1 mA at 5 V  $V_{CC}$ .

When either  $CE_0\#$  or  $CE_1\#$ , and  $RP\#$  pins are at  $V_{CC}$ , the  $I_{CC}$  CMOS standby mode is enabled. When the  $RP\#$  pin is at GND, deep power-down mode is enabled which minimizes power consumption and provides write protection during reset. A reset time ( $t_{PHQV}$ ) is required from  $RP\#$  switching high until outputs are valid. Likewise, the device has a wake time ( $t_{PHEL}$ ) from  $RP\#$ -high until writes to the CUI are recognized. With  $RP\#$  at GND, the WSM is reset and the status register is cleared.

1FFFFF	64 k-Byte Block	31
1F0000	64 k-Byte Block	30
1EFFFF	64 k-Byte Block	29
1E0000	64 k-Byte Block	28
1DFFFF	64 k-Byte Block	27
1D0000	64 k-Byte Block	26
1CFFFF	64 k-Byte Block	25
1C0000	64 k-Byte Block	24
1BFFFF	64 k-Byte Block	23
1B0000	64 k-Byte Block	22
1AFFFF	64 k-Byte Block	21
1A0000	64 k-Byte Block	20
19FFFF	64 k-Byte Block	19
190000	64 k-Byte Block	18
18FFFF	64 k-Byte Block	17
180000	64 k-Byte Block	16
17FFFF	64 k-Byte Block	15
170000	64 k-Byte Block	14
16FFFF	64 k-Byte Block	13
160000	64 k-Byte Block	12
15FFFF	64 k-Byte Block	11
150000	64 k-Byte Block	10
14FFFF	64 k-Byte Block	9
140000	64 k-Byte Block	8
13FFFF	64 k-Byte Block	7
130000	64 k-Byte Block	6
12FFFF	64 k-Byte Block	5
120000	64 k-Byte Block	4
11FFFF	64 k-Byte Block	3
110000	64 k-Byte Block	2
10FFFF	64 k-Byte Block	1
100000	64 k-Byte Block	0
0FFFFF	64 k-Byte Block	31
0F0000	64 k-Byte Block	30
0EFFFF	64 k-Byte Block	29
0E0000	64 k-Byte Block	28
0DFFFF	64 k-Byte Block	27
0D0000	64 k-Byte Block	26
0CFFFF	64 k-Byte Block	25
0C0000	64 k-Byte Block	24
0BFFFF	64 k-Byte Block	23
0B0000	64 k-Byte Block	22
0AFFFF	64 k-Byte Block	21
0A0000	64 k-Byte Block	20
09FFFF	64 k-Byte Block	19
090000	64 k-Byte Block	18
08FFFF	64 k-Byte Block	17
080000	64 k-Byte Block	16
07FFFF	64 k-Byte Block	15
070000	64 k-Byte Block	14
06FFFF	64 k-Byte Block	13
060000	64 k-Byte Block	12
05FFFF	64 k-Byte Block	11
050000	64 k-Byte Block	10
04FFFF	64 k-Byte Block	9
040000	64 k-Byte Block	8
03FFFF	64 k-Byte Block	7
030000	64 k-Byte Block	6
02FFFF	64 k-Byte Block	5
020000	64 k-Byte Block	4
01FFFF	64 k-Byte Block	3
010000	64 k-Byte Block	2
00FFFF	64 k-Byte Block	1
000000	64 k-Byte Block	0

Fig. 1 Memory Map

## 2 PRINCIPLES OF OPERATION

The LH28F160S5-L/S5H-L flash memories include an on-chip WSM to manage block erase, full chip erase, (multi) word/byte write and block lock-bit configuration functions. It allows for : 100% TTL-level control inputs, fixed power supplies during block erase, full chip erase, (multi) word/byte write and block lock-bit configuration, and minimal processor overhead with RAM-like interface timings.

After initial device power-up or return from deep power-down mode (see **Table 2.1** and **Table 2.2 "Bus Operations"**), the device defaults to read array mode. Manipulation of external memory control pins allow array read, standby, and output disable operations.

Status register, query structure and identifier codes can be accessed through the CUI independent of the VPP voltage. High voltage on VPP enables successful block erase, full chip erase, (multi) word/byte write and block lock-bit configuration. All functions associated with altering memory contents—block erase, full chip erase, (multi) word/byte write and block lock-bit configuration, status, query and identifier codes—are accessed via the CUI and verified through the status register.

Commands are written using standard micro-processor write timings. The CUI contents serve as input to the WSM, which controls the block erase, full chip erase, (multi) word/byte write and block lock-bit configuration. The internal algorithms are regulated by the WSM, including pulse repetition, internal verification, and margining of data. Addresses and data are internally latched during write cycles. Writing the appropriate command outputs array data, accesses the identifier codes, outputs query structure or outputs status register data.

Interface software that initiates and polls progress of block erase, full chip erase, (multi) word/byte write and block lock-bit configuration can be stored in any block. This code is copied to and executed from system RAM during flash memory updates. After successful completion, reads are again possible via the Read Array command. Block erase suspend allows system software to suspend a block erase to read/write data from/to blocks other than that which is suspended. Write suspend allows system software to suspend a (multi) word/byte write to read data from any other flash memory array location.

### 2.1 Data Protection

Depending on the application, the system designer may choose to make the VPP power supply switchable (available only when block erase, full chip erase, (multi) word/byte write and block lock-bit configuration are required) or hardwired to VPPH1. The device accommodates either design practice and encourages optimization of the processor-memory interface.

When  $V_{PP} \leq V_{PPLK}$ , memory contents cannot be altered. The CUI, with multi-step block erase, full chip erase, (multi) word/byte write and block lock-bit configuration command sequences, provides protection from unwanted operations even when high voltage is applied to VPP. All write functions are disabled when VCC is below the write lockout voltage VLKO or when RP# is at VIL. The device's block locking capability provides additional protection from inadvertent code or data alteration by gating block erase, full chip erase and (multi) word/byte write operations.



### 3 BUS OPERATION

The local CPU reads and writes flash memory in-system. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

#### 3.1 Read

Information can be read from any block, identifier codes, query structure, or status register independent of the  $V_{PP}$  voltage.  $RP\#$  must be at  $V_{IH}$ .

The first task is to write the appropriate read mode command (Read Array, Read Identifier Codes, Query or Read Status Register) to the CUI. Upon initial device power-up or after exit from deep power-down mode, the device automatically resets to read array mode. Five control pins dictate the data flow in and out of the component :  $CE\#$  ( $CE0\#$ ,  $CE1\#$ ),  $OE\#$ ,  $WE\#$ ,  $RP\#$  and  $WP\#$ .  $CE0\#$ ,  $CE1\#$  and  $OE\#$  must be driven active to obtain data at the outputs.  $CE0\#$  and  $CE1\#$  are the device selection control, and when active enables the selected memory device.  $OE\#$  is the data output ( $DQ0$ - $DQ15$ ) control and when active drives the selected memory data onto the I/O bus.  $WE\#$  and  $RP\#$  must be at  $V_{IH}$ . **Fig. 15** and **Fig. 16**, illustrate a read cycle.

#### 3.2 Output Disable

With  $OE\#$  at a logic-high level ( $V_{IH}$ ), the device outputs are disabled. Output pins  $DQ0$ - $DQ15$  are placed in a high-impedance state.

#### 3.3 Standby

Either  $CE0\#$  or  $CE1\#$  at a logic-high level ( $V_{IH}$ ) places the device in standby mode which substantially reduces device power consumption.  $DQ0$ - $DQ15$  outputs are placed in a high-impedance state independent of  $OE\#$ . If deselected during block erase, full chip erase, (multi) word/byte write and block lock-bit configuration, the device continues functioning, and consuming active power until the operation completes.

#### 3.4 Deep Power-Down

$RP\#$  at  $V_{IL}$  initiates the deep power-down mode.

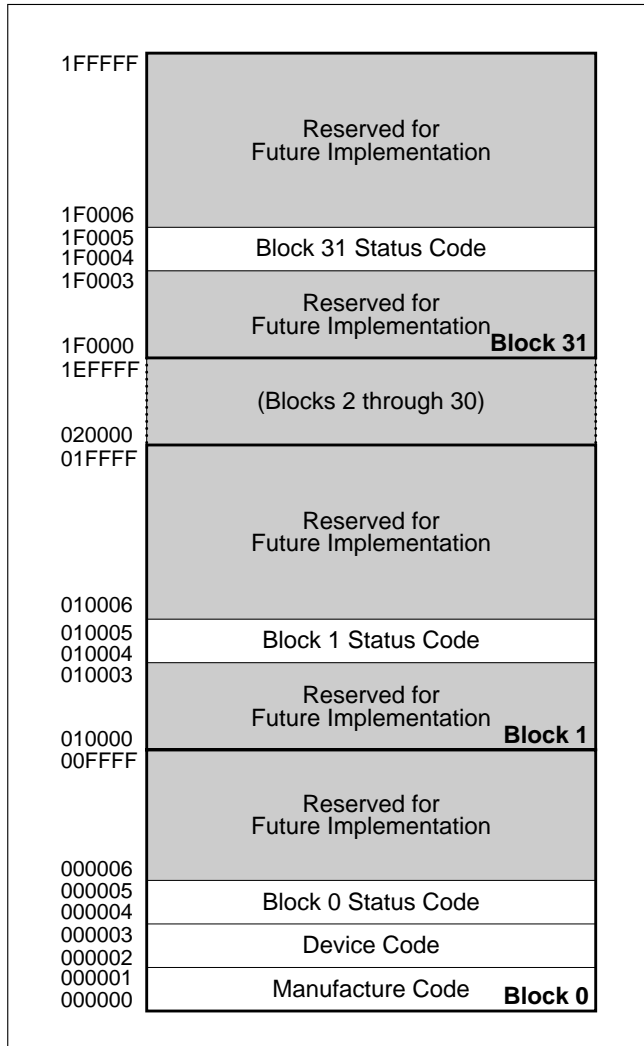
In read modes,  $RP\#$ -low deselects the memory, places output drivers in a high-impedance state and turns off all internal circuits.  $RP\#$  must be held low for a minimum of 100 ns. Time  $t_{PHQV}$  is required after return from power-down until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI is reset to read array mode and status register is set to 80H.

During block erase, full chip erase, (multi) word/byte write or block lock-bit configuration modes,  $RP\#$ -low will abort the operation.  $STS$  remains low until the reset operation is complete. Memory contents being altered are no longer valid; the data may be partially erased or written. Time  $t_{PHWL}$  is required after  $RP\#$  goes to logic-high ( $V_{IH}$ ) before another command can be written.

As with any automated device, it is important to assert  $RP\#$  during system reset. When the system comes out of reset, it expects to read from the flash memory. Automated flash memories provide status information when accessed during block erase, full chip erase, (multi) word/byte write and block lock-bit configuration. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. SHARP's flash memories allow proper CPU initialization following a system reset through the use of the  $RP\#$  input. In this application,  $RP\#$  is controlled by the same  $RESET\#$  signal that resets the system CPU.

### 3.5 Read Identifier Codes Operation

The read identifier codes operation outputs the manufacture code, device code, block status codes for each block (see **Fig. 2**). Using the manufacture and device codes, the system CPU can automatically match the device with its proper algorithms. The block status codes identify locked or unlocked block setting and erase completed or erase uncompleted condition.



**Fig. 2 Device Identifier Code Memory Map**

### 3.6 Query Operation

The query operation outputs the query structure. Query database is stored in the 48-byte ROM. Query structure allows system software to gain critical information for controlling the flash

component. Query structures are always presented on the lowest-order data output (DQ0-DQ7) only.

### 3.7 Write

Writing commands to the CUI enable reading of device data and identifier codes. They also control inspection and clearing of the status register. When  $V_{CC} = V_{CC1/2}$  and  $V_{PP} = V_{PPH1}$ , the CUI additionally controls block erase, full chip erase, (multi) word/byte write and block lock-bit configuration.

The Block Erase command requires appropriate command data and an address within the block to be erased. The Word/Byte Write command requires the command and address of the location to be written. Set Block Lock-Bit command requires the command and block address within the device (Block Lock) to be locked. The Clear Block Lock-Bits command requires the command and address within the device.

The CUI does not occupy an addressable memory location. It is written when  $WE\#$  and  $CE\#$  are active. The address and data needed to execute a command are latched on the rising edge of  $WE\#$  or  $CE\#$  (whichever goes high first). Standard microprocessor write timings are used. **Fig. 17** and **Fig. 18** illustrate  $WE\#$  and  $CE\#$ -controlled write operations.

## 4 COMMAND DEFINITIONS

When the  $V_{PP}$  voltage  $\leq V_{PPLK}$ , read operations from the status register, identifier codes, query, or blocks are enabled. Placing  $V_{PPH1}$  on  $V_{PP}$  enables successful block erase, full chip erase, (multi) word/byte write and block lock-bit configuration operations.

Device operations are selected by writing specific commands into the CUI. **Table 3** defines these commands.

Table 2.1 Bus Operations (BYTE# = VIH)

MODE	NOTE	RP#	CE0#	CE1#	OE#	WE#	ADDRESS	VPP	DQ0-15	STS
Read	1, 2, 3, 9	VIH	VIL	VIL	VIL	VIH	X	X	DOUT	X
Output Disable	3	VIH	VIL	VIL	VIH	VIH	X	X	High Z	X
Standby	3	VIH	VIH VIL	VIH VIH	X	X	X	X	High Z	X
Deep Power-Down	4	VIL	X	X	X	X	X	X	High Z	High Z
Read Identifier Codes	9	VIH	VIL	VIL	VIL	VIH	See Fig. 2	X	(NOTE 5)	High Z
Query	9	VIH	VIL	VIL	VIL	VIH	See Table 6 through 10	X	(NOTE 6)	High Z
Write	3, 7, 8, 9	VIH	VIL	VIL	VIH	VIL	X	X	DIN	X

Table 2.2 Bus Operations (BYTE# = VIL)

MODE	NOTE	RP#	CE0#	CE1#	OE#	WE#	ADDRESS	VPP	DQ0-7	STS
Read	1, 2, 3, 9	VIH	VIL	VIL	VIL	VIH	X	X	DOUT	X
Output Disable	3	VIH	VIL	VIL	VIH	VIH	X	X	High Z	X
Standby	3	VIH	VIH VIL	VIH VIH	X	X	X	X	High Z	X
Deep Power-Down	4	VIL	X	X	X	X	X	X	High Z	High Z
Read Identifier Codes	9	VIH	VIL	VIL	VIL	VIH	See Fig. 2	X	(NOTE 5)	High Z
Query	9	VIH	VIL	VIL	VIL	VIH	See Table 6 through 10	X	(NOTE 6)	High Z
Write	3, 7, 8, 9	VIH	VIL	VIL	VIH	VIL	X	X	DIN	X

**NOTES :**

1. Refer to **Section 6.2.3 "DC CHARACTERISTICS"**. When  $V_{PP} \leq V_{PPLK}$ , memory contents can be read, but not altered.
2. X can be VIL or VIH for control pins and addresses, and VPPLK or VPPH1 for VPP. See **Section 6.2.3 "DC CHARACTERISTICS"** for VPPLK and VPPH1 voltages.
3. STS is VOL (if configured to RY/BY# mode) when the WSM is executing internal block erase, full chip erase, (multi) word/byte write or block lock-bit configuration algorithms. It is floated during when the WSM is not busy, in block erase suspend mode with (multi) word/byte write inactive, (multi) word/byte write suspend mode, or deep power-down mode.
4. RP# at  $GND \pm 0.2$  V ensures the lowest deep power-down current.
5. See **Section 4.2** for read identifier code data.
6. See **Section 4.5** for query data.
7. Command writes involving block erase, full chip erase, (multi) word/byte write or block lock-bit configuration are reliably executed when  $V_{PP} = V_{PPH1}$  and  $V_{CC} = V_{CC1/2}$ .
8. Refer to **Table 3** for valid DIN during a write operation.
9. Don't use the timing both OE# and WE# are VIL.

Table 3 Command Definitions (NOTE 10)

COMMAND	BUS CYCLES REQ'D.	NOTE	FIRST BUS CYCLE			SECOND BUS CYCLE		
			Oper (NOTE 1)	Addr (NOTE 2)	Data (NOTE 3)	Oper (NOTE 1)	Addr (NOTE 2)	Data (NOTE 3)
Read Array/Reset	1		Write	X	FFH			
Read Identifier Codes	≥ 2	4	Write	X	90H	Read	IA	ID
Query	≥ 2		Write	X	98H	Read	QA	QD
Read Status Register	2		Write	X	70H	Read	X	SRD
Clear Status Register	1		Write	X	50H			
Block Erase Setup/Confirm	2	5	Write	BA	20H	Write	BA	D0H
Full Chip Erase Setup/Confirm	2		Write	X	30H	Write	X	D0H
Word/Byte Write Setup/Write	2	5, 6	Write	WA	40H	Write	WA	WD
Alternate Word/Byte Write Setup/Write	2	5, 6	Write	WA	10H	Write	WA	WD
Multi Word/Byte Write Setup/Confirm	≥ 4	9	Write	WA	E8H	Write	WA	N-1
Block Erase and (Multi) Word/Byte Write Suspend	1	5	Write	X	B0H			
Confirm and Block Erase and (Multi) Word/Byte Write Resume	1	5	Write	X	D0H			
Block Lock-Bit Set Setup/Confirm	2	7	Write	BA	60H	Write	BA	01H
Block Lock-Bit Reset Setup/Confirm	2	8	Write	X	60H	Write	X	D0H
STS Configuration Level-Mode for Erase and Write (RY/BY# Mode)	2		Write	X	B8H	Write	X	00H
STS Configuration Pulse-Mode for Erase	2		Write	X	B8H	Write	X	01H
STS Configuration Pulse-Mode for Write	2		Write	X	B8H	Write	X	02H
STS Configuration Pulse-Mode for Erase and Write	2		Write	X	B8H	Write	X	03H

**NOTES :**

- Bus operations are defined in **Table 2.1** and **Table 2.2**.
- X = Any valid address within the device.  
IA = Identifier code address : see **Fig. 2**.  
QA = Query offset address.  
BA = Address within the block being erased or locked.  
WA = Address of memory location to be written.
- SRD = Data read from status register. See **Table 13.1** for a description of the status register bits.  
WD = Data to be written at location WA. Data is latched on the rising edge of WE# or CE# (whichever goes high first).  
ID = Data read from identifier codes.  
QD = Data read from query database.
- Following the Read Identifier Codes command, read operations access manufacture, device and block status codes. See **Section 4.2** for read identifier code data.
- If the block is locked, WP# must be at V<sub>IH</sub> to enable block erase or (multi) word/byte write operations. Attempts to issue a block erase or (multi) word/byte write to a locked block while RP# is V<sub>IH</sub>.
- Either 40H or 10H is recognized by the WSM as the byte write setup.
- A block lock-bit can be set while WP# is V<sub>IH</sub>.
- WP# must be at V<sub>IH</sub> to clear block lock-bits. The clear block lock-bits operation simultaneously clears all block lock-bits.
- Following the Third Bus Cycle, inputs the write address and write data of "N" times. Finally, input the confirm command "D0H".
- Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

## 4.1 Read Array Command

Upon initial device power-up and after exit from deep power-down mode, the device defaults to read array mode. This operation is also initiated by writing the Read Array command. The device remains enabled for reads until another command is written. Once the internal WSM has started a block erase, full chip erase, (multi) word/byte write or block lock-bit configuration, the device will not recognize the Read Array command until the WSM completes its operation unless the WSM is suspended via an Erase Suspend and (Multi) Word/Byte Write Suspend command. The Read Array command functions independently of the V<sub>PP</sub> voltage and RP# must be V<sub>IH</sub>.

## 4.2 Read Identifier Codes Command

The identifier code operation is initiated by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in **Fig. 2** retrieve the manufacture, device, block lock configuration and block erase status (see **Table 4** for identifier code values). To terminate the operation, write another valid command. Like the Read Array command, the Read Identifier Codes command functions independently of the V<sub>PP</sub> voltage and RP# must be V<sub>IH</sub>. Following the Read Identifier Codes command, the following information can be read :

**Table 4 Identifier Codes**

CODE	ADDRESS	DATA
Manufacture Code	00000H 00001H	B0
Device Code	00002H 00003H	D0
Block Status Code	X0004H (NOTE 1) X0005H (NOTE 1)	
•Block is Unlocked		DQ <sub>0</sub> = 0
•Block is Locked		DQ <sub>0</sub> = 1
•Last erase operation completed successfully		DQ <sub>1</sub> = 0
•Last erase operation did not completed successfully		DQ <sub>1</sub> = 1
•Reserved for Future Use		DQ <sub>2-7</sub>

### NOTE :

1. X selects the specific block status code to be read. See **Fig. 2** for the device identifier code memory map.

## 4.3 Read Status Register Command

The status register may be read to determine when a block erase, full chip erase, (multi) word/byte write or block lock-bit configuration is complete and whether the operation completed successfully (see **Table 13.1**). It may be read at any time by writing the Read Status Register command. After writing this command, all subsequent read operations output data from the status register until another valid command is written. The status register contents are latched on the falling edge of OE# or CE# (Either CE<sub>0</sub># or CE<sub>1</sub>#), whichever occurs. OE# or CE# (Either CE<sub>0</sub># or CE<sub>1</sub>#) must toggle to V<sub>IH</sub> before further reads to update the status register latch. The Read Status Register command functions independently of the V<sub>PP</sub> voltage. RP# must be V<sub>IH</sub>.

The extended status register may be read to determine multi byte write availability (see **Table 13.2**). The extended status register may be read at any time by writing the Multi Byte Write command. After writing this command, all subsequent read operations output data from the extended status register, until another valid command is written. The contents of the extended status register are latched on the falling edge of OE# or CE# (Either CE<sub>0</sub># or CE<sub>1</sub>#), whichever occurs last in the read cycle. Multi Byte Write command must be re-issued to update the extended status register latch.

## 4.4 Clear Status Register Command

Status register bits SR.5, SR.4, SR.3 and SR.1 are set to "1"s by the WSM and can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see **Table 13.1**). By allowing system software to reset these bits, several operations (such as cumulatively erasing or locking multiple blocks or writing several bytes in

sequence) may be performed. The status register may be polled to determine if an error occurs during the sequence.

To clear the status register, the Clear Status Register command (50H) is written. It functions independently of the applied VPP voltage. RP# must be VIH. This command is not functional during block erase, full chip erase, (multi) word/byte write, block lock-bit configuration, block erase suspend or (multi) word/byte write suspend modes.

## 4.5 Query Command

Query database can be read by writing Query command (98H). Following the command write, read cycle from address shown in **Table 6 through Table 10** retrieve the critical information to write, erase and otherwise control the flash component. A0 of query offset address is ignored when x8 mode (BYTE# = VL).

Query data are always presented on the low-byte data output (DQ0-DQ7). In x16 mode, high-byte (DQ8-DQ15) outputs 00H. The bytes not assigned

to any information or reserved for future use are set to "0". This command functions independently of the VPP voltage. RP# must be VIH.

**Table 5 Example of Query Structure Output**

MODE	OFFSET ADDRESS	OUTPUT	
		DQ15-8	DQ7-0
x8 mode	A5, A4, A3, A2, A1, A0 1, 0, 0, 0, 0, 0 (20H)	High Z	"Q"
	1, 0, 0, 0, 0, 1 (21H)	High Z	"Q"
	1, 0, 0, 0, 1, 0 (22H)	High Z	"R"
	1, 0, 0, 0, 1, 1 (23H)	High Z	"R"
x16 mode	A5, A4, A3, A2, A1 1, 0, 0, 0, 0 (10H)	00H	"Q"
	1, 0, 0, 0, 1 (11H)	00H	"R"

### 4.5.1 BLOCK STATUS REGISTER

This field provides lock configuration and erase status for the specified block. These informations are only available when device is ready (SR.7 = 1). If block erase or full chip erase operation is finished irregularly, block erase status bit will be set to "1". If bit 1 is "1", this block is invalid.

**Table 6 Query Block Status Register**

OFFSET (Word Address)	LENGTH	DESCRIPTION
(BA+2)H	01H	Block Status Register bit0 Block Lock Configuration 0 = Block is unlocked 1 = Block is locked bit1 Block Erase Status 0 = Last erase operation completed successfully 1 = Last erase operation not completed successfully bit2-7 Reserved for future use

#### NOTE :

BA = The beginning of a Block Address.

#### 4.5.2 CFI QUERY IDENTIFICATION STRING

The identification string provides verification that the component supports the Common Flash Interface specification. Additionally, it indicates which version

of the spec and which vendor-specified command set(s) is(are) supported.

**Table 7 CFI Query Identification String**

OFFSET (Word Address)	LENGTH	DESCRIPTION
10H, 11H, 12H	03H	Query Unique ASCII string "QRY" 51H, 52H, 59H
13H, 14H	02H	Primary Vendor Command Set and Control Interface ID Code 01H, 00H (SCS ID Code)
15H, 16H	02H	Address for Primary Algorithm Extended Query Table 31H, 00H (SCS Extended Query Table Offset)
17H, 18H	02H	Alternate Vendor Command Set and Control Interface ID Code 0000H (0000H means that no alternate exists)
19H, 1AH	02H	Address for Alternate Algorithm Extended Query Table 0000H (0000H means that no alternate exists)

#### 4.5.3 SYSTEM INTERFACE INFORMATION

The following device information can be useful in optimizing system interface software.

**Table 8 System Information String**

OFFSET (Word Address)	LENGTH	DESCRIPTION
1BH	01H	Vcc Logic Supply Minimum Write/Erase voltage 27H (2.7 V)
1CH	01H	Vcc Logic Supply Maximum Write/Erase voltage 55H (5.5 V)
1DH	01H	VPP Programming Supply Minimum Write/Erase voltage 27H (2.7 V)
1EH	01H	VPP Programming Supply Maximum Write/Erase voltage 55H (5.5 V)
1FH	01H	Typical Time-Out per Single Byte/Word Write 03H ( $2^3 = 8 \mu\text{s}$ )
20H	01H	Typical Time-Out for Maximum Size Buffer Write (32 Bytes) 06H ( $2^6 = 64 \mu\text{s}$ )
21H	01H	Typical Time-Out per Individual Block Erase 0AH (0AH = 10, $2^{10} = 1\ 024 \text{ ms}$ )
22H	01H	Typical Time-Out for Full Chip Erase 0FH (0FH = 15, $2^{15} = 32\ 768 \text{ ms}$ )
23H	01H	Maximum Time-Out per Single Byte/Word Write, $2^N$ times of typical. 04H ( $2^4 = 16, 8 \mu\text{s} \times 16 = 128 \mu\text{s}$ )
24H	01H	Maximum Time-Out per Maximum Size Buffer Write, $2^N$ times of typical. 04H ( $2^4 = 16, 64 \mu\text{s} \times 16 = 1\ 024 \mu\text{s}$ )
25H	01H	Maximum Time-Out per Individual Block Erase, $2^N$ times of typical. 04H ( $2^4 = 16, 1\ 024 \text{ ms} \times 16 = 16\ 384 \text{ ms}$ )
26H	01H	Maximum Time-Out for Full Chip Erase, $2^N$ times of typical. 04H ( $2^4 = 16, 32\ 768 \text{ ms} \times 16 = 524\ 288 \text{ ms}$ )

#### 4.5.4 DEVICE GEOMETRY DEFINITION

This field provides critical details of the flash device geometry.

**Table 9 Device Geometry Definition**

OFFSET (Word Address)	LENGTH	DESCRIPTION
27H	01H	Device Size 15H (15H = 21, $2^{21} = 2\,097\,152 = 2\text{ M Bytes}$ )
28H, 29H	02H	Flash Device Interface Description 02H, 00H (x8/x16 supports x8 and x16 via BYTE#)
2AH, 2BH	02H	Maximum Number of Bytes in Multi Word/Byte Write 05H, 00H ( $2^5 = 32\text{ Bytes}$ )
2CH	01H	Number of Erase Block Regions within Device 01H (symmetrically blocked)
2DH, 2EH	02H	The Number of Erase Blocks 1FH, 00H (1FH = 31 $\Rightarrow$ 31 + 1 = 32 Blocks)
2FH, 30H	02H	The Number of "256 Bytes" cluster in a Erase Block 00H, 01H (0100H = 256 $\Rightarrow$ 256 Bytes x 256 = 64k Bytes in a Erase Block)



#### 4.5.5 SCS OEM SPECIFIC EXTENDED QUERY TABLE

Certain flash features and commands may be optional in a vendor-specific algorithm specification. The optional vendor-specific query table(s) may be

used to specify this and other types of information. These structures are defined solely by the flash vendor(s).

**Table 10 SCS OEM Specific Extended Query Table**

OFFSET (Word Address)	LENGTH	DESCRIPTION
31H, 32H, 33H	03H	PRI 50H, 52H, 49H
34H	01H	31H (1) Major Version Number , ASCII
35H	01H	30H (0) Minor Version Number, ASCII
36H, 37H, 38H, 39H	04H	0FH, 00H, 00H, 00H Optional Command Support bit0 = 1 : Chip Erase Supported bit1 = 1 : Suspend Erase Supported bit2 = 1 : Suspend Write Supported bit3 = 1 : Lock/Unlock Supported bit4 = 0 : Queued Erase Not Supported bit5-31 = 0 : Reserved for future use
3AH	01H	01H Supported Functions after Suspend bit0 = 1 : Write Supported after Erase Suspend bit1-7 = 0 : Reserved for future use
3BH, 3CH	02H	03H, 00H Block Status Register Mask bit0 = 1 : Block Status Register Lock Bit [BSR.0] active bit1 = 1 : Block Status Register Valid Bit [BSR.1] active bit2-15 = 0 : Reserved for future use
3DH	01H	Vcc Logic Supply Optimum Write/Erase voltage (highest performance) 50H (5.0 V)
3EH	01H	VPP Programming Supply Optimum Write/Erase voltage (highest performance) 50H (5.0 V)
3FH	reserved	Reserved for future versions of the SCS specification

## 4.6 Block Erase Command

Block erase is executed one block at a time and initiated by a two-cycle command. A block erase setup is first written, followed by a block erase confirm. This command sequence requires appropriate sequencing and an address within the block to be erased (erase changes all block data to FFH). Block preconditioning, erase and verify are handled internally by the WSM (invisible to the system). After the two-cycle block erase sequence is written, the device automatically outputs status register data when read (see **Fig. 3**). The CPU can detect block erase completion by analyzing the output data of the STS pin or status register bit SR.7.

When the block erase is complete, status register bit SR.5 should be checked. If a block erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1". Also, reliable block erasure can only occur when  $V_{CC} = V_{CC1/2}$  and  $V_{PP} = V_{PPH1}$ . In the absence of this high voltage, block contents are protected against erasure. If block erase is attempted while  $V_{PP} \leq V_{PPLK}$ , SR.3 and SR.5 will be set to "1". Successful block erase requires that the corresponding block lock-bit be cleared or if set, that  $WP\# = V_{IH}$ . If block erase is attempted when the corresponding block lock-bit is set and  $WP\# = V_{IL}$ , SR.1 and SR.5 will be set to "1".

## 4.7 Full Chip Erase Command

This command followed by a confirm command (D0H) erases all of the unlocked blocks. A full chip erase setup is first written, followed by a full chip erase confirm. After a confirm command is written, device erases the all unlocked blocks from block 0 to block 31 block by block. This command sequence requires appropriate sequencing. Block preconditioning, erase and verify are handled internally by the WSM (invisible to the system). After the two-cycle full chip erase sequence is written, the device automatically outputs status register data when read (see **Fig. 4**). The CPU can detect full chip erase completion by analyzing the output data of the STS pin or status register bit SR.7.

When the full chip erase is complete, status register bit SR.5 should be checked. If erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued. If error is detected on a block during full chip erase operation, WSM stops erasing. Reading the block valid status by issuing Read ID Codes command or Query command informs which blocks failed to its erase.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Full Chip Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1". Also, reliable full chip erasure can only occur when  $V_{CC} = V_{CC1/2}$  and  $V_{PP} = V_{PPH1}$ . In the absence of this high voltage, block contents are protected against erasure. If full chip erase is attempted while  $V_{PP} \leq V_{PPLK}$ , SR.3 and SR.5 will be set to "1". When  $WP\# = V_{IH}$ , all blocks are erased independent of block lock-bits status. When  $WP\# = V_{IL}$ , only unlocked blocks are erased. In this case, SR.1 and SR.4 will not be set to "1". Full chip erase can not be suspended.

## 4.8 Word/Byte Write Command

Word/byte write is executed by a two-cycle command sequence. Word/Byte Write setup (standard 40H or alternate 10H) is written, followed by a second write that specifies the address and data (latched on the rising edge of WE#). The WSM then takes over, controlling the word/byte write and write verify algorithms internally. After the word/byte write sequence is written, the device automatically outputs status register data when read (see Fig. 5). The CPU can detect the completion of the word/byte write event by analyzing the STS pin or status register bit SR.7.

When word/byte write is complete, status register bit SR.4 should be checked. If word/byte write error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully write to "0"s. The CUI remains in read status register mode until it receives another command.

Reliable word/byte writes can only occur when  $V_{CC} = V_{CC1/2}$  and  $V_{PP} = V_{PPH1}$ . In the absence of this high voltage, memory contents are protected against word/byte writes. If word/byte write is attempted while  $V_{PP} \leq V_{PPLK}$ , status register bits SR.3 and SR.4 will be set to "1". Successful word/byte write requires that the corresponding block lock-bit be cleared or, if set, that  $WP\# = V_{IH}$ . If word/byte write is attempted when the corresponding block lock-bit is set and  $WP\# = V_{IL}$ , SR.1 and SR.4 will be set to "1". Word/byte write operations with  $V_{IL} < WP\# < V_{IH}$  produce spurious results and should not be attempted.

## 4.9 Multi Word/Byte Write Command

Multi word/byte write is executed by at least four-cycle or up to 35-cycle command sequence. Up to 32 bytes in x8 mode (16 words in x16 mode) can be loaded into the buffer and written to the flash array. First, multi word/byte write setup (E8H) is written with the write address. At this point, the

device automatically outputs extended status register data (XSR) when read (see Fig. 6 and Fig. 7). If extended status register bit XSR.7 is 0, no Multi Word/Byte Write command is available and multi word/byte write setup which just has been written is ignored. To retry, continue monitoring XSR.7 by writing multi word/byte write setup with write address until XSR.7 transitions to "1". When XSR.7 transitions to "1", the device is ready for loading the data to the buffer. A word/byte count (N)-1 is written with write address. After writing a word/byte count (N)-1, the device automatically turns back to output status register data. The word/byte count (N)-1 must be less than or equal to 1FH in x8 mode (0FH in x16 mode). On the next write, device start address is written with buffer data. Subsequent writes provide additional device address and data, depending on the count. All subsequent address must lie within the start address plus the count. After the final buffer data is written, write confirm (D0H) must be written. This initiates WSM to begin copying the buffer data to the flash array. An invalid Multi Word/Byte Write command sequence will result in both status register bits SR.4 and SR.5 being set to "1". For additional multi word/byte write, write another multi word/byte write setup and check XSR.7. The Multi Word/Byte Write command can be queued while WSM is busy as long as XSR.7 indicates "1", because LH28F160S5-L/S5H-L have two buffers. If an error occurs while writing, the device will stop writing and flush next Multi Word/Byte Write command loaded in Multi Word/Byte Write command. Status register bit SR.4 will be set to "1". No Multi Word/Byte Write command is available if either SR.4 or SR.5 is set to "1". SR.4 and SR.5 should be cleared before issuing Multi Word/Byte Write command. If a Multi Word/Byte Write command is attempted past an erase block boundary, the device will write the data to flash array up to an erase block boundary and then stop writing. Status register bits SR.4 and SR.5 will be set to "1".

Reliable multi byte writes can only occur when  $V_{CC} = V_{CC1/2}$  and  $V_{PP} = V_{PPH1}$ . In the absence of this high voltage, memory contents are protected against multi word/byte writes. If multi word/byte write is attempted while  $V_{PP} \leq V_{PPLK}$ , status register bits SR.3 and SR.4 will be set to "1". Successful multi word/byte write requires that the corresponding block lock-bit be cleared or, if set, that  $WP\# = V_{IH}$ . If multi byte write is attempted when the corresponding block lock-bit is set and  $WP\# = V_{IL}$ , SR.1 and SR.4 will be set to "1".

#### 4.10 Block Erase Suspend Command

The Block Erase Suspend command allows block erase interruption to read or (multi) word/byte write data in another block of memory. Once the block erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. The device outputs status register data when read after the Block Erase Suspend command is written. Polling status register bits SR.7 and SR.6 can determine when the block erase operation has been suspended (both will be set to "1"). STS will also transition to High Z. Specification  $t_{WHRH2}$  defines the block erase suspend latency.

At this point, a Read Array command can be written to read data from blocks other than that which is suspended. A (Multi) Word/Byte Write command sequence can also be issued during erase suspend to program data in other blocks. Using the (Multi) Word/Byte Write Suspend command (see **Section 4.11**), a (multi) word/byte write operation can also be suspended. During a (multi) word/byte write operation with block erase suspended, status register bit SR.7 will return to "0" and the STS (if set to RY/BY#) output will transition to VOL. However, SR.6 will remain "1" to indicate block erase suspend status.

The only other valid commands while block erase is

suspended are Read Status Register and Block Erase Resume. After a Block Erase Resume command is written to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear and STS will return to VOL. After the Erase Resume command is written, the device automatically outputs status register data when read (see **Fig. 8**).  $V_{PP}$  must remain at  $V_{PPH1}$  (the same  $V_{PP}$  level used for block erase) while block erase is suspended.  $RP\#$  must also remain at  $V_{IH}$ . Block erase cannot resume until (multi) word/byte write operations initiated during block erase suspend have completed.

#### 4.11 (Multi) Word/Byte Write Suspend Command

The (Multi) Word/Byte Write Suspend command allows (multi) word/byte write interruption to read data in other flash memory locations. Once the (multi) word/byte write process starts, writing the (Multi) Word/Byte Write Suspend command requests that the WSM suspend the (multi) word/byte write sequence at a predetermined point in the algorithm. The device continues to output status register data when read after the (Multi) Word/Byte Write Suspend command is written. Polling status register bits SR.7 and SR.2 can determine when the (multi) word/byte write operation has been suspended (both will be set to "1"). STS will also transition to High Z. Specification  $t_{WHRH1}$  defines the (multi) word/byte write suspend latency.

At this point, a Read Array command can be written to read data from locations other than that which is suspended. The only other valid commands while (multi) word/byte write is suspended are Read Status Register and (Multi) Word/Byte Write Resume. After (Multi) Word/Byte Write Resume command is written to the flash memory, the WSM will continue the (multi) word/byte write process. Status register bits SR.2

and SR.7 will automatically clear and STS will return to VOL. After the (Multi) Word/Byte Write command is written, the device automatically outputs status register data when read (see **Fig. 9**). VPP must remain at VPPH1 (the same VPP level used for (multi) word/byte write) while in (multi) word/byte write suspend mode. WP# must also remain at VIH or VIL.

#### 4.12 Set Block Lock-Bit Command

A flexible block locking and unlocking scheme is enabled via block lock-bits. The block lock-bits gate program and erase operations. With WP# = VIH, individual block lock-bits can be set using the Set Block Lock-Bit command. See **Table 12** for a summary of hardware and software write protection options.

Set block lock-bit is executed by a two-cycle command sequence. The set block lock-bit setup along with appropriate block or device address is written followed by either the set block lock-bit confirm (and an address within the block to be locked). The WSM then controls the set block lock-bit algorithm. After the sequence is written, the device automatically outputs status register data when read (see **Fig. 10**). The CPU can detect the completion of the set block lock-bit event by analyzing the STS pin output or status register bit SR.7.

When the set block lock-bit operation is complete, status register bit SR.4 should be checked. If an error is detected, the status register should be cleared. The CUI will remain in read status register mode until a new command is issued.

This two-step sequence of set-up followed by execution ensures that block lock-bits are not accidentally set. An invalid Set Block Lock-Bit command will result in status register bits SR.4 and SR.5 being set to "1". Also, reliable operations occur only when  $V_{CC} = V_{CC1/2}$  and  $V_{PP} = V_{PPH1}$ . In

the absence of this high voltage, block lock-bit contents are protected against alteration.

A successful set block lock-bit operation requires WP# = VIH. If it is attempted with WP# = VIL, SR.1 and SR.4 will be set to "1" and the operation will fail. Set block lock-bit operations with WP# < VIH produce spurious results and should not be attempted.

#### 4.13 Clear Block Lock-Bits Command

All set block lock-bits are cleared in parallel via the Clear Block Lock-Bits command. With WP# = VIH, block lock-bits can be cleared using only the Clear Block Lock-Bits command. See **Table 12** for a summary of hardware and software write protection options.

Clear block lock-bits operation is executed by a two-cycle command sequence. A clear block lock-bits setup is first written. After the command is written, the device automatically outputs status register data when read (see **Fig. 11**). The CPU can detect completion of the clear block lock-bits event by analyzing the STS pin output or status register bit SR.7.

When the operation is complete, status register bit SR.5 should be checked. If a clear block lock-bits error is detected, the status register should be cleared. The CUI will remain in read status register mode until another command is issued.

This two-step sequence of set-up followed by execution ensures that block lock-bits are not accidentally cleared. An invalid Clear Block Lock-Bits command sequence will result in status register bits SR.4 and SR.5 being set to "1". Also, a reliable clear block lock-bits operation can only occur when  $V_{CC} = V_{CC1/2}$  and  $V_{PP} = V_{PPH1}$ . If a clear block lock-bits operation is attempted while  $V_{PP} \leq V_{PPLK}$ , SR.3 and SR.5 will be set to "1". In the absence of this high voltage, the block lock-bit contents are

protected against alteration. A successful clear block lock-bits operation requires  $WP\# = V_{IH}$ . If it is attempted with  $WP\# = V_{IL}$ , SR.1 and SR.5 will be set to "1" and the operation will fail. Clear block lock-bits operation with  $V_{IH} < RP\#$  produce spurious results and should not be attempted.

If a clear block lock-bits operation is aborted due to  $V_{PP}$  or  $V_{CC}$  transition out of valid range or  $RP\#$  active transition, block lock-bit values are left in an undetermined state. A repeat of clear block lock-bits is required to initialize block lock-bit contents to known values.

#### 4.14 STS Configuration Command

The Status (STS) pin can be configured to different states using the STS Configuration command. Once the STS pin has been configured, it remains in that configuration until another configuration command is issued, the device is powered down or  $RP\#$  is set to  $V_{IL}$ . Upon initial device power-up and after exit from deep power-down mode, the STS pin defaults to RY/BY# operation where STS low indicates that the WSM is busy. STS High Z indicates that the WSM is ready for a new operation.

To reconfigure the STS pin to other modes, the STS Configuration is issued followed by the appropriate configuration code. The three alternate

configurations are all pulse mode for use as a system interrupt. The STS Configuration command functions independently of the  $V_{PP}$  voltage and  $RP\#$  must be  $V_{IH}$ .

**Table 11 STS Configuration Coding Description**

CONFIGURATION BITS	EFFECTS
00H	Set STS pin to default level mode (RY/BY#). RY/BY# in the default level-mode of operation will indicate WSM status condition.
01H	Set STS pin to pulsed output signal for specific erase operation. In this mode, STS provides low pulse at the completion of Block Erase, Full Chip Erase and Clear Block Lock-Bits operations.
02H	Set STS pin to pulsed output signal for a specific write operation. In this mode, STS provides low pulse at the completion of (Multi) Byte Write and Set Block Lock-Bit operation.
03H	Set STS pin to pulsed output signal for specific write and erase operation. STS provides low pulse at the completion of Block Erase, Full Chip Erase, (Multi) Word/Byte Write and Block Lock-Bit Configuration operations.

**Table 12 Write Protection Alternatives**

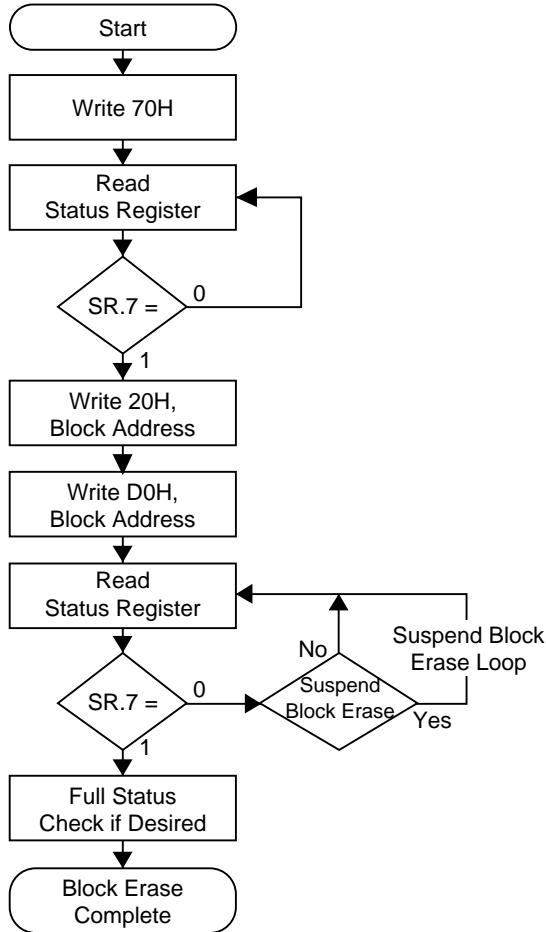
OPERATION	BLOCK LOCK-BIT	WP#	EFFECT
Block Erase or (Multi) Word/Byte Write	0	$V_{IL}$ or $V_{IH}$	Block Erase and (Multi) Word/Byte Write Enabled
	1	$V_{IL}$	Block is Locked. Block Erase and (Multi) Word/Byte Write Disabled
		$V_{IH}$	Block Lock-Bit Override. Block Erase and (Multi) Word/Byte Write Enabled
Full Chip Erase	0, 1	$V_{IL}$	All unlocked blocks are erased, locked blocks are not erased
	X	$V_{IH}$	All blocks are erased
Set Block Lock-Bit	X	$V_{IL}$	Set Block Lock-Bit Disabled
		$V_{IH}$	Set Block Lock-Bit Enabled
Clear Block Lock-Bits	X	$V_{IL}$	Clear Block Lock-Bits Disabled
		$V_{IH}$	Clear Block Lock-Bits Enabled

Table 13.1 Status Register Definition

WSMS	BESS	ECBLBS	WSBLBS	VPPS	WSS	DPS	R
7	6	5	4	3	2	1	0
SR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy SR.6 = BLOCK ERASE SUSPEND STATUS (BESS) 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed SR.5 = ERASE AND CLEAR BLOCK LOCK-BITS STATUS (ECBLBS) 1 = Error in Erase or Clear Block Lock-Bits 0 = Successful Erase or Clear Block Lock-Bits SR.4 = WRITE AND SET BLOCK LOCK-BIT STATUS (WSBLBS) 1 = Error in Write or Set Block Lock-Bit 0 = Successful Write or Set Block Lock-Bit SR.3 = VPP STATUS (VPPS) 1 = VPP Low Detect, Operation Abort 0 = VPP OK SR.2 = WRITE SUSPEND STATUS (WSS) 1 = Write Suspended 0 = Write in Progress/Completed SR.1 = DEVICE PROTECT STATUS (DPS) 1 = Block Lock-Bit and/or WP# Lock Detected, Operation Abort 0 = Unlock SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)				<b>NOTES :</b> Check STS or SR.7 to determine block erase, full chip erase, (multi) word/byte write or block lock-bit configuration completion. SR.6-0 are invalid while SR.7 = "0". If both SR.5 and SR.4 are "1"s after a block erase, full chip erase, (multi) word/byte write, block lock-bit configuration or STS configuration attempt, an improper command sequence was entered. SR.3 does not provide a continuous indication of VPP level. The WSM interrogates and indicates the VPP level only after block erase, full chip erase, (multi) word/byte write or block lock-bit configuration command sequences. SR.3 is not guaranteed to reports accurate feedback only when VPP ≠ VPPH1. SR.1 does not provide a continuous indication of block lock-bit values. The WSM interrogates block lock-bit, and WP# only after block erase, full chip erase, (multi) word/byte write or block lock-bit configuration command sequences. It informs the system, depending on the attempted operation, if the block lock-bit is set and/or WP# is not VIH. Reading the block lock configuration codes after writing the Read Identifier Codes command indicates block lock-bit status. SR.0 is reserved for future use and should be masked out when polling the status register.			

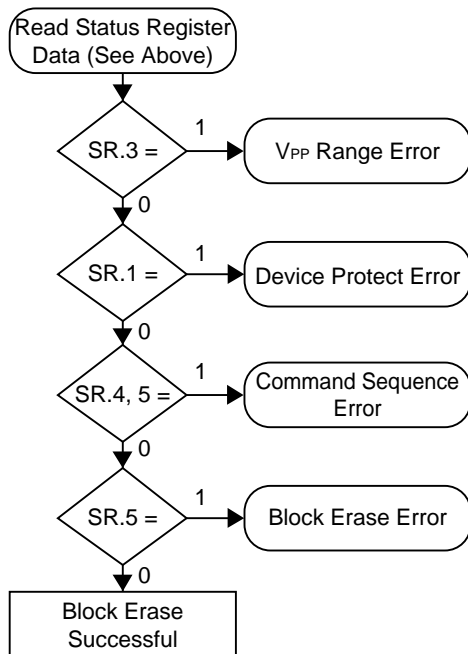
Table 13.2 Extended Status Register Definition

SMS	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
XSR.7 = STATE MACHINE STATUS (SMS) 1 = Multi Word/Byte Write available 0 = Multi Word/Byte Write not available XSR.6-0 = RESERVED FOR FUTURE ENHANCEMENTS (R)				<b>NOTES :</b> After issue a Multi Word/Byte Write command : XSR.7 indicates that a next Multi Word/Byte Write command is available. XSR.6-0 are reserved for future use and should be masked out when polling the extended status register.			



BUS OPERATION	COMMAND	COMMENTS
Write	Read Status Register	Data = 70H Addr = X
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Write	Erase Setup	Data = 20H Addr = Within Block to be Erased
Write	Erase Confirm	Data = D0H Addr = Within Block to be Erased
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Repeat for subsequent block erasures.		
Full status check can be done after each block erase or after a sequence of block erasures.		
Write FFH after the last block erase operation to place device in read array mode.		

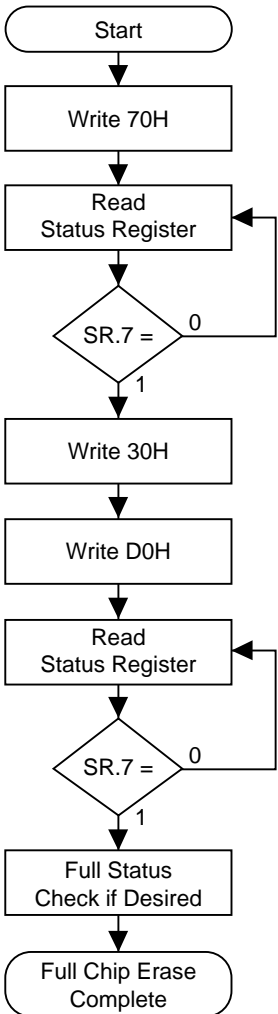
**FULL STATUS CHECK PROCEDURE**



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SR.3 1 = VPP Error Detect
Standby		Check SR.1 1 = Device Protect Detect WP# = VIL, Block Lock-Bit is Set Only required for systems implementing block lock-bit configuration
Standby		Check SR.4, 5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Block Erase Error
SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple blocks are erased before full status is checked.		
If error is detected, clear the status register before attempting retry or other error recovery.		

**Fig. 3 Automated Block Erase Flowchart**

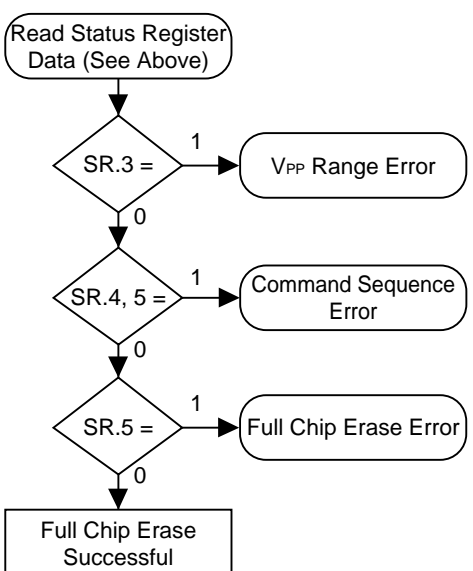




BUS OPERATION	COMMAND	COMMENTS
Write	Read Status Register	Data = 70H Addr = X
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Write	Full Chip Erase Setup	Data = 30H Addr = X
Write	Full Chip Erase Confirm	Data = D0H Addr = X
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

Full status check can be done after each full chip erase. Write FFH after the last full chip erase operation to place device in read array mode.

**FULL STATUS CHECK PROCEDURE**

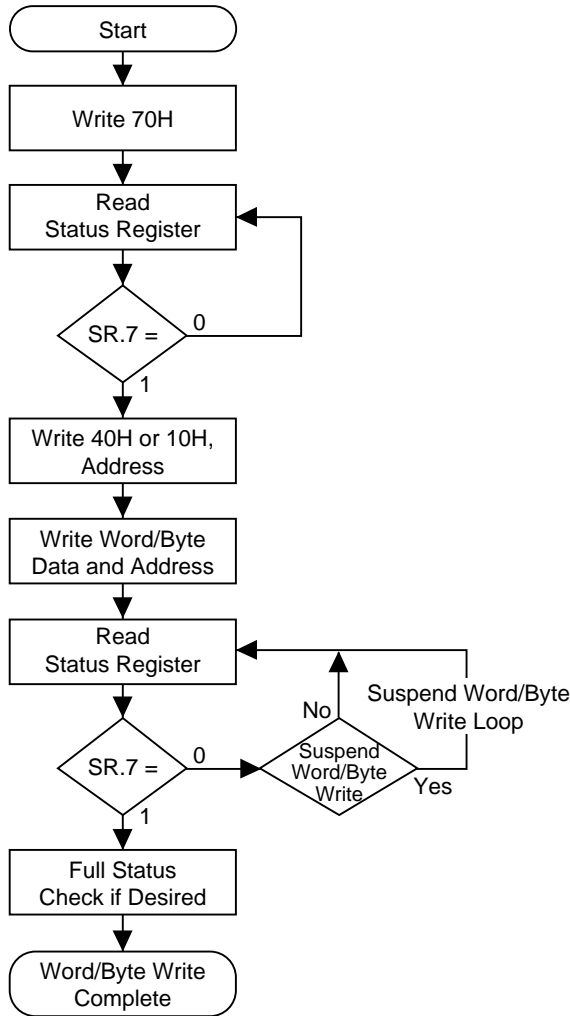


BUS OPERATION	COMMAND	COMMENTS
Standby		Check SR.3 1 = VPP Error Detect
Standby		Check SR.4, 5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Full Chip Erase Error

SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple blocks are erased before full status is checked.

If error is detected, clear the status register before attempting retry or other error recovery.

**Fig. 4 Automated Full Chip Erase Flowchart**



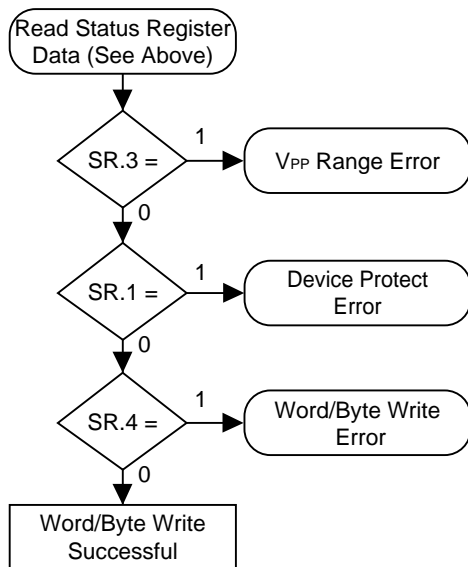
BUS OPERATION	COMMAND	COMMENTS
Write	Read Status Register	Data = 70H Addr = X
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Write	Setup Word/Byte Write	Data = 40H or 10H Addr = Location to be Written
Write	Word/Byte Write	Data = Data to be Written Addr = Location to be Written
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent word/byte writes.

SR full status check can be done after each word/byte write or after a sequence of word/byte writes.

Write FFH after the last word/byte write operation to place device in read array mode.

**FULL STATUS CHECK PROCEDURE**

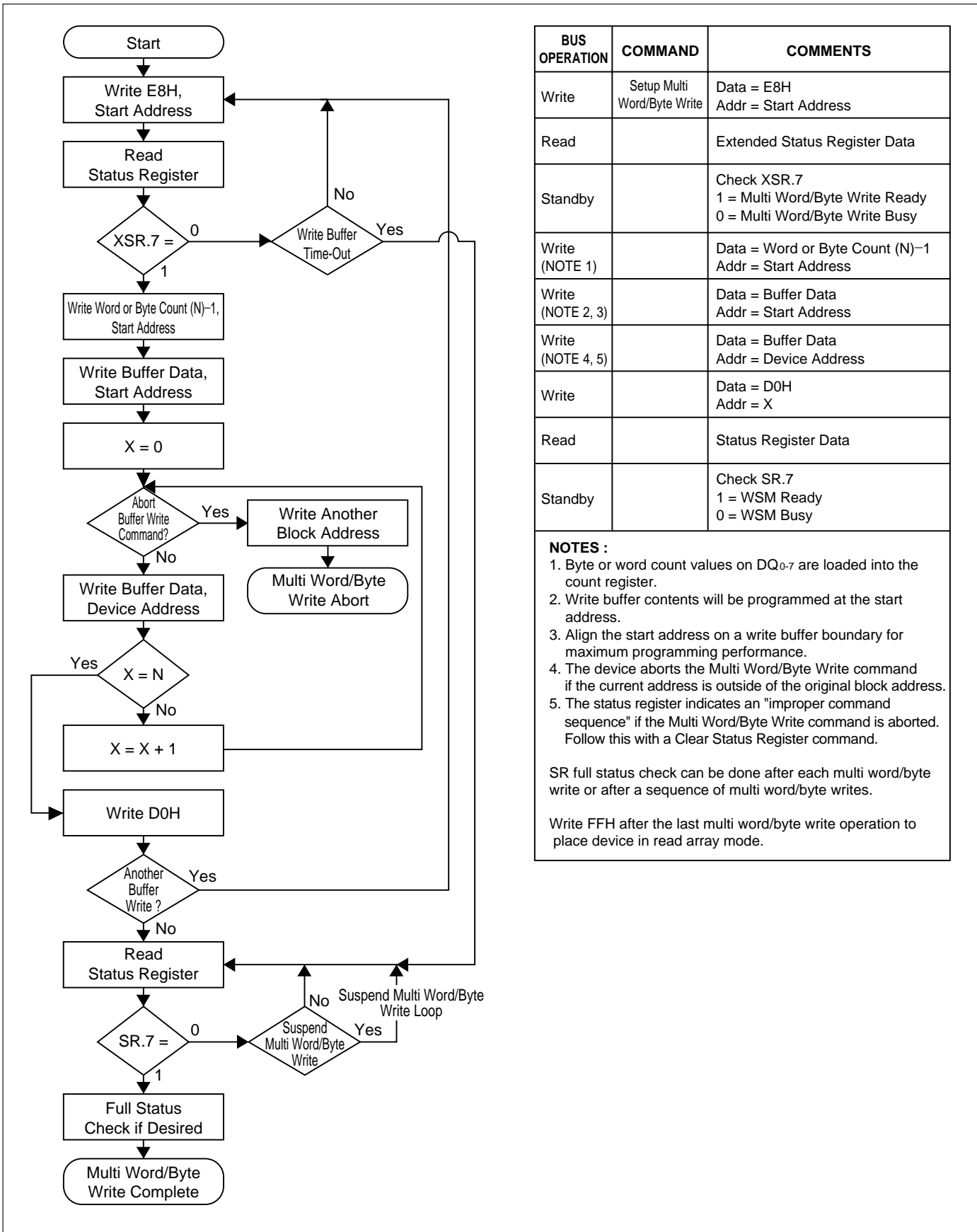


BUS OPERATION	COMMAND	COMMENTS
Standby		Check SR.3 1 = VPP Error Detect
Standby		Check SR.1 1 = Device Protect Detect WP# = V <sub>IL</sub> , Block Lock-Bit is Set Only required for systems implementing block lock-bit configuration
Standby		Check SR.4 1 = Data Write Error

SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple locations are written before full status is checked.

If error is detected, clear the status register before attempting retry or other error recovery.

**Fig. 5 Automated Word/Byte Write Flowchart**



BUS OPERATION	COMMAND	COMMENTS
Write	Setup Multi Word/Byte Write	Data = E8H Addr = Start Address
Read		Extended Status Register Data
Standby		Check XSR.7 1 = Multi Word/Byte Write Ready 0 = Multi Word/Byte Write Busy
Write (NOTE 1)		Data = Word or Byte Count (N)-1 Addr = Start Address
Write (NOTE 2, 3)		Data = Buffer Data Addr = Start Address
Write (NOTE 4, 5)		Data = Buffer Data Addr = Device Address
Write		Data = D0H Addr = X
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

**NOTES :**

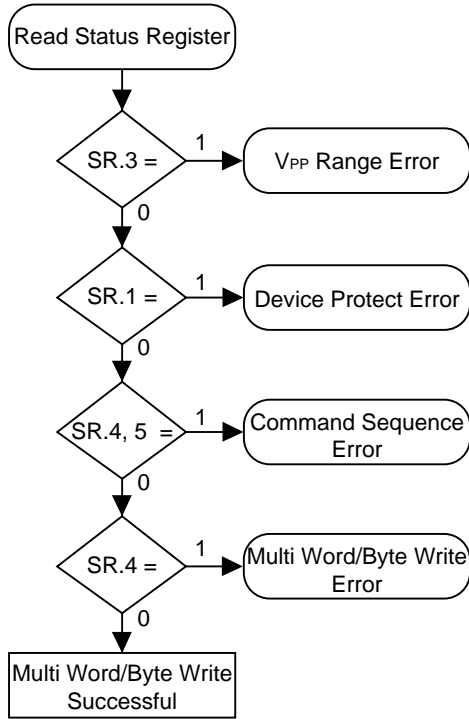
1. Byte or word count values on DQ<sub>0-7</sub> are loaded into the count register.
2. Write buffer contents will be programmed at the start address.
3. Align the start address on a write buffer boundary for maximum programming performance.
4. The device aborts the Multi Word/Byte Write command if the current address is outside of the original block address.
5. The status register indicates an "improper command sequence" if the Multi Word/Byte Write command is aborted. Follow this with a Clear Status Register command.

SR full status check can be done after each multi word/byte write or after a sequence of multi word/byte writes.

Write FFH after the last multi word/byte write operation to place device in read array mode.

**Fig. 6 Automated Multi Word/Byte Write Flowchart**

**FULL STATUS CHECK PROCEDURE FOR MULTI WORD/BYTE WRITE OPERATION**



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SR.3 1 = VPP Error Detect
Standby		Check SR.1 1 = Device Protect Detect WP# = V <sub>IL</sub> , Block Lock-Bit is Set Only required for systems implementing block lock-bit configuration
Standby		Check SR.4, 5 Both 1 = Command Sequence Error
Standby		Check SR.4 1 = Data Write Error
SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple locations are written before full status is checked.  If error is detected, clear the status register before attempting retry or other error recovery.		

**Fig. 7 Full Status Check Procedure for Automated Multi Word/Byte Write**

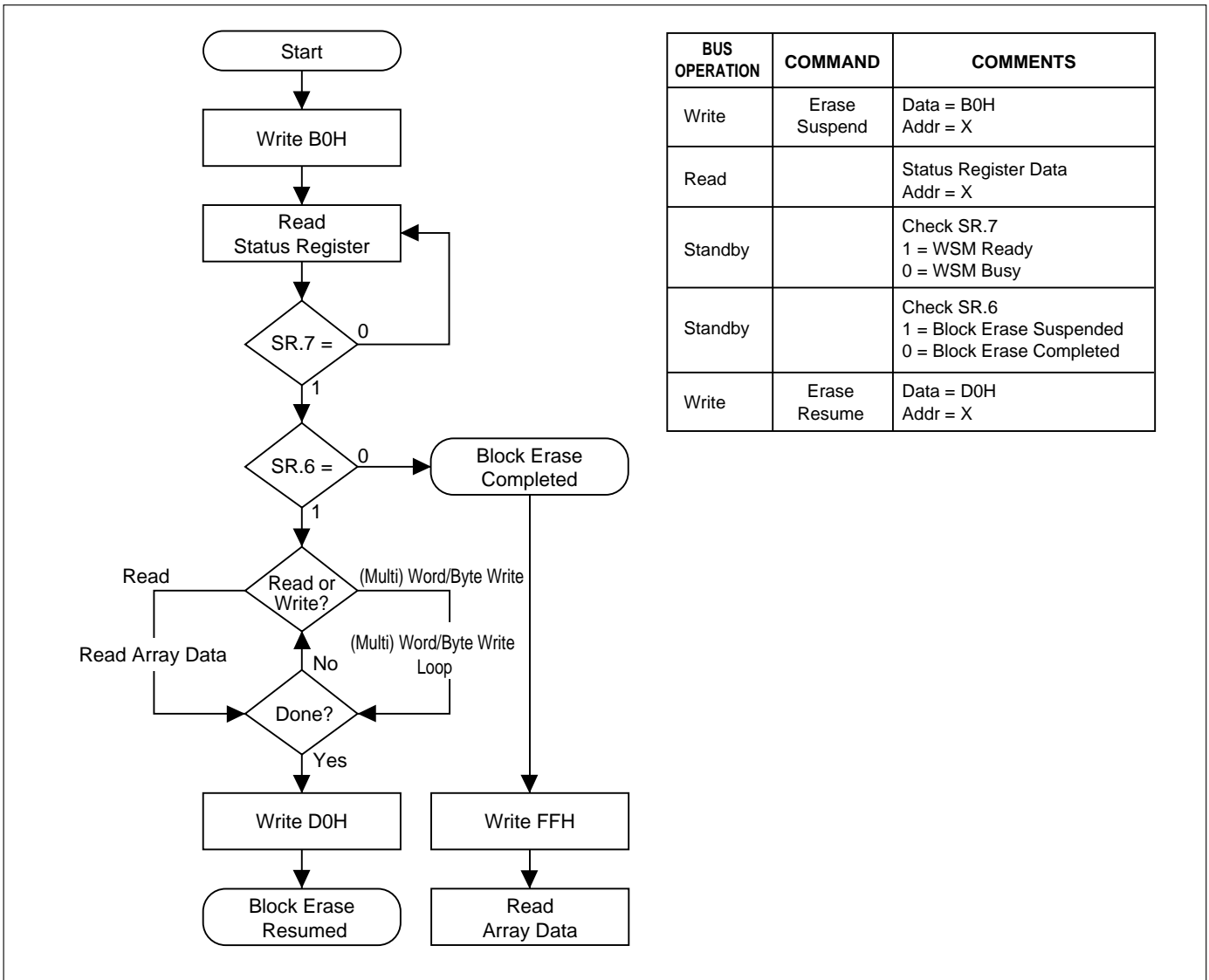
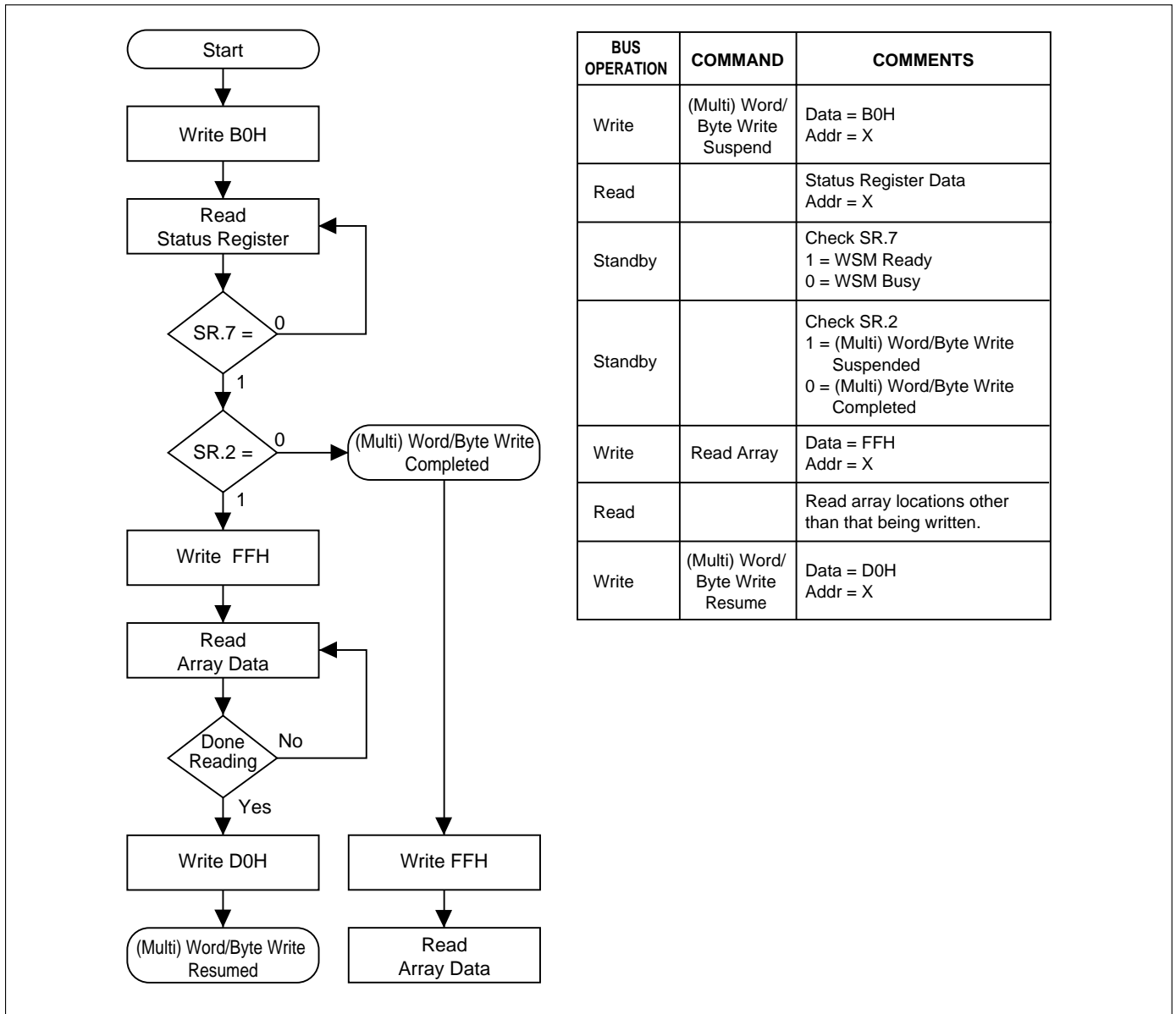
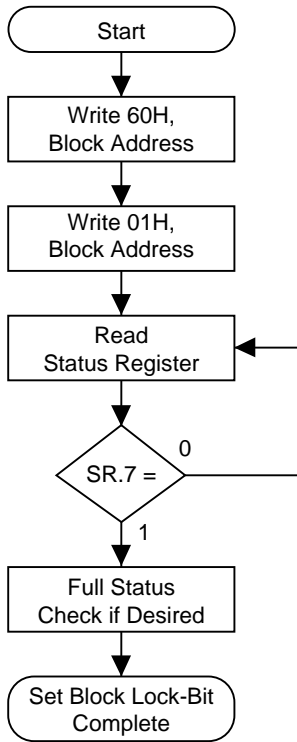


Fig. 8 Block Erase Suspend/Resume Flowchart



BUS OPERATION	COMMAND	COMMENTS
Write	(Multi) Word/Byte Write Suspend	Data = B0H Addr = X
Read		Status Register Data Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.2 1 = (Multi) Word/Byte Write Suspended 0 = (Multi) Word/Byte Write Completed
Write	Read Array	Data = FFH Addr = X
Read		Read array locations other than that being written.
Write	(Multi) Word/Byte Write Resume	Data = D0H Addr = X

Fig. 9 (Multi) Word/Byte Write Suspend/Resume Flowchart



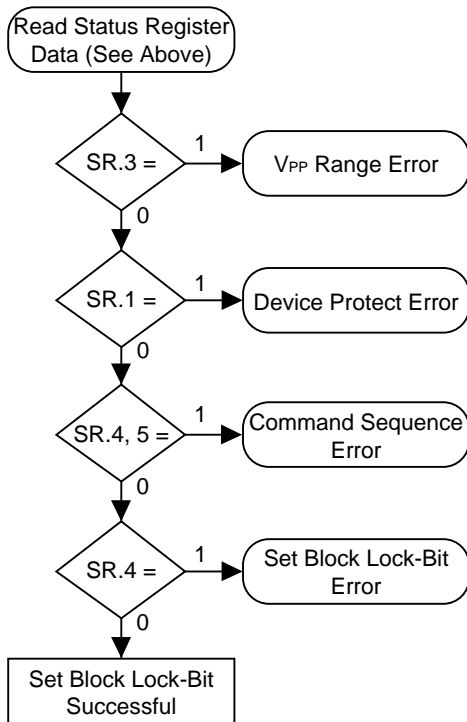
BUS OPERATION	COMMAND	COMMENTS
Write	Set Block Lock-Bit Setup	Data = 60H Addr = Block Address
Write	Set Block Lock-Bit Confirm	Data = 01H Addr = Block Address
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent block lock-bit set operations.

Full status check can be done after each block lock-bit set operation or after a sequence of block lock-bit set operations.

Write FFH after the last block lock-bit set operation to place device in read array mode.

**FULL STATUS CHECK PROCEDURE**

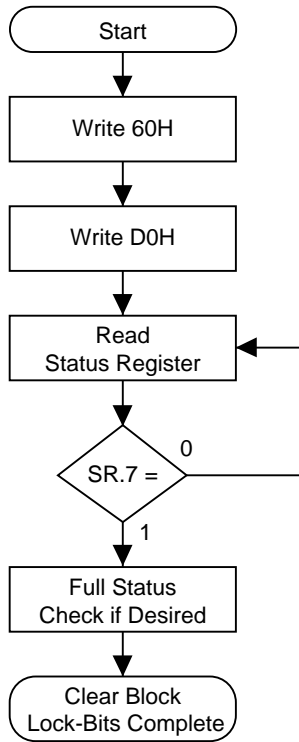


BUS OPERATION	COMMAND	COMMENTS
Standby		Check SR.3 1 = VPP Error Detect
Standby		Check SR.1 1 = Device Protect Detect WP# = VIL
Standby		Check SR.4, 5 Both 1 = Command Sequence Error
Standby		Check SR.4 1 = Set Block Lock-Bit Error

SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple block lock-bits are set before full status is checked.

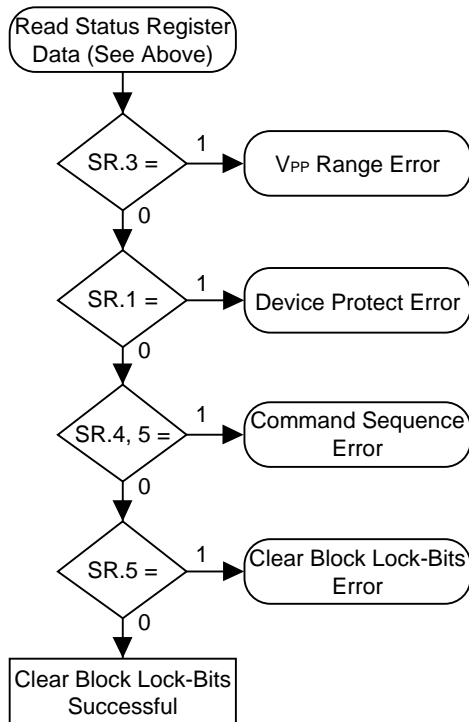
If error is detected, clear the status register before attempting retry or other error recovery.

**Fig. 10 Set Block Lock-Bit Flowchart**



BUS OPERATION	COMMAND	COMMENTS
Write	Clear Block Lock-Bits Setup	Data = 60H Addr = X
Write	Clear Block Lock-Bits Confirm	Data = D0H Addr = X
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Write FFH after the last clear block lock-bits operation to place device in read array mode.		

**FULL STATUS CHECK PROCEDURE**



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SR.3 1 = VPP Error Detect
Standby		Check SR.1 1 = Device Protect Detect WP# = VIL
Standby		Check SR.4, 5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Clear Block Lock-Bits Error
SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command. If error is detected, clear the status register before attempting retry or other error recovery.		

**Fig. 11 Clear Block Lock-Bits Flowchart**



## 5 DESIGN CONSIDERATIONS

### 5.1 Three-Line Output Control

The device will often be used in large memory arrays. SHARP provides three control inputs to accommodate multiple memory connections. Three-line control provides for :

- a. Lowest possible memory power consumption.
- b. Complete assurance that data bus contention will not occur.

To use these control inputs efficiently, an address decoder should enable CE# while OE# should be connected to all memory devices and the system's READ# control line. This assures that only selected memory devices have active outputs while deselected memory devices are in standby mode. RP# should be connected to the system POWERGOOD signal to prevent unintended writes during system power transitions. POWERGOOD should also toggle during system reset.

### 5.2 STS and Block Erase, Full Chip Erase, (Multi) Word/Byte Write and Block Lock-Bit Configuration Polling

STS is an open drain output that should be connected to VCC by a pullup resistor to provide a hardware method of detecting block erase, full chip erase, (multi) word/byte write and block lock-bit configuration completion. In default mode, it transitions low after block erase, full chip erase, (multi) word/byte write or block lock-bit configuration commands and returns to VOH when the WSM has finished executing the internal algorithm. For alternate STS pin configurations, see the Configuration command (Table 3 and Section 4.14).

STS can be connected to an interrupt input of the system CPU or controller. It is active at all times. STS, in default mode, is also High Z when the device is in block erase suspend (with (multi) word/byte write inactive), (multi) word/byte write suspend or deep power-down modes.

### 5.3 Power Supply Decoupling

Flash memory power switching characteristics require careful device decoupling. System designers are interested in three supply current issues; standby current levels, active current levels and transient peaks produced by falling and rising edges of CE# and OE#. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1  $\mu$ F ceramic capacitor connected between its VCC and GND and between its VPP and GND. These high-frequency, low inductance capacitors should be placed as close as possible to package leads. Additionally, for every eight devices, a 4.7  $\mu$ F electrolytic capacitor should be placed at the array's power supply connection between VCC and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductance.

### 5.4 VPP Trace on Printed Circuit Boards

Updating flash memories that reside in the target system requires that the printed circuit board designers pay attention to the VPP power supply trace. The VPP pin supplies the memory cell current for block erase, full chip erase, (multi) word/byte write and block lock-bit configuration. Use similar trace widths and layout considerations given to the VCC power bus. Adequate VPP supply traces and decoupling will decrease VPP voltage spikes and overshoots.

### 5.5 VCC, VPP, RP# Transitions

Block erase, full chip erase, (multi) word/byte write and block lock-bit configuration are not guaranteed if VPP falls outside of a valid VPPH1 range, VCC falls outside of a valid VCC1/2 range, or RP# = VIL. If VPP error is detected, status register bit SR.3 is set to "1" along with SR.4 or SR.5, depending on the attempted operation. If RP# transitions to VIL during block erase, full chip erase, (multi) word/byte write or block lock-bit configuration, STS (if set to

RY/BY# mode) will remain low until the reset operation is complete. Then, the operation will abort and the device will enter deep power-down. The aborted operation may leave data partially altered. Therefore, the command sequence must be repeated after normal operation is restored. Device power-off or RP# transitions to VIL clear the status register.

The CUI latches commands issued by system software and is not altered by VPP or CE# transitions or WSM actions. Its state is read array mode upon power-up, after exit from deep power-down or after VCC transitions below VLKO.

After block erase, full chip erase, (multi) word/byte write or block lock-bit configuration, even after VPP transitions down to VPP<sub>PLK</sub>, the CUI must be placed in read array mode via the Read Array command if subsequent access to the memory array is desired.

## 5.6 Power-Up/Down Protection

The device is designed to offer protection against accidental block and full chip erasure, (multi) word/byte writing or block lock-bit configuration during power transitions. Upon power-up, the device is indifferent as to which power supply (VPP or VCC) powers-up first. Internal circuitry resets the CUI to read array mode at power-up.

A system designer must guard against spurious writes for VCC voltages above VLKO when VPP is active. Since both WE# and CE# must be low for a command write, driving either to VIH will inhibit writes. The CUI's two-step command sequence architecture provides added level of protection against data alteration.

In-system block lock and unlock capability prevents inadvertent data alteration. The device is disabled while RP# = VIL regardless of its control inputs state.

## 5.7 Power Consumption

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash memory's nonvolatility increases usable battery life because data is retained when system power is removed.

In addition, deep power-down mode ensures extremely low power consumption even when system power is applied. For example, portable computing products and other power sensitive applications that use an array of devices for solid-state storage can consume negligible power by lowering RP# to VIL standby or sleep modes. If access is again needed, the devices can be read following the t<sub>PHQV</sub> and t<sub>PHWL</sub> wake-up cycles required after RP# is first raised to VIH. See **Section 6.2.4 through 6.2.6 "AC CHARACTERISTICS - READ-ONLY and WRITE OPERATIONS"** and **Fig. 15, Fig. 16, Fig. 17 and Fig. 18** for more information.

## 6 ELECTRICAL SPECIFICATIONS

### 6.1 Absolute Maximum Ratings\*

Operating Temperature

- LH28F160S5-L  
During Read, Erase, Write and  
Block Lock-Bit Configuration ... 0 to +70°C (NOTE 1)  
Temperature under Bias ..... -10 to +80°C
- LH28F160S5H-L  
During Read, Erase, Write and  
Block Lock-Bit Configuration .... -40 to +85°C (NOTE 2)  
Temperature under Bias ..... -40 to +85°C

Storage Temperature ..... -65 to +125°C

Voltage On Any Pin  
(except VCC, VPP) ..... -0.5 V to VCC+0.5 V (NOTE 3)

VCC Supply Voltage ..... -0.2 to +7.0 V (NOTE 3)

VPP Update Voltage during  
Erase, Write and  
Block Lock-Bit Configuration .... -0.2 to +7.0 V (NOTE 3)

Output Short Circuit Current ..... 100 mA (NOTE 4)

### 6.2 Operating Conditions

SYMBOL	PARAMETER	NOTE	MIN.	MAX.	UNIT	VERSIONS
TA	Operating Temperature	1	0	+70	°C	LH28F160S5-L
			-40	+85	°C	LH28F160S5H-L
VCC1	VCC Supply Voltage (5.0±0.25 V)		4.75	5.25	V	LH28F160S5-L70/S5H-L70
VCC2	VCC Supply Voltage (5.0±0.5 V)		4.50	5.50	V	

**NOTE :**

1. Test condition : Ambient temperature

#### 6.2.1 CAPACITANCE (NOTE 1)

TA = +25°C, f = 1 MHz

SYMBOL	PARAMETER	TYP.	MAX.	UNIT	CONDITION
CIN	Input Capacitance	7	10	pF	VIN = 0.0 V
COU	Output Capacitance	9	12	pF	VOUT = 0.0 V

**NOTE :**

1. Sampled, not 100% tested.

**NOTICE :** The specifications are subject to change without notice. Verify with your local SHARP sales office that you have the latest datasheet before finalizing a design.

*\*WARNING : Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

**NOTES :**

1. Operating temperature is for commercial product defined by this specification.
2. Operating temperature is for extended temperature product defined by this specification.
3. All specified voltages are with respect to GND. Minimum DC voltage is -0.5 V on input/output pins and -0.2 V on VCC and VPP pins. During transitions, this level may undershoot to -2.0 V for periods < 20 ns. Maximum DC voltage on input/output pins and VCC is VCC+0.5 V which, during transitions, may overshoot to VCC+2.0 V for periods < 20 ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.

6.2.2 AC INPUT/OUTPUT TEST CONDITIONS

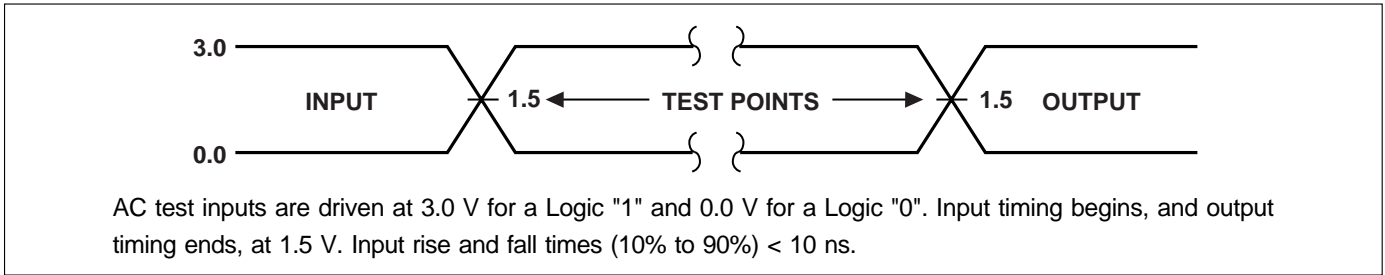


Fig. 12 Transient Input/Output Reference Waveform for  $V_{CC} = 5.0 \pm 0.25$  V (High Speed Testing Configuration)

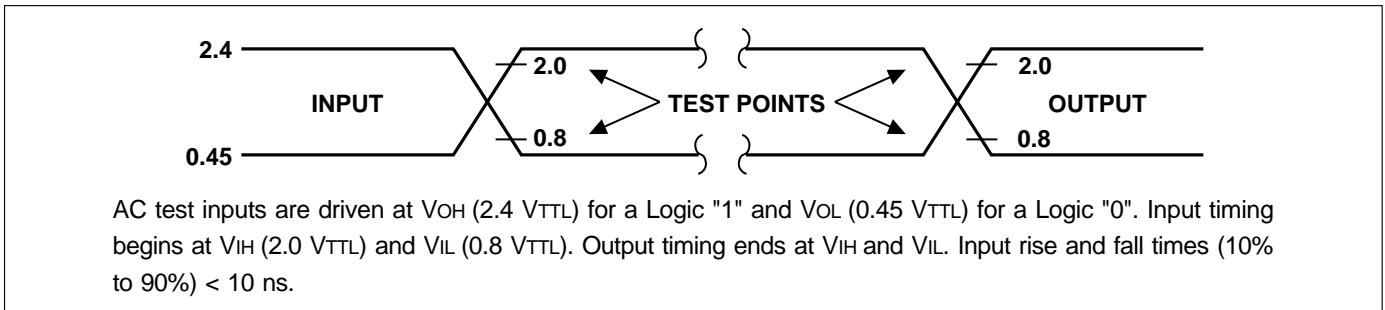


Fig. 13 Transient Input/Output Reference Waveform for  $V_{CC} = 5.0 \pm 0.5$  V (Standard Testing Configuration)

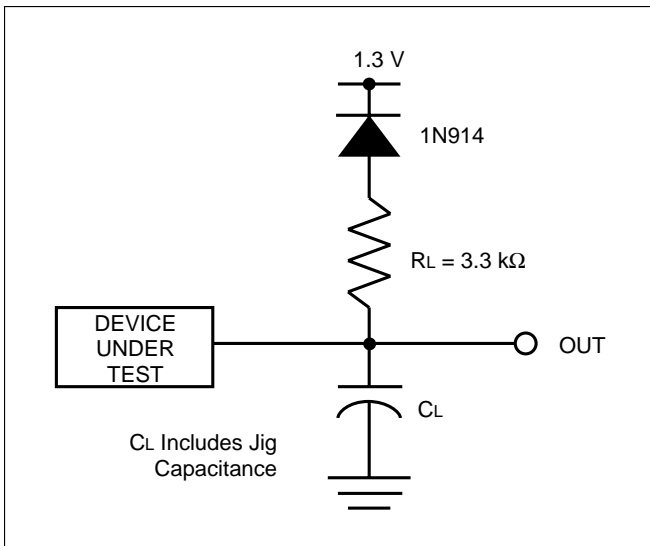


Fig. 14 Transient Equivalent Testing Load Circuit

Test Configuration Capacitance Loading Value

TEST CONFIGURATION	CL (pF)
$V_{CC} = 5.0 \pm 0.25$ V (NOTE 1)	30
$V_{CC} = 5.0 \pm 0.5$ V	100

NOTE :

1. Applied to high-speed products, LH28F160S5-L70 and LH28F160S5H-L70.

## 6.2.3 DC CHARACTERISTICS

SYMBOL	PARAMETER		NOTE	V <sub>CC</sub> = 5.0±0.5 V		UNIT	TEST CONDITIONS
				TYP.	MAX.		
ILI	Input Load Current		1		±1	μA	V <sub>CC</sub> = V <sub>CC</sub> Max. V <sub>IN</sub> = V <sub>CC</sub> or GND
ILO	Output Leakage Current		1		±10	μA	V <sub>CC</sub> = V <sub>CC</sub> Max. V <sub>OUT</sub> = V <sub>CC</sub> or GND
I <sub>CCS</sub>	V <sub>CC</sub> Standby Current		1, 3, 6	25	100	μA	CMOS Inputs V <sub>CC</sub> = V <sub>CC</sub> Max. CE# = RP# = V <sub>CC</sub> ±0.2 V
				2	4	mA	TTL Inputs V <sub>CC</sub> = V <sub>CC</sub> Max. CE# = RP# = V <sub>IH</sub>
I <sub>CCD</sub>	V <sub>CC</sub> Deep Power-Down Current	LH28F160S5-L	1		15	μA	RP# = GND±0.2 V I <sub>OUT</sub> (STS) = 0 mA
		LH28F160S5H-L			20		
I <sub>CCR</sub>	V <sub>CC</sub> Read Current		1, 5, 6		50	mA	CMOS Inputs V <sub>CC</sub> = V <sub>CC</sub> Max. CE# = GND f = 8 MHz, I <sub>OUT</sub> = 0 mA
					65	mA	TTL Inputs V <sub>CC</sub> = V <sub>CC</sub> Max. CE# = V <sub>IL</sub> f = 8 MHz, I <sub>OUT</sub> = 0 mA
I <sub>CCW</sub>	V <sub>CC</sub> Write Current (Multi) W/B Write or Set Block Lock-Bit)		1, 7		35	mA	V <sub>PP</sub> = 5.0±0.5 V
I <sub>CCE</sub>	V <sub>CC</sub> Erase Current (Block Erase, Full Chip Erase, Clear Block Lock-Bits)		1, 7		30	mA	V <sub>PP</sub> = 5.0±0.5 V
I <sub>CCWS</sub> I <sub>CCES</sub>	V <sub>CC</sub> Write or Block Erase Suspend Current		1, 2	1	10	mA	CE# = V <sub>IH</sub>
I <sub>PPS</sub>	V <sub>PP</sub> Standby Current		1	±2	±15	μA	V <sub>PP</sub> ≤ V <sub>CC</sub>
I <sub>PPR</sub>	V <sub>PP</sub> Read Current		1	10	200	μA	V <sub>PP</sub> > V <sub>CC</sub>
I <sub>PPD</sub>	V <sub>PP</sub> Deep Power-Down Current		1	0.1	5	μA	RP# = GND±0.2 V
I <sub>PPW</sub>	V <sub>PP</sub> Write Current (Multi) W/B Write or Set Block Lock-Bit)		1, 7		80	mA	V <sub>PP</sub> = 5.0±0.5 V
I <sub>PPE</sub>	V <sub>PP</sub> Erase Current (Block Erase, Full Chip Erase, Clear Block Lock-Bits)		1, 7		40	mA	V <sub>PP</sub> = 5.0±0.5V
I <sub>PPWS</sub> I <sub>PPES</sub>	V <sub>PP</sub> Write or Block Erase Suspend Current		1	10	200	μA	V <sub>PP</sub> = V <sub>PPH1</sub>

## 6.2.3 DC CHARACTERISTICS (contd.)

SYMBOL	PARAMETER	NOTE	V <sub>CC</sub> = 5.0±0.5 V		UNIT	TEST CONDITIONS
			MIN.	MAX.		
V <sub>IL</sub>	Input Low Voltage	7	-0.5	0.8	V	
V <sub>IH</sub>	Input High Voltage	7	2.0	V <sub>CC</sub> +0.5	V	
V <sub>OL</sub>	Output Low Voltage	3, 7		0.45	V	V <sub>CC</sub> = V <sub>CC</sub> Min. I <sub>OL</sub> = 5.8 mA
V <sub>OH1</sub>	Output High Voltage (TTL)	3, 7	2.4		V	V <sub>CC</sub> = V <sub>CC</sub> Min. I <sub>OH</sub> = -2.5 mA
V <sub>OH2</sub>	Output High Voltage (CMOS)	3, 7	0.85 V <sub>CC</sub>		V	V <sub>CC</sub> = V <sub>CC</sub> Min. I <sub>OH</sub> = -2.5 mA
			V <sub>CC</sub> -0.4		V	V <sub>CC</sub> = V <sub>CC</sub> Min. I <sub>OH</sub> = -100 µA
V <sub>PPLK</sub>	V <sub>PP</sub> Lockout Voltage during Normal Operations	4, 7		1.5	V	
V <sub>PPH1</sub>	V <sub>PP</sub> Voltage during Write or Erase Operations		4.5	5.5	V	
V <sub>LKO</sub>	V <sub>CC</sub> Lockout Voltage		2.0		V	

## NOTES :

- All currents are in RMS unless otherwise noted. Typical values at nominal V<sub>CC</sub> voltage and T<sub>A</sub> = +25°C. These currents are valid for all product versions (packages and speeds).
- I<sub>CCWS</sub> and I<sub>CCES</sub> are specified with the device deselected. If reading or (multi) word/byte writing in erase suspend mode, the device's current draw is the sum of I<sub>CCWS</sub> or I<sub>CCES</sub> and I<sub>CCR</sub> or I<sub>CCW</sub>, respectively.
- Includes STS.
- Block erases, full chip erases, (multi) word/byte writes and block lock-bit configurations are inhibited when V<sub>PP</sub> ≤ V<sub>PPLK</sub>, and not guaranteed in the range between V<sub>PPLK</sub> (max.) and V<sub>PPH1</sub> (min.) and above V<sub>PPH1</sub> (max.).
- Automatic Power Saving (APS) reduces typical I<sub>CCR</sub> to 1 mA at 5 V V<sub>CC</sub> in static operation.
- CMOS inputs are either V<sub>CC</sub>±0.2 V or GND±0.2 V. TTL inputs are either V<sub>IL</sub> or V<sub>IH</sub>.
- Sampled, not 100% tested.

## 6.2.4 AC CHARACTERISTICS - READ-ONLY OPERATIONS (NOTE1)

## [LH28F160S5-L]

•  $V_{CC} = 5.0 \pm 0.25 \text{ V}, 5.0 \pm 0.5 \text{ V}, T_A = 0 \text{ to } +70^\circ\text{C}$

VERSIONS		$V_{CC} \pm 0.25 \text{ V}$	(NOTE 4) LH28F160S5-L70				(NOTE 5) LH28F160S5-L10		UNIT
		$V_{CC} \pm 0.5 \text{ V}$			MIN.	MAX.	MIN.	MAX.	
SYMBOL	PARAMETER	NOTE	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tAVAV	Read Cycle Time		70		80		100		ns
tAVQV	Address to Output Delay			70		80		100	ns
tELQV	CE# to Output Delay	2		70		80		100	ns
tPHQV	RP# High to Output Delay			400		400		400	ns
tGLQV	OE# to Output Delay	2		30		35		40	ns
tELQX	CE# to Output in Low Z	3	0		0		0		ns
tEHQZ	CE# High to Output in High Z	3		25		30		35	ns
tGLQX	OE# to Output in Low Z	3	0		0		0		ns
tGHQZ	OE# High to Output in High Z	3		10		10		15	ns
tOH	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		0		0		ns
tFLQV tFHQV	BYTE# to Output Delay	3		70		80		100	ns
tFLQZ	BYTE# to Output in High Z	3		25		30		30	ns
tELFL tELFH	CE# Low to BYTE# High or Low	3		5		5		5	ns

## NOTES :

1. See AC Input/Output Reference Waveform (Fig. 12 and Fig. 13) for maximum allowable input slew rate.
2. OE# may be delayed up to tELQV-tGLQV after the falling edge of CE# without impact on tELQV.
3. Sampled, not 100% tested.
4. See Fig. 12 "Transient Input/Output Reference Waveform" and Fig. 14 "Transient Equivalent Testing Load Circuit" (High Speed Configuration) for testing characteristics.
5. See Fig. 13 "Transient Input/Output Reference Waveform" and Fig. 14 "Transient Equivalent Testing Load Circuit" (Standard Configuration) for testing characteristics.

## 6.2.4 AC CHARACTERISTICS - READ-ONLY OPERATIONS (contd.) (NOTE1)

## [LH28F160S5H-L]

•  $V_{CC} = 5.0 \pm 0.25 \text{ V}, 5.0 \pm 0.5 \text{ V}, T_A = -40 \text{ to } +85^\circ\text{C}$

VERSIONS		V <sub>CC</sub> ±0.25 V	(NOTE 4) LH28F160S5H-L70		(NOTE 5) LH28F160S5H-L70		(NOTE 5) LH28F160S5H-L10		UNIT
			V <sub>CC</sub> ±0.5 V	MIN.	MAX.	MIN.	MAX.	MIN.	
SYMBOL	PARAMETER	NOTE	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tAVAV	Read Cycle Time		70		90		100		ns
tAVQV	Address to Output Delay			70		90		100	ns
tELQV	CE# to Output Delay	2		70		90		100	ns
tPHQV	RP# High to Output Delay			400		400		400	ns
tGLQV	OE# to Output Delay	2		30		35		40	ns
tELQX	CE# to Output in Low Z	3	0		0		0		ns
tEHQZ	CE# High to Output in High Z	3		25		30		35	ns
tGLQX	OE# to Output in Low Z	3	0		0		0		ns
tGHQZ	OE# High to Output in High Z	3		10		10		15	ns
tOH	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		0		0		ns
tFLQV tFHQV	BYTE# to Output Delay	3		70		90		100	ns
tFLQZ	BYTE# to Output in High Z	3		25		30		30	ns
tELFL	CE# Low to BYTE#	3		5		5		5	ns
tELFH	High or Low								

## NOTES :

1. See AC Input/Output Reference Waveform (Fig. 12 and Fig. 13) for maximum allowable input slew rate.
2. OE# may be delayed up to tELQV-tGLQV after the falling edge of CE# without impact on tELQV.
3. Sampled, not 100% tested.
4. See Fig. 12 "Transient Input/Output Reference Waveform" and Fig. 14 "Transient Equivalent Testing Load Circuit" (High Speed Configuration) for testing characteristics.
5. See Fig. 13 "Transient Input/Output Reference Waveform" and Fig. 14 "Transient Equivalent Testing Load Circuit" (Standard Configuration) for testing characteristics.



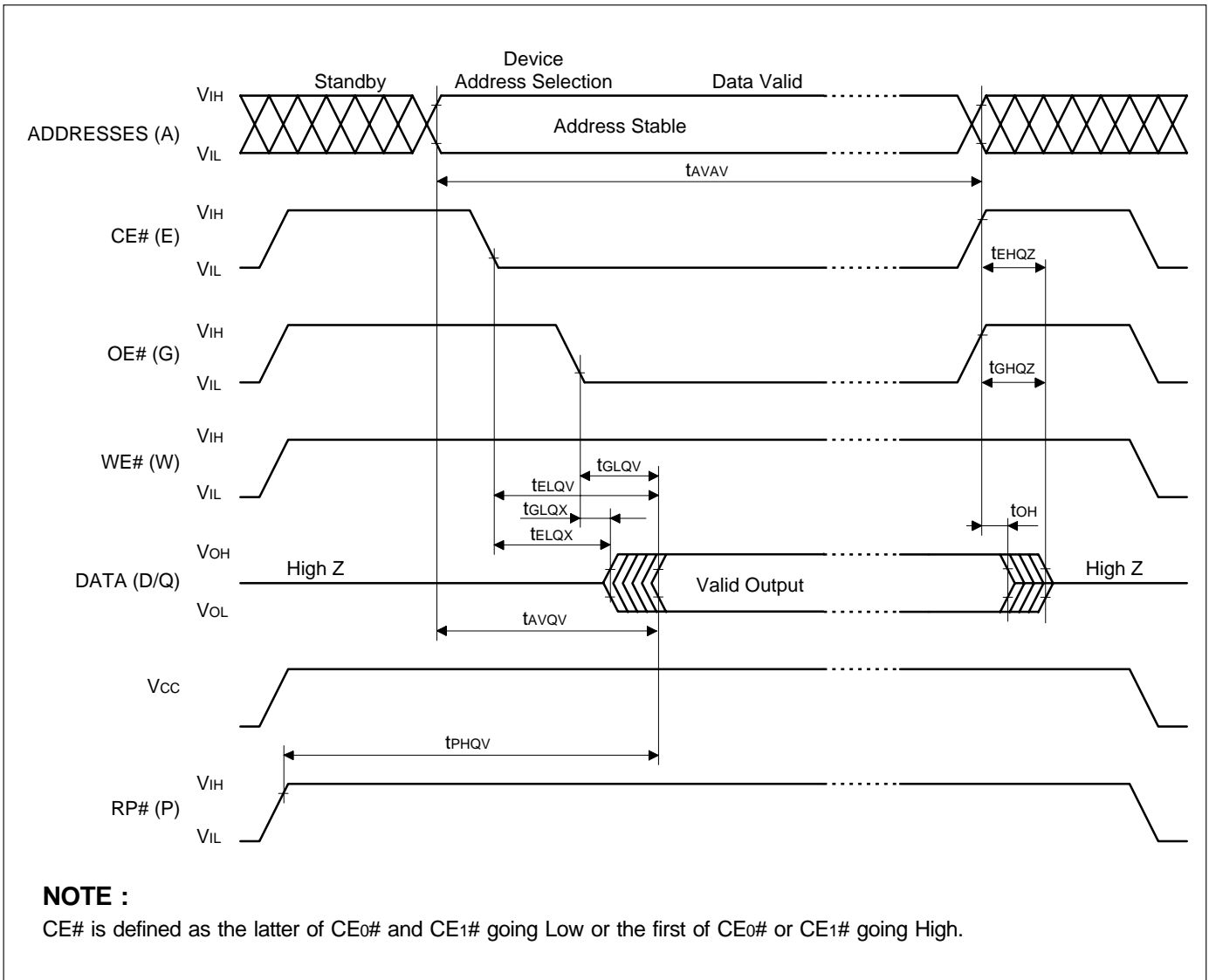


Fig. 15 AC Waveform for Read Operations

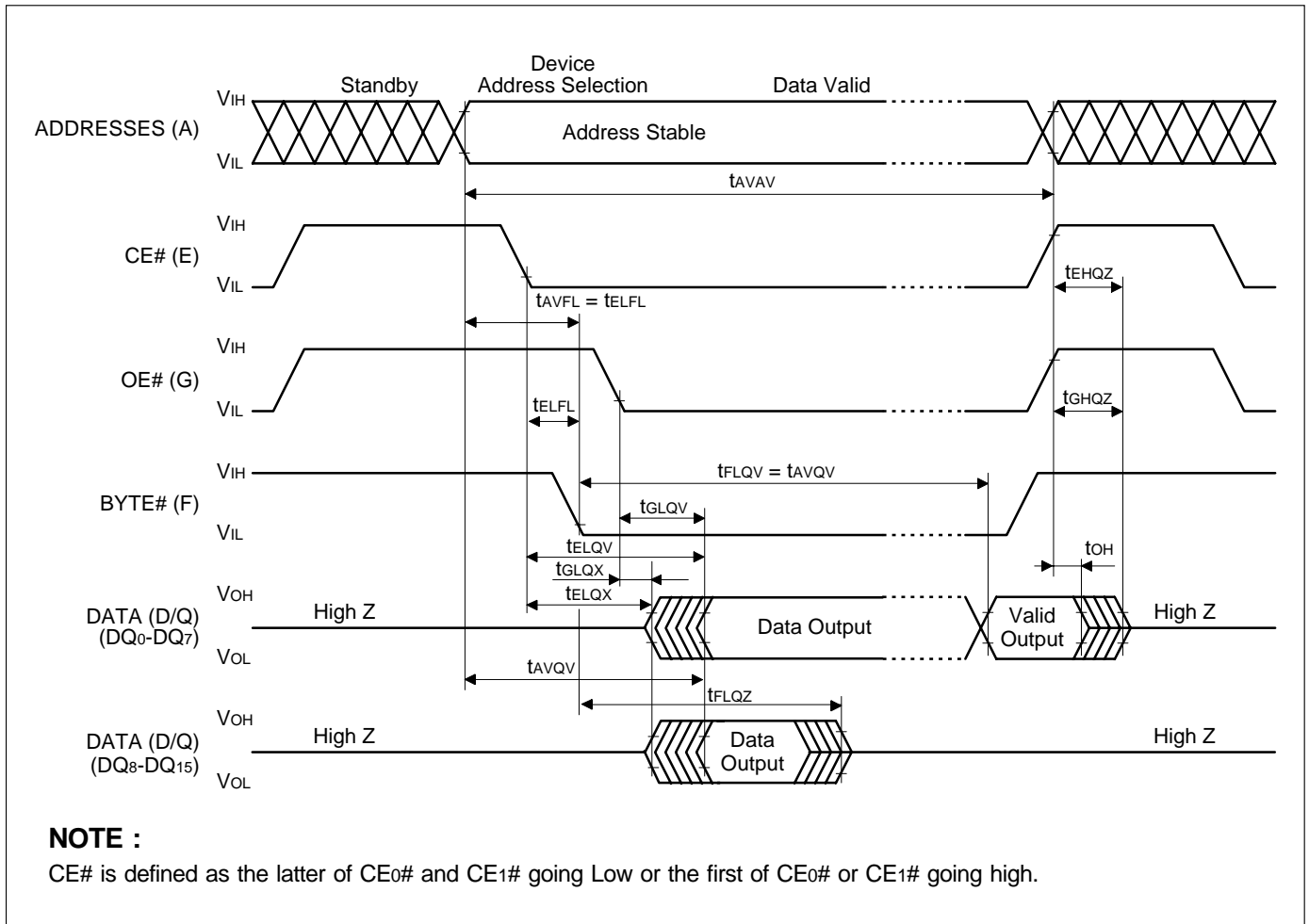


Fig. 16 BYTE# Timing Waveforms

## 6.2.5 AC CHARACTERISTICS - WRITE OPERATIONS (NOTE 1)

## [LH28F160S5-L]

•  $V_{CC} = 5.0 \pm 0.25 \text{ V}, 5.0 \pm 0.5 \text{ V}, T_A = 0 \text{ to} +70^\circ\text{C}$

VERSIONS		$V_{CC} \pm 0.25 \text{ V}$	(NOTE 5) LH28F160S5-L70				(NOTE 6) LH28F160S5-L10		UNIT
		$V_{CC} \pm 0.5 \text{ V}$			(NOTE 6) LH28F160S5-L70		(NOTE 6) LH28F160S5-L10		
SYMBOL	PARAMETER	NOTE	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tAVAV	Write Cycle Time		70		80		100		ns
tPHWL	RP# High Recovery to WE# Going Low	2	1		1		1		$\mu\text{s}$
tELWL	CE# Setup to WE# Going Low		10		10		10		ns
tWLWH	WE# Pulse Width		40		40		40		ns
tSHWH	WP# $V_{IH}$ Setup to WE# Going High	2	100		100		100		ns
tVPWH	VPP Setup to WE# Going High	2	100		100		100		ns
tAVWH	Address Setup to WE# Going High	3	40		40		40		ns
tdVWH	Data Setup to WE# Going High	3	40		40		40		ns
tWHDX	Data Hold from WE# High		5		5		5		ns
tWHAX	Address Hold from WE# High		5		5		5		ns
tWHEH	CE# Hold from WE# High		10		10		10		ns
tWHWL	WE# Pulse Width High		30		30		30		ns
tWHRL	WE# High to STS Going Low			90		90		90	ns
tWHGL	Write Recovery before Read		0		0		0		ns
tQVVL	VPP Hold from Valid SRD, STS High Z	2, 4	0		0		0		ns
tQVSL	WP# $V_{IH}$ Hold from Valid SRD, STS High Z	2, 4	0		0		0		ns

## NOTES :

1. Read timing characteristics during block erase, full chip erase, (multi) word/byte write and block lock-bit configuration operations are the same as during read-only operations. Refer to **Section 6.2.4 "AC CHARACTERISTICS"** for read-only operations.
2. Sampled, not 100% tested.
3. Refer to **Table 3** for valid AIN and DIN for block erase, full chip erase, (multi) word/byte write or block lock-bit configuration.
4. VPP should be held at VPPH1 until determination of block erase, full chip erase, (multi) word/byte write or block lock-bit configuration success (SR.1/3/4/5 = 0).
5. See **Fig. 12 "Transient Input/Output Reference Waveform"** and **Fig. 14 "Transient Equivalent Testing Load Circuit"** (High Speed Configuration) for testing characteristics.
6. See **Fig. 13 "Transient Input/Output Reference Waveform"** and **Fig. 14 "Transient Equivalent Testing Load Circuit"** (Standard Configuration) for testing characteristics.

## 6.2.5 AC CHARACTERISTICS - WRITE OPERATIONS (contd.) (NOTE 1)

## [LH28F160S5H-L]

•  $V_{CC} = 5.0 \pm 0.25 \text{ V}$ ,  $5.0 \pm 0.5 \text{ V}$ ,  $T_A = -40$  to  $+85^\circ\text{C}$ 

VERSIONS		$V_{CC} \pm 0.25 \text{ V}$	(NOTE 5) LH28F160S5H-L70						UNIT
		$V_{CC} \pm 0.5 \text{ V}$			(NOTE 6) LH28F160S5H-L70		(NOTE 6) LH28F160S5H-L10		
SYMBOL	PARAMETER	NOTE	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tAVAV	Write Cycle Time		70		90		100		ns
tPHWL	RP# High Recovery to WE# Going Low	2	1		1		1		$\mu\text{s}$
tELWL	CE# Setup to WE# Going Low		10		10		10		ns
tWLWH	WE# Pulse Width		40		40		40		ns
tSHWH	WP# $V_{IH}$ Setup to WE# Going High	2	100		100		100		ns
tVPWH	VPP Setup to WE# Going High	2	100		100		100		ns
tAVWH	Address Setup to WE# Going High	3	40		40		40		ns
tDVWH	Data Setup to WE# Going High	3	40		40		40		ns
tWHDX	Data Hold from WE# High		5		5		5		ns
tWHAX	Address Hold from WE# High		5		5		5		ns
tWHEH	CE# Hold from WE# High		10		10		10		ns
tWHWL	WE# Pulse Width High		30		30		30		ns
tWHRL	WE# High to STS Going Low			90		90		90	ns
tWHGL	Write Recovery before Read		0		0		0		ns
tQVVL	VPP Hold from Valid SRD, STS High Z	2, 4	0		0		0		ns
tQVSL	WP# $V_{IH}$ Hold from Valid SRD, STS High Z	2, 4	0		0		0		ns

## NOTES :

1. Read timing characteristics during block erase, full chip erase, (multi) word/byte write and block lock-bit configuration operations are the same as during read-only operations. Refer to **Section 6.2.4 "AC CHARACTERISTICS"** for read-only operations.
2. Sampled, not 100% tested.
3. Refer to **Table 3** for valid AIN and DIN for block erase, full chip erase, (multi) word/byte write or block lock-bit configuration.
4. VPP should be held at VPPH1 until determination of block erase, full chip erase, (multi) word/byte write or block lock-bit configuration success (SR.1/3/4/5 = 0).
5. See **Fig. 12 "Transient Input/Output Reference Waveform"** and **Fig. 14 "Transient Equivalent Testing Load Circuit"** (High Speed Configuration) for testing characteristics.
6. See **Fig. 13 "Transient Input/Output Reference Waveform"** and **Fig. 14 "Transient Equivalent Testing Load Circuit"** (Standard Configuration) for testing characteristics.

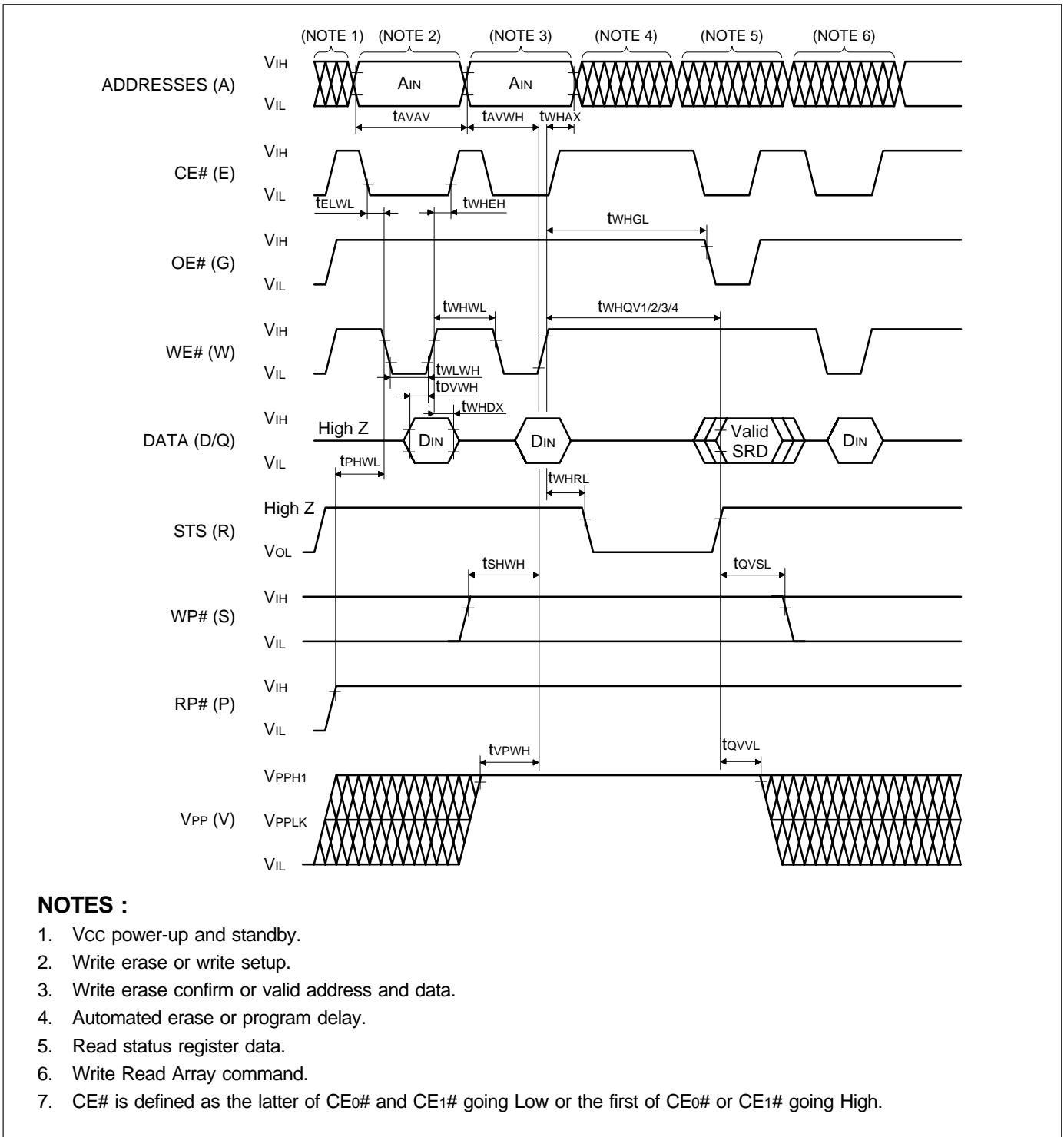


Fig. 17 AC Waveform for WE#-Controlled Write Operations

## 6.2.6 ALTERNATIVE CE#-CONTROLLED WRITES (NOTE 1)

## [LH28F160S5-L]

•  $V_{CC} = 5.0 \pm 0.25 \text{ V}$ ,  $5.0 \pm 0.5 \text{ V}$ ,  $T_A = 0 \text{ to } +70^\circ\text{C}$

VERSIONS		$V_{CC} \pm 0.25 \text{ V}$	(NOTE 5) LH28F160S5-L70				(NOTE 6) LH28F160S5-L70		(NOTE 6) LH28F160S5-L10		UNIT
		$V_{CC} \pm 0.5 \text{ V}$				MIN.	MAX.	MIN.	MAX.		
SYMBOL	PARAMETER	NOTE	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tAVAV	Write Cycle Time		70		80		100				ns
tPHEL	RP# High Recovery to CE# Going Low	2	1		1		1		1		$\mu\text{s}$
tWLEL	WE# Setup to CE# Going Low		0		0		0		0		ns
tELEH	CE# Pulse Width		50		50		50		50		ns
tSHEH	WP# $V_{IH}$ Setup to CE# Going High	2	100		100		100		100		ns
tVPEH	VPP Setup to CE# Going High	2	100		100		100		100		ns
tAVEH	Address Setup to CE# Going High	3	40		40		40		40		ns
tDVEH	Data Setup to CE# Going High	3	40		40		40		40		ns
tEHDX	Data Hold from CE# High		5		5		5		5		ns
tEHAX	Address Hold from CE# High		5		5		5		5		ns
tEHWL	WE# Hold from CE# High		0		0		0		0		ns
tEHEL	CE# Pulse Width High		25		25		25		25		ns
tEHRL	CE# High to STS Going Low			90		90			90		ns
tEHGL	Write Recovery before Read		0		0		0		0		ns
tQVVL	VPP Hold from Valid SRD, STS High Z	2, 4	0		0		0		0		ns
tQVSL	WP# $V_{IH}$ Hold from Valid SRD, STS High Z	2, 4	0		0		0		0		ns

## NOTES :

- In systems where CE# defines the write pulse width (within a longer WE# timing waveform), all setup, hold and inactive WE# times should be measured relative to the CE# waveform.
- Sampled, not 100% tested.
- Refer to **Table 3** for valid AIN and DIN for block erase, full chip erase, (multi) word/byte write or block lock-bit configuration.
- VPP should be held at VPPH1 until determination of block erase, full chip erase, (multi) word/byte write or block lock-bit configuration success (SR.1/3/4/5 = 0).
- See **Fig. 12** "Transient Input/Output Reference Waveform" and **Fig. 14** "Transient Equivalent Testing Load Circuit" (High Speed Configuration) for testing characteristics.
- See **Fig. 13** "Transient Input/Output Reference Waveform" and **Fig. 14** "Transient Equivalent Testing Load Circuit" (Standard Configuration) for testing characteristics.

## 6.2.6 ALTERNATIVE CE#-CONTROLLED WRITES (contd.) (NOTE 1)

## [LH28F160S5H-L]

•  $V_{CC} = 5.0 \pm 0.25 \text{ V}$ ,  $5.0 \pm 0.5 \text{ V}$ ,  $T_A = -40 \text{ to } +85^\circ\text{C}$

VERSIONS		$V_{CC} \pm 0.25 \text{ V}$	(NOTE 5) LH28F160S5H-L70						UNIT
		$V_{CC} \pm 0.5 \text{ V}$			(NOTE 6) LH28F160S5H-L70		(NOTE 6) LH28F160S5H-L10		
SYMBOL	PARAMETER	NOTE	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tAVAV	Write Cycle Time		70		90		100		ns
tPHEL	RP# High Recovery to CE# Going Low	2	1		1		1		$\mu\text{s}$
tWLEL	WE# Setup to CE# Going Low		0		0		0		ns
tELEH	CE# Pulse Width		50		50		50		ns
tSHEH	WP# $V_{IH}$ Setup to CE# Going High	2	100		100		100		ns
tVPEH	VPP Setup to CE# Going High	2	100		100		100		ns
tAVEH	Address Setup to CE# Going High	3	40		40		40		ns
tDVEH	Data Setup to CE# Going High	3	40		40		40		ns
tEHDX	Data Hold from CE# High		5		5		5		ns
tEHAX	Address Hold from CE# High		5		5		5		ns
tEHWL	WE# Hold from CE# High		0		0		0		ns
tEHEL	CE# Pulse Width High		25		25		25		ns
tEHL	CE# High to STS Going Low			90		90		90	ns
tEHL	Write Recovery before Read		0		0		0		ns
tQVVL	VPP Hold from Valid SRD, STS High Z	2, 4	0		0		0		ns
tQVSL	WP# $V_{IH}$ Hold from Valid SRD, STS High Z	2, 4	0		0		0		ns

## NOTES :

- In systems where CE# defines the write pulse width (within a longer WE# timing waveform), all setup, hold and inactive WE# times should be measured relative to the CE# waveform.
- Sampled, not 100% tested.
- Refer to **Table 3** for valid AIN and DIN for block erase, full chip erase, (multi) word/byte write or block lock-bit configuration.
- VPP should be held at VPPH1 until determination of block erase, full chip erase, (multi) word/byte write or block lock-bit configuration success (SR.1/3/4/5 = 0).
- See **Fig. 12 "Transient Input/Output Reference Waveform"** and **Fig. 14 "Transient Equivalent Testing Load Circuit"** (High Speed Configuration) for testing characteristics.
- See **Fig. 13 "Transient Input/Output Reference Waveform"** and **Fig. 14 "Transient Equivalent Testing Load Circuit"** (Standard Configuration) for testing characteristics.

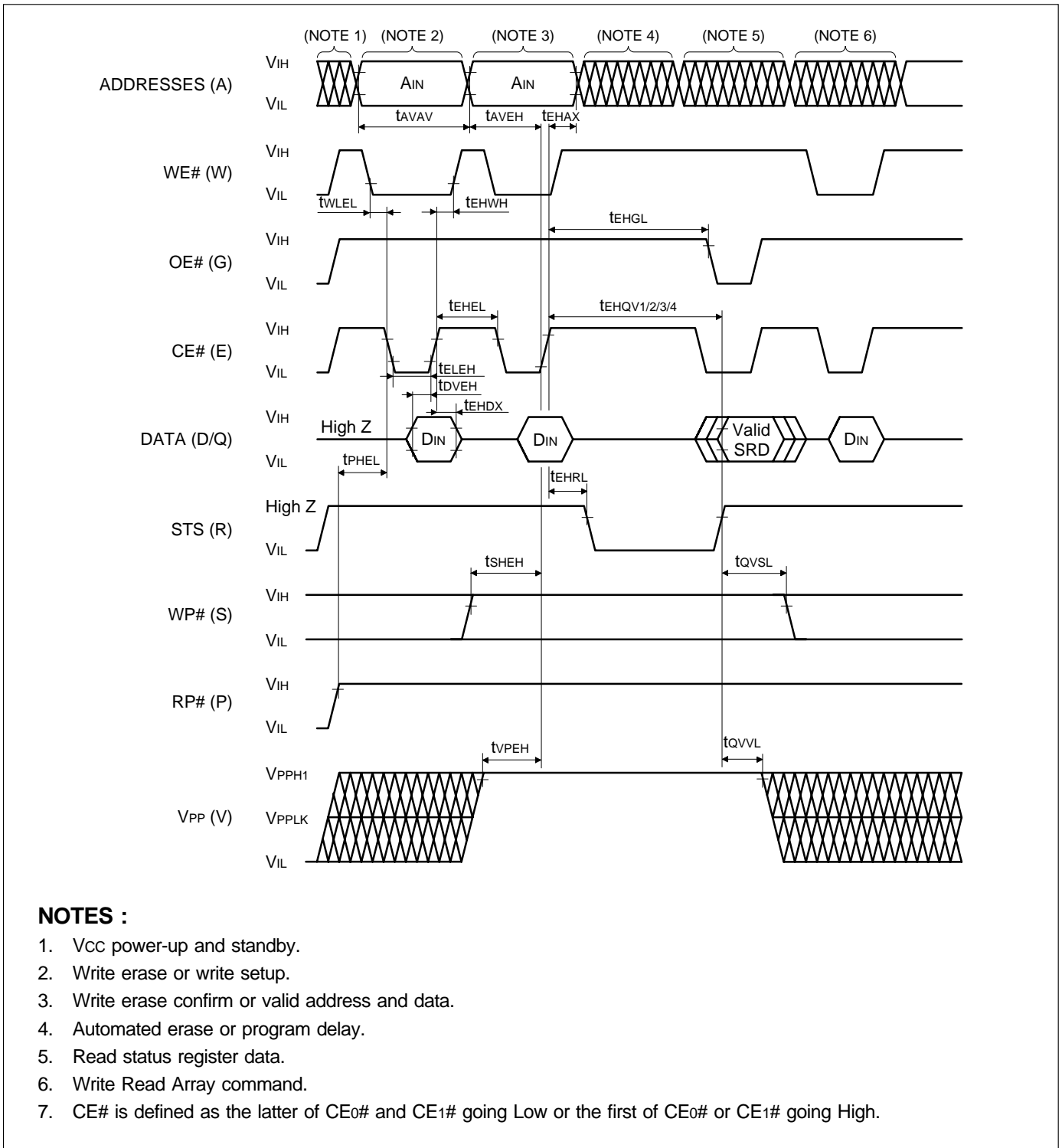


Fig. 18 AC Waveform for CE#-Controlled Write Operations



6.2.7 RESET OPERATIONS

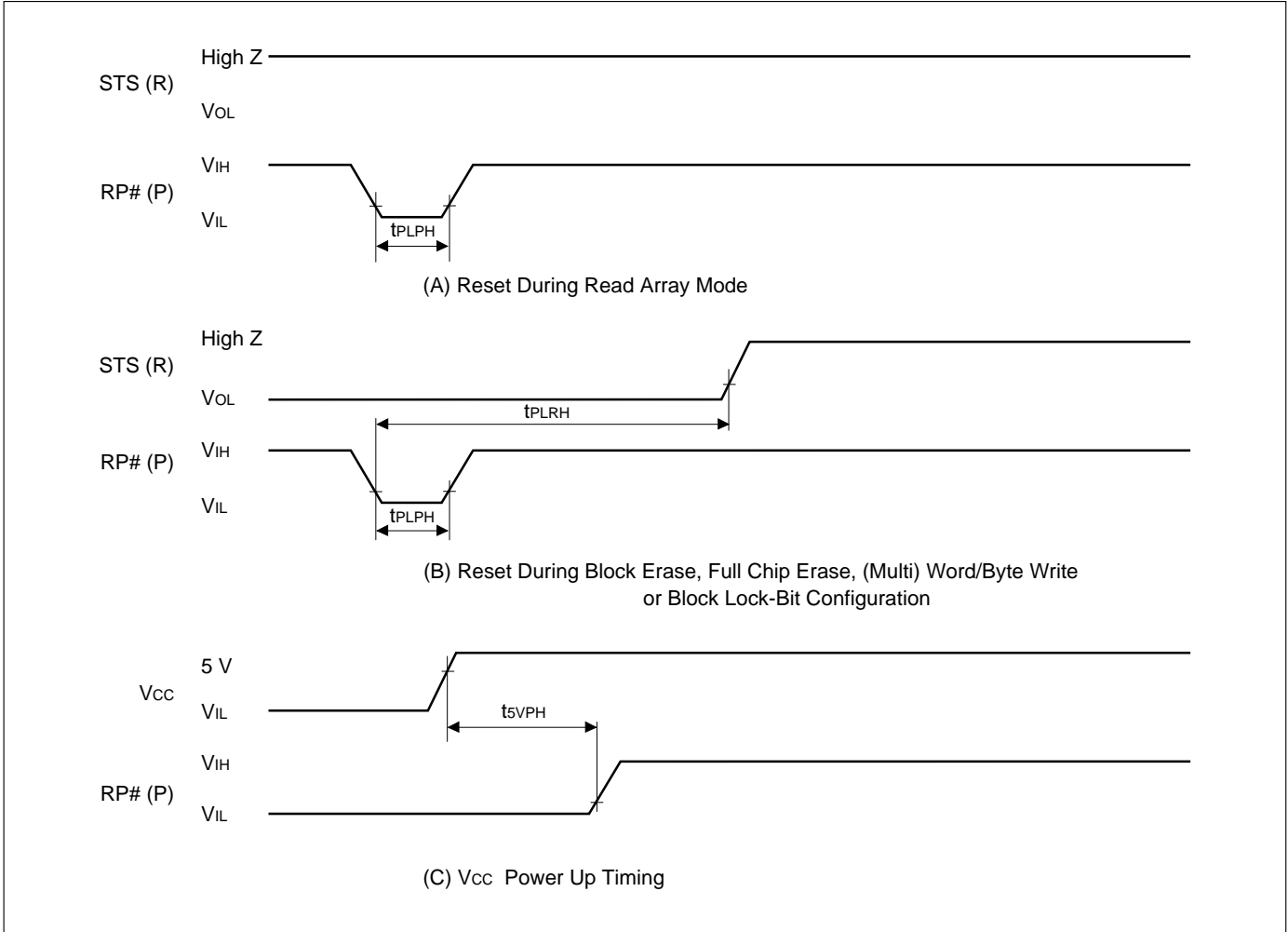


Fig. 19 AC Waveform for Reset Operation

Reset AC Specifications (NOTE 1)

SYMBOL	PARAMETER	NOTE	V <sub>CC</sub> = 5.0±0.5 V		UNIT
			MIN.	MAX.	
t <sub>PLPH</sub>	RP# Pulse Low Time (If RP# is tied to V <sub>CC</sub> , this specification is not applicable)		100		ns
t <sub>PLRH</sub>	RP# Low to Reset during Block Erase, Full Chip Erase, (Multi) Word/Byte Write or Block Lock-Bit Configuration	2, 3		13.1	µs
t <sub>5VPH</sub>	V <sub>CC</sub> 4.5 V to RP# High	4	100		ns

NOTES :

1. These specifications are valid for all product versions (packages and speeds).
2. If RP# is asserted while a block erase, full chip erase, (multi) word/byte write or block lock-bit configuration operation is not executing, the reset will complete within 100 ns.
3. A reset time, t<sub>PHQV</sub>, is required from the latter of STS going High Z or RP# going high until outputs are valid.
4. When the device power-up, holding RP#-low minimum 100 ns is required after V<sub>CC</sub> has been in predefined range and also has been in stable there.

## 6.2.8 BLOCK ERASE, FULL CHIP ERASE, (MULTI) WORD/BYTE WRITE AND BLOCK LOCK-BIT CONFIGURATION PERFORMANCE (NOTE 3, 4)

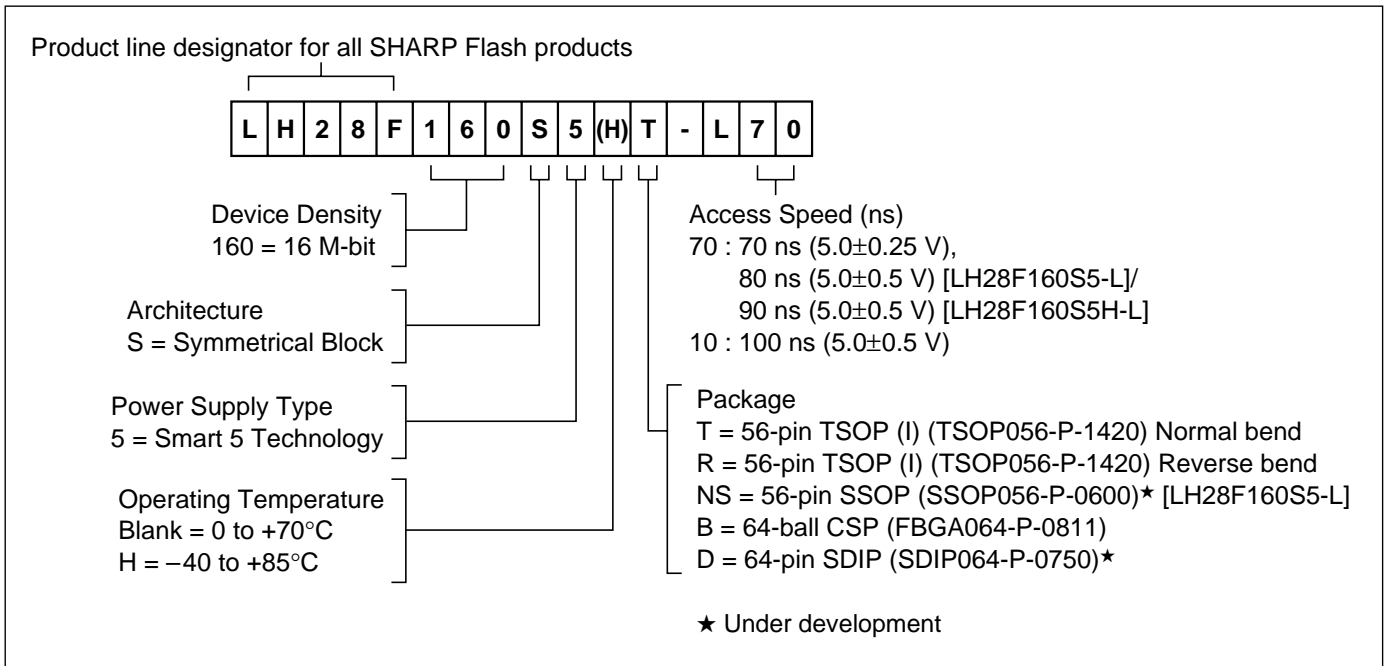
•  $V_{CC} = 5.0 \pm 0.25 \text{ V}$ ,  $5.0 \pm 0.5 \text{ V}$ ,  $T_A = 0 \text{ to } +70^\circ\text{C}$  or  $-40 \text{ to } +85^\circ\text{C}$

SYMBOL	PARAMETER	NOTE	$V_{CC} = 5.0 \pm 0.5 \text{ V}$			UNIT
			MIN.	TYP. (NOTE 1)	MAX.	
t <sub>WHQV1</sub> t <sub>EHQV1</sub>	Word/Byte Write Time (using W/B write, in word mode)	2		9.24	TBD	μs
t <sub>WHQV1</sub> t <sub>EHQV1</sub>	Word/Byte Write Time (using W/B write, in byte mode)	2		9.24	TBD	μs
	Word/Byte Write Time (using multi word/byte write)	2		2	TBD	μs
	Block Write Time (using W/B write, in word mode)	2		0.31	3.7	s
	Block Write Time (using W/B write, in byte mode)	2		0.61	7.5	s
	Block Write Time (using multi word/byte write)	2		0.13	1.5	s
t <sub>WHQV2</sub> t <sub>EHQV2</sub>	Block Erase Time	2		0.34	10	s
	Full Chip Erase Time			10.9	TBD	s
t <sub>WHQV3</sub> t <sub>EHQV3</sub>	Set Block Lock-Bit Time	2		9.24	TBD	μs
t <sub>WHQV4</sub> t <sub>EHQV4</sub>	Clear Block Lock-Bits Time	2		0.34	TBD	s
t <sub>WHRH1</sub> t <sub>EHRH1</sub>	Write Suspend Latency Time to Read			5.6	7	μs
t <sub>WHRH2</sub> t <sub>EHRH2</sub>	Erase Suspend Latency Time to Read			9.4	13.1	μs

### NOTES :

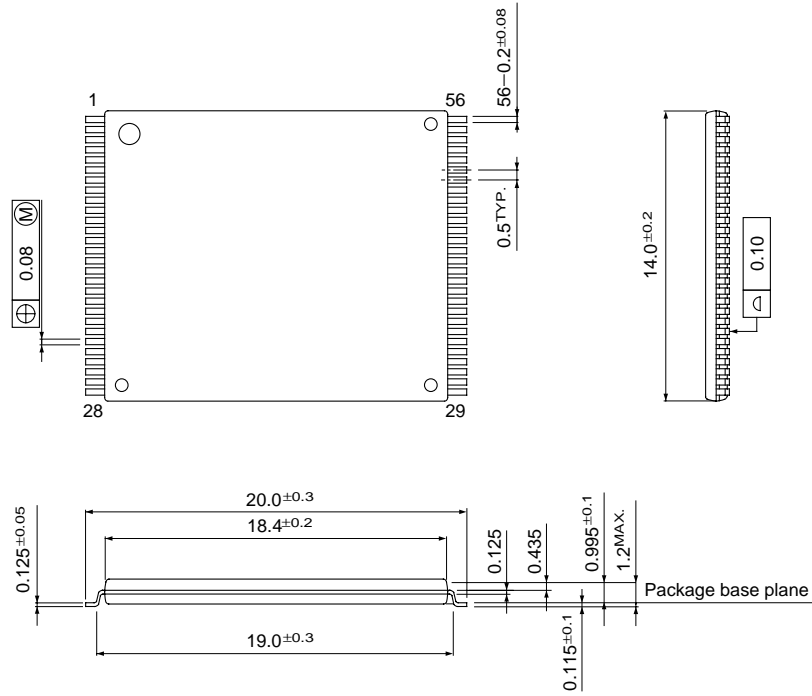
1. Typical values measured at  $T_A = +25^\circ\text{C}$  and nominal voltages. Assumes corresponding block lock-bits are not set. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. These performance numbers are valid for all speed versions.
4. Sampled, not 100% tested.

## 7 ORDERING INFORMATION

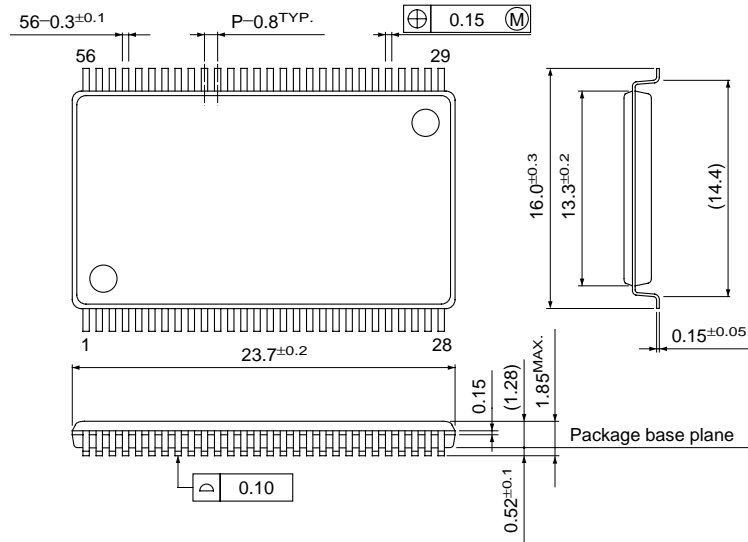


OPTION	ORDER CODE	VALID OPERATIONAL COMBINATIONS	
		V <sub>CC</sub> = 5.0±0.5 V 100 pF load, TTL I/O Levels	V <sub>CC</sub> = 5.0±0.25 V 30 pF load, 1.5 V I/O Levels
1	LH28F160S5X-L70	80 ns	70 ns
2	LH28F160S5HX-L70	90 ns	70 ns
3	LH28F160S5XX-L10	100 ns	

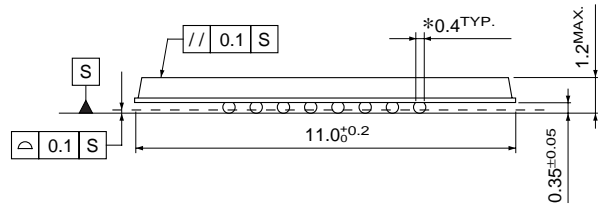
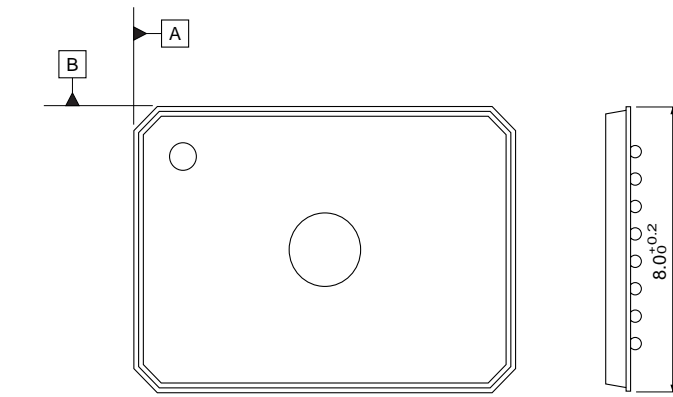
### 56 TSOP (TSOP056-P-1420)



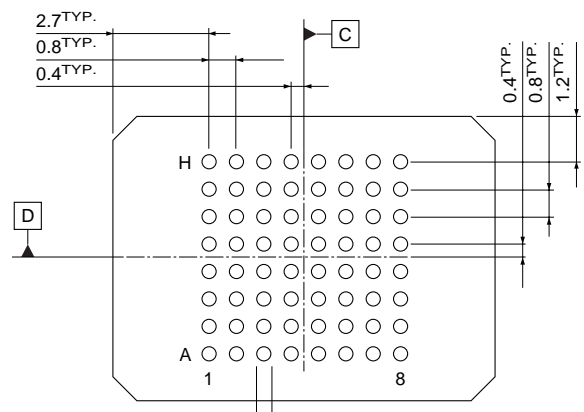
## 56 SSOP (SSOP056-P-0600)



### 64 CSP (FBGA064-P-0811)



\*Land hole diameter for ball mounting

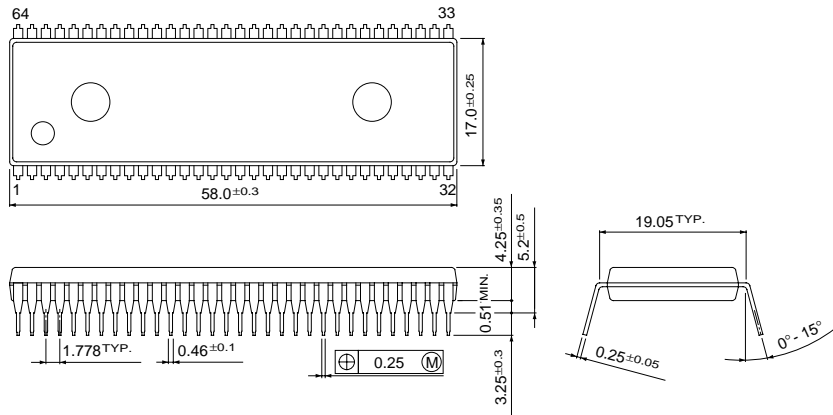


⊕	φ0.30	(M)	S	AB
⊕	φ0.15	(M)	S	CD

# Package Outline

(Unit : mm)

## 64 SDIP (SDIP064-P-0750)



- SDIP : Shrink DIP\*
- SOP : Small Outline Package
- SSOP : Shrink SOP
- TSOP : Thin SOP
- CSP : Chip Size Package (FBGA)
- \*DIP : Dual In-line Package