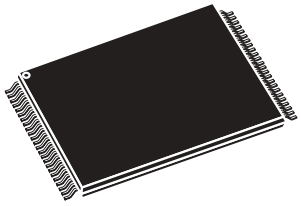
NAND08GW3C2A
NAND16GW3C4A

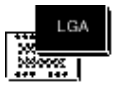
8/16 Gbit, 2112 byte page, 3 V supply, multilevel, multiplane, NAND Flash memory

Features

- High density multilevel cell (MLC) Flash memory
  - Up to 16 Gbit memory array
  - Up to 512 Mbit spare area
  - Cost-effective solutions for mass storage applications
- NAND interface
  - x 8 bus width
  - Multiplexed address/data
- Supply voltage: V_{DD} = 2.7 to 3.6 V
- Page size: (2048 + 64 spare) bytes
- Block size: (256K + 8K spare) bytes
- Multiplane architecture
  - Array split into two independent planes
  - Program/erase operations can be performed on both planes at the same time
- Page read/program
  - Random access: 60 µs (max)
  - Sequential access: 25 ns (min)
  - Page program operation time: 800 µs (typ)
- Multipage program time (2 pages): 800 µs (typ)
- Fast block erase
  - Block erase time: 2.5 ms (typ)
- Multiblock erase time (2 blocks): 2.5 ms (typ)
- Status register
- Electronic signature
- Serial number option
- Chip enable ‘don’t care’



TSOP48 12 x 20 mm (N)



LGA52 12 x 17 mm (N)

- Data protection
  - Hardware program/erase locked during power transitions
- Development tools
  - Error correction code models
  - Bad block management and wear leveling algorithm
  - HW simulation models
- Data integrity
  - 10,000 program/erase cycles (with ECC)
  - 10 years data retention
- ECOPACK® packages available

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1 Description

The NAND08GW3C2A and NAND16GW3C2A are multilevel cell (MLC) devices from the NAND Flash 2112-byte page family of non-volatile Flash memories. The NAND08GW3C2A and the NAND16GW3C2A have a density of 8- and 16-Gbit, respectively. The NAND16GW3C2A is composed of two 8-Gbit dice; each die can be accessed independently using two Chip Enable and two Ready/Busy signals. The devices operate from a 3 V VDD power supply.

The address lines are multiplexed with the Data Input/Output signals on a multiplexed x8 input/output bus. This interface reduces the pin count and makes it possible to migrate to other densities without changing the footprint.

Each block can be programmed and erased over 10,000 cycles (with ECC on). The device also has hardware security features; a write protect pin is available to give hardware protection against Program and Erase operations.

The devices feature an open-drain, ready/busy output that can be used to identify if the Program/Erase/Read (P/E/R) Controller is currently active. The use of an open-drain output allows the ready/busy pins of several memories to be connected to a single pull-up resistor.

The memory array is split into 2 planes of 2048 blocks each. This multiplane architecture makes it possible to program 2 pages at a time (one in each plane) or to erase 2 blocks at a time (one in each plane), dividing by two the average program and erase times.

The devices have the Chip Enable “Don’t Care” feature, which allows code to be directly downloaded by a microcontroller, as Chip Enable transitions during the latency time do not stop the Read operation.

There is the option of a unique identifier (serial number), which allows the NAND08GW3C2A and the NAND16GW3C2A to be uniquely identified. It is subject to an NDA (non-disclosure agreement) and is, therefore, not described in the datasheet. For more details of this option contact your nearest Numonyx Sales office.

The devices are available in TSOP48 (12 × 20 mm) and LGA52 (12 x 17 x 0.65 mm) packages. To meet environmental requirements, Numonyx offers the devices in ECOPACK® packages. ECOPACK packages are lead-free. In compliance with JEDEC Standard JESD97, the category of second level interconnect is marked on the package and on the inner box label. The maximum ratings related to soldering conditions are also marked on the inner box label.

The devices are shipped from the factory with block 0 always valid and the memory content bits, in valid blocks, erased to ‘1’.

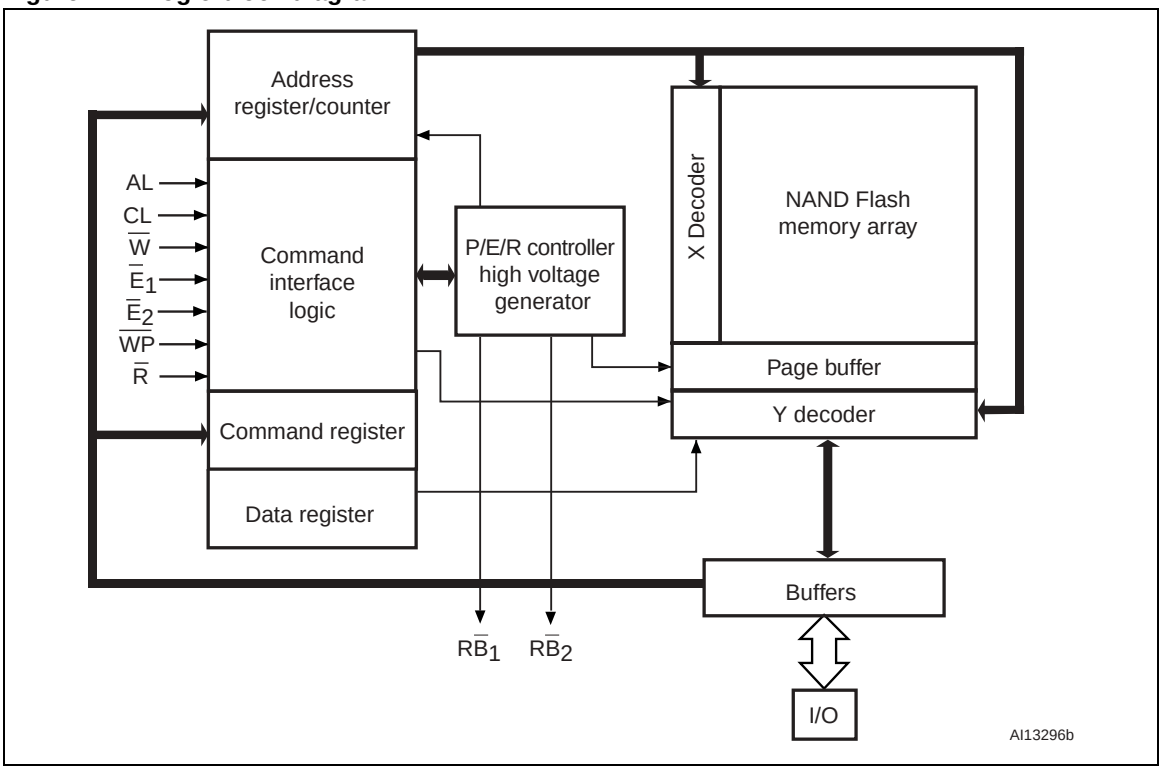
Refer to the list of available part numbers and to *Table 24: Ordering information scheme* for information on how to order these options.

Table 1. Device summary

Part number	Density	Bus width	Page size	Block size	Memory array	Operating voltage (V_{DD})	Timings				Package
							Random access time (max)	Sequential access time (min)	Page program (typ)	Block erase (typ)	
NAND08GW3C2A	8 Gb	x 8	2048+64 bytes	256 K + 8 K bytes	128 pages x 4096 blocks	2.7 to 3.6 V	60 µs	25 ns	800 µs	2.5 ms	TSOP48 ULGA52
NAND16GW3C4A(1)	16 Gb				128 pages x 8192 blocks						TSOP48 ULGA52

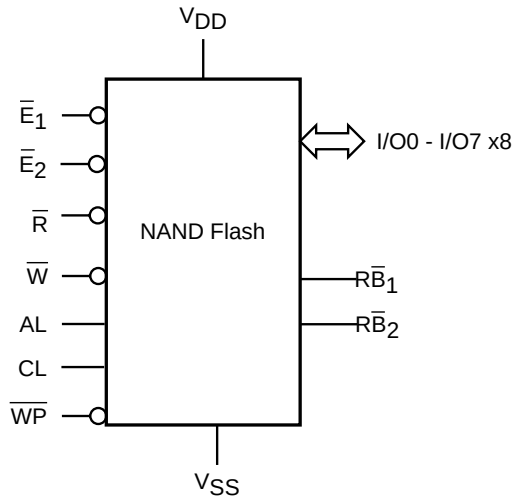
1. The NAND16GW3C2A is composed of two 8-Gbit dice.

Figure 1. Logic block diagram



1. $\overline{E}2$ and $R\overline{B}2$ are only present in the NAND16GW3C4A.

Figure 2. Logic diagram



1. $\overline{E}2$ and $R\overline{B}2$ are only present in the NAND16GW3C4A.

Table 2. Signal names

Signal	Function	Direction
I/O0 - I/O7	Data input/outputs(1)	Input/output
CL	Command Latch Enable	Input
AL	Address Latch Enable	Input
$\overline{E}_1$, $\overline{E}_2$	Chip Enable(2)	Input
$\overline{R}$	Read Enable	Input
$\overline{W}$	Write Enable	Input
$\overline{WP}$	Write Protect	Input
$R\overline{B}_1$, $R\overline{B}_2$	Ready/Busy (open drain output)(2)	Output
V_{DD}	Power supply	Power supply
V_{SS}	Ground	Ground
NC	No connection	
DU	Do not use	

1. On the LGA52 package, each 8-Gbit die is accessed and controlled via two sets of I/Os and control signals.
2. $\overline{E}2$ and $R\overline{B}2$ are only present in the NAND16GW3C4A.

Figure 3. TSOP48 connections for NAND08GW3C2A

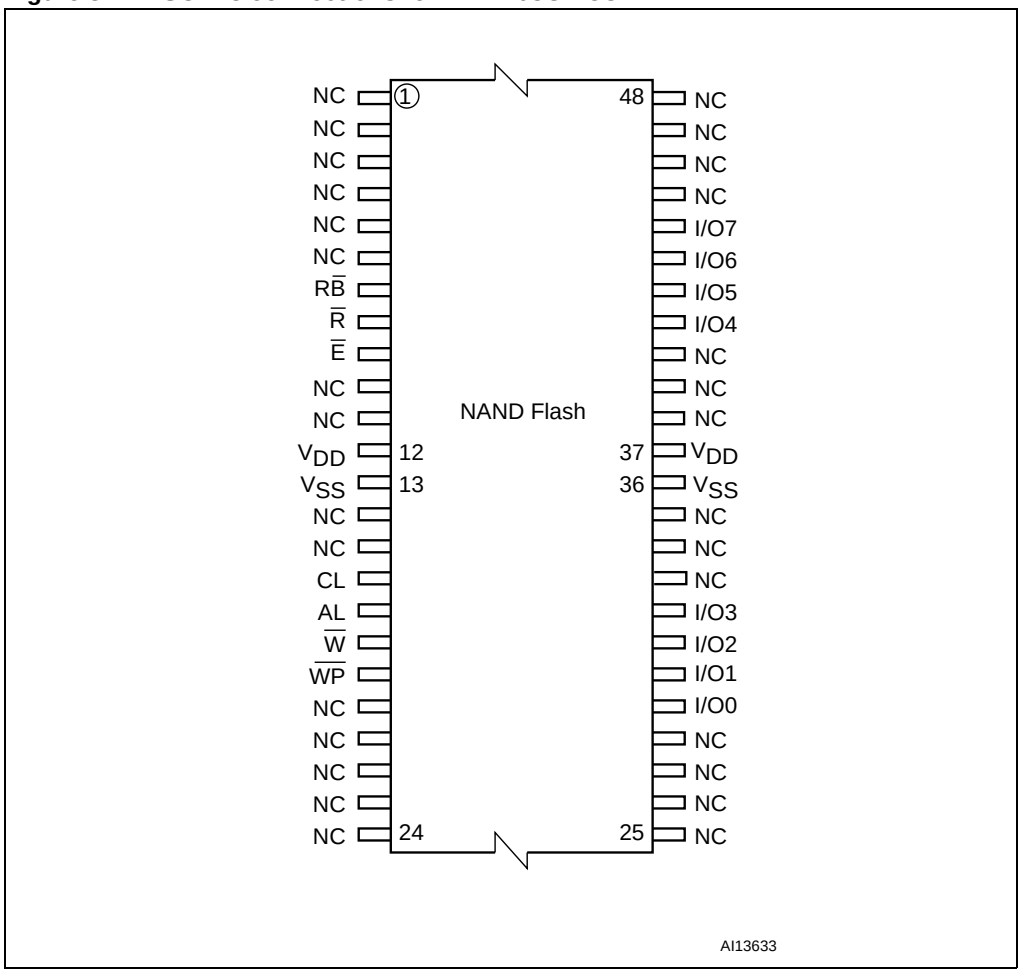


Figure 4. TSOP48 connections for NAND16GW3C4A

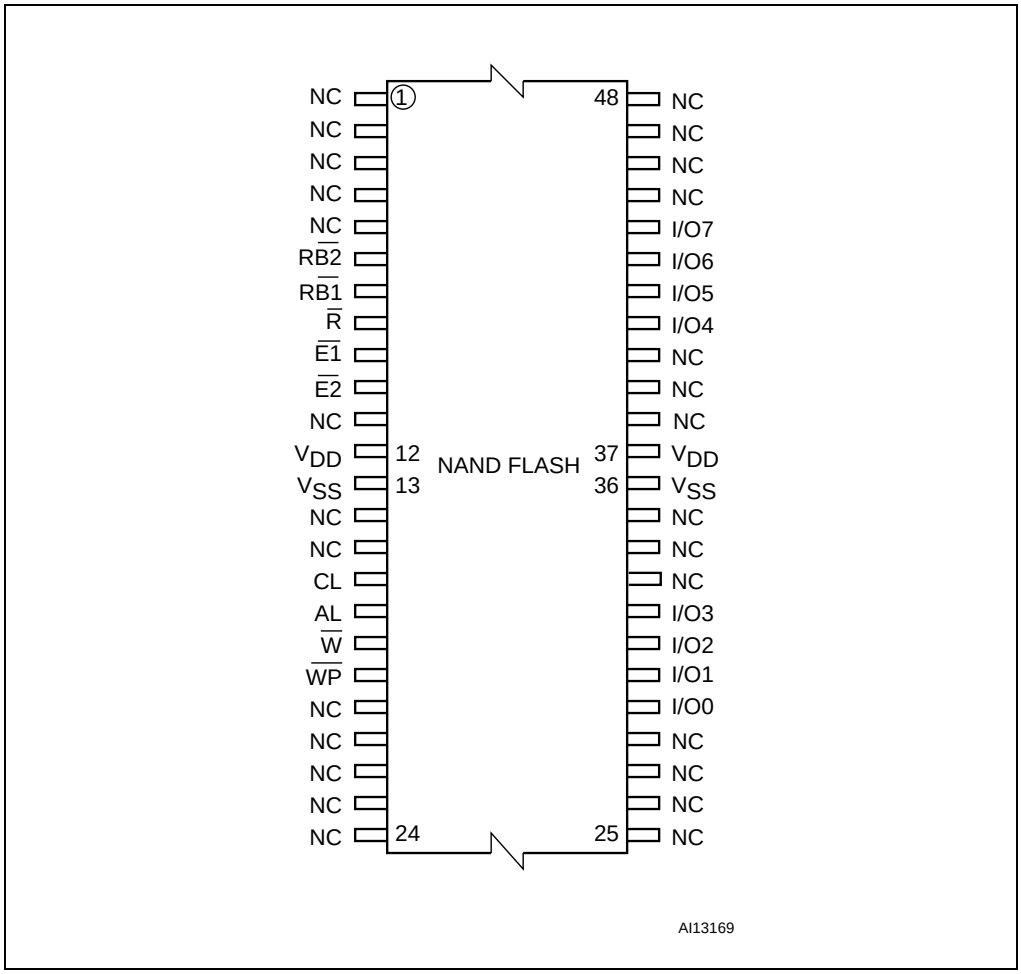
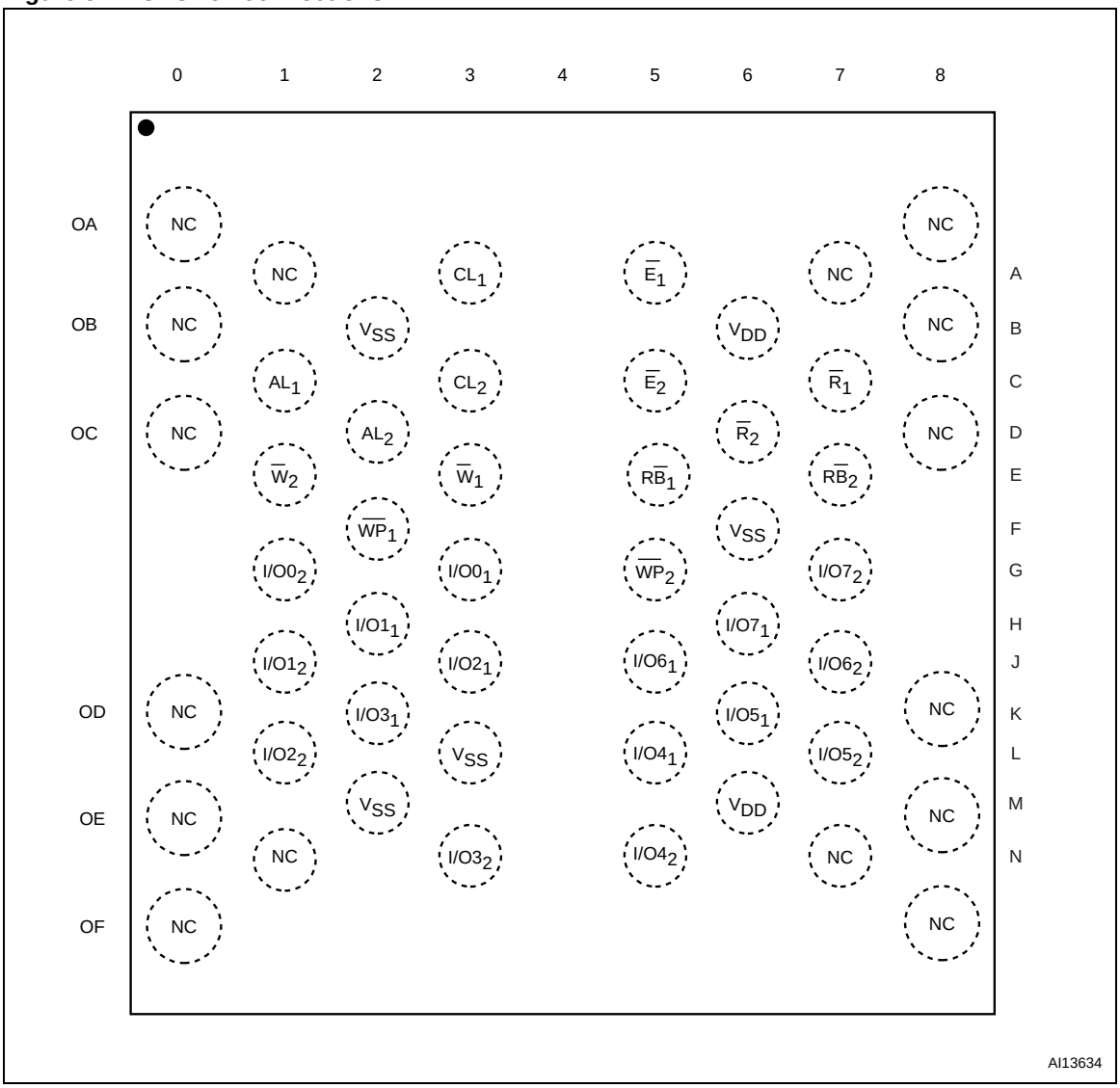


Figure 5. ULGA52 connections



1. On the LGA52 package, each 8-Gbit die is accessed and controlled via two sets of signals.

2 Memory array organization

The memory array is comprised of NAND structures where 32 cells are connected in series.

The memory array is organized in blocks where each block contains 128 pages. The array is split into two areas, the main area and the spare area. The main area of the array is used to store data, whereas the spare area is typically used to store software flags or bad block identification.

The pages are split into a 2048-byte main area and a spare area of 64 bytes. Refer to *Figure 6: Memory array organization*.

2.1 Bad blocks

The NAND08GW3C2A and NAND16GW3C2A devices may contain bad blocks, where the reliability of blocks that contain one or more invalid bits is not guaranteed. Additional bad blocks may develop during the lifetime of the device.

The bad block Information is written prior to shipping (refer to *Section 9.1: Bad block management* for more details).

Table 3: Valid blocks shows the minimum number of valid blocks in each device. The values shown include both the bad blocks that are present when the device is shipped and the bad blocks that could develop later on.

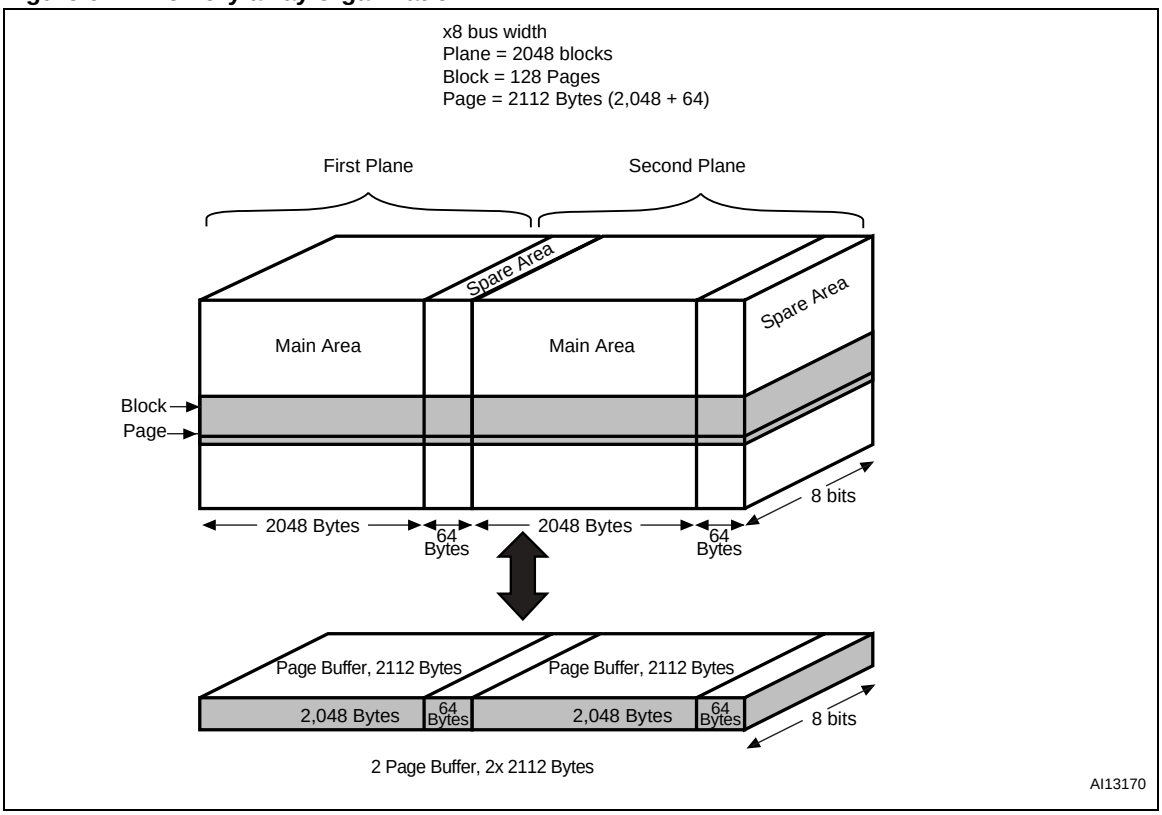
These blocks need to be managed using Bad Blocks Management and Block Replacement (refer to *Section 9: Software algorithms*).

Table 3. Valid blocks(1)

Density of device	Minimum	Maximum
8 Gbits	4016	4096
16 Gbits	8032	8192

1. The NAND16GW3C4A is composed of two 8-Gbit dice. The minimum number of valid blocks is 4096 for each die.

Figure 6. Memory array organization



3 Signal descriptions

See *Figure 1: Logic block diagram*, and *Table 2: Signal names*, for a brief overview of the signals connected to this device.

3.1 Inputs/outputs (I/O0-I/O7)

Input/outputs 0 to 7 are used to input the selected address, output the data during a Read operation, or input a command or data during a Write operation. The inputs are latched on the rising edge of Write Enable. I/O0-I/O7 are left floating when the device is deselected or the outputs are disabled.

3.2 Address Latch Enable (AL)

The Address Latch Enable activates the latching of the address inputs in the command interface. When AL is High, the inputs are latched on the rising edge of Write Enable.

3.3 Command Latch Enable (CL)

The Command Latch Enable activates the latching of the command inputs in the command interface. When CL is High, the inputs are latched on the rising edge of Write Enable.

3.4 Chip Enable ($\overline{E}_1$, $\overline{E}_2$)

The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is Low, V_{IL}, the device is selected. If Chip Enable goes High, v_{IH}, while the device is busy, the device remains selected and does not go into standby mode.

$\overline{E}_2$ is only available on the NAND16GW3C4A.

3.5 Read Enable ($\overline{R}$)

The Read Enable pin, $\overline{R}$, controls the sequential data output during Read operations. Data is valid t_{RLQV} after the falling edge of $\overline{R}$. The falling edge of $\overline{R}$ also increments the internal column address counter by one.

3.6 Write Enable ($\overline{W}$)

The Write Enable input, $\overline{W}$, controls writing to the command interface, input address and data latches. Both addresses and data are latched on the rising edge of Write Enable.

During power-up and power-down a recovery time of 10 µs (min) is required before the command interface is ready to accept a command. It is recommended to keep Write Enable High during the recovery time.

3.7 Write Protect ($\overline{WP}$)

The Write Protect pin is an input that gives a hardware protection against unwanted Program or Erase operations. When Write Protect is Low, V_{IL}, the device does not accept any Program or Erase operations.

It is recommended to keep the Write Protect pin Low, V_{IL}, during power-up and power-down.

3.8 Ready/Busy ($R\overline{B}_1$, $R\overline{B}_2$)

The Ready/Busy output, $R\overline{B}$, is an open-drain output that can be used to identify if the P/E/R controller is currently active.

When Ready/Busy is Low, V_{OL}, a Read, Program or Erase operation is in progress. When the operation completes, Ready/Busy goes High, V_{OH}.

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A Low will then indicate that one, or more, of the memories is busy.

During power-up and power-down a minimum recovery time of 10 µs is required before the command interface is ready to accept a command. During this period the Ready/Busy signal is Low, V_{OL}.

$R\overline{B}_2$ is only available on the NAND16GW3C4A.

Refer to *Section 12.1: Ready/Busy signal electrical characteristics* for details on how to calculate the value of the pull-up resistor.

3.9 V_{DD} supply voltage

V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for operations (Read, Program and Erase).

3.10 V_{SS} ground

Ground, $V_{SS,}$ is the reference for the power supply. It must be connected to the system ground.

4 Bus operations

There are six standard bus operations that control the memory. Each of these is described in this section. See the summary in *Table 4: Bus operations*.

Typically, glitches of less than 5 ns on Chip Enable, Write Enable and Read Enable are ignored by the memory and do not affect bus operations.

4.1 Command Input

Command Input bus operations are used to give commands to the memory. Commands are accepted when Chip Enable is Low, Command Latch Enable is High, Address Latch Enable is Low and Read Enable is High. They are latched on the rising edge of the Write Enable signal.

Only I/O0 to I/O7 are used to input commands.

See *Figure 16* and *Table 20* for details of the timings requirements.

4.2 Address Input

Address Input bus operations are used to input the memory addresses. Five bus cycles are required to input the addresses (refer to *Table 5: Address insertion*).

The addresses are accepted when Chip Enable is Low, Address Latch Enable is High, Command Latch Enable is Low and Read Enable is High. They are latched on the rising edge of the Write Enable signal. Only I/O0 to I/O7 are used to input addresses.

See *Figure 17* and *Table 20* for details of the timings requirements.

4.3 Data Input

Data Input bus operations are used to input the data to be programmed. Data is only accepted when Chip Enable is Low, Address Latch Enable is Low, Command Latch Enable is Low and Read Enable is High. The data is latched on the rising edge of the Write Enable signal. The data is input sequentially using the Write Enable signal.

See *Figure 18* and *Table 20* for details of the timing requirements.

4.4 Data Output

Data Output bus operations are used to read: the data in the memory array, the status register, the electronic signature and the unique identifier.

Data is output when Chip Enable is Low, Write Enable is High, Address Latch Enable is Low, and Command Latch Enable is Low.

The data is output sequentially using the Read Enable signal.

If the Read Enable pulse frequency is lower then 33 MHz (t_{RLRL} higher than 30 ns), the output data is latched on the rising edge of Read Enable signal (see *Figure 19*).

For higher frequencies (t_{RLRL} lower than 30 ns), the Extended Data Out (EDO) mode must be considered. In this mode, data output is valid on the input/output bus for a time of t_{RLQX} after the falling edge of Read Enable signal (see *Figure 20*).

See *Table 21* for details on the timings requirements.

4.5 Write Protect

Write Protect bus operations are used to protect the memory against Program or Erase operations. When the Write Protect signal is Low the device does not accept Program or Erase operations, therefore, the contents of the memory array cannot be altered. The Write Protect signal is not latched by Write Enable to ensure protection, even during power-up.

4.6 Standby

The memory enters Standby mode by driving Chip Enable, $\overline{E}$, High. In Standby mode, the device is deselected, outputs are disabled and power consumption is reduced.

Table 4. Bus operations

Bus operation	$\overline{E}$	AL	CL	$\overline{R}$	$\overline{W}$	$\overline{WP}$	I/O0 - I/O7
Command input	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Rising	X(1)	Command
Address input	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Rising	X	Address
Data input	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Rising	V_{IH}	Data input
Data output	V_{IL}	V_{IL}	V_{IL}	Falling	V_{IH}	X	Data output
Write protect	X	X	X	X	X	V_{IL}	X
Standby	V_{IH}	X	X	X	X	V_{IL}/V_{DD}	X

1. $\overline{WP}$ must be V_{IH} when issuing a program or erase command.

Table 5. Address insertion(1)

Bus Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st	A7	A6	A5	A4	A3	A2	A1	A0
2nd	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A11	A10	A9	A8
3rd	A19	A18	A17	A16	A15	A14	A13	A12
4th	A27	A26	A25	A24	A23	A22	A21	A20
5th	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A31(2)	A30	A29	A28

1. Any additional address input cycles will be ignored.
2. A31 is valid only for the NAND16GW3C2A.

Table 6. Address definitions

Address	Definition
A0 - A11	Column address
A12 - A18	Page address
A19 - A31	Block address

5 Command set

All bus write operations to the device are interpreted by the command interface. The commands are input on I/O0-I/O7 and are latched on the rising edge of Write Enable when the Command Latch Enable signal is High. Device operations are selected by writing specific commands to the Command Register. The two-step command sequences for Program and Erase operations are imposed to maximize data security.

The commands are summarized in *Table 7: Commands*.

Table 7. Commands

Command	Bus write operations(1)				Commands accepted during busy
	1st cycle	2nd cycle	3rd cycle	4th cycle	
Read	00h	30h	–	–	
Random Data Output	05h	E0h	–	–	
Page Program (sequential input default)	80h	10h	–	–	
Multiplane Page Program	80h	11h	81h	10h	
Random Data Input	85h	–	–	–	
Block Erase	60h	D0h	–	–	
Multiplane Block Erase	60h	60h	D0h	–	
Reset	FFh	–	–	–	Yes
Read Electronic Signature	90h	–	–	–	
Read Status Register	70h	–	–	–	Yes

1. The bus cycles are only shown for issuing the codes. The cycles required to input the addresses or input/output data are not shown.

6 Device operations

This section gives the details of the device operations.

6.1 Read Memory Array

At power-up the device defaults to Read mode. To enter Read mode from another mode the Read command must be issued, see *Table 7: Commands*. Once a Read command is issued, subsequent consecutive Read commands only require the confirm command code (30h).

Once a Read command is issued, two types of operations are available: Random Read and Page Read.

6.2 Random Read

Each time the Read command is issued, the first read is random-read.

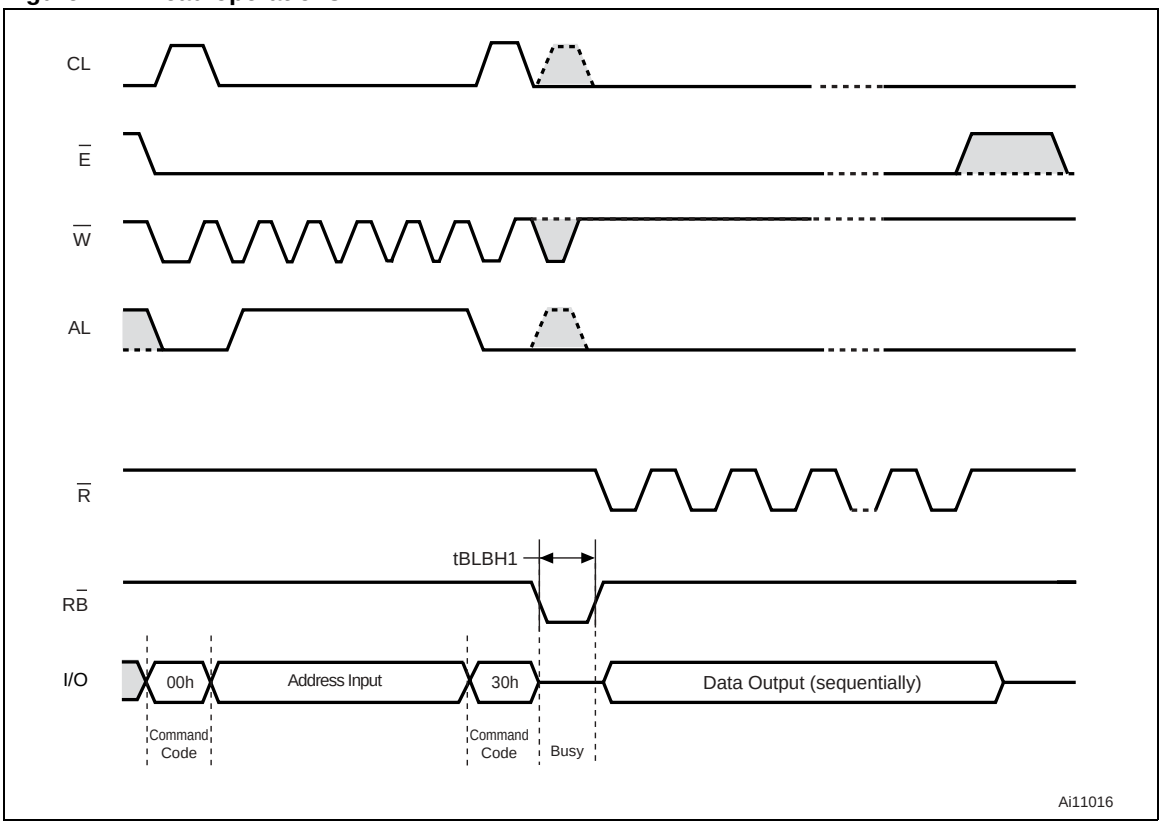
6.3 Page Read

After the first random read access, the page data (2112 bytes) is transferred to the page buffer in a time of t_{WHBH} (refer to *Table 21* for value). Once the transfer is complete, the Ready/Busy signal goes High. The data can then be read out sequentially (from the selected column address to last column address) by pulsing the Read Enable signal.

The device can output random data in a page, instead of the consecutive sequential data, by issuing a Random Data Output command. The Random Data Output command can be used to skip some data during a sequential data output.

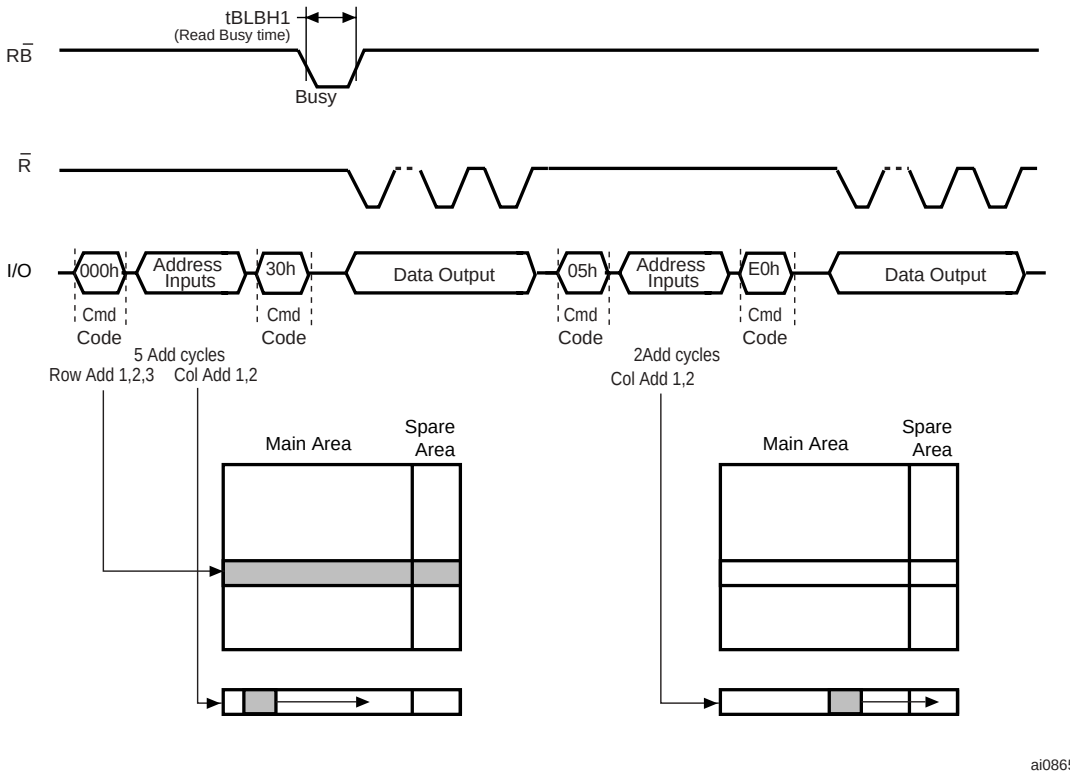
The sequential operation can be resumed by changing the column address of the next data to be output, to the address which follows the Random Data Output command.The Random Data Output command can be issued as many times as required within a page.

Figure 7. Read operations



1. Highest address depends on device density.

Figure 8. Random data output



6.4 Page Program

The Page Program operation is the standard operation to program data to the memory array. Generally, data is programmed sequentially, however, the device does support random input within a page.

The memory array is programmed by page, however, partial page programming is allowed where any number of bytes (1 to 2112) can be programmed.

Only one consecutive partial Page Program operation is allowed on the same page. After exceeding this a Block Erase command must be issued before any further Program operations can take place in that page.

6.5 Sequential Input

To input data sequentially the addresses must be sequential and remain in one block.

For Sequential Input, each Page Program operation comprises five steps:

1. One bus cycle is required to set up the Page Program (Sequential Input) command (see *Table 7*).
2. Five bus cycles are then required to input the program address (refer to *Table 5*).
3. The data is loaded into the data registers.
4. One bus cycle is required to issue the Page Program Confirm command to start the P/E/R controller. The P/E/R only starts if the data has been loaded in step 3.
5. The P/E/R controller then programs the data into the array.

6.6 Random Data Input

During a Sequential Input operation, the next sequential address to be programmed can be replaced by a random address issuing a Random Data Input command. The following two steps are required to issue the command:

1. One bus cycle is required to setup the Random Data Input command (see *Table 7*).
2. Two bus cycles are then required to input the new column address (refer to *Table 5*).

Random Data Input can be repeated as often as required in any given page.

Once the Program operation has started the Status Register can be read using the Read Status Register command. During program operations the status register only flags errors for bits set to ‘1’ that have not been successfully programmed to ‘0’.

During the Program operation, only the Read Status Register and Reset commands are accepted; all other commands are ignored. Once the Program operation has completed, the P/E/R controller bit SR6 is set to ‘1’ and the Ready/Busy signal goes High.

The device remains in Read Status Register mode until another valid command is written to the command interface.

Figure 9. Page Program operation

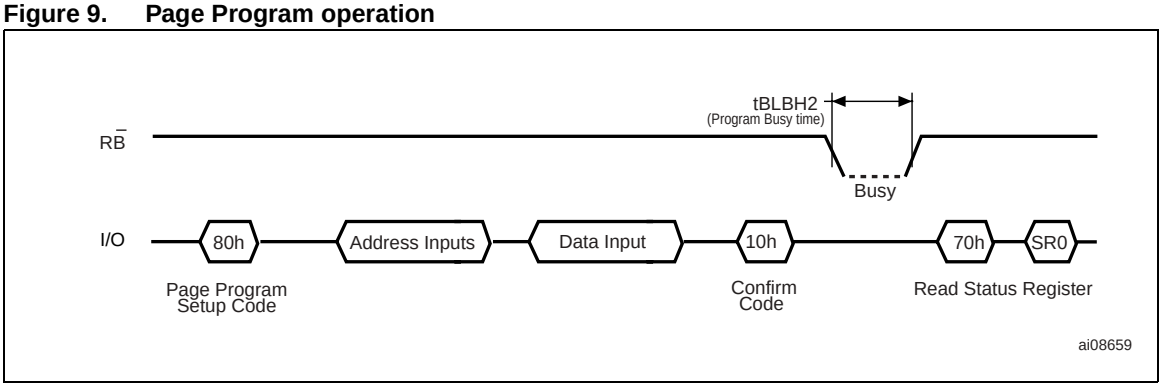
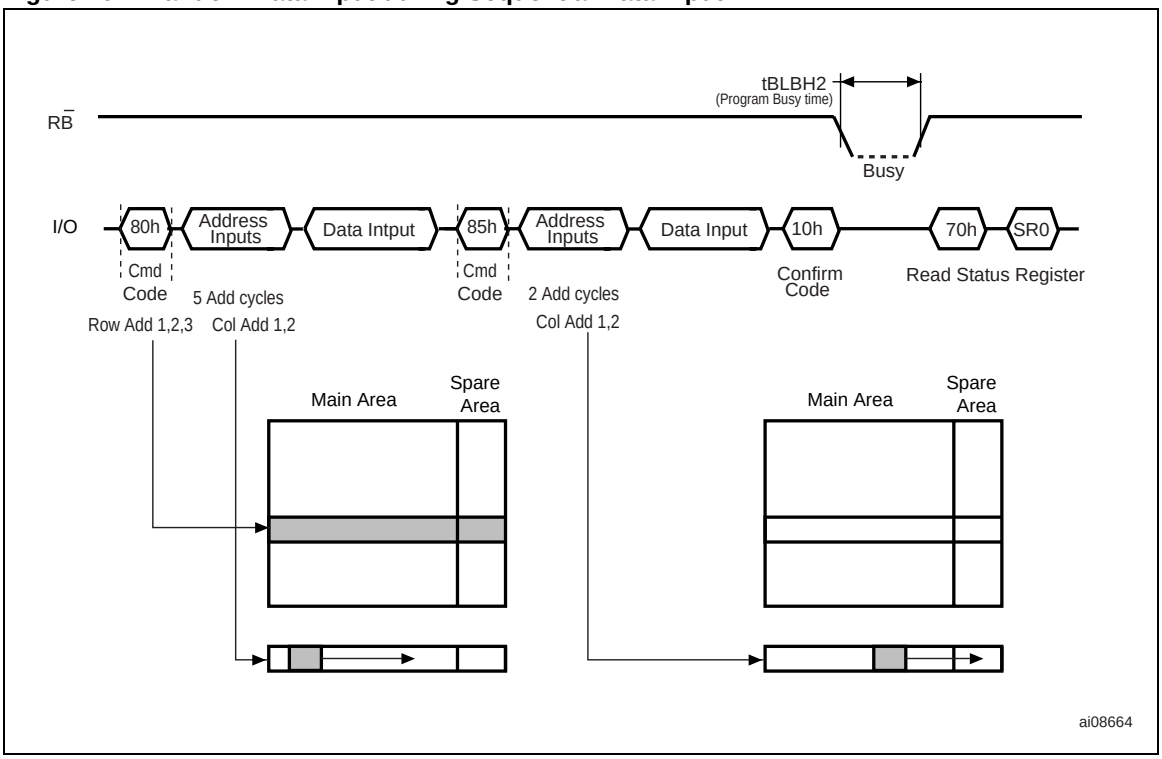


Figure 10. Random Data Input during Sequential Data Input



6.7 Multiplane Page Program

The devices support Multiplane Page Program, that allows the programming of two pages in parallel, one in each plane.

A Multiplane Page Program operation requires two steps:

1. The first step loads serially up to two pages of data (4224 bytes) into the data buffer. It requires:
   - One clock cycle to set up the Page Program command (see *Section 6.5: Sequential Input*).
   - Five bus write cycles to input the first page address and data. The address of the first page must be within the first plane (A19 = 0).
   - One bus write cycle to issue the Page Program Confirm code. After this the device is busy for a time of t_{BLBH5}.
   - When the device returns to the ready state (Ready/Busy High), a Multiplane Page Program Setup code must be issued, followed by the second page address (5 write cycles) and data. The address of the second page must be within the second plane (A19=1), and A18 to A12 must be the address bits loaded during the first address insertion.

2. The second step programs, in parallel, the two pages of data loaded into the data buffer into the appropriate memory pages. It is started by issuing a Program Confirm command.

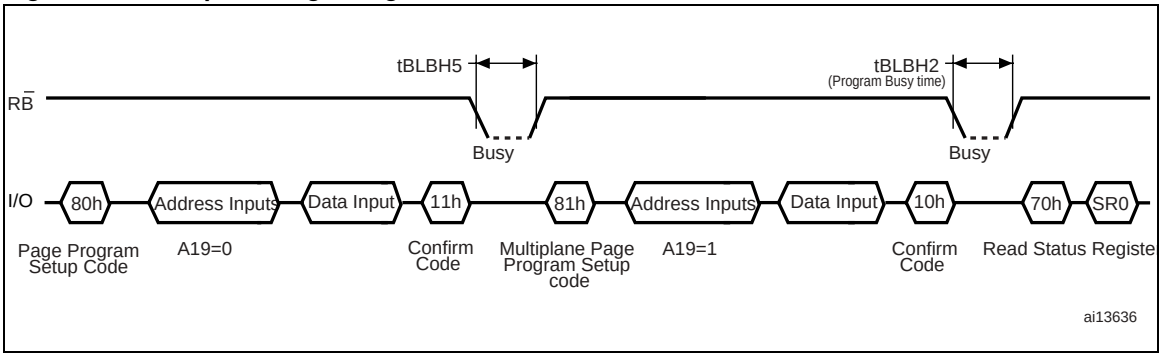
As for standard Page Program operations, the device supports Random Data Input during both data loading phases.

Once the Multiplane Page Program operation has started, maintaining a delay of t_{BLBH5}, the Status Register can be read using the Read Status Register command. Once the Multiplane Page Program operation has completed, the P/E/R controller bit SR6 is set to '1' and the Ready/Busy signal goes High.

If the Multiplane Page Program fails, an error is signaled on bit SR0 of the Status Register. However, there is no way to identify for which page the program operation failed.

See *Figure 11* for a description of Multiplane Page Program waveforms.

Figure 11. Multiplane Page Program



6.8 Block Erase

Erase operations are done one block at a time. An Erase operation sets all of the bits in the addressed block to '1'. All previous data in the block is lost.

An Erase operation consists of three steps (refer to *Figure 12*):

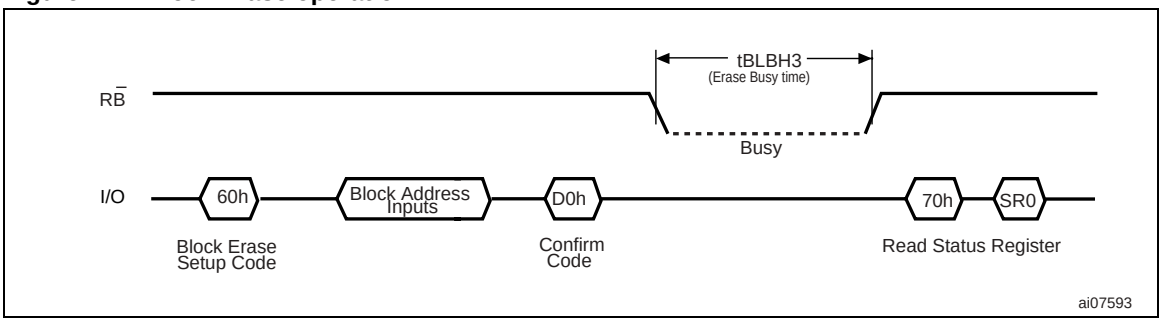
1. One bus cycle is required to setup the Block Erase command. Only addresses A19 to A31 are used; the other address inputs are ignored.
2. Three bus cycles are then required to load the address of the block to be erased. Refer to *Table 6* for the block addresses of each device.
3. One bus cycle is required to issue the Block Erase Confirm command to start the P/E/R controller.

The Erase operation is initiated on the rising edge of write Enable, $\overline{W}$, after the Confirm command is issued. The P/E/R Controller handles Block Erase and implements the verify process.

During the Block Erase operation, only the Read Status Register and Reset commands are accepted; all other commands are ignored.

Once the program operation has completed, the P/E/R controller bit SR6 is set to ‘1’ and the Ready/Busy signal goes High. If the operation completes successfully, the write status bit SR0 is ‘0’, otherwise it is set to ‘1’.

Figure 12. Block Erase operation



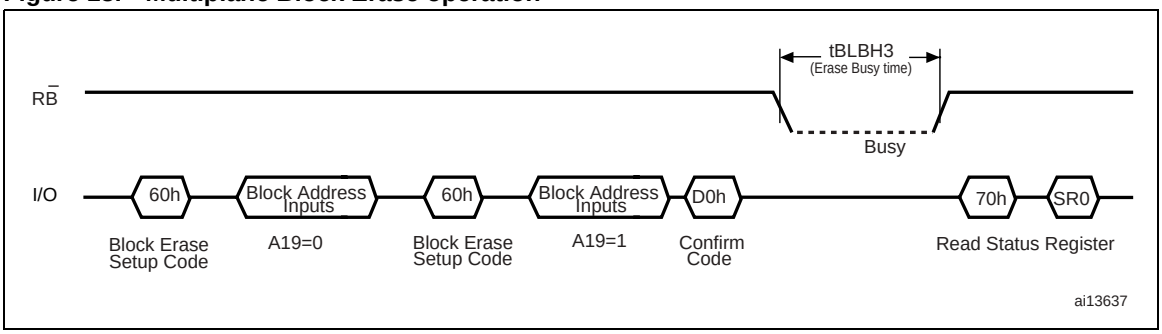
6.9 Multiplane Block Erase

The Multiplane Block Erase operation allows erasing two blocks in parallel, one in each plane. It consists of three steps (refer to *Figure 13: Multiplane Block Erase operation*):

1. Eight bus cycles are required to set up the Block Erase command and load the addresses of the blocks to be erased. The Setup command, followed by the address of the block to be erased, must be issued for each block. No dummy busy time is required between the first and second block address insertion. As for Multiplane Page Program, the address of the first and second page must be within the first plane (A19 = 0) and second plane (A19 = 1), respectively.
2. One bus cycle is then required to issue the Multiplane Block Erase confirm command and start the P/E/R controller.

If the Multiplane Block Erase fails, an error is signaled on bit SR0 of the status register. However, there is no way to identify for which page the Multiplane Block Erase operation failed.

Figure 13. Multiplane Block Erase operation



6.10 Reset

The Reset command is used to reset the command interface and Status Register. If the Reset command is issued during any operation, the operation is aborted. If it is a Program or Erase operation that is being aborted, the contents of the memory locations being modified are no longer valid as the data is partially programmed or erased.

If the device has already been reset, then the new Reset command is not accepted.

The Ready/Busy signal goes Low for t_{BLBH4} after the Reset command is issued. The value of t_{BLBH4} depends on the operation that the device was performing when the command was issued. Refer to *Table 21* for the values.

6.11 Read Status Register

The device contains a Status Register that provides information on the current or previous Program or Erase operation. The various bits in the Status Register convey information and errors on the operation.

The Status Register is read by issuing the Read Status Register command. The Status Register information is present on the output data bus (I/O0-I/O7) on the falling edge of Chip Enable or Read Enable, whichever occurs last. When several memories are connected in a system, the use of Chip Enable and Read Enable signals allows the system to poll each device separately, even when the Ready/Busy pins are common-wired. It is not necessary to toggle the Chip Enable or Read Enable signals to update the contents of the status register.

After the Read Status Register command has been issued, the device remains in Read Status Register mode until another command is issued. Therefore, if a Read Status Register command is issued during a random read cycle a new Read command must be issued to continue with a Page Read operation.

Refer to *Table 8* which summarizes Status Register bits and should be read in conjunction with the following text descriptions.

6.11.1 Write protection bit (SR7)

The write protection bit can identify if the device is protected or not. If the write protection bit is set to ‘1’ the device is not protected and Program or Erase operations are allowed. If the write protection bit is set to ‘0’ the device is protected and Program or Erase operations are not allowed.

6.11.2 P/E/R controller bit (SR6)

Status register bit SR6 acts as a P/E/R controller bit, which indicates whether the P/E/R controller is active or inactive. When the P/E/R controller bit is set to ‘0’, the P/E/R controller is active (device is busy); when the bit is set to ‘1’, the P/E/R controller is inactive (device is ready).

6.11.3 Error bit (SR0)

The error bit is used to identify if any errors have been detected by the P/E/R controller. The error bit is set to ‘1’ when a Program or Erase operation has failed to write the correct data to the memory. If the error bit is set to ‘0’, the operation has completed successfully.

6.12 SR5, SR4, SR3, SR2 and SR1 bits are reserved

Table 8. Status Register bits

Bit	Name	Logic level	Definition
SR7	Write protection	‘1’	Not protected
		‘0’	Protected
SR6	Program/erase/read controller	‘1’	P/E/R C inactive, device ready
		‘0’	P/E/R C active, device busy
SR5, SR4, SR3, SR2, SR1	Reserved	Don’t care	
SR0	Generic error	‘1’	Error – operation failed
		‘0’	No error – operation successful

6.13 Read Electronic Signature

The device contains a manufacturer code and device code. The following three steps are required to read these codes:

1. One bus write cycle to issue the Read Electronic Signature command (90h)
2. One bus write cycle to input the address (00h)
3. Four bus read cycles to sequentially output the data (as shown in *Table 9: Electronic signature*)

Table 9. Electronic signature

Part number	Byte/word 1	Byte/word 2	Byte 3 (see *Table 10*)	Byte 4 (see *Table 11*)	Byte 5 (see *Table 12*)
	Manufacturer code	Device code			
NAND08GW3C2A	20h	D3h	14h	A5h	6Ch
NAND16GW3C2A(1)					

1. Each 8-Gbit die returns its own electronic signature.

Table 10. Electronic signature byte 3

I/O	Definition	Value	Description
I/O1-I/O0	Internal chip number	0 0 0 1 1 0 1 1	1 2 4 8
I/O3-I/O2	Cell type	0 0 0 1 1 0 1 1	2-level cell 4-level cell 8-level cell 16-level cell
I/O5-I/O4	Number of simultaneously programmed pages	0 0 0 1 1 0 1 1	1 2 4 8
I/O6	Interleaved programming between multiple devices	0 1	Not supported Supported
I/O7	Cache program	0 1	Not supported Supported

Table 11. Electronic signature byte 4

I/O	Definition	Value	Description
I/O1-I/O0	Page size (without spare area)	0 0 0 1 1 0 1 1	1 KBytes 2 Kbytes 4 Kbytes 8 Kbytes
I/O2	Spare area size (byte/512 byte)	0 1	8 16
I/O7, I/O3	Minimum sequential access time	0 0 1 0 0 1 1 1	30/50 ns 25 ns Reserved Reserved
I/O5-I/O4	Block size (without spare area)	0 0 0 1 1 0 1 1	64 Kbytes 128 Kbytes 256 Kbytes 512 Kbytes
I/O6	Organization	0 1	x8 x16

Table 12. Electronic signature byte 5

I/O	Definition	Value	Description
I/O1 - I/O0	Reserved	0 0	
I/O3 - I/O2	Plane number	0 0 0 1 1 0 1 1	1 Plane 2 Planes 4 Planes 8 Planes
I/O6 - I/O4	Plane size (without spare area)	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	64 Mbits 128 Mbits 256 Mbits 512 Mbits 1 Gb 2 Gb 4 Gb 8 Gb
I/O7	Reserved	0	

7 Concurrent operations and ERS on the NAND16GW3C2A

The NAND16GW3C2A is composed by two 8-Gbit dice stacked together. This configuration allows the device to support concurrent operations. This means that while performing an operation in one die (Erase, Read, Program, etc.), another operation is possible in the other die.

The standard Read Status Register (ERS) operation returns the status of the NAND16GW3C2A device. To provide information on each 8-Gbit die, the NAND16GW3C2A features an Extended Read Status Register command that allows to check independently the status of each die.

The following steps are required to perform concurrent operations:

1. Select one of the two dice by setting the most significant address bit A31 to ‘0’ or ‘1’.
2. Execute one operation on this die.
3. Launch a concurrent operation on the other die.
4. Check the status of these operations by performing an Extended Read Status Register operation.

All combinations of operations are possible except executing Read on both dice. This is due to the fact that the input/output bus is common to both dice.

Refer to *Table 13* for the description of the Extended Read Status Register command sequence, and to *Table 8*. for the definition of the Status Register bits.

Table 13. Extended Read Status Register commands

Command	Address range	1 bus write cycle
Read 1st die status	Address ≤ 0x7FFFFFFF	F1h
Read 2nd die status	0x7FFFFFFF < Address ≤ 0xFFFFFFF	F2h

8 Data protection

The device has hardware features to protect against Program and Erase operations. It features a Write Protect, $\overline{WP}$, pin, which protects the device against program and erase operations. It is recommended to keep $\overline{WP}$ at V_{IL} during power-up and power-down.

9 Software algorithms

This section gives information on the software algorithms that Numonyx recommends implementing to manage the bad blocks and extend the lifetime of the NAND device.

NAND Flash memories are programmed and erased by Fowler-Nordheim tunneling using high voltage. Exposing the device to high voltage for extended periods can cause the oxide layer to be damaged. For this reason, the number of program and erase cycles is limited (see *Table 15* for value). It is recommended to implement garbage collection, wear-leveling and error correction code algorithms to extend the number of program and erase cycles and to increase data retention.

To help integrate a NAND memory into an application Numonyx can provide a File System OS Native reference software, which supports the basic commands of file management.

Contact the nearest Numonyx sales office for more details.

9.1 Bad block management

Devices with bad blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A bad block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor.

The devices are supplied with all the locations inside valid blocks erased (FFh). The bad block information is written prior to shipping. Any block, where the 1st byte in the spare area of the last page, does not contain FFh, is a bad block.

The bad block information must be read before any erase is attempted as the bad block Information may be erased. For the system to be able to recognize the bad blocks based on the original information it is recommended to create a bad block table following the flowchart shown in *Figure 14.*

9.2 NAND Flash memory failure modes

The NAND08GW3C2A and NAND16GW3C2A devices may contain bad blocks, where the reliability of blocks that contain one or more invalid bits is not guaranteed. Additional bad blocks may develop during the lifetime of the device.

To implement a highly reliable system, all the possible failure modes must be considered:

- Program/erase failure

  in this case, the block has to be replaced by copying the data to a valid block. These additional bad blocks can be identified as attempts to program or erase them and will give errors in the Status Register.

  Because the failure of a Page Program operation does not affect the data in other pages in the same block, the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block. The Copy Back Program command can be used to copy the data to a valid block. See *Section Figure 10.: Random Data Input during Sequential Data Input* for more details.

- Read failure

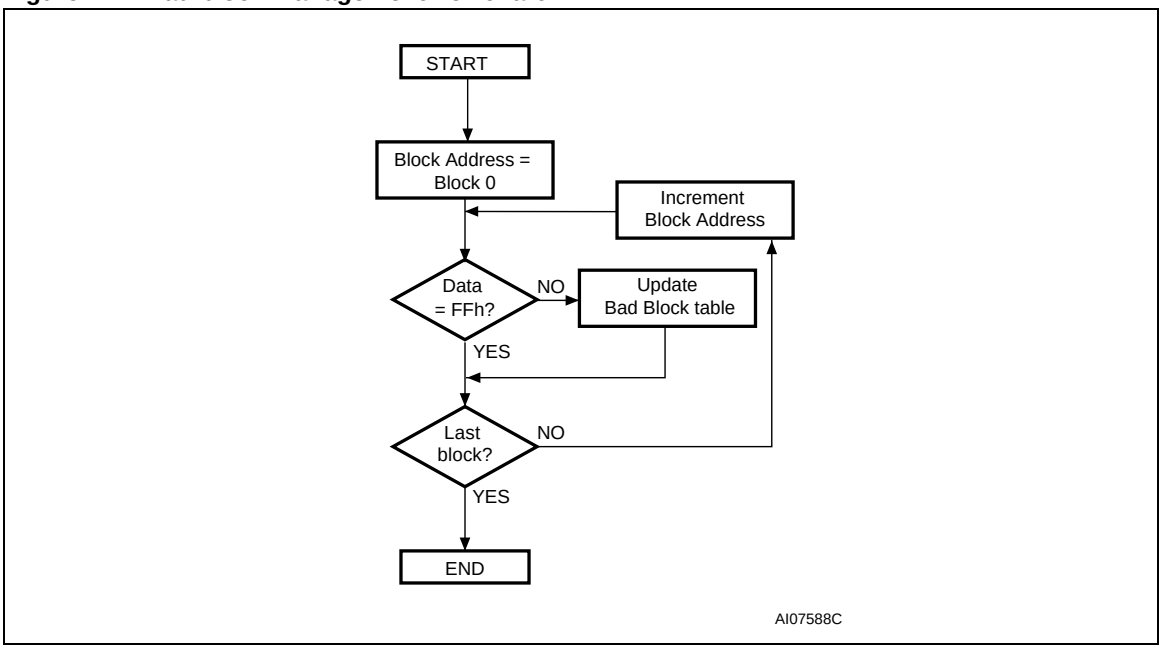
  in this case, ECC correction must be implemented. To efficiently use the memory space, it is recommended to recover single-bit errors in read by ECC, without replacing the whole block.

Refer to *Table 14* for the procedure to follow if an error occurs during an operation.

Table 14. Block failure

Operation	Procedure
Erase	Block replacement
Program	Block replacement or ECC (with 4 bit/528 byte)
Read	ECC (with 4 bit/528 byte)

Figure 14. Bad block management flowchart

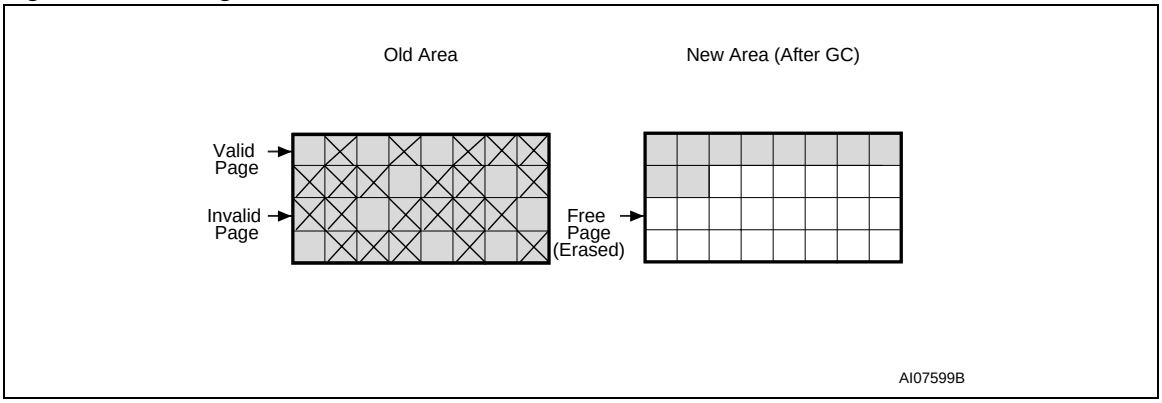


9.3 Garbage collection

When a data page needs to be modified, it is faster to write to the first available page and mark the previous page as invalid. After several updates it is necessary to remove invalid pages to free some memory space.

To free this memory space and allow further program operations, it is recommended to implement a garbage collection algorithm. In a garbage collection software the valid pages are copied into a free area and the block containing the invalid pages is erased (see *Figure 15*).

Figure 15. Garbage collection



9.4 Wear-leveling algorithm

For write-intensive applications, it is recommended to implement a wear-leveling algorithm to monitor and spread the number of write cycles per block.

In memories that do not use a wear-leveling algorithm, not all blocks get used at the same rate. The wear-leveling algorithm ensures that equal use is made of all the available write cycles for each block.

There are two wear-leveling levels:

1. First level wear-leveling, where new data is programmed to the free blocks that have had the fewest write cycles
2. Second level wear-leveling, where long-lived data is copied to another block so that the original block can be used for more frequently changed data.

The second level wear-leveling is triggered when the difference between the maximum and the minimum number of write cycles per block reaches a specific threshold.

9.5 Hardware simulation models

9.5.1 Behavioral simulation models

Denali Software Corporation models are platform-independent functional models designed to assist customers in performing entire system simulations (typical VHDL/Verilog). These models describe the logic behavior and timings of NAND Flash devices, and, therefore, allow software to be developed before hardware.

9.5.2 IBIS simulations models

I/O buffer information specification (IBIS) models describe the behavior of the I/O buffers and electrical characteristics of Flash devices.

These models provide information such as AC characteristics, rise/fall times, and package mechanical data, all of which are measured or simulated at voltage and temperature ranges wider than those allowed by target specifications.

IBIS models are used to simulate PCB connections and can be used to resolve compatibility issues when upgrading devices. They can be imported into SPICETOOLS.

10 Program and erase times and endurance cycles

Table 15 shows the program and erase times and the number of program/erase cycles per block.

Table 15. Program and erase times and program erase endurance cycles

Parameters	NAND08GW3C2A, NAND16GW3C2A			Unit
	Min	Typ	Max	
Page program time		800	2000	µs
Block erase time		2.5	3	ms
Program/erase cycles (per block (with ECC)	10,000			cycles
Data retention	10			years

11 Maximum ratings

Stressing the device above the ratings listed in *Table 16: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the Numonyx SURE Program and other relevant quality documents.

Table 16. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_{BIAS}	Temperature under bias	– 50	125	°C
T_{STG}	Storage temperature	– 65	150	°C
V_{IO}(1)	Input or output voltage	– 0.6	4.6	V
V_{DD}	Supply voltage	– 0.6	4.6	V

1. Minimum voltage may undershoot to –2 V for less than 20 ns during transitions on input and I/O pins. Maximum voltage may overshoot to V_{DD} + 2 V for less than 20 ns during transitions on I/O pins.

12 DC and AC parameters

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC characteristics tables are derived from tests performed under the measurement conditions summarized in *Table 17: Operating and ac measurement conditions*. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 17. Operating and ac measurement conditions

Parameter	NAND08GW3C2A, NAND16GW3C2A		Units
	Min	Max	
Supply voltage (V_{DD})	2.7	3.6	V
Ambient temperature (T_A)	0	70	°C
	–40	85	°C
Load capacitance (C_L) (1 TTL GATE and C_L)	50		pF
Input pulses voltages	0.4	2.4	V
Input and output timing ref. voltages	1.5		V
Output circuit resistor R_{ref}	8.35		kΩ
Input rise and fall times	5		ns

Table 18. Capacitance(1)

Symbol	Parameter	Test condition	Typ	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V		10	pF
$C_{I/O}$	Input/output capacitance	V_{IL} = 0 V		10	pF

1. T_A = 25 °C, f = 1 MHz. C_{IN} and $C_{I/O}$ are not 100% tested.

Table 19. DC characteristics

Symbol	Parameter		Test conditions	Min	Typ	Max	Unit
I_{DD1}	Operating current	Sequential read	t_{RLRL} minimum $\overline{E}=V_{IL}$, I_{OUT} = 0 mA	-	15	30	mA
I_{DD2}		Program	-	-	15	30	mA
I_{DD3}		Erase	-	-	15	30	mA
I_{DD4}	Standby current (TTL)		E=V_{IH}, $\overline{WP}$=0/V_{DD}			1	mA
I_{DD5}	Standby current (CMOS)		$\overline{E}=V_{DD}$-0.2, $\overline{WP}$=0/V_{DD}	-	10	50	µA
I_{LI}	Input leakage Current		V_{IN}= 0 to 3.6V	-	-	±10	µA
I_{LO}	Output leakage Current		V_{OUT}= 0 to 3.6V	-	-	±10	µA
V_{IH}	Input high voltage		-	2.0	-	V_{DD}+0.3	V
V_{IL}	Input low voltage		-	-0.3	-	0.8	V
V_{OH}	Output high voltage level		I_{OH} = -400µA	2.4	-	-	V
V_{OL}	Output low voltage level		I_{OL} = 2.1mA	-	-	0.4	V
I_{OL} ($R\overline{B}$)	Output low current ($R\overline{B}$)		V_{OL} = 0.4V	8	10		mA

Table 20. AC characteristics for command, address, data input

Symbol	Alt. symbol	Parameter			Value	Unit
t_{ALLWH}	t_{ALS}	Address Latch Low to Write Enable High	AL setup time	Min	12	ns
t_{ALHWH}		Address Latch High to Write Enable High				
t_{CLHWH}	t_{CLS}	Command Latch High to Write Enable High	CL setup time	Min	12	ns
t_{CLLWH}		Command Latch Low to Write Enable High				
t_{DVWH}	t_{DS}	Data Valid to Write Enable High	Data setup time	Min	12	ns
t_{ELWH}	t_{CS}	Chip Enable Low to Write Enable High	$\overline{E}$ setup time	Min	20	ns
t_{WHALH}	t_{ALH}	Write Enable High to Address Latch High	AL hold time	Min	5	ns
t_{WHALL}		Write Enable High to Address Latch Low				
t_{WHCLH}	t_{CLH}	Write Enable High to Command Latch High	CL hold time	Min	5	ns
t_{WHCLL}		Write Enable High to Command Latch Low				
t_{WHDX}	t_{DH}	Write Enable High to Data Transition	Data hold time	Min	5	ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	$\overline{E}$ hold time	Min	5	ns
t_{WHWL}	t_{WH}	Write Enable High to Write Enable Low	$\overline{W}$ High hold time	Min	10	ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	$\overline{W}$ pulse width	Min	12	ns
t_{WLWL}	t_{WC}	Write Enable Low to Write Enable Low	Write cycle time	Min	25	ns

Table 21. AC characteristics for operations

Symbol	Alt. Symbol	Parameter		Value			Unit
				Min	Typ	Max	
t_{ALLRL1}	t_{AR}	Address Latch Low to Read Enable Low	Read Electronic Signature	10			ns
t_{ALLRL2}			Read cycle	10			ns
t_{BHRL}	t_{RR}	Ready/Busy High to Read Enable Low		20			ns
t_{BLBH1}		Ready/Busy Low to Ready/Busy High	Read Busy time			60	µs
t_{BLBH2}	t_{PROG}		Program Busy time			2000	µs
t_{BLBH3}	t_{BERS}		Erase Busy time			3	ms
t_{BLBH4}	t_{RST}	Reset Busy time, during ready				5	µs
		Reset Busy time, during read				5	µs
		Reset Busy time, during program				10	µs
		Reset Busy time, during erase				500	µs
t_{BLBH5}	t_{CBSY}	Dummy Busy Time for Multiplane operations			1	2	µs
t_{CLLRL}	t_{CLR}	Command Latch Low to Read Enable Low		10			ns
t_{DZRL}	t_{IR}	Data Hi-Z to Read Enable Low		0			ns
t_{EHQZ}	t_{CHZ}	Chip Enable High to Output Hi-Z				30	ns
t_{ELQV}	t_{CEA}	Chip Enable Low to Output Valid				25	ns
t_{RHRL}	t_{REH}	Read Enable High to Read Enable Low	Read Enable High Hold time	10			ns
t_{EHQX}	t_{COH}	Chip Enable High to Output Hold		15			ns
t_{RHQX}	t_{RHOH}	Read Enable High to Output Hold		15			ns
t_{RLQX}	t_{RLOH}	Read Enable Low to Output Hold (EDO Mode)		5			ns
t_{RHQZ}	t_{RHZ}	Read Enable High to Output Hi-Z				100	ns
t_{RLRH}	t_{RP}	Read Enable Low to Read Enable High	Read Enable Pulse Width	12			ns
t_{RLRL}	t_{RC}	Read Enable Low to Read Enable Low	Read Cycle time	25			ns
t_{RLQV}	t_{REA}	Read Enable Low to Output Valid	Read Enable Access time			20	ns
			Read ES Access time(1)				
t_{WHBH}	t_{R}	Write Enable High to Ready/Busy High	Read Busy time			60	µs
t_{WHBL}	t_{WB}	Write Enable High to Ready/Busy Low				100	ns
t_{WHRL}	t_{WHR}	Write Enable High to Read Enable Low		80			ns
t_{WHWH}(2)	t_{ADL}	Last Address latched on Data Loading Time during Program operations		70			ns
t_{VHWH}(3)	t_{WW}	Write Protection time		100			ns
t_{VLWH}(3)				100			ns

1. ES = Electronic Signature.
2. t_{WHWH} is the delay from Write Enable rising edge during the final address cycle to Write Enable rising edge during the first data cycle.
3. $\overline{WP}$ High to $\overline{W}$ High during Program/Erase Enable operations.

Figure 16. Command latch AC waveforms

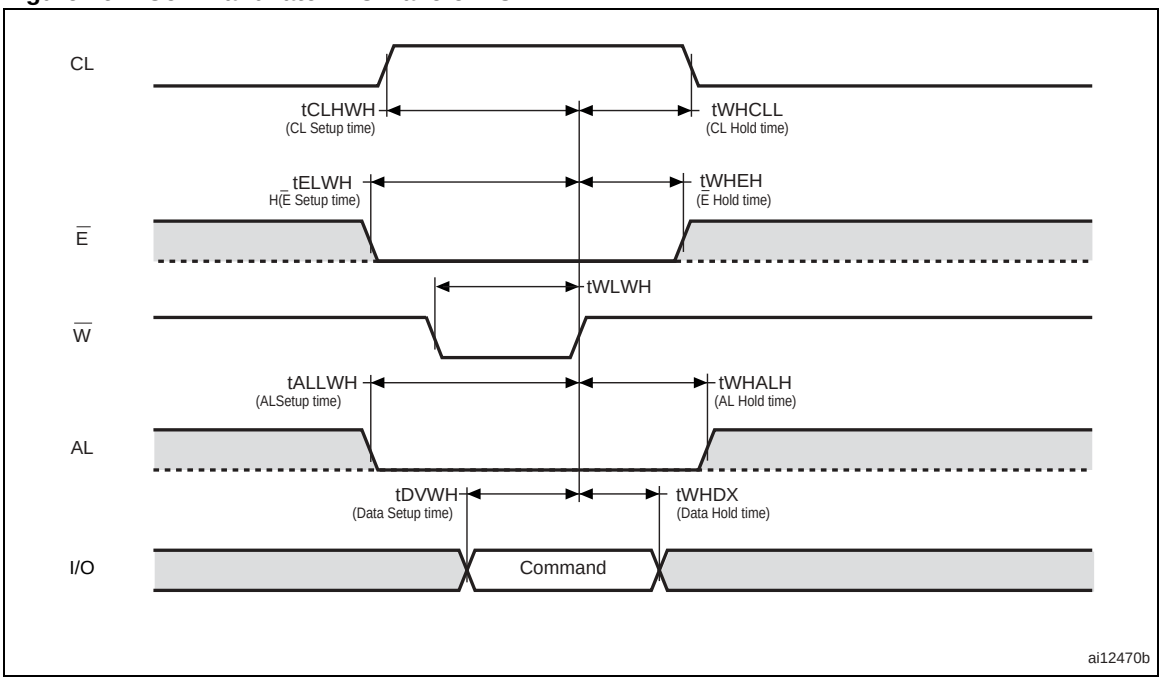


Figure 17. Address latch AC waveforms

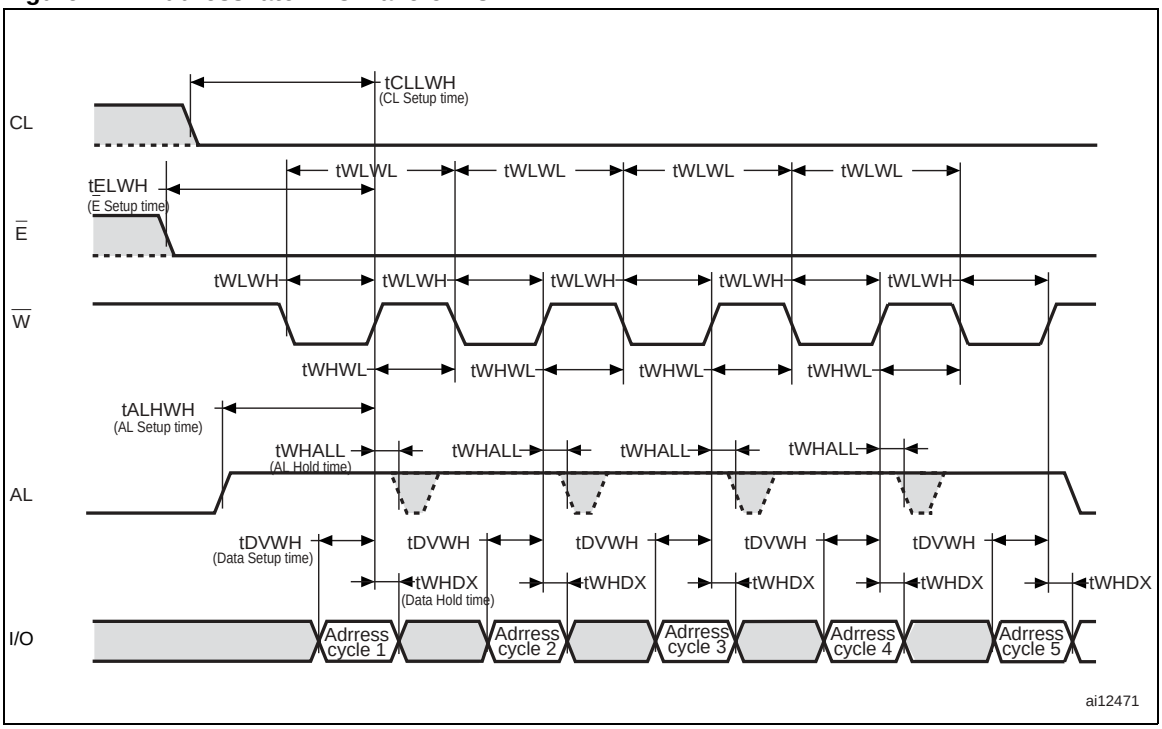
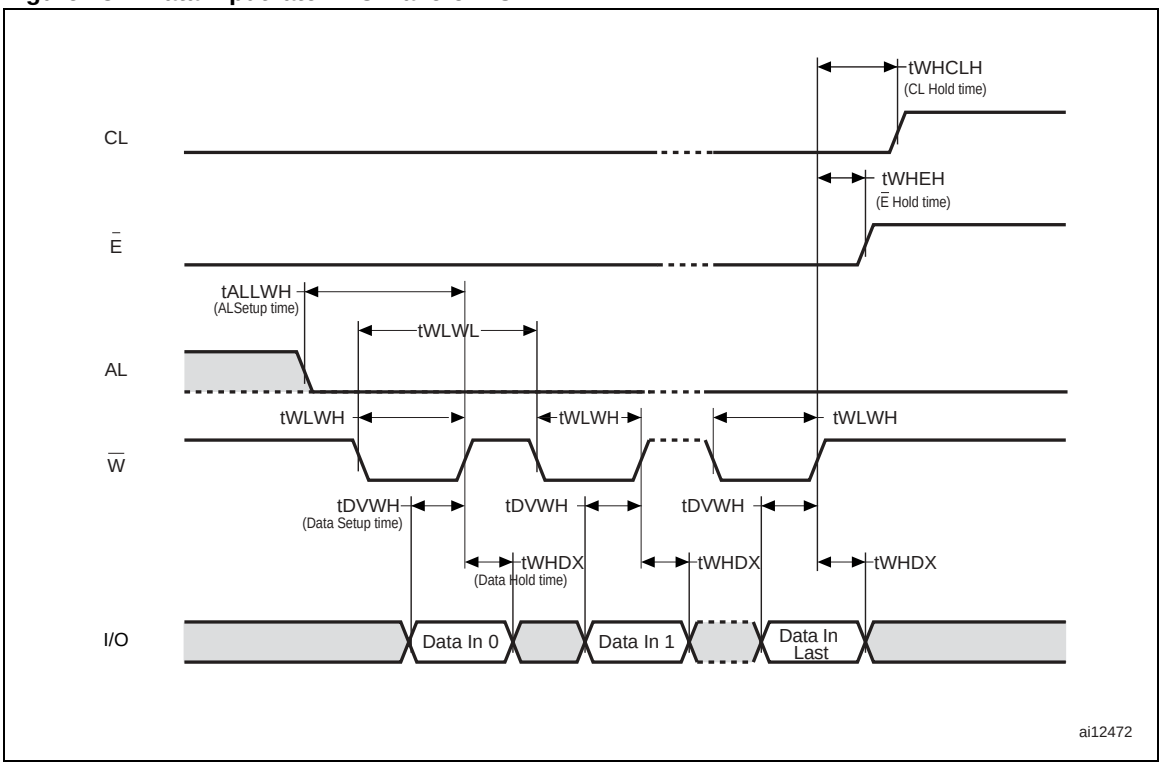
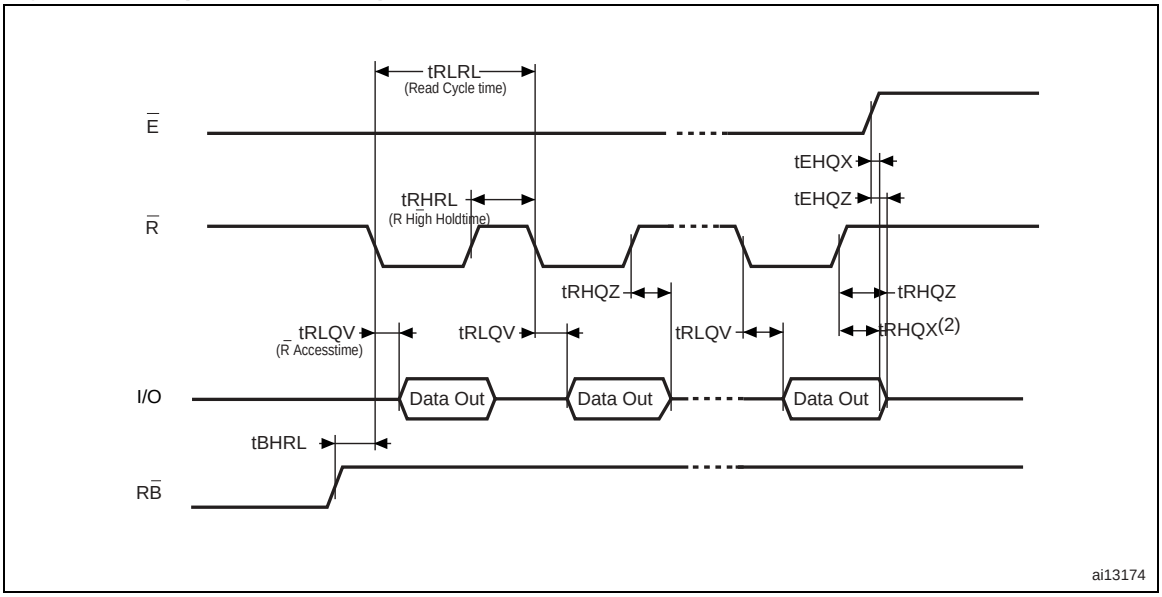


Figure 18. Data input latch AC waveforms



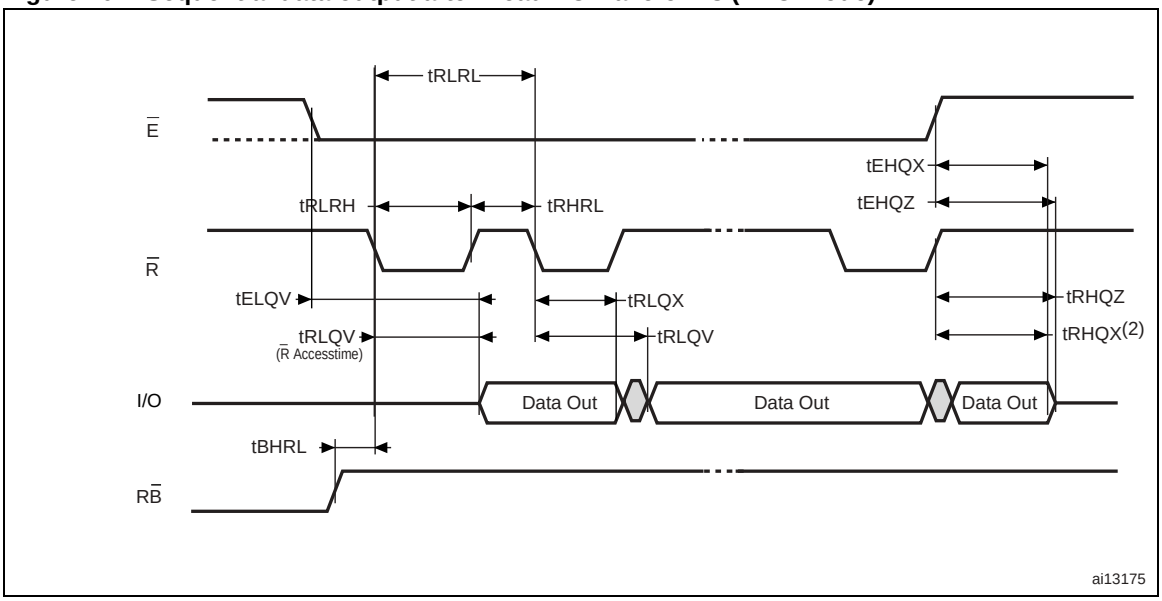
1. The last data input is the 2112th.

Figure 19. Sequential data output after Read AC waveforms



1. CL = Low, AL = Low, $\overline{W}$ = High.
2. t_{RHQX} is applicable for frequencies lower than 33 MHz (i.e. t_{RLRL} higher than 30 ns).

Figure 20. Sequential data output after Read AC waveforms (EDO mode)



1. In EDO mode, CL and AL are Low, V_{IL}, and $\overline{W}$ is High, V_{IH}.
2. t_{RLQX} is applicable for frequencies higher than 33 MHz (i.e. t_{RLRL} lower than 30 ns).

Figure 21. Read Status Register AC waveform

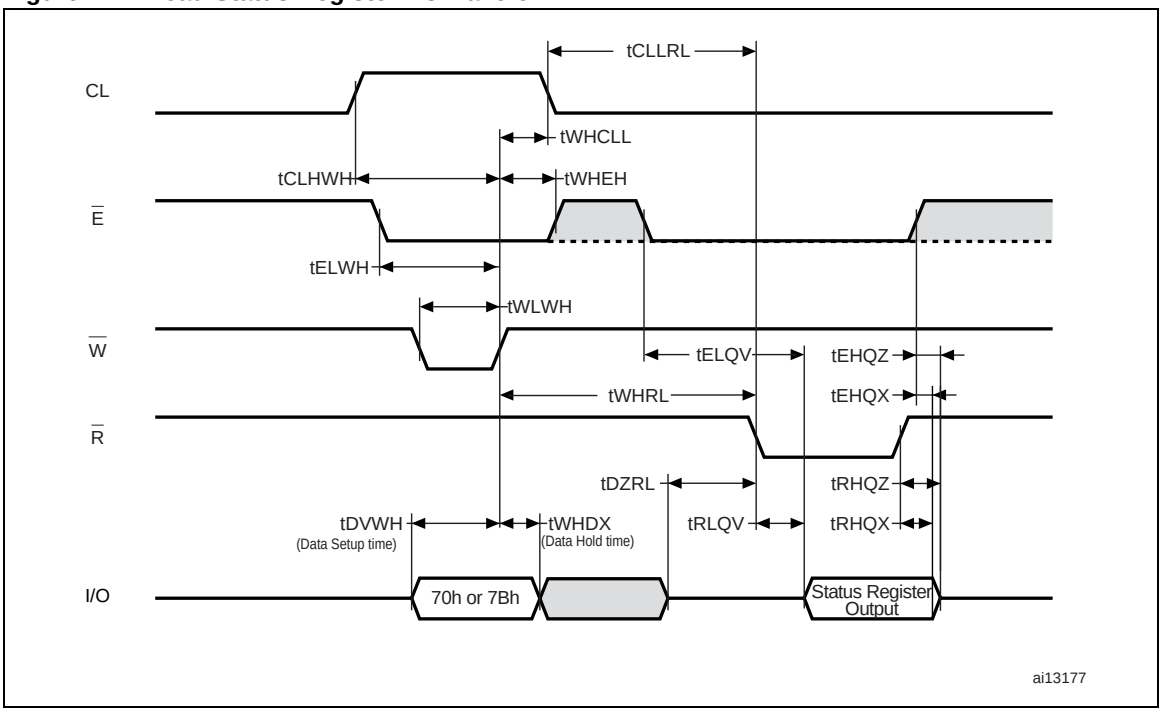
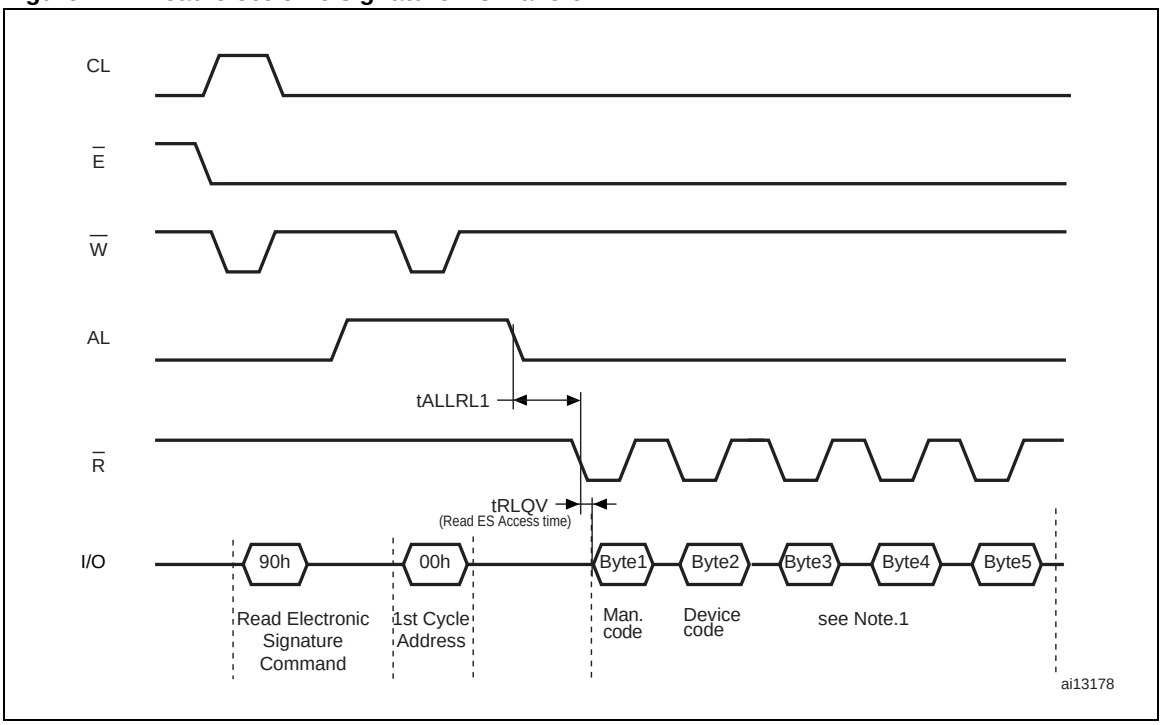


Figure 22. Read electronic signature AC waveform



1. Refer to *Table 9* for the values of the manufacturer and device codes, and to *Table 10*, *Table 11*, and *Table 12* for the information contained in byte 3, byte 4, and byte 5.

Figure 23. Page Read operation AC waveform

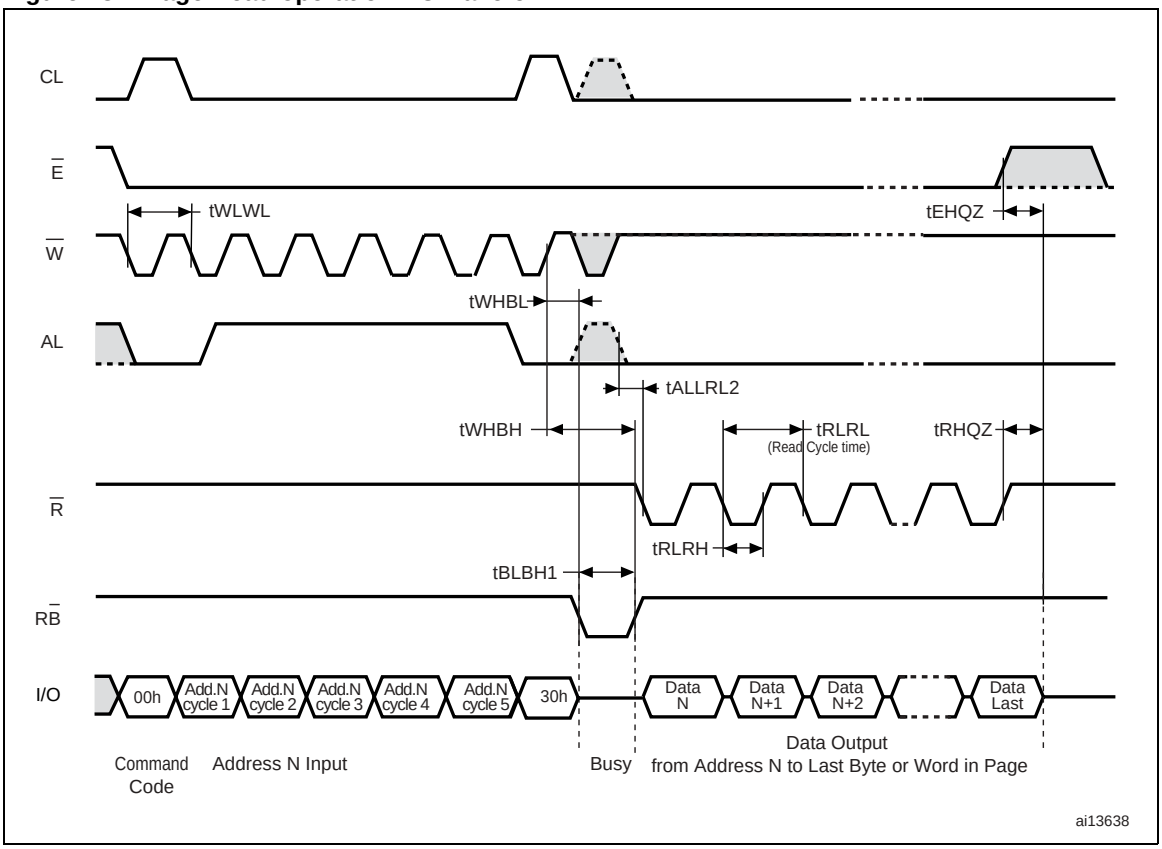


Figure 24. Page Program AC waveform

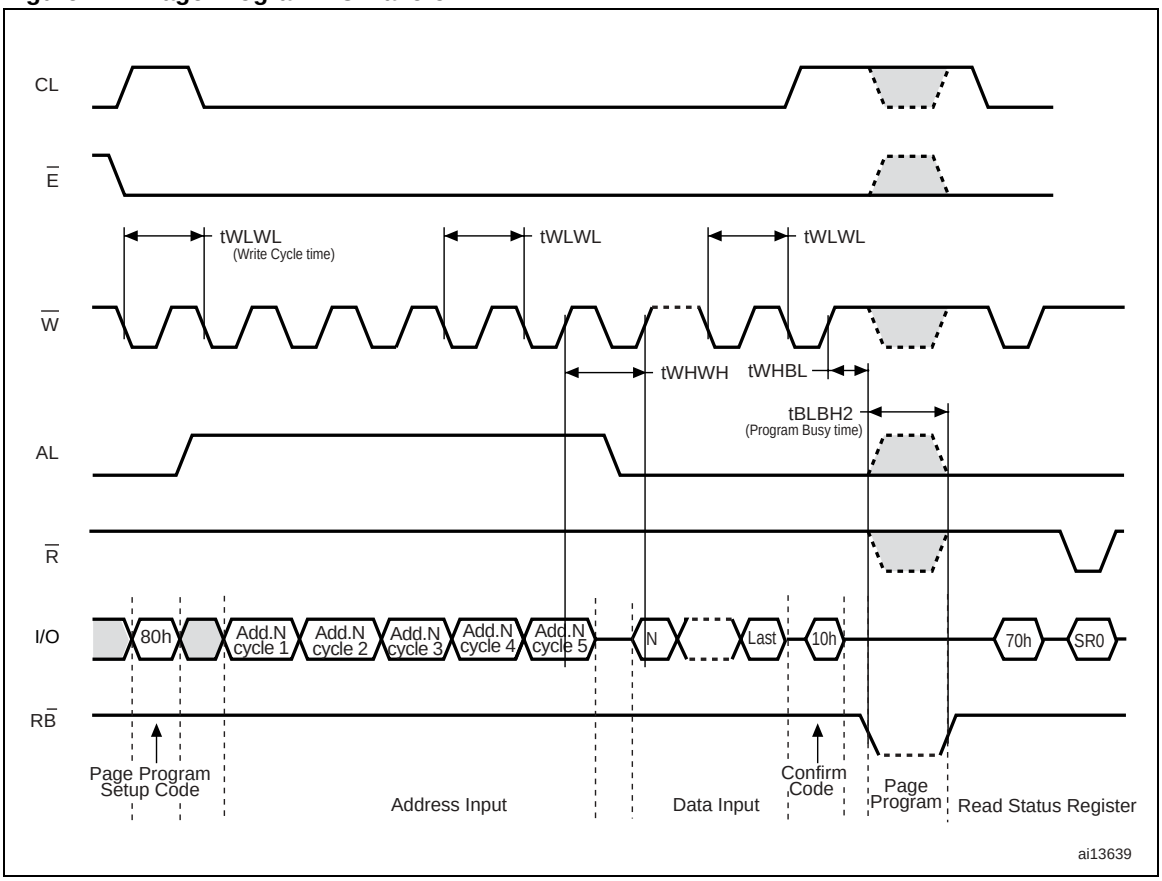


Figure 25. Block Erase AC waveform

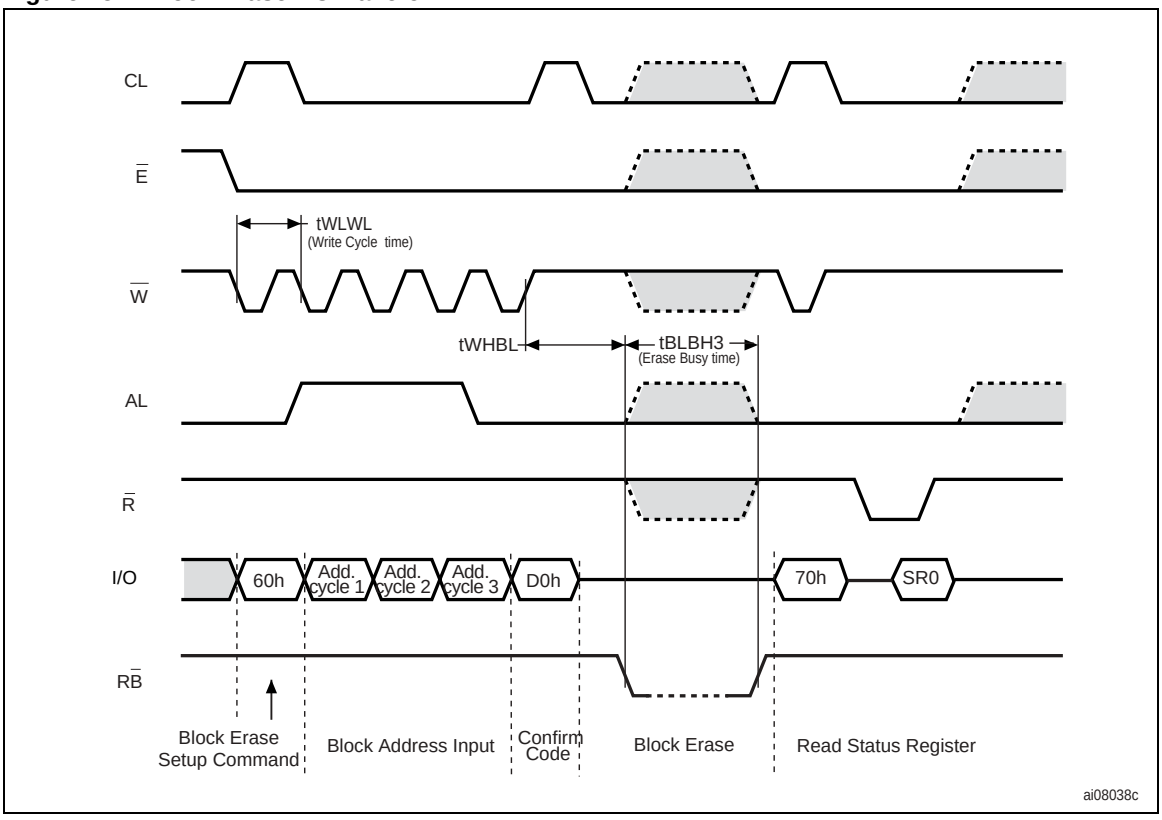


Figure 26. Reset AC waveform

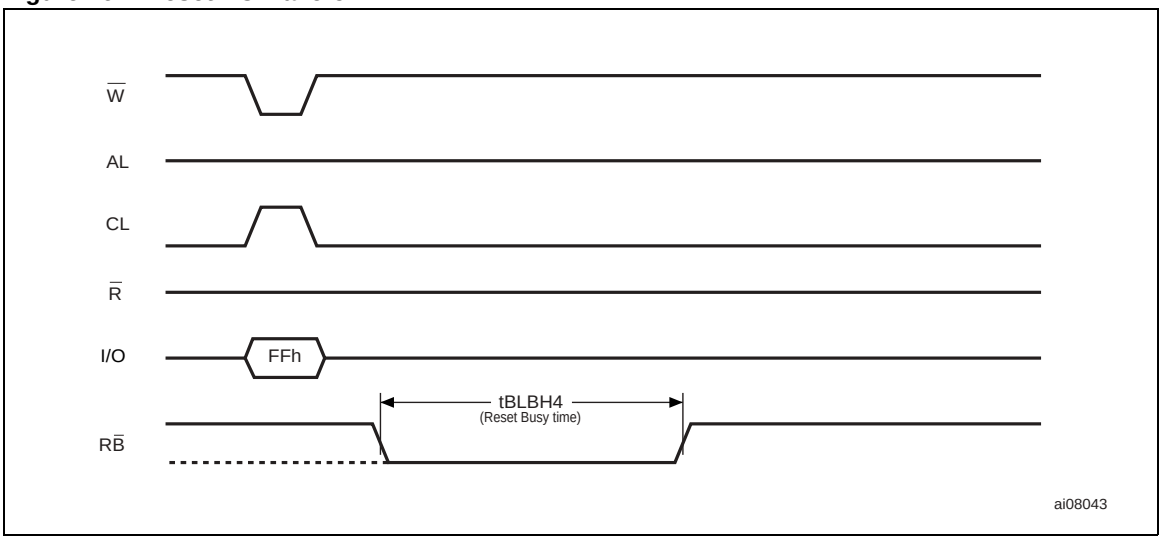


Figure 27. Program/Erase Enable waveform

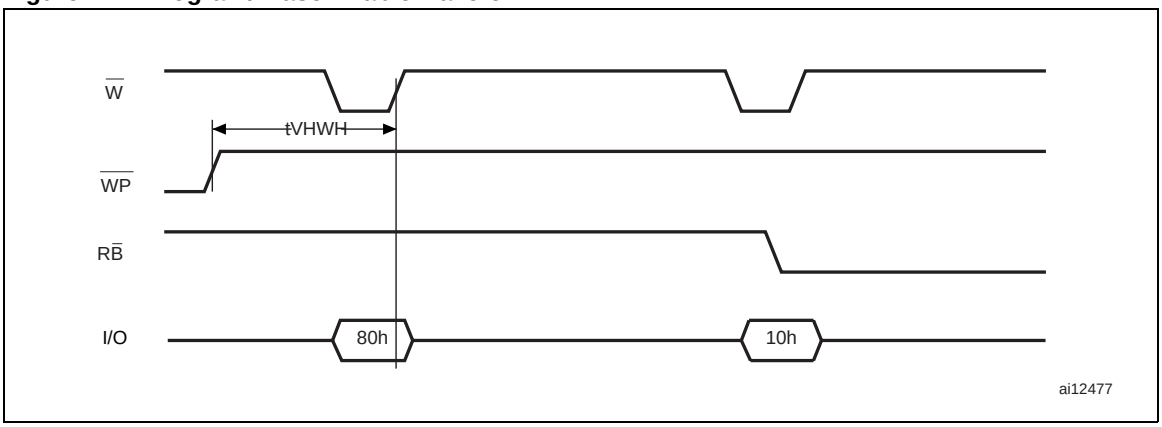
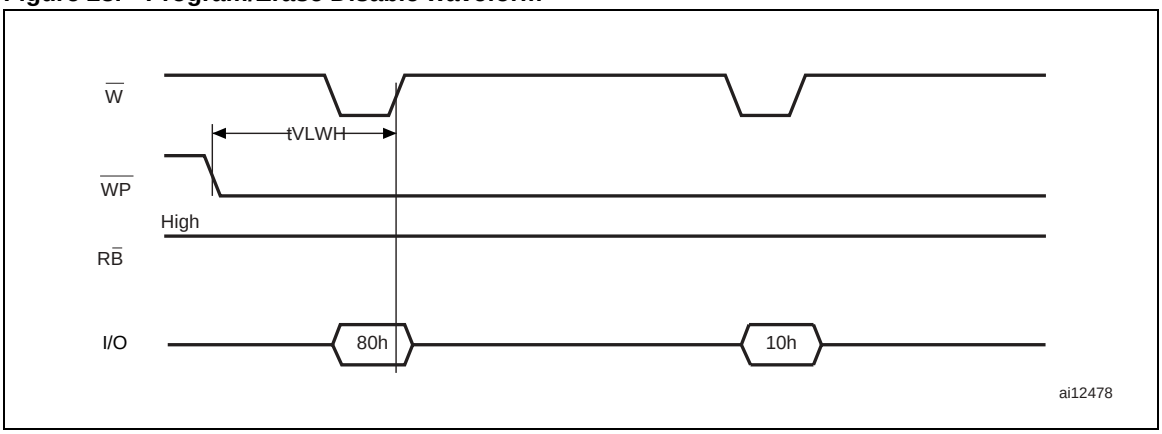


Figure 28. Program/Erase Disable waveform



12.1 Ready/Busy signal electrical characteristics

Figure 30, *Figure 29* and *Figure 31* show the electrical characteristics for the Ready/Busy signal. The value required for the resistor R_P can be calculated using the following equation:

$$R_P min = \frac{(V_{DDmax} - V_{OLmax})}{I_{OL} + I_L}$$

So,

$$R_P min = \frac{3.2V}{8mA + I_L}$$

where I_L is the sum of the input currents of all the devices tied to the Ready/Busy signal. R_P max is determined by the maximum value of t_r.

Figure 29. Ready/Busy AC waveform

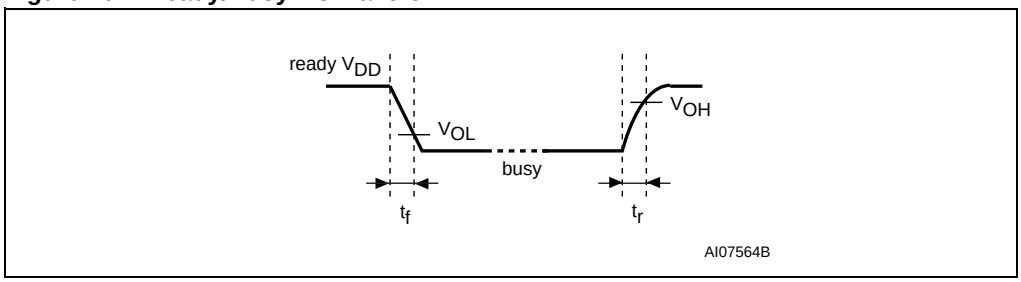


Figure 30. Ready/Busy load circuit

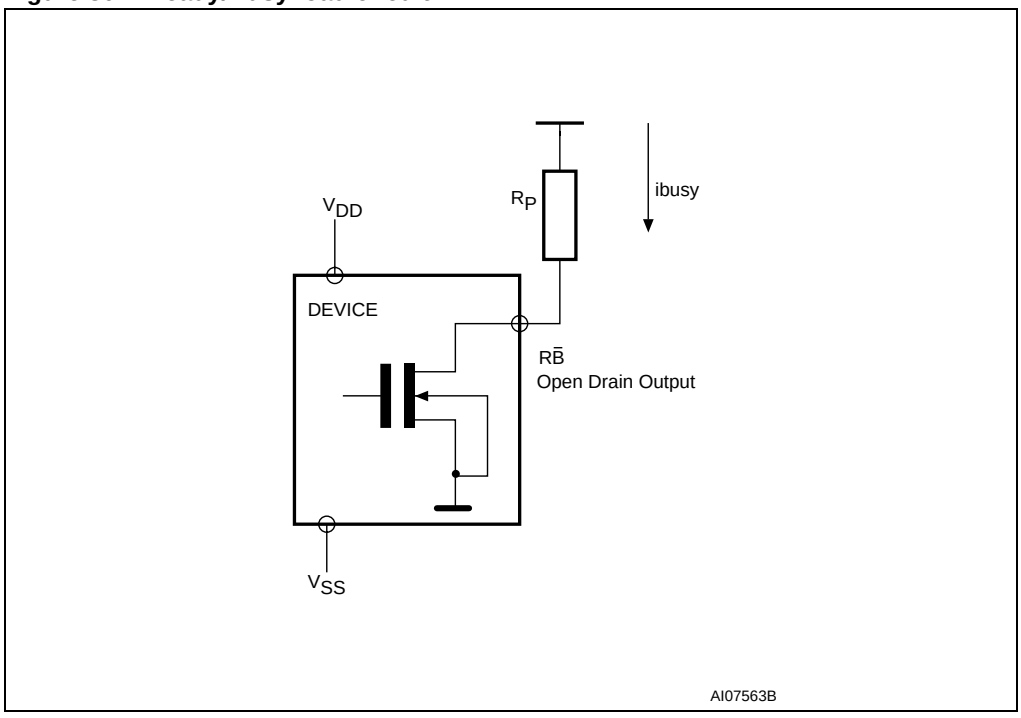
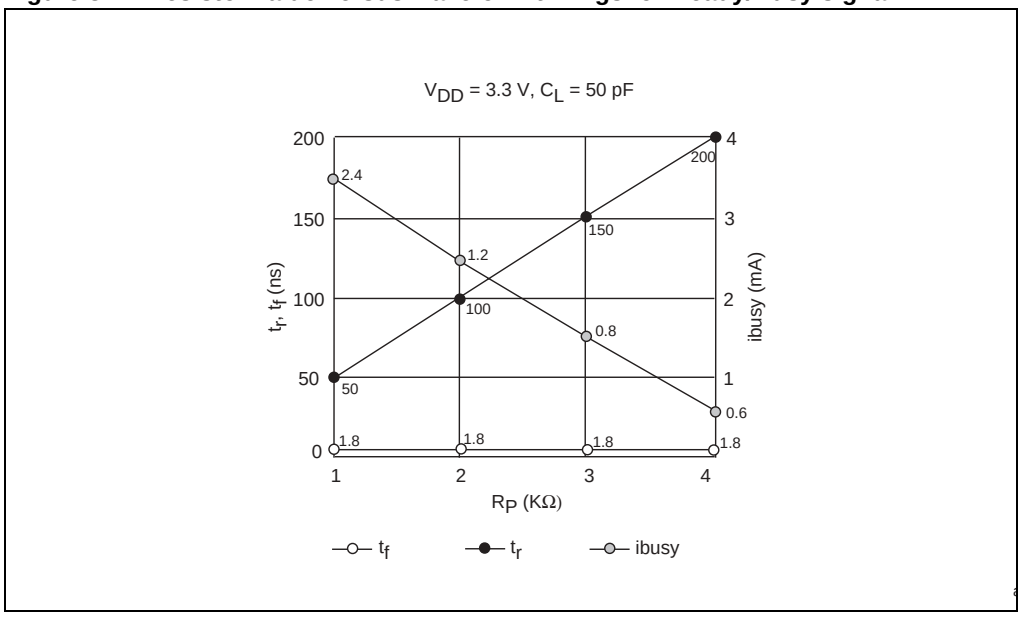


Figure 31. Resistor value versus waveform timings for Ready/Busy signal



1. T = 25°C.

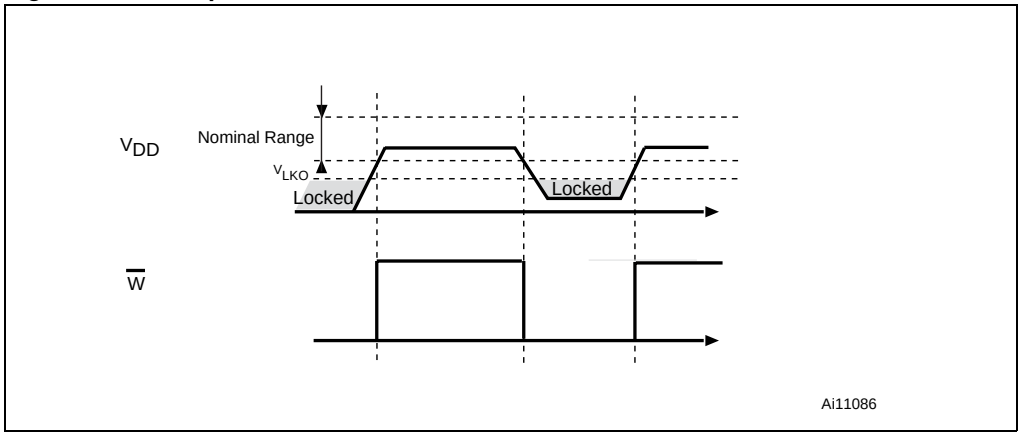
12.2 Data protection

The Numonyx NAND device is designed to guarantee data protection during power transitions.

A V_{DD} detection circuit disables all NAND operations, if V_{DD} is below the V_{LKO} threshold.

In the V_{DD} range from V_{LKO} to the lower limit of nominal range, the $\overline{WP}$ pin should be kept Low (V_{IL}) to guarantee hardware protection during power transitions as shown in *Figure 32.*

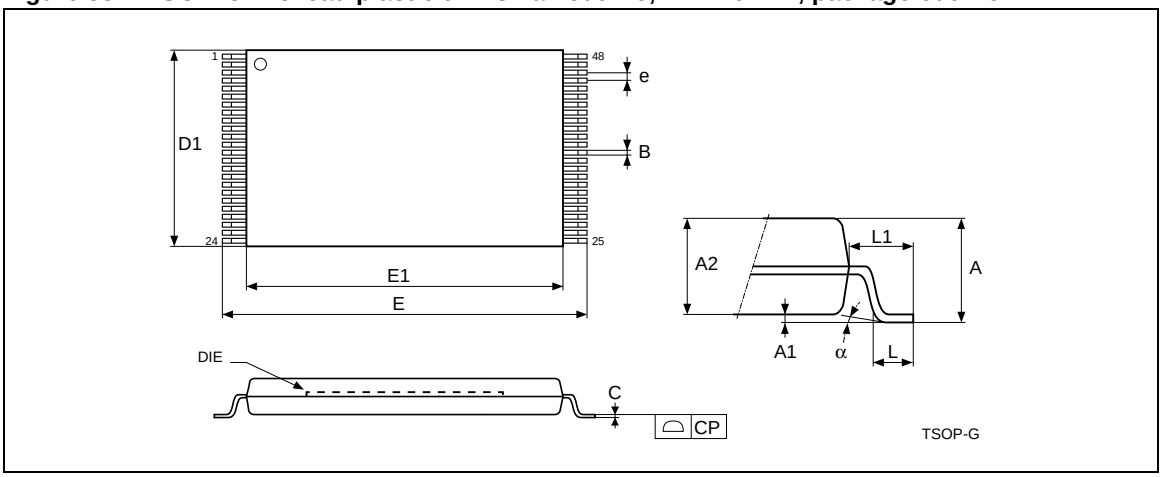
Figure 32. Data protection



13 Package mechanical

This section contains mechanical data for the packages.

Figure 33. TSOP48 - 48 lead plastic thin small outline, 12 x 20 mm, package outline



1. Drawing is not to scale.

Table 22. TSOP48 - 48 lead plastic thin small outline, 12 x 20 mm, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1	0.100	0.050	0.150	0.0039	0.0020	0.0059
A2	1.000	0.950	1.050	0.0394	0.0374	0.0413
B	0.220	0.170	0.270	0.0087	0.0067	0.0106
C		0.100	0.210		0.0039	0.0083
CP			0.080			0.0031
D1	12.000	11.900	12.100	0.4724	0.4685	0.4764
E	20.000	19.800	20.200	0.7874	0.7795	0.7953
E1	18.400	18.300	18.500	0.7244	0.7205	0.7283
e	0.500	–	–	0.0197	–	
L	0.600	0.500	0.700	0.0236	0.0197	0.0276
L1	0.800			0.0315		
a	3°	0°	5°	3°	0°	5°

Figure 34. LGA52 12 x 17 mm, 1 mm pitch, package outline

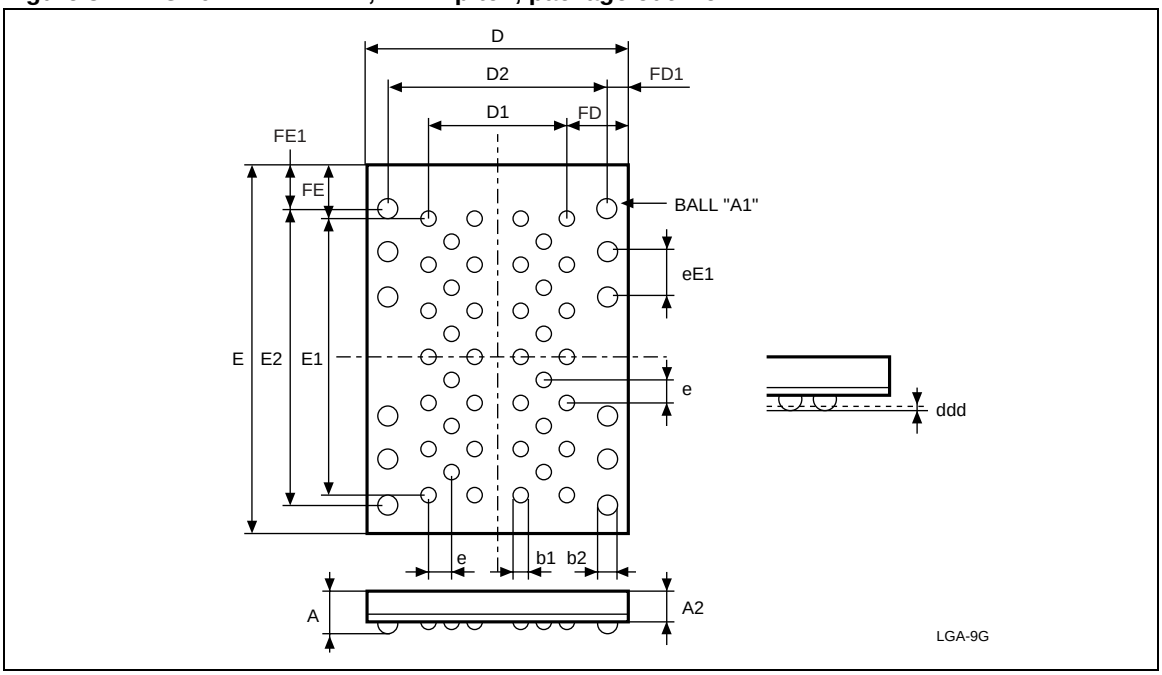


Table 23. LGA52 12 x 17 mm, 1 mm pitch, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			0.650			0.0256
A2			0.650			0.0256
b1	0.700	0.650	0.750	0.0276	0.0256	0.0295
b2	1.000	0.950	1.050	0.0394	0.0374	0.0413
D	12.000	11.900	12.100	0.4724	0.4685	0.4764
D1	6.000			0.2362		
D2	10.000			0.3937		
ddd			0.100			0.0039
E	17.000	16.900	17.100	0.6693	0.6654	0.6732
E1	12.000			0.4724		
E2	13.000			0.5118		
e	1.000	–	–	0.0394	–	–
eE1	2.000	–	–	0.0787	–	–
FD	3.000			0.1181		
FD1	1.000			0.0394		
FE	2.500			0.0984		
FE1	2.000			0.0787		

14 Ordering information

Table 24. Ordering information scheme

Example: NAND08G W 3 C 2 A N 1 E

Device type

NAND Flash memory

Density

08G = 8 Gbits

16G = 16 Gbits

Operating voltage

W = V_{DD} = 2.7 to 3.6 V

Bus width

3 = x 8

Family identifier

C = 2112 bytes Page MLC

Device options

2 = Chip Enable Don't Care Enabled

4 = Chip Enable Don't Care Enabled with 2 Chip Enable and 2 Ready/Busy signals

Product version

A = First version

Package

N = TSOP48 12 x 20 mm

ZL = ULGA52 12 x 17 mm

Temperature range

1 = 0 to 70 °C

6 = –40 to 85 °C

Option

E = ECOPACK® package, standard packing

F = ECOPACK® package, tape & reel packing

Devices are shipped from the factory with the memory content bits, in valid blocks, erased to '1'. For further information on any aspect of this device, please contact your nearest Numonyx Sales Office.

15 Revision history

Table 25. Document revision history

Date	Revision	Changes
22-Dec-2006	0.1	Initial release.
11-Jun-2007	1	– Changed throughout the document "NAND16GW3C2A" to "NAND16GW3C4A. – Listed throughout document the details relating to the two 8-Gbit dice, the two Chip Enable, and two Ready/Busy signals in the NAND16GZ3C4A, which required changes in several figures and tables. – Added power-up and power-down minimum recovery time information in *Section 3.8: Ready/Busy (RB1, RB2)*. – Added program and read information in *Section Table 14.: Block failure*. – Modified page program time parameters and program/erase cycles parameters in *Section Table 15.: Program and erase times and program erase endurance cycles*. – Modified AC characteristics in *Section Table 21.: AC characteristics for operations*.
04-Jan-2008	2	Applied Numonyx branding.

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