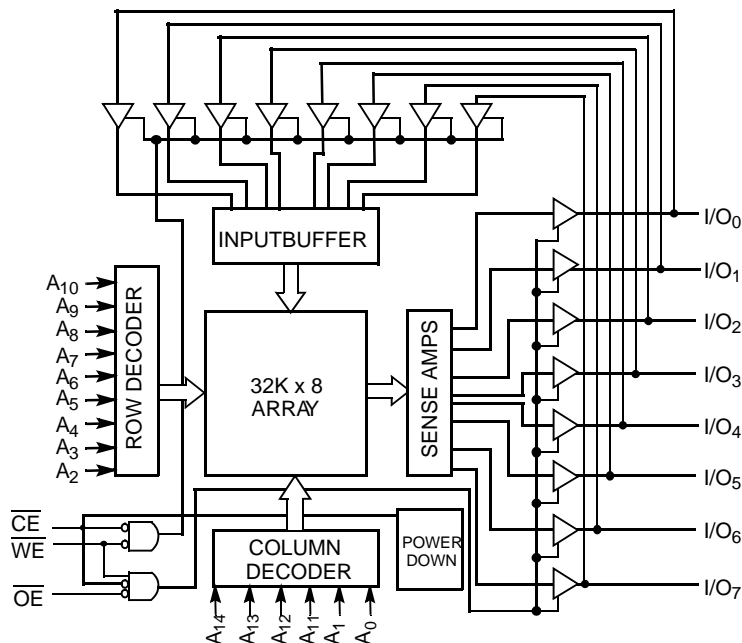


## Features

- Temperature ranges
  - Commercial: 0 °C to +70 °C
  - Industrial: -40 °C to +85 °C
  - Automotive-A: -40 °C to +85 °C
  - Automotive-E: -40 °C to +125 °C
- Speed: 70 ns
- Low voltage range: 2.7 V to 3.6 V
- Low active power and standby power
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- TTL compatible inputs and outputs
- Automatic power down when deselected
- CMOS for optimum speed and power
- Available in standard Pb-free and non Pb-free 28-pin (300-mil) narrow SOIC, 28-pin TSOP-I, and 28-pin reverse TSOP-I packages

## Logic Block Diagram



## Functional Description

The CY62256VN<sup>[1]</sup> family is composed of two high performance CMOS static RAM's organized as 32K words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}$ ) and active LOW output enable ( $\overline{OE}$ ) and tristate drivers. These devices have an automatic power down feature, reducing the power consumption by over 99% when deselected.

An active LOW write enable signal ( $\overline{WE}$ ) controls the writing/reading operation of the memory. When  $\overline{CE}$  and  $\overline{WE}$  inputs are both LOW, data on the eight data input/output pins ( $I/O_0$  through  $I/O_7$ ) is written into the memory location addressed by the address present on the address pins ( $A_0$  through  $A_{14}$ ). Reading the device is accomplished by selecting the device and enabling the outputs,  $\overline{CE}$  and  $\overline{OE}$  active LOW, while  $\overline{WE}$  remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

The input/output pins remain in a high impedance state unless the chip is selected, outputs are enabled, and write enable ( $\overline{WE}$ ) is HIGH.

### Note

1. For best practice recommendations, refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

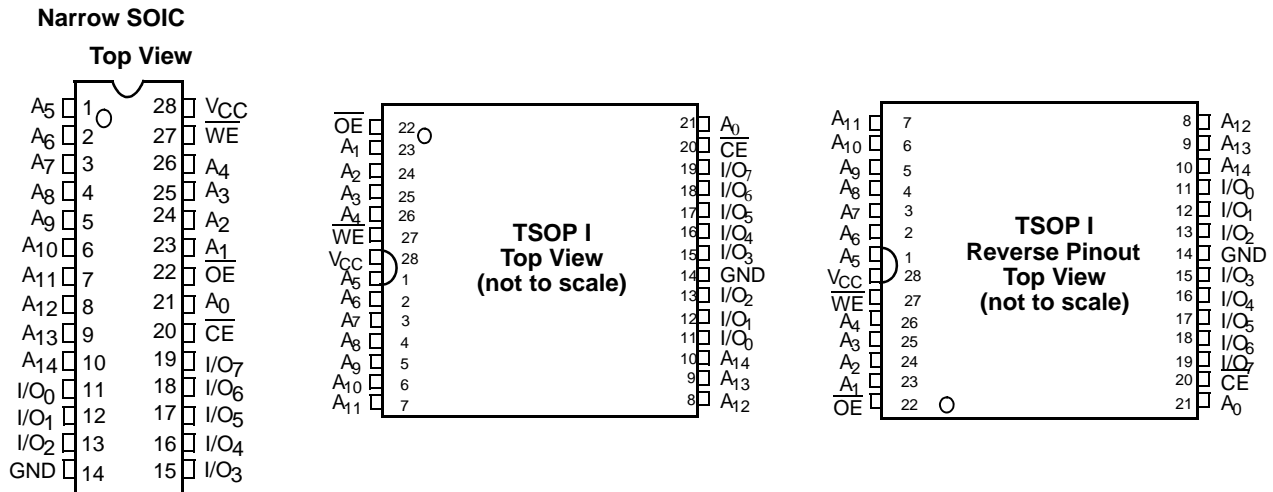
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Product Portfolio

Product	Range	V <sub>CC</sub> Range (V)			Power Dissipation			
					Operating, I <sub>CC</sub> (mA)		Standby, I <sub>SB2</sub> (μA)	
		Min	Typ <sup>[2]</sup>	Max	Typ <sup>[2]</sup>	Max	Typ <sup>[2]</sup>	Max
CY62256VNLL	Commercial	2.7	3.0	3.6	11	30	0.1	5
CY62256VNLL	Industrial	2.7	3.0	3.6	11	30	0.1	10
CY62256VNLL	Automotive-A	2.7	3.0	3.6	11	30	0.1	10
CY62256VNLL	Automotive-E	2.7	3.0	3.6	11	30	0.1	130

Pin Configurations



Pin Definitions

Pin Number	Type	Description
1–10, 21, 23–26	Input	A <sub>0</sub> –A <sub>14</sub> . Address inputs
11–13, 15–19	Input/Output	I/O <sub>0</sub> –I/O <sub>7</sub> . Data lines. Used as input or output lines depending on operation.
27	Input/Control	WE. When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted.
20	Input/Control	CE. When LOW, selects the chip. When HIGH, deselects the chip
22	Input/Control	OE. Output Enable. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins
14	Ground	GND. Ground for the device
28	Power Supply	V <sub>CC</sub> . Power supply for the device

Note

2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub> Typ, T<sub>A</sub> = 25 °C, and t<sub>AA</sub> = 70 ns.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature with power applied ..... -55 °C to +125 °C

Supply voltage to ground potential (pin 28 to pin 14).....-0.5 V to +4.6 V

DC voltage applied to outputs in high Z State<sup>[3]</sup> .....-0.5 V to  $V_{CC} + 0.5 V$

DC input voltage<sup>[3]</sup> .....-0.5 V to  $V_{CC} + 0.5 V$

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage..... > 2001 V (per MIL-STD-883, method 3015)

Latch-up current ..... > 200 mA

## Operating Range

Device	Range	Ambient Temperature (T <sub>A</sub> ) <sup>[4]</sup>	V <sub>CC</sub>
CY62256VN	Commercial	0 °C to +70 °C	2.7 V to 3.6 V
	Industrial	-40 °C to +85 °C	
	Automotive-A	-40 °C to +85 °C	
	Automotive-E	-40 °C to +125 °C	

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-70			Unit		
			Min	Typ <sup>[5]</sup>	Max			
V <sub>OH</sub>	Output HIGH voltage	I <sub>OH</sub> = -1.0 mA	V <sub>CC</sub> = 2.7 V		2.4	-	-	V
V <sub>OL</sub>	Output LOW voltage	I <sub>OL</sub> = 2.1 mA	V <sub>CC</sub> = 2.7 V		-	-	0.4	V
V <sub>IH</sub>	Input HIGH voltage				2.2	-	V <sub>CC</sub> + 0.3V	V
V <sub>IL</sub>	Input LOW voltage				-0.5	-	0.8	V
I <sub>IX</sub>	Input leakage current	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	Commercial/Industrial/Automotive-A	-1	-	+1	μA	
			Automotive-E	-10	-	+10	μA	
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> , Output Disabled	Commercial/Industrial/Automotive-A	-1	-	+1	μA	
			Automotive-E	-10	-	+10	μA	
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	V <sub>CC</sub> = 3.6 V, I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	All ranges		-	11	30	mA
I <sub>SB1</sub>	Automatic CE power down current - TTL inputs	V <sub>CC</sub> = 3.6 V, $\overline{CE} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>	All ranges		-	100	300	μA
I <sub>SB2</sub>	Automatic CE power down current - CMOS inputs	V <sub>CC</sub> = 3.6 V, $\overline{CE} \geq V_{CC} - 0.3 V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3 V or V <sub>IN</sub> ≤ 0.3 V, f = 0	Commercial	-	0.1	5	μA	
			Industrial/Automotive-A	-		10		
			Automotive-E	-		130		

### Notes

3. V<sub>IL</sub> (min) = -2.0 V for pulse durations of less than 20 ns.

4. T<sub>A</sub> is the "Instant-On" case temperature.

5. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub> Typ, T<sub>A</sub> = 25 °C, and t<sub>AA</sub> = 70 ns.

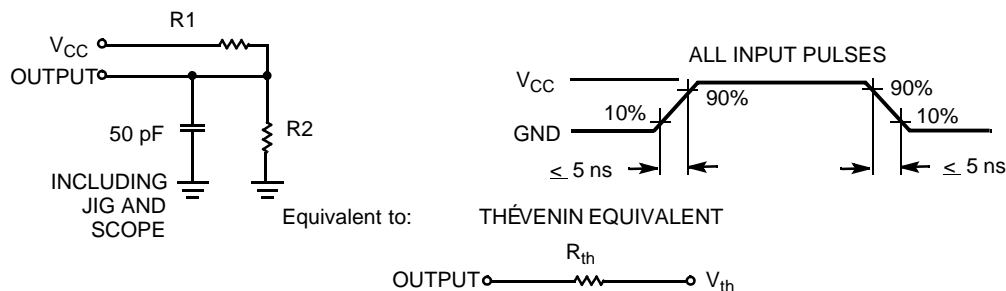
## Capacitance

Parameter <sup>[6]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = 3.0 V	6	pF
C <sub>OUT</sub>	Output capacitance		8	pF

## Thermal Resistance

Parameter <sup>[6]</sup>	Description	Test Conditions	SOIC	TSOPI	RTSOPI	Unit
Θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	68.45	87.62	87.62	°C/W
Θ <sub>JC</sub>	Thermal resistance (junction to case)		26.94	23.73	23.73	°C/W

**Figure 1. AC Test Loads and Waveforms**



Parameter	Value	Units
R1	1100	Ohms
R2	1500	Ohms
R <sub>TH</sub>	645	Ohms
V <sub>TH</sub>	1.750	Volts

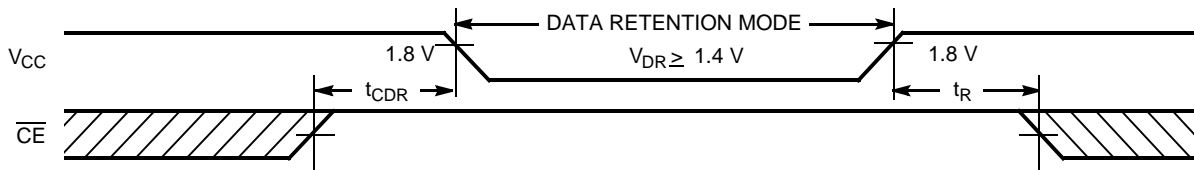
## Data Retention Characteristics

(Over the Operating Range)

Parameter	Description	Conditions <sup>[7]</sup>	Min	Typ <sup>[8]</sup>	Max	Unit
V <sub>DR</sub>	V <sub>CC</sub> for data retention		1.4	–	–	V
I <sub>CCDR</sub>	Data retention current	V <sub>CC</sub> = 1.4 V, CE ≥ V <sub>CC</sub> – 0.3 V, V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.3 V or V <sub>IN</sub> ≤ 0.3 V	Commercial Industrial/ Automotive-A Automotive-E	– 0.1 –	3 6 50	μA
t <sub>CDR</sub> <sup>[6]</sup>	Chip deselect to data retention time		0	–	–	ns
t <sub>R</sub> <sup>[6]</sup>	Operation recovery time		t <sub>RC</sub>	–	–	ns

### Notes

- Tested initially and after any design or process changes that may affect these parameters.
- No input may exceed V<sub>CC</sub> + 0.3 V.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub> Typ, T<sub>A</sub> = 25 °C, and t<sub>AA</sub> = 70 ns.

**Figure 2. Data Retention Waveform**


## Switching Characteristics

 Over the Operating Range<sup>[9]</sup>

Parameter	Description	CY62256VN-70		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{RC}$	Read cycle time	70	–	ns
$t_{AA}$	Address to data valid	–	70	ns
$t_{OHA}$	Data hold from address change	10	–	ns
$t_{ACE}$	$\overline{CE}$ LOW to data valid	–	70	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid	–	35	ns
$t_{LZOE}$	$\overline{OE}$ LOW to low $Z^{[10]}$	5	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to high $Z^{[10, 11]}$	–	25	ns
$t_{LZCE}$	$\overline{CE}$ LOW to low $Z^{[10]}$	10	–	ns
$t_{HZCE}$	$\overline{CE}$ HIGH to high $Z^{[10, 11]}$	–	25	ns
$t_{PU}$	$\overline{CE}$ LOW to power up	0	–	ns
$t_{PD}$	$\overline{CE}$ HIGH to power down	–	70	ns
<b>Write Cycle<sup>[12, 13]</sup></b>				
$t_{WC}$	Write cycle time	70	–	ns
$t_{SCE}$	$\overline{CE}$ LOW to write end	60	–	ns
$t_{AW}$	Address setup to write end	60	–	ns
$t_{HA}$	Address hold from write end	0	–	ns
$t_{SA}$	Address setup to write start	0	–	ns
$t_{PWE}$	$\overline{WE}$ pulse width	50	–	ns
$t_{SD}$	Data setup to write end	30	–	ns
$t_{HD}$	Data hold from write end	0	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to high $Z^{[10, 11]}$	–	25	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to low $Z^{[10]}$	10	–	ns

**Notes**

9. Test conditions assume signal transition time of 5 ns or less timing reference levels of  $V_{CC}/2$ , input pulse levels of 0 to  $V_{CC}$ , and output loading of the specified  $I_{OL}/I_{OH}$  and 100-pF load capacitance.
10. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
11.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with  $C_L = 5$  pF as in (b) of AC Test Loads. Transition is measured  $\pm 200$  mV from steady-state voltage.
12. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
13. The minimum write cycle time for write cycle #3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

Switching Waveforms

Figure 3. Read Cycle No. 1<sup>[14, 15]</sup>

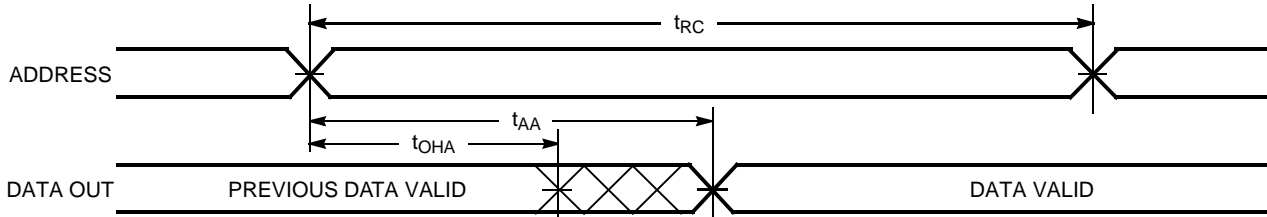


Figure 4. Read Cycle No. 2<sup>[15, 16]</sup>

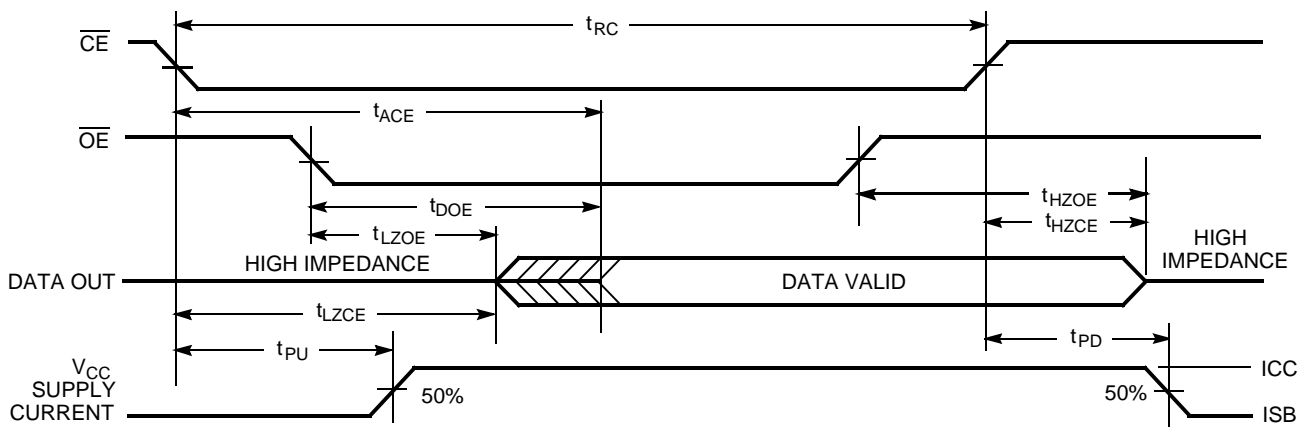
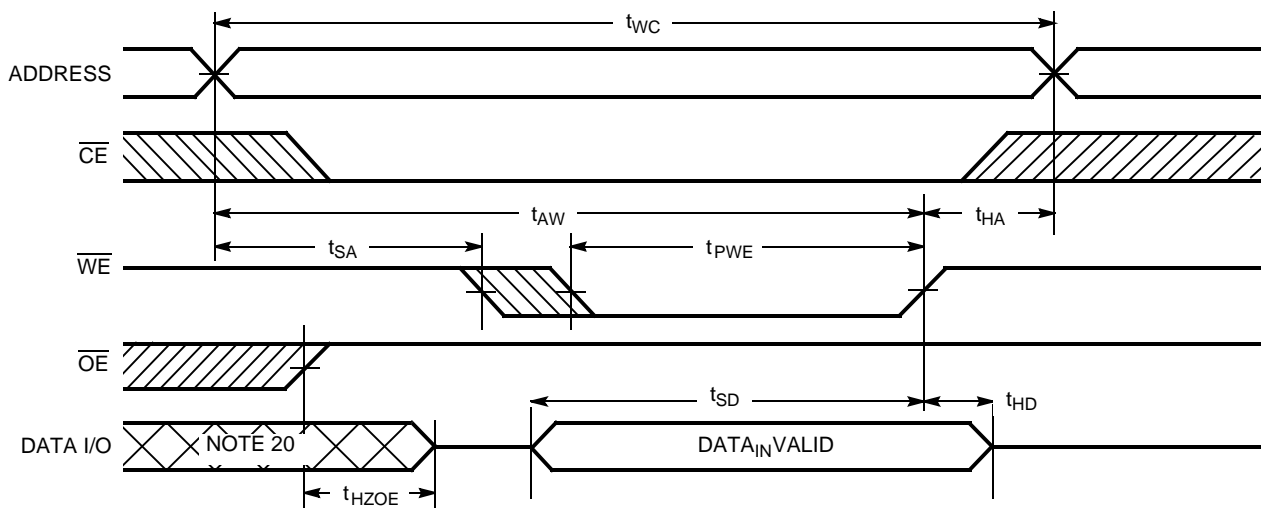


Figure 5. Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[17, 18, 19]</sup>



Notes

- 14. Device is continuously selected.  $\overline{OE}, \overline{CE} = V_{IL}$ .
- 15.  $\overline{WE}$  is HIGH for read cycle.
- 16. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
- 17. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- 18. Data I/O is high impedance if  $OE = V_{IH}$ .
- 19. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.
- 20. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 2 ( $\overline{\text{CE}}$  Controlled)<sup>[21, 22, 23]</sup>

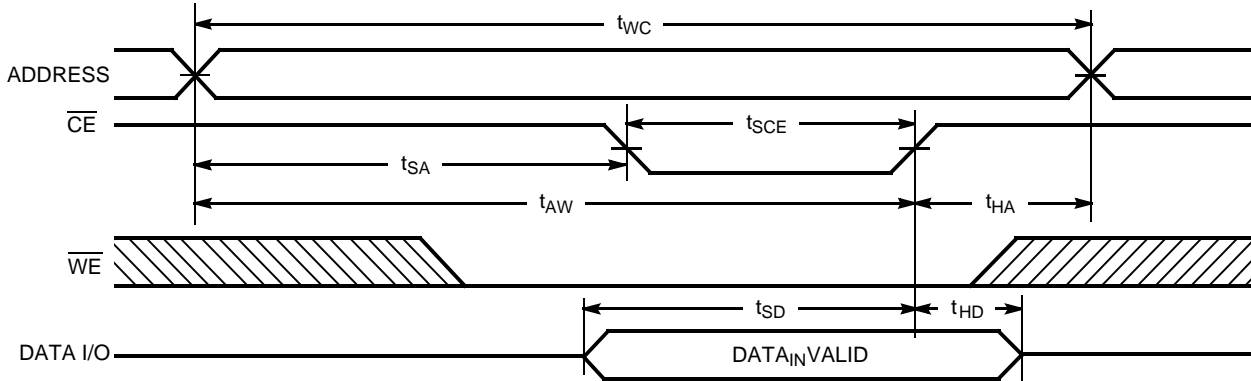
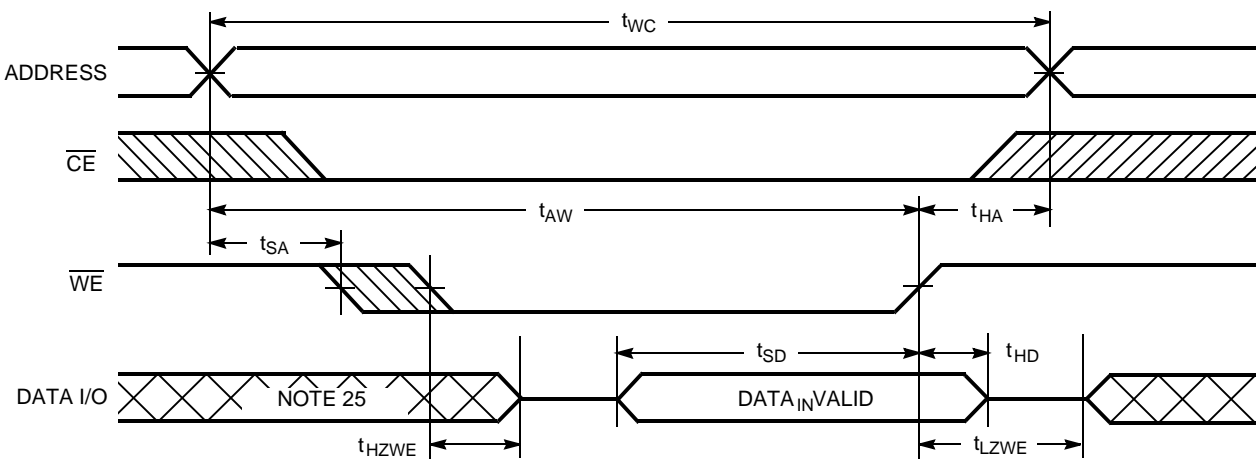


Figure 7. Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[23, 24]</sup>

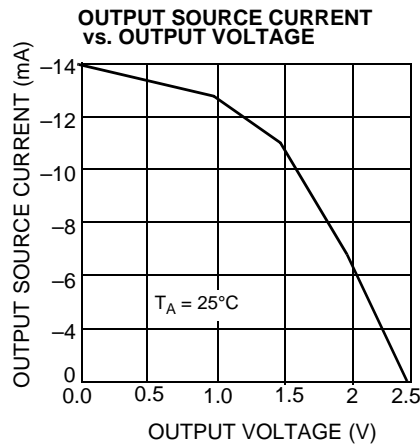
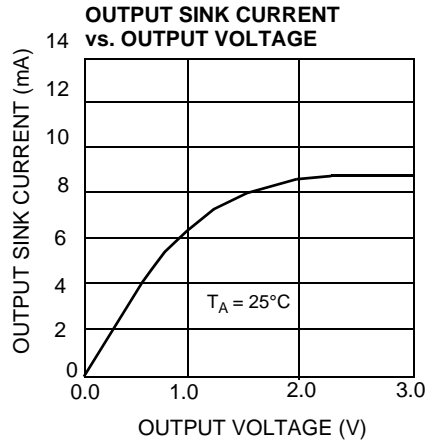
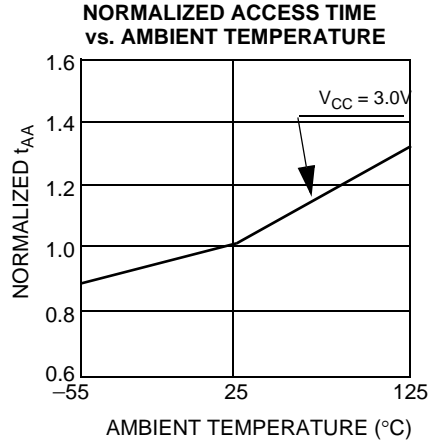
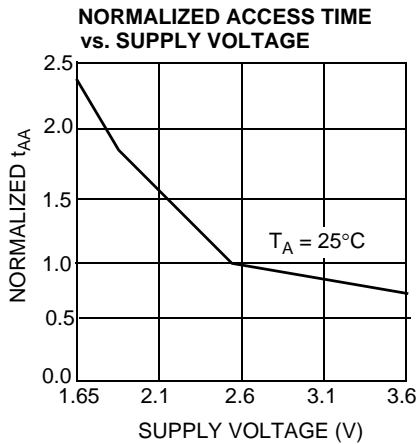
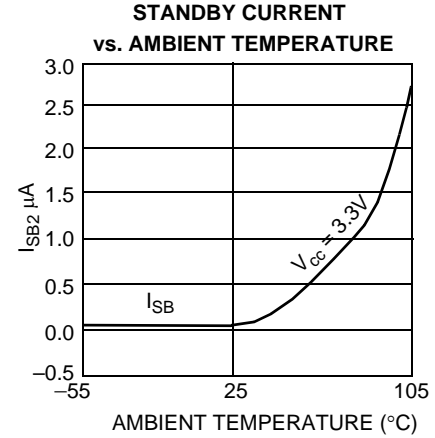
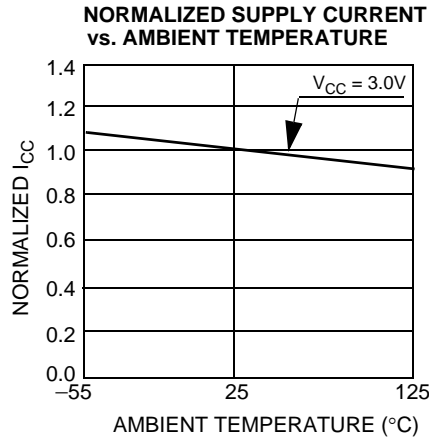
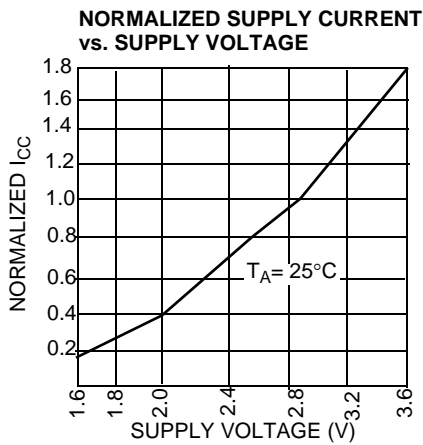


Notes

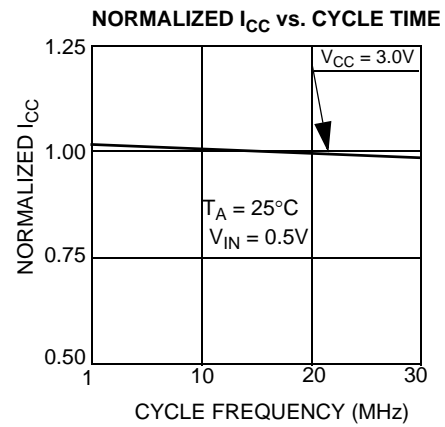
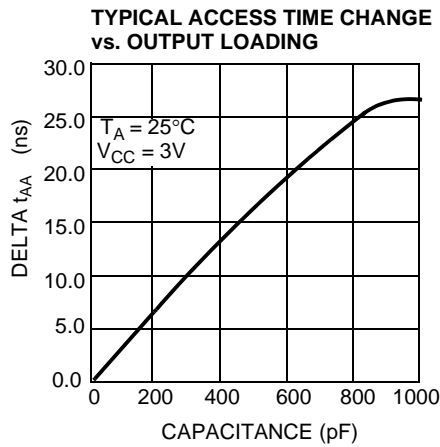
- 21. The internal write time of the memory is defined by the overlap of  $\overline{\text{CE}}$  LOW and  $\overline{\text{WE}}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- 22. Data I/O is high impedance if  $\text{OE} = V_{IH}$ .
- 23. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  HIGH, the output remains in a high impedance state.
- 24. The minimum write cycle time for write cycle #3 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .
- 25. During this period, the I/Os are in output state and input signals should not be applied.



### Typical DC and AC Characteristics



Typical DC and AC Characteristics (continued)



Truth Table

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/power down	Standby (I <sub>SB</sub> )
L	H	L	Data Out	Read	Active (I <sub>CC</sub> )
L	L	X	Data In	Write	Active (I <sub>CC</sub> )
L	H	H	High Z	Deselect, output disabled	Active (I <sub>CC</sub> )

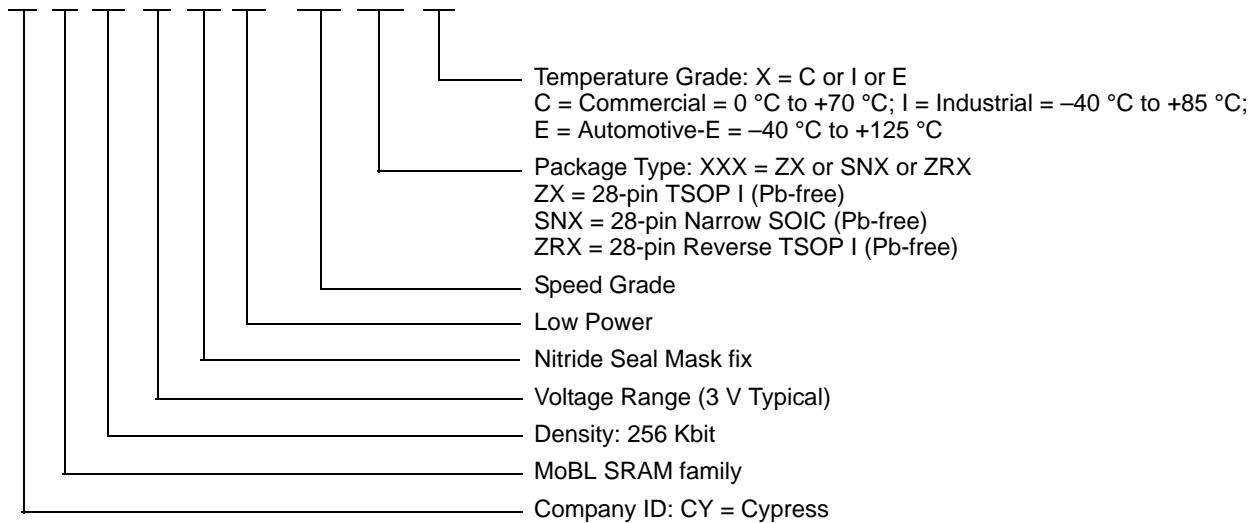
**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
70	CY62256VNLL-70ZXC	51-85071	28-pin TSOP I (Pb-free)	Commercial
	CY62256VNLL-70SNXI	51-85092	28-pin (300-mil) Narrow SOIC (Pb-free)	Industrial
	CY62256VNLL-70ZXI	51-85071	28-pin TSOP I (Pb-free)	
	CY62256VNLL-70ZRXI	51-85074	28-pin Reverse TSOP I (Pb-free)	
	CY62256VNLL-70SNXE	51-85092	28-pin (300-mil) Narrow SOIC (Pb-free)	Automotive-E
	CY62256VNLL-70ZXE	51-85071	28-pin TSOP I (Pb-free)	

Contact your local Cypress sales representative for availability of other parts

**Ordering Code Definitions**

CY 62 256 V N LL - 70 XXX X



Package Diagrams

Figure 8. 28-pin (300-mil) SNC (Narrow Body), 51-85092

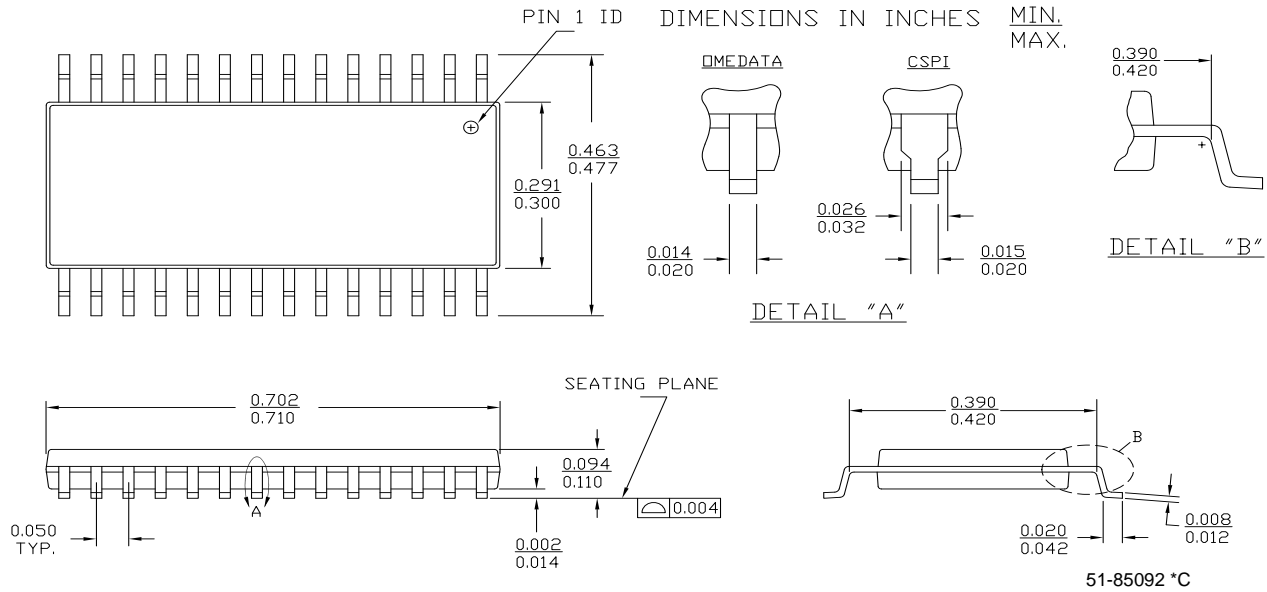


Figure 9. 28-pin TSOP 1 (8 x 13.4 mm), 51-85071

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2

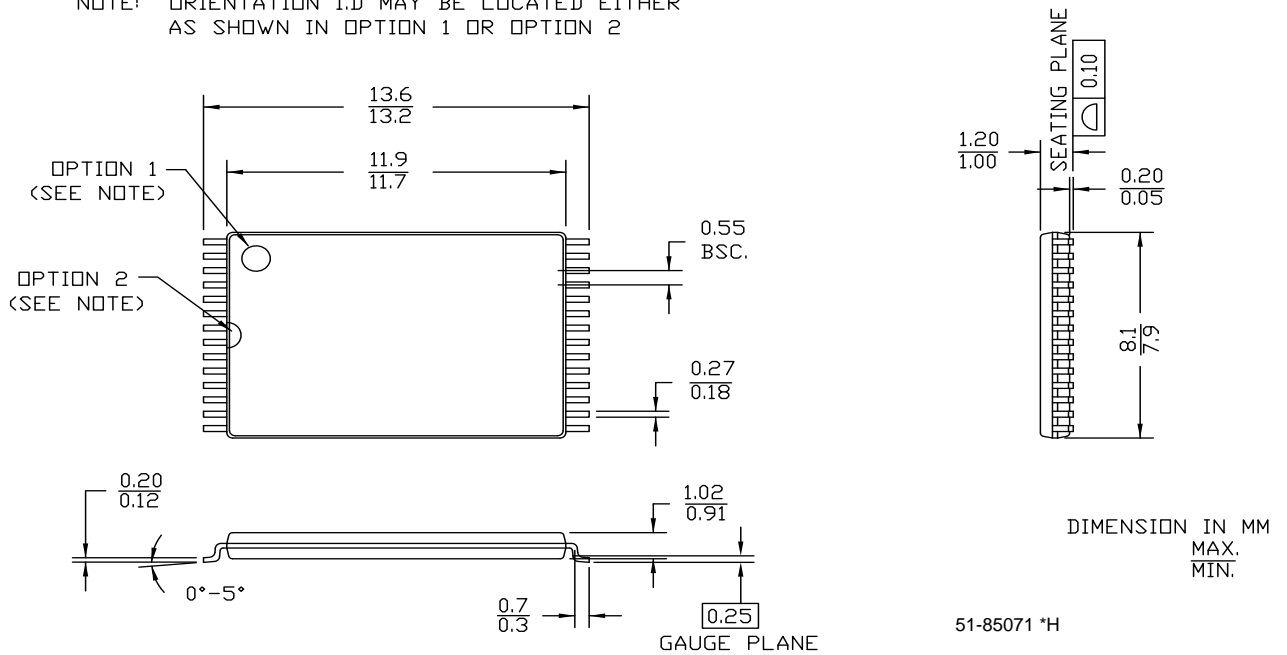
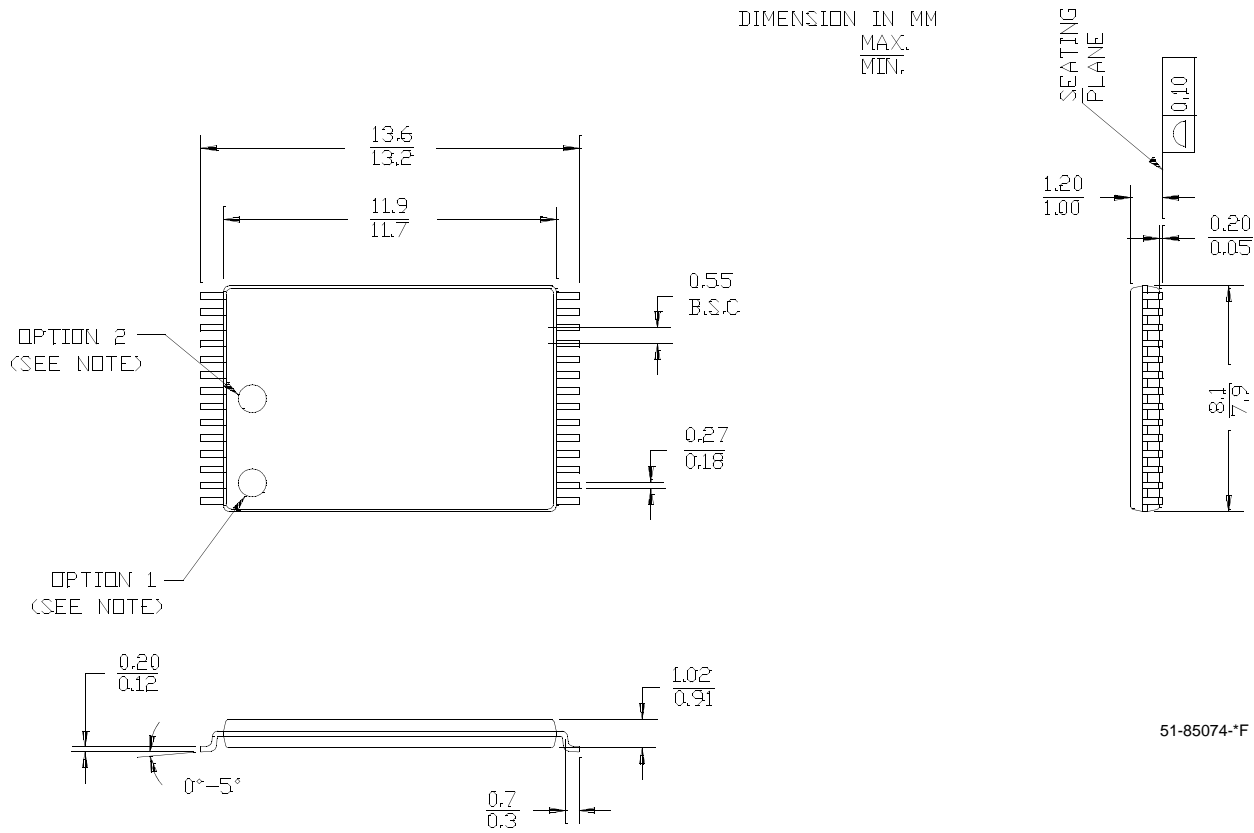


Figure 10. 28-pin Reverse TSOP 1 (8 x 13.4 mm), 51-85074

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2



51-85074-F

## Document History Page

Document Title: CY62256VN 256K (32K × 8) Static RAM Document Number: 001-06512				
Rev.	ECN No.	Submission Date	Orig. of Change	Description of Change
**	426504	See ECN	NXR	New Data Sheet
*A	488954	See ECN	NXR	Added Automotive product Updated ordering Information table
*B	2769239	09/25/09	VKN/AESA	Corrected V <sub>IL</sub> description in the Electrical Characteristics table
*C	2901521	03/30/2010	AJU	Removed inactive parts from Ordering Information. Updated Package Diagram
*D	3119519	01/04/2011	AJU	Updated <a href="#">Ordering Information</a> . Added <a href="#">Ordering Code Definitions</a> .

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturers representatives, and distributors. To find the office closest to you, visit us at [cypress.com/sales](http://cypress.com/sales).

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