M34E02

2 Kbit Serial I²C Bus EEPROM
Serial Presence Detect for DDR2 DIMMs

FEATURES SUMMARY

- Software Data Protection for lower 128 bytes
- Two Wire I^2C Serial Interface
- 100kHz Transfer Rates
- 1.7 to 3.6V Single Supply Voltage:
- BYTE and PAGE WRITE (up to 16 bytes)
- RANDOM and SEQUENTIAL READ Modes
- Self-Timed Programming Cycle
- Automatic Address Incrementing
- Enhanced ESD/Latch-Up Protection
- More than 1 Million Erase/Write Cycles
- More than 40 Year Data Retention

Figure 1. Packages

UFDFPN8 (MB)
2x3mm² (MLP)

TSSOP8 (DW)
4.4x3mm²

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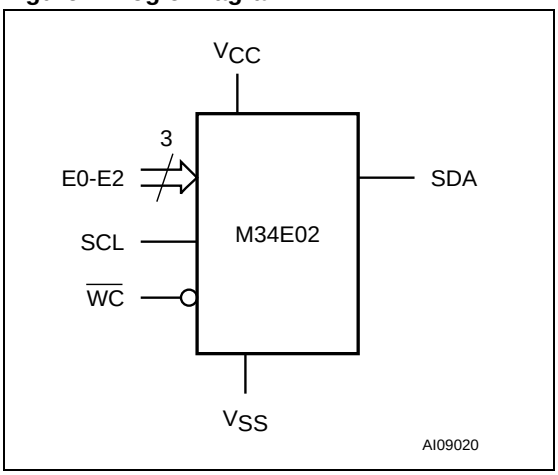
SUMMARY DESCRIPTION

The M34E02 is a 2 Kbit serial EEPROM memory able to lock permanently the data in its first half (from location 00h to 7Fh). This facility has been designed specifically for use in DRAM DIMMs (dual interline memory modules) with Serial Presence Detect. All the information concerning the DRAM module configuration (such as its access speed, its size, its organization) can be kept write protected in the first half of the memory.

This bottom half of the memory area can be write-protected using two different software write protection mechanisms. By sending the device a specific sequence, the first 128 bytes of the memory become write protected: permanently or resetable. In addition, the device allows the entire memory area to be write protected, using the $\overline{WC}$ input (for example by tieing this input to V_{CC}).

These I^2C-compatible electrically erasable programmable memory (EEPROM) devices are organized as 256x8 bits.

Figure 2. Logic Diagram

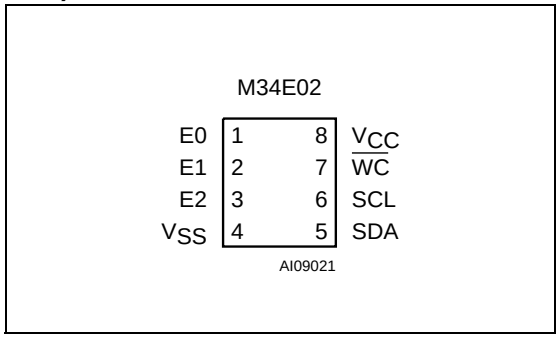


I^2C uses a two wire serial interface, comprising a bi-directional data line and a clock line. The device carries a built-in 4-bit Device Type Identifier code (1010) in accordance with the I^2C bus definition to access the memory area and a second Device Type Identifier Code (0110) to define the protection. These codes are used together with the voltage level applied on the three chip enable inputs (E2, E1, E0).

The device behaves as a slave device in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a START condition, generated by the bus master. The START condition is followed by a Device Select Code and $\overline{RW}$ bit (as described in Table 2), terminated by an acknowledge bit.

When writing data to the memory, the memory inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a STOP condition after an Ack for WRITE, and after a NoAck for READ.

Figure 3. TSSOP and MLP Connections (Top View)



Note: 1. See the pages after page 19 for package dimensions, and how to identify pin-1.

Table 1. Signal Names

E0, E1, E2	Chip Enable
SDA	Serial Data
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Power On Reset: V_{CC} Lock-Out Write Protect

In order to prevent data corruption and inadvertent Write operations during power up, a Power On Reset (POR) circuit is included. At Power-on, the internal reset is held active until V_{CC} has reached the POR threshold value, and all operations are disabled – the device will not respond to any command. In the same way, when V_{CC} drops from the operating voltage, below the POR threshold value, all operations are disabled and the device will not respond to any command.

A stable and valid V_{CC} (as defined in Table 8) must be applied before applying any logic signal.

SIGNAL DESCRIPTION

Serial Clock (SCL)

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor can be connected from Serial Clock (SCL) to V_{CC}. (Figure 4 indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

Serial Data (SDA)

This bi-directional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to V_{CC}. (Figure 4 indicates how the value of the pull-up resistor can be calculated).

Chip Enable (E0, E1, E2)

These input signals are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit Device Select Code. In the end application, E0, E1 and E2 must be directly (not through a pull-up or pull-down resistor) connected to V_{CC} or V_{SS} to establish the Device Select Code. When these inputs are not connected, an internal pull-down circuitry makes (E0,E1,E2) = (0,0,0).

The E0 input is used to detect the V_{HV} voltage, when decoding an SWP or CWP instruction.

Write Control (WC)

This input signal is provided for protecting the contents of the whole memory from inadvertent write operations. Write Control (WC) is used to enable (when driven Low) or disable (when driven High) write instructions to the entire memory area or to the Protection Register.

When Write Control ($\overline{WC}$) is tied Low or left unconnected, the write protection of the first half of the memory is determined by the status of the Protection Register.

Figure 4. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus

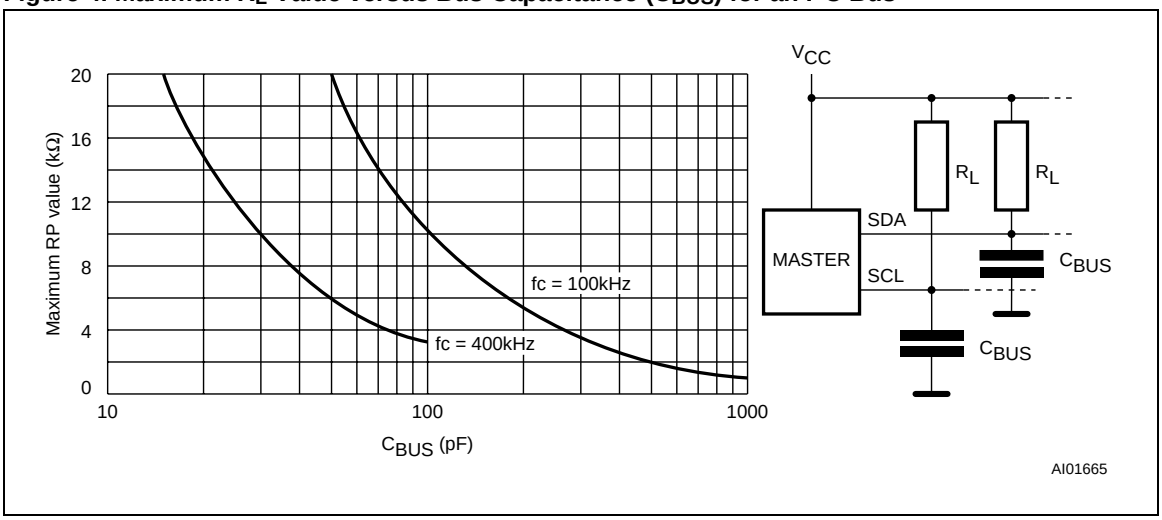


Figure 5. I²C Bus Protocol

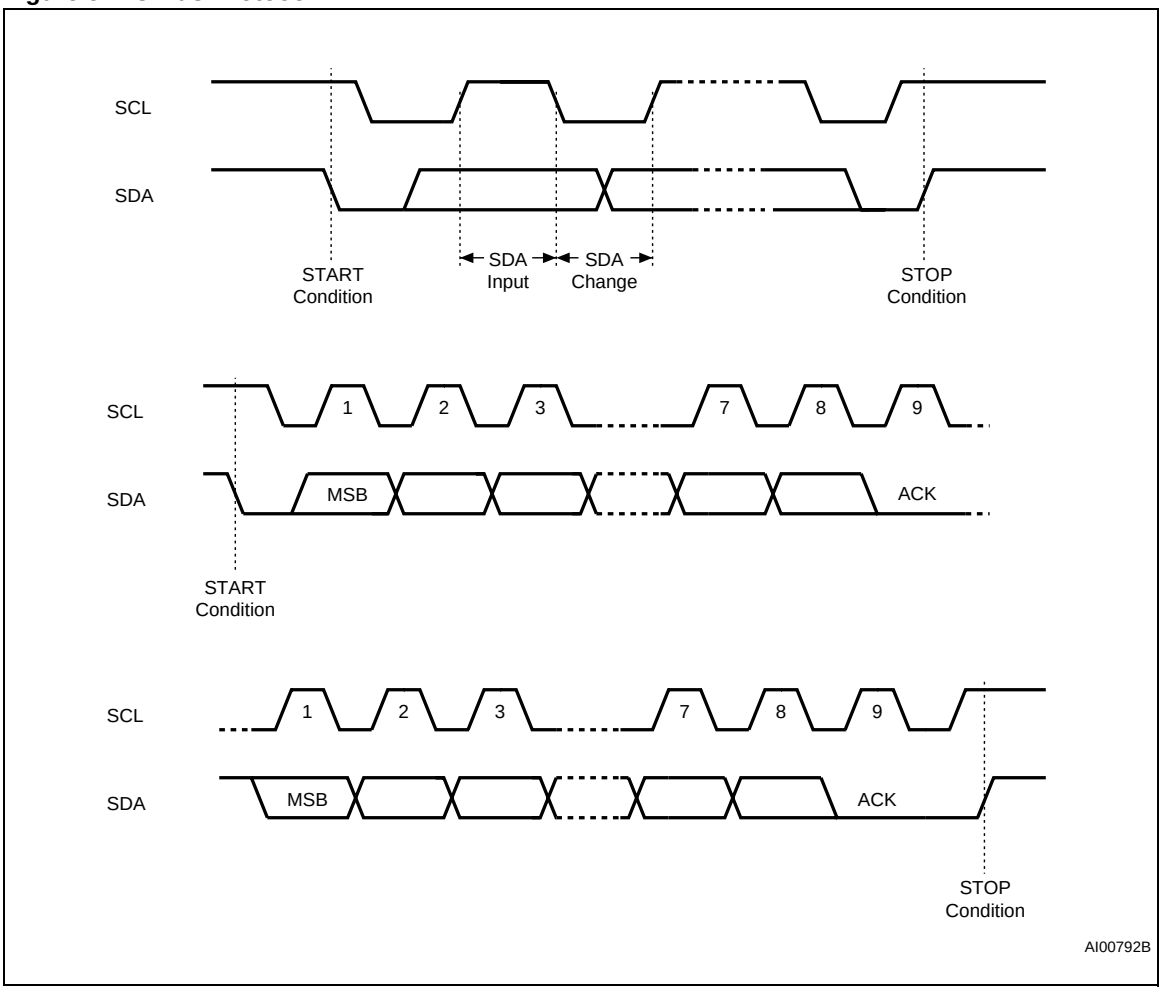


Table 2. Device Select Code

	Chip Enable Signals			Device Type Identifier				Chip Enable Bits			RW
				b7 [1]	b6	b5	b4	b3	b2	b1	b0
Memory Area Select Code (two arrays) [2]	E2	E1	E0	1	0	1	0	E2	E1	E0	RW
Set Write Protection (SWP)	V_{SS}	V_{SS}	V_{HV}	0	1	1	0	0	0	1	0
Clear Write Protection (CWP)	V_{SS}	V_{CC}	V_{HV}					0	1	1	0
Permanently Set Write Protection (PSWP) [2]	E2	E1	E0					E2	E1	E0	0
Read SWP	V_{SS}	V_{SS}	V_{HV}					0	0	1	1
Read CWP	V_{SS}	V_{CC}	V_{HV}					0	1	1	1
Read PSWP [2]	E2	E1	E0					E2	E1	E0	1

Note: 1. The most significant bit, b7, is sent first.
2. E0, E1 and E2 are compared against the respective external pins on the memory device.

DEVICE OPERATION

The device supports the I^2C protocol. This is summarized in Figure 5. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The memory device is always a slave in all communication.

Start Condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the High state. A Start condition must precede any data transfer command. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition, and will not respond unless one is given.

Stop Condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven High. A Stop condition terminates communication between the device and the bus master. A Read command that is followed by NoAck can be followed by a Stop condition to force the device into the Stand-by mode. A Stop condition at the end of a Write command triggers the internal EEPROM Write cycle.

Acknowledge Bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9^{th} clock pulse period, the receiver pulls Serial Data (SDA) Low to acknowledge the receipt of the eight data bits.

Data Input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change *only* when Serial Clock (SCL) is driven Low.

Memory Addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the Device Select Code, shown in Table 2 (on Serial Data (SDA), most significant bit first).

The Device Select Code consists of a 4-bit Device Type Identifier, and a 3-bit Chip Enable “Address” (E2, E1, E0). To address the memory array, the 4-bit Device Type Identifier is 1010b; to access the write-protection settings, it is 0110b.

Up to eight memory devices can be connected on a single I^2C bus. Each one is given a unique 3-bit code on the Chip Enable (E0, E1, E2) inputs. When the Device Select Code is received, the device only responds if the Chip Enable Address is the same as the value on the Chip Enable (E0, E1, E2) inputs.

The 8^{th} bit is the Read/$\overline{\text{Write}}$ bit ($\overline{\text{RW}}$). This bit is set to 1 for Read and 0 for Write operations.

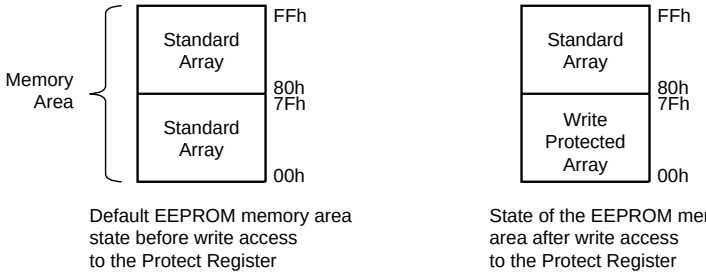
If a match occurs on the Device Select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9^{th} bit time. If the device does not match the Device Select code, it deselects itself from the bus, and goes into Stand-by mode.

Table 3. Operating Modes

Mode	$\overline{\text{RW}}$ bit	$\overline{\text{WC}}$ [1]	Bytes	Initial Sequence
Current Address Read	1	X	1	START, Device Select, $\overline{\text{RW}}$ = 1
Random Address Read	0	X	1	START, Device Select, $\overline{\text{RW}}$ = 0, Address
	1	X		reSTART, Device Select, $\overline{\text{RW}}$ = 1
Sequential Read	1	X	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V_{IL}	1	START, Device Select, $\overline{\text{RW}}$ = 0
Page Write	0	V_{IL}	≤ 16	START, Device Select, $\overline{\text{RW}}$ = 0

Note: 1. X = V_{IH} or V_{IL}.

Figure 6. Result of Setting the Write Protection



Setting the Write-Protection

The M34E02 has a hardware write-protection feature, using the Write Control (WC) signal. This signal can be driven High or Low, and must be held constant for the whole instruction sequence. When Write Control (WC) is held High, the whole memory array (addresses 00h to FFh) is write protected. When Write Control (WC) is held Low, the write protection of the memory array is dependent on whether software write-protection has been set.

Software write-protection allows the bottom half of the memory area (addresses 00h to 7Fh) to be write protected irrespective of subsequent states of the Write Control (WC) signal.

Software write-protection is handled by three instructions:

– SWP: Set Write Protection

– CWP: Clear Write Protection

– PSWP: Permanently Set Write Protection

The level of write-protection (set or cleared) that has been defined using these instructions, remains defined even after a power cycle.

SWP and CWP. If the software write-protection has been set with the SWP instruction, it can be cleared again with a CWP instruction.

The two instructions (SWP and CWP) have the same format as a Byte Write instruction, but with a different Device Type Identifier (as shown in Table 2). Like the Byte Write instruction, it is followed by an address byte and a data byte, but in this case the contents are all “Don’t Care” (Figure 7). Another difference is that the voltage, V_{HV}, must be applied on the E0 pin, and specific logical levels must be applied on the other two (E1 and E2, as shown in Table 2).

PSWP. If the software write-protection has been set with the PSWP instruction, the first 128 bytes of the memory are permanently write-protected. This write-protection cannot be cleared by any instruction, or by power-cycling the device, and regardless the state of Write Control (WC). Also, once the PSWP instruction has been successfully executed, the M34E02 no longer acknowledges any instruction (with a Device Type Identifier of 0110) to access the write-protection settings.

Figure 7. Setting the Write Protection ($\overline{WC}$ = 0)

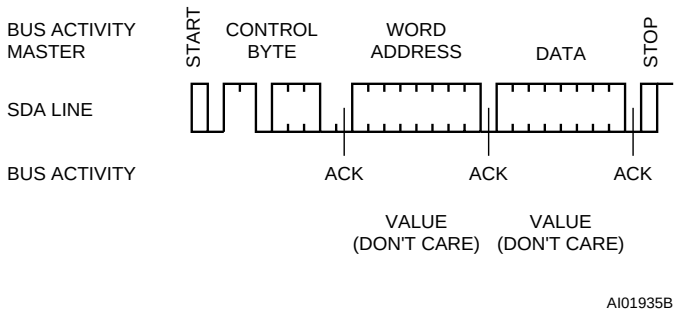
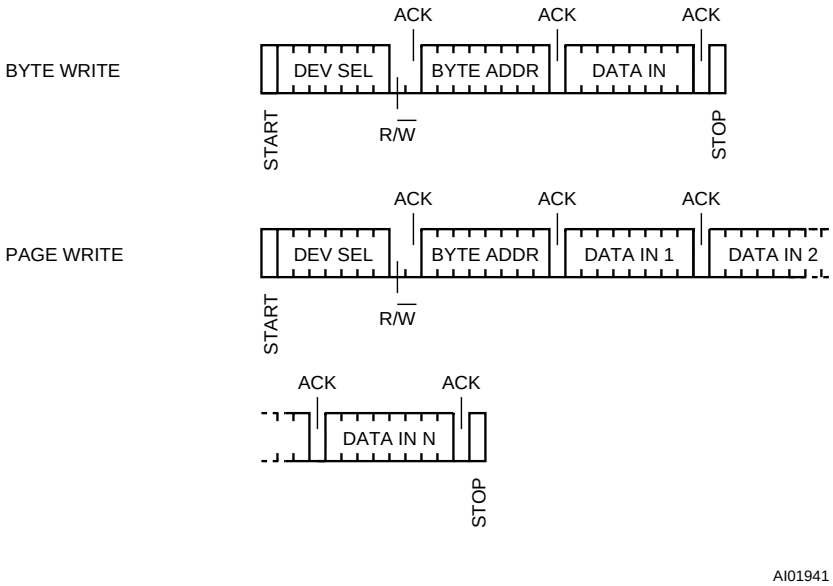


Figure 8. Write Mode Sequences in a Non Write-Protected Area



Write Operations

Following a Start condition the bus master sends a Device Select Code with the RW bit reset to 0. The device acknowledges this, as shown in Figure 8, and waits for an address byte. The device responds to the address byte with an acknowledge bit, and then waits for the data byte.

When the bus master generates a Stop condition immediately after the Ack bit (in the "10^{th} bit" time slot), either at the end of a Byte Write or a Page Write, the internal memory Write cycle is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

During the internal Write cycle, Serial Data (SDA) and Serial Clock (SCL) are ignored, and the device does not respond to any requests.

Byte Write

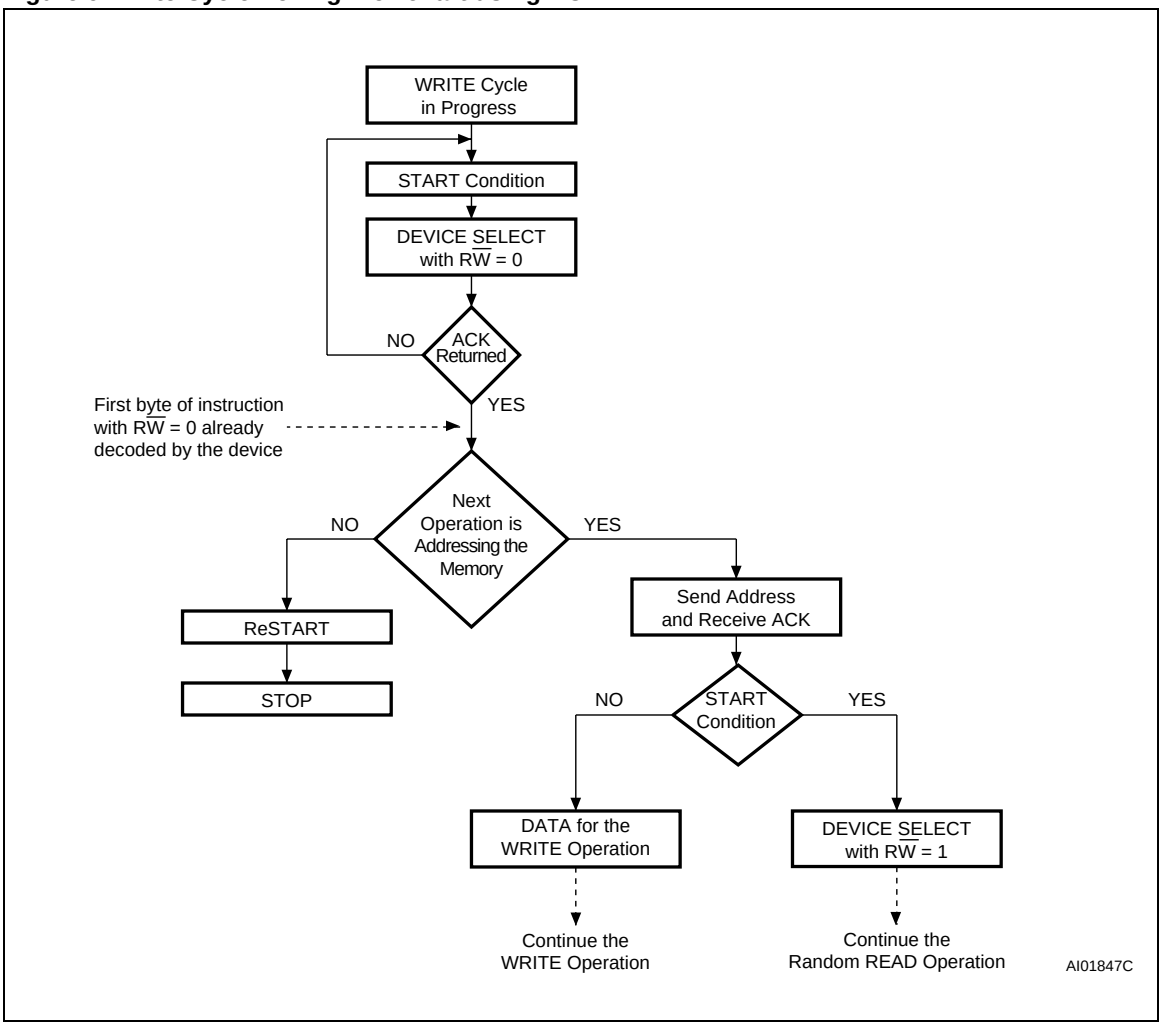
After the Device Select Code and the address byte, the bus master sends one data byte. If the addressed location is hardware write-protected, the device replies to the data byte with NoAck, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in Figure 8.

Page Write

The Page Write mode allows up to 16 bytes to be written in a single Write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits are the same. If more bytes are sent than will fit up to the end of the page, a condition known as 'roll-over' occurs. This should be avoided, as data starts to become overwritten in an implementation dependent way.

The bus master sends from 1 to 16 bytes of data, each of which is acknowledged by the device if Write Control (WC) is Low. If the addressed location is hardware write-protected, the device replies to the data byte with NoAck, and the locations are not modified. After each byte is transferred, the internal byte address counter (the 4 least significant address bits only) is incremented. The transfer is terminated by the bus master generating a Stop condition.

Figure 9. Write Cycle Polling Flowchart using ACK



Minimizing System Delays by Polling On ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time (t_W) is shown in Table 12, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

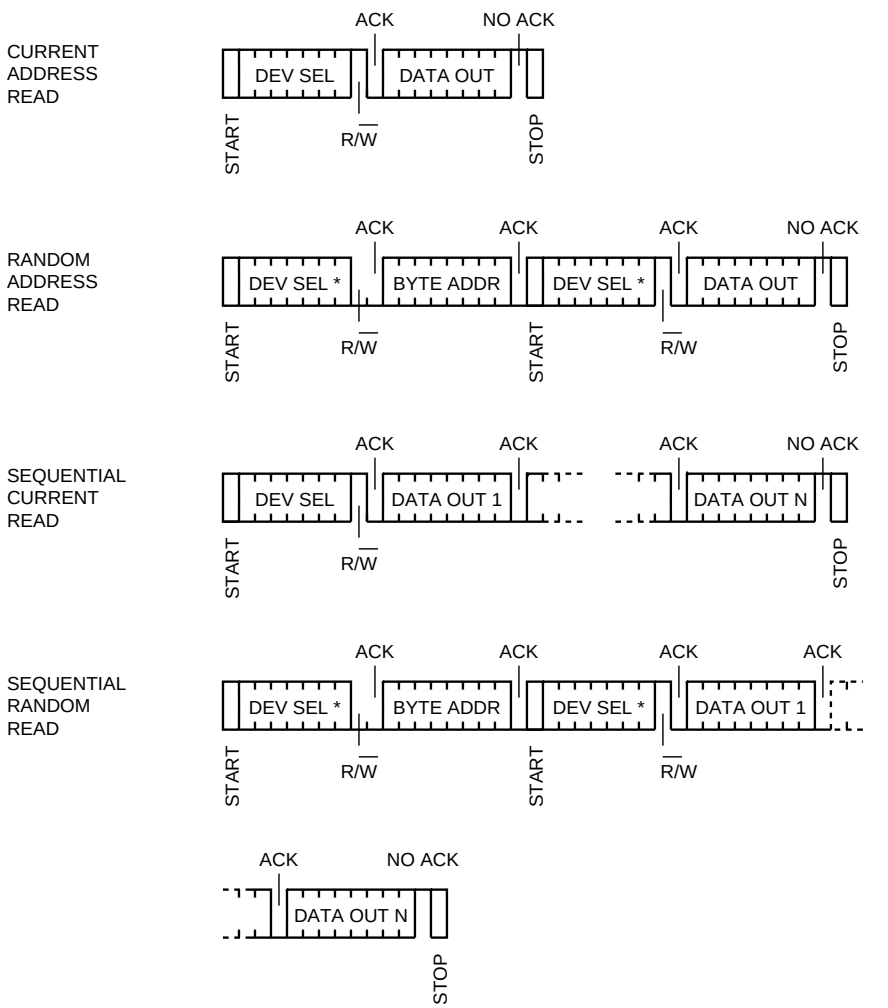
The sequence, as shown in Figure 9, is:

– Initial condition: a Write cycle is in progress.

– Step 1: the bus master issues a Start condition followed by a Device Select Code (the first byte of the new instruction).

– Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

Figure 10. Read Mode Sequences



Note: 1. The seven most significant bits of the Device Select Code of a Random Read (in the 1st and 3rd bytes) must be identical.

Read Operations

Read operations are performed independently of whether hardware or software protection has been set.

The device has an internal address counter which is incremented each time a byte is read.

Random Address Read

A dummy Write is first performed to load the address into this address counter (as shown in Figure 10) but *without* sending a Stop condition. Then, the bus master sends another Start condition, and repeats the Device Select Code, with the RW bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must *not* acknowledge the byte, and terminates the transfer with a Stop condition.

Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a Device Select Code with the RW bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in Figure 10, *without* acknowledging the byte.

Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master *does* acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in Figure 10.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over', and the device continues to output data from memory address 00h.

Acknowledge in Read Mode

For all Read commands, the device waits, after each byte read, for an acknowledgment during the 9th bit time. If the bus master does not drive Serial Data (SDA) Low during this time, the device terminates the data transfer and switches to its Standby mode.

INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh).

USE WITHIN A DDR2 DIMM

In the application, the M34E02 is soldered directly in the printed circuit module. The three Chip Enable inputs (E0, E1, E2) must be connected to V_{SS} or V_{CC} directly (that is without using a pull-up or pull-down resistor) through the DIMM socket (see Table 4.). The pull-up resistors needed for normal behavior of the I^2C bus are connected on the I^2C bus of the mother-board (as shown in Figure 11).

The Write Control ($\overline{WC}$) of the M34E02 can be left unconnected. However, connecting it to V_{SS} is recommended, to maintain full read and write access.

Table 4. DRAM DIMM Connections

DIMM Position	E2	E1	E0
0	V_{SS}	V_{SS}	V_{SS}
1	V_{SS}	V_{SS}	V_{CC}
2	V_{SS}	V_{CC}	V_{SS}
3	V_{SS}	V_{CC}	V_{CC}
4	V_{CC}	V_{SS}	V_{SS}
5	V_{CC}	V_{SS}	V_{CC}
6	V_{CC}	V_{CC}	V_{SS}
7	V_{CC}	V_{CC}	V_{CC}

Programming the M34E02

The situations in which the M34E02 is programmed can be considered under two headings:

– when the DDR2 DIMM is isolated (not inserted on the PCB motherboard)

– when the DDR2 DIMM is inserted on the PCB motherboard

DDR2 DIMM Isolated. With specific programming equipment, it is possible to define the M34E02 content, using Byte and Page Write instructions, and its write-protection using the SWP and CWP instructions. To issue the SWP and CWP instructions, the DDR2 DIMM must be inserted in the DDR2-specific slot where the E0 signal can be driven to V_{HV} during the whole instruction. This programming step is mainly intended for use by DDR2 DIMM makers, whose end application manufacturers will want to clear this write-protection with the CWP on their own specific programming equipment, to modify the lower 128 Bytes, and finally to set permanently the write-protection with the PSWP instruction.

DDR2 DIMM Inserted in the Application Mother Board. As the final application cannot drive the E0 pin to V_{HV}, the only possible action is to freeze the write-protection with the PSWP instruction.

Table 5 and Table 6 show how the Ack bits can be used to identify the write-protection status.

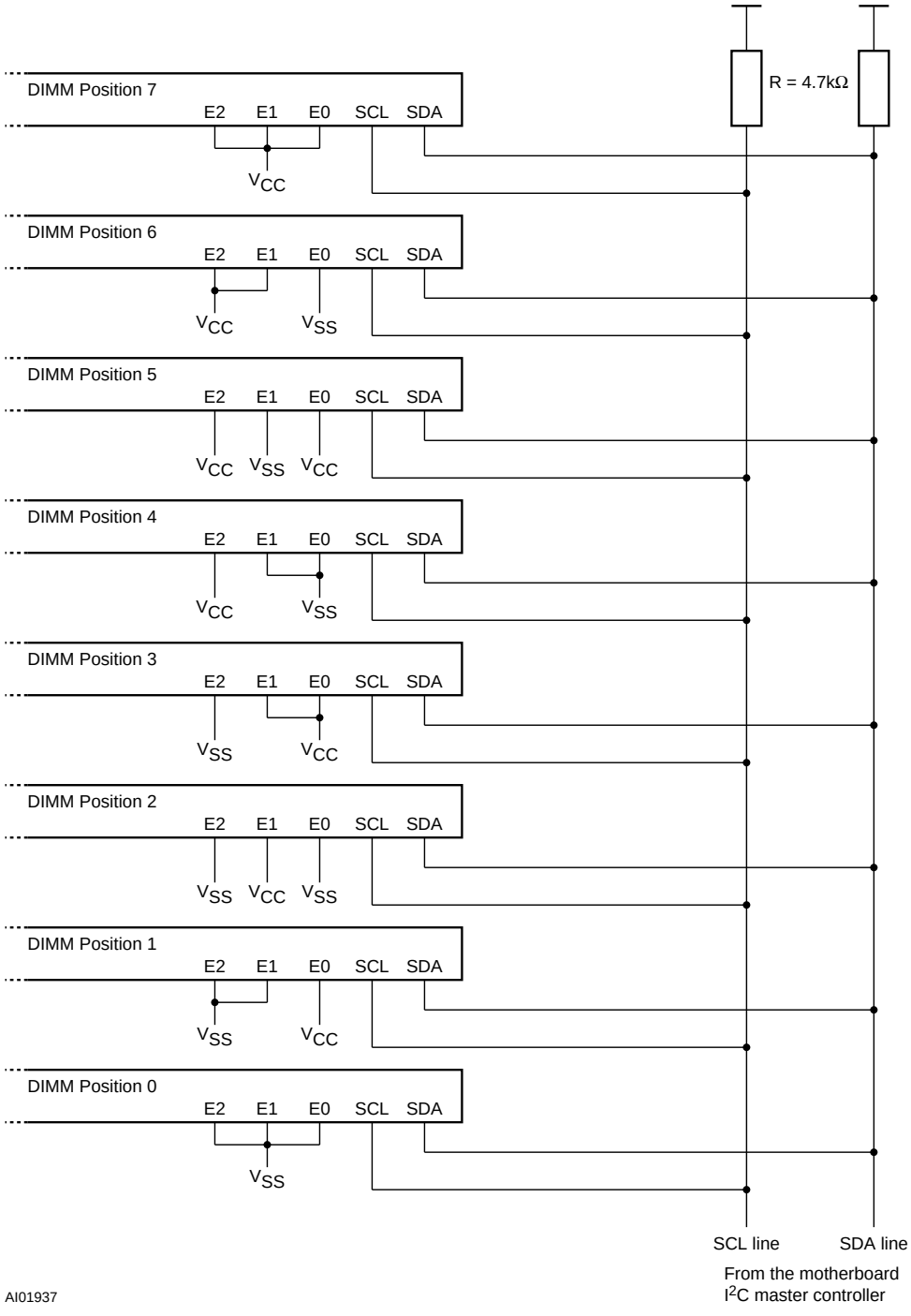
Table 5. Acknowledge when Writing Data or Defining the Write-protection (Instructions with R/W bit=0)

Status	$\overline{WC}$ Input Level	Instruction	Ack	Address	Ack	Data Byte	Ack	Write Cycle (t_W)
Permanently protected	X	PSWP, SWP or CWP	NoAck	Not significant	NoAck	Not significant	NoAck	No
		Page or Byte Write in lower 128 Bytes	Ack	Address	Ack	Data	NoAck	No
Protected with SWP	0	SWP	NoAck	Not significant	NoAck	Not significant	NoAck	No
		CWP	Ack	Not significant	Ack	Not significant	Ack	Yes
		PSWP	Ack	Not significant	Ack	Not significant	Ack	Yes
		Page or Byte Write in lower 128 Bytes	Ack	Address	Ack	Data	NoAck	No
	1	SWP	NoAck	Not significant	NoAck	Not significant	NoAck	No
		CWP	Ack	Not significant	Ack	Not significant	NoAck	No
		PSWP	Ack	Not significant	Ack	Not significant	NoAck	No
		Page or Byte Write	Ack	Address	Ack	Data	NoAck	No
Not Protected	0	PSWP, SWP or CWP	Ack	Not significant	Ack	Not significant	Ack	Yes
		Page or Byte Write	Ack	Address	Ack	Data	Ack	Yes
	1	PSWP, SWP or CWP	Ack	Not significant	Ack	Not significant	NoAck	No
		Page or Byte Write	Ack	Address	Ack	Data	NoAck	No

Table 6. Acknowledge when Reading the Write Protection (Instructions with R/W bit=1)

Status	Instruction	Ack	Address	Ack	Data byte	Ack
Permanently protected	PSWP, SWP or CWP	NoAck	Not significant	NoAck	Not significant	NoAck
Protected with SWP	SWP	NoAck	Not significant	NoAck	Not significant	NoAck
	CWP	Ack	Not significant	NoAck	Not significant	NoAck
	PSWP	Ack	Not significant	NoAck	Not significant	NoAck
Not Protected	PSWP, SWP or CWP	Ack	Not significant	NoAck	Not significant	NoAck

Figure 11. Serial Presence Detect Block Diagram



Note: 1. E0, E1 and E2 are wired at each DIMM socket in a binary sequence for a maximum of 8 devices.
2. Common clock and common data are shared across all the devices.
3. Pull-up resistors are required on all SDA and SCL bus lines (typically 4.7 kΩ) because these lines are open drain when used as outputs.

MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 7. Absolute Maximum Ratings

Symbol	Parameter		Min.	Max.	Unit
T_{STG}	Storage Temperature		–65	150	°C
T_{LEAD}	Lead Temperature during Soldering [1]		See note [1]		°C
V_{IO}	Input or Output range	E0 Others	–0.50 –0.50	10.0 6.5	V
V_{CC}	Supply Voltage		–0.5	6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [2]		–4000	4000	V

Note: 1. Compliant with JEDEC Std J-STD-020B (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
2. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω)

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 8. Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	1.7	3.6	V
T_A	Ambient Operating Temperature	0	70	°C

Table 9. AC Measurement Conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load Capacitance	100		pF
	Input Rise and Fall Times		50	ns
	Input Levels	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input and Output Timing Reference Levels	$0.3V_{CC}$ to $0.7V_{CC}$		V

Figure 12. AC Measurement I/O Waveform

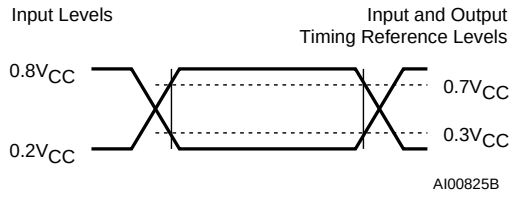


Table 10. Input Parameters

Symbol	Parameter[1,2]	Test Condition	Min.	Max.	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{EiL}	Ei (E0, E1, E2) Input Impedance	$V_{IN} < 0.3V_{CC}$	30		kΩ
Z_{EiH}	Ei (E0, E1, E2) Input Impedance	$V_{IN} > 0.7V_{CC}$	800		kΩ
Z_{WCL}	$\overline{WC}$ Input Impedance	$V_{IN} < 0.3V_{CC}$	5		kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance	$V_{IN} > 0.7V_{CC}$	500		kΩ
t_{NS}	Pulse width ignored (Input Filter on SCL and SDA)	Single glitch		100	ns

Note: 1. T_A = 25 °C, f = 400 kHz
2. Sampled only, not 100% tested.

Table 11. DC Characteristics

Symbol	Parameter	Test Condition (in addition to those in Table 8)	Min.[1]	Max.[1]	Unit
I_{LI}	Input Leakage Current (SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ or V_{CC}, SDA in Hi-Z		± 2	µA
I_{CC}	Supply Current	V_{CC} =1.7V, f_c=100kHz (rise/fall time < 30ns)		1	mA
I_{CC1}	Stand-by Supply Current	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 3.6V		1	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.7V		0.5	µA
V_{IL}	Input Low Voltage (SCL, SDA, $\overline{WC}$)		–0.45	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA, $\overline{WC}$)		0.7V_{CC}	V_{CC}+1	V
V_{HV}	E0 High Voltage	$V_{HV} – V_{CC} \geq 4.8V$	7	10	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA, 2.2V ≤ V_{CC} ≤ 3.6V		0.4	V
		I_{OL} = 0.7mA, V_{CC} = 1.7V		0.2	V

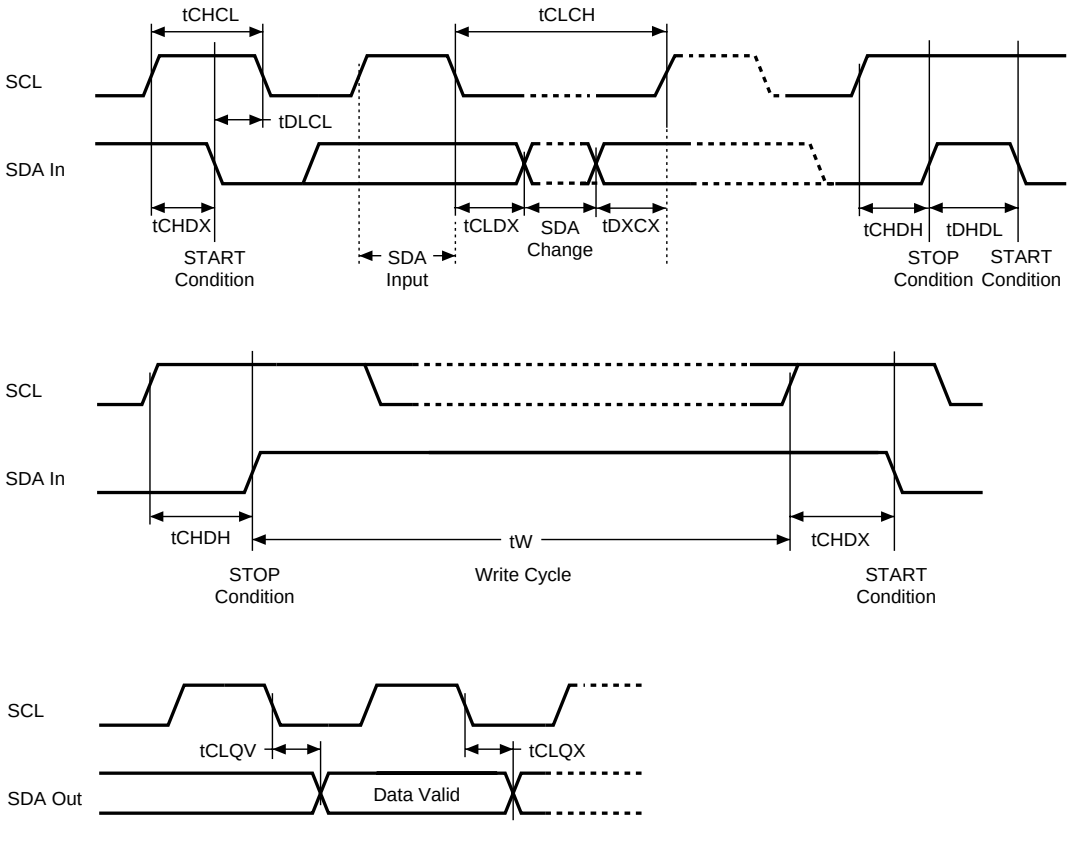
Note: 1. Preliminary Data.

Table 12. AC Characteristics

Test conditions specified in Table 9 and 8					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCL}	Clock Frequency		100	kHz
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4000		ns
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4700		ns
t_{DL1DL2} [2]	t_F	SDA Fall Time	20	300	ns
t_{DXCX}	$t_{SU:DAT}$	Data In Set Up Time	250		ns
t_{CLDX}	$t_{HD:DAT}$	Data In Hold Time	0		ns
t_{CLQX}	t_{DH}	Data Out Hold Time	200		ns
t_{CLQV} [3]	t_{AA}	Clock Low to Next Data Valid (Access Time)	200	3500	ns
t_{CHDX} [1]	$t_{SU:STA}$	Start Condition Set Up Time	4700		ns
t_{DLCL}	$t_{HD:STA}$	Start Condition Hold Time	4000		ns
t_{CHDH}	$t_{SU:STO}$	Stop Condition Set Up Time	4000		ns
t_{DHDL}	t_{BUF}	Time between Stop Condition and Next Start Condition	4700		ns
t_W	t_{WR}	Write Time		10	ms

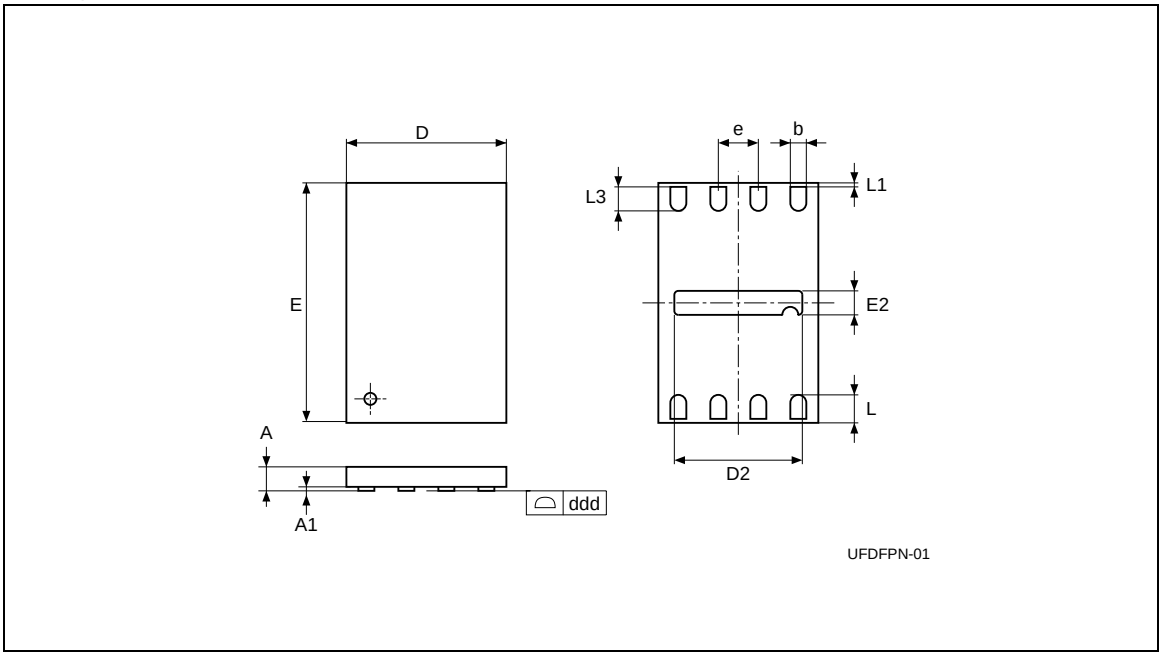
Note: 1. For a reSTART condition, or following a Write cycle.
2. Sampled only, not 100% tested.
3. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.

Figure 13. AC Waveforms



PACKAGE MECHANICAL

Figure 14. UFDFPN8 (MLP8) 8-lead Ultra thin Fine pitch Dual Flat Package No lead 2x3mm², Package Outline

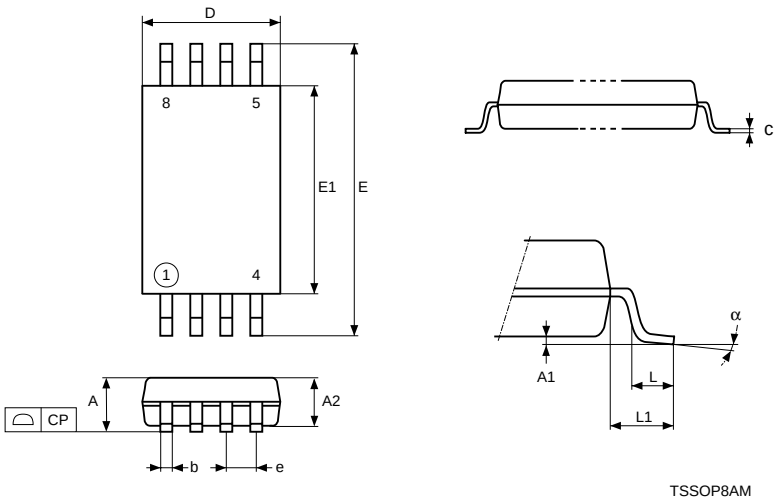


Note: 1. Drawing is not to scale.
2. The central pad (the area E2 by D2 in the above illustration) is pulled, internally, to V_{SS}. It must not be allowed to be connected to any other voltage or signal line on the PCB, for example during the soldering process.

Table 13. UFDFPN8 (MLP8) 8-lead Ultra thin Fine pitch Dual Flat Package No lead 2x3mm², Package Mechanical Data

Symbol	millimeters			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	0.55	0.50	0.60	0.022	0.020	0.024
A1		0.00	0.05		0.000	0.002
b	0.25	0.20	0.30	0.010	0.008	0.012
D	2.00			0.079		
D2		1.55	1.65		0.061	0.065
ddd			0.05			0.002
E	3.00			0.118		
E2		0.15	0.25		0.006	0.010
e	0.50	–	–	0.020	–	–
L	0.45	0.40	0.50	0.018	0.016	0.020
L1			0.15			0.006
L3		0.30			0.012	
N	8			8		

Figure 15. TSSOP8 – 8 lead Thin Shrink Small Outline, Package Outline



Notes: 1. Drawing is not to scale.

Table 14. TSSOP8 – 8 lead Thin Shrink Small Outline, Package Mechanical Data

Symbol	millimeters			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b		0.190	0.300		0.0075	0.0118
c		0.090	0.200		0.0035	0.0079
CP			0.100			0.0039
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	–	–	0.0256	–	–
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
α		0°	8°		0°	8°
N	8			8		

PART NUMBERING

Table 15. Ordering Information Scheme

Example: M34E02 – F DW 1 T P

Device Type

M34 = ASSP I^2C serial access EEPROM

Device Function

E02 = 2 Kbit (256 x 8) SPD (Serial Presence Detect) for DDR2

Operating Voltage

F = V_{CC} = 1.7 to 3.6V (100kHz)

Package

MB = UDFDFPN8 (MLP8)

DW = TSSOP8 (4.4x3mm² body size)

Temperature Range

1 = 0 to 70 °C

Option

blank = Standard Packing

T = Tape & Reel Packing

Plating Technology

blank = Standard SnPb plating

P = Lead-Free and RoHS compliant

G = Lead-Free, RoHS compliant, Sb_2O_3-free and TBBA-free

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

REVISION HISTORY

Table 16. Revision History

Date	Rev.	Description of Revision
13-Nov-2003	1.0	First release
01-Dec-2003	1.1	TSSOP8 4.4x3 package replaces TSSOP8 3x3 (MSOP8) package. Correction to sentence in “Setting the Write Protection”. Correction to specification of t_{NS} values.
29-Mar-2004	1.2	Always NoACK after Address and Data bytes in Table 6. Improvement in V_{IO} and V_{CC} (min) in Absolute Maximum Ratings table. I_{OL} changed for test condition of V_{OL}. MLP package mechanical data respecified. Soldering temperature information clarified for RoHS compliant devices.
14-Apr-2004	2.0	First public release
24-Nov-2004	3.0	Direct connection of E0, E1, E2 to V_{SS} and V_{CC} (see Chip Enable (E0, E1, E2) and USE WITHIN A DDR2 DIMM paragraphs). Z_{EiL} and Z_{EiH} parameters added to Table 10., Input Parameters. E0, E1, E2 removed from the Parameter descriptions of V_{IL} and V_{IH} in Table 11., DC Characteristics. Document status promoted from Product Preview to full Datasheet.